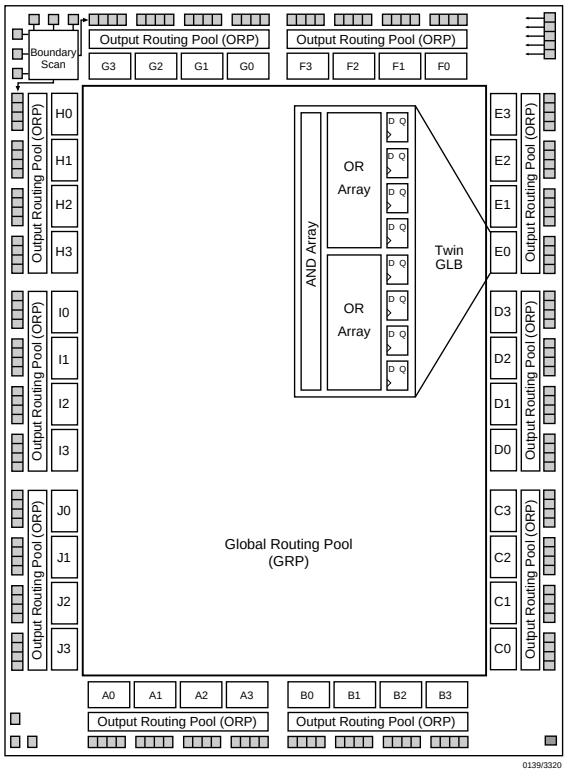
ispLSI® 3320

In-System Programmable High Density PLD

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 160 I/O Pins**
  - **— 14000 PLD Gates**
  - **— 480 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH-PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 100 MHz Maximum Operating Frequency**
  - **— t_{pd} = 10 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI FEATURES:**
  - **— 5V In-System Programmable (ISP™) Using Lattice ISP or Boundary Scan Test (IEEE 1149.1) Protocol**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Five Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
  - **— Pin Compatible with ispLSI 3160**
- **ispDesignEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **— Superior Quality of Results**
  - **— Tightly Integrated with Leading CAE Vendor Tools**
  - **— Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **— PC and UNIX Platforms**

Functional Block Diagram



Description

The ispLSI 3320 is a High-Density Programmable Logic Device containing 480 Registers, 160 Universal I/O pins, five Dedicated Clock Input Pins, ten Output Routing Pools (ORP) and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3320 features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 3320 offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 3320 device is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...J3. There are a total of 40 of these Twin GLBs in the ispLSI 3320 device. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

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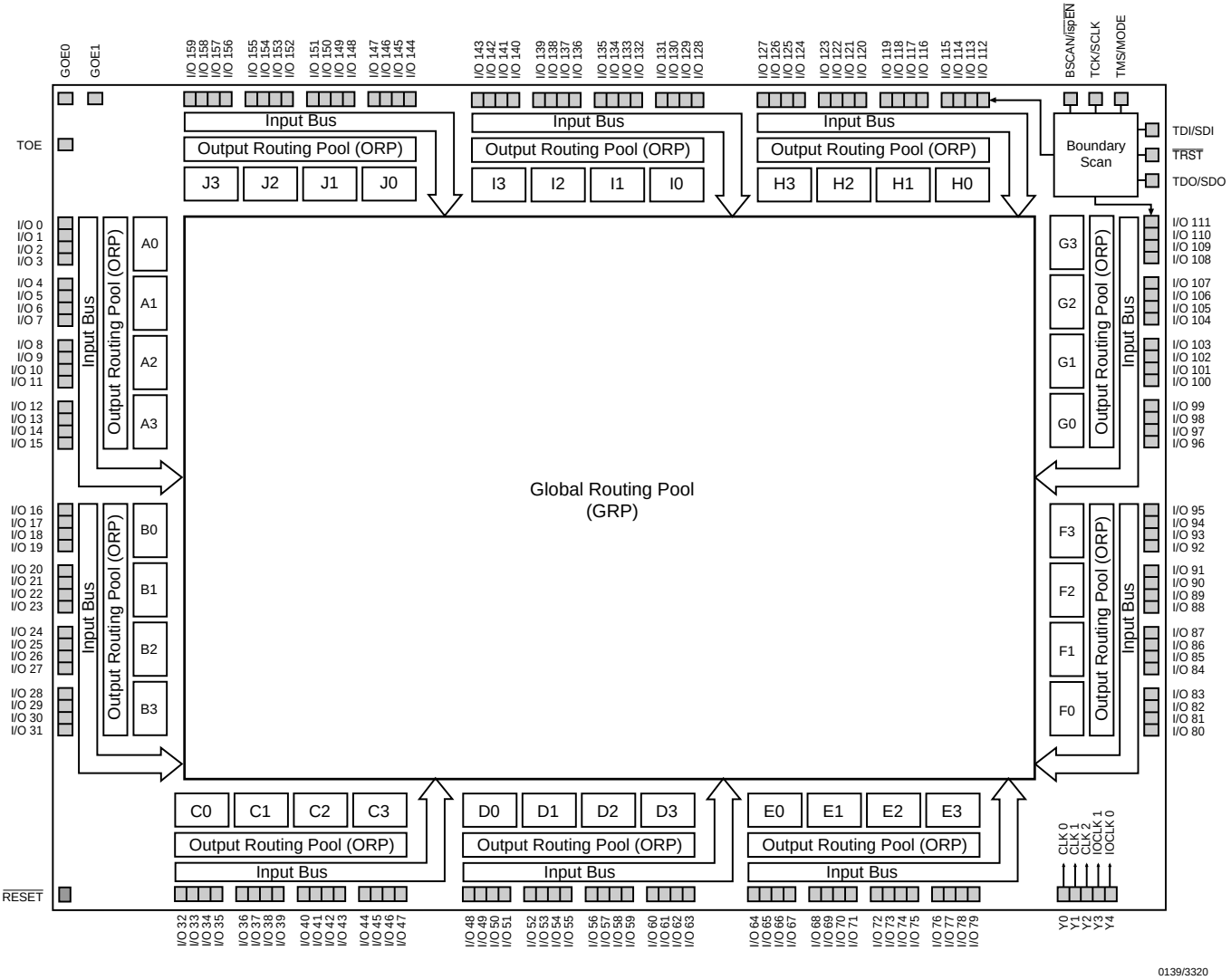
Functional Block Diagram

Figure 1. ispLSI 3320 Functional Block Diagram



Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 160 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 160 I/O cells are grouped into ten sets of 16 bits. Each of these I/O groups is associated with a logic Megablock through the use of the ORP. Each Megablock is able to provide one Product Term Output Enable (PTOE) signal which is globally distributed to all I/O cells. That PTOE signal can be generated within any GLB in the Megablock. Each I/O cell can select one of 12 available OEs (two Global OEs and ten PTOEs).

Four Twin GLBs, 16 I/O cells and one ORP are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI 3320 Device contains ten of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI 3320 device are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI 3320 is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI 3320 supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI 3320

Attribute	Quantity
Twin GLBs	40
Registers	480
I/O Pins	160
Global Clocks	5
Global OE	2
Test OE	1

Table 1-0003/3320

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied (208-Pin PQFP) ..... 150°C

Max. Junction Temp. (T_J) with Power Applied (320-Ball BGA) ..... 140°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2-0005/3320

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	11	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2-0006/3320

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/3320

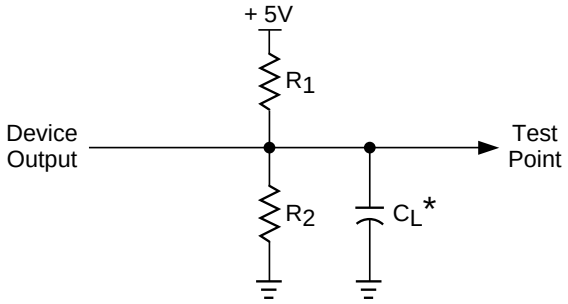
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3 ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

Table 2-0003/3320

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

Output Load conditions (See Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
$I_{IL\text{-}isp}$	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V, f_{CLOCK} = 1 MHz	–	370	–	mA

Table 2-0007/3320

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using twenty 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	13.0	–	18.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback [3]	100	–	70.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	77.0	–	50.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Maximum Toggle [4]	100	–	83.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	6.0	–	9.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	6.0	–	9.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	7.0	–	11.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	7.0	–	10.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	15.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	12.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	18.0	–	21.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	18.0	–	21.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	9.0	–	12.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	9.0	–	12.0	ns
t_{toeen}	B	18	Test OE Output Enable	–	12.0	–	15.0	ns
t_{toedis}	C	19	Test OE Output Disable	–	12.0	–	15.0	ns
t_{wh}	–	20	Ext. Synchronous Clock Pulse Duration, High	5.0	–	6.0	–	ns
t_{wl}	–	21	Ext. Synchronous Clock Pulse Duration, Low	5.0	–	6.0	–	ns
t_{su3}	–	22	I/O Reg Setup Time before Ext. Synchronous Clock (Y3, Y4)	4.5	–	5.0	–	ns
t_{h3}	–	23	I/O Reg Hold Time after Ext. Sync Clock (Y3, Y4)	0.0	–	0.0	–	ns

Table 2-0030/3320

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	24	I/O Register Bypass	–	1.5	–	3.2	ns
t_{iolat}	25	I/O Latch Delay	–	13.0	–	18.2	ns
t_{iosu}	26	I/O Register Setup Time before Clock	7.5	–	9.0	–	ns
t_{ioh}	27	I/O Register Hold Time after Clock	-3.0	–	-4.0	–	ns
t_{ioco}	28	I/O Register Clock to Out Delay	–	2.5	–	4.2	ns
t_{ior}	29	I/O Register Reset to Out Delay	–	2.5	–	4.2	ns
GRP							
t_{grp}	30	GRP Delay	–	3.0	–	3.5	ns
$t_{feedback}$	31	Feedback Delay	–	1.1	–	1.6	ns
GLB							
t_{4ptbp}	32	4 Product Term Bypass Path Delay (Comb.)	–	3.5	–	5.3	ns
t_{4ptbr}	33	4 Product Term Bypass Path Delay (Reg.)	–	3.5	–	3.8	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	4.5	–	5.8	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	4.5	–	5.8	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	5.5	–	7.3	ns
t_{gbp}	37	GLB Register Bypass Delay	–	0.5	–	0.5	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.0	–	2.5	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	4.9	–	6.3	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	0.5	–	1.0	ns
t_{gro}	41	GLB Register Reset to Output Delay	–	1.0	–	1.0	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	7.9	–	11.5	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.5	–	9.3	ns
t_{ptck}	44	GLB Product Term Clock Delay	3.2	3.2	4.5	4.5	ns
ORP							
t_{orp}	45	ORP Delay	–	1.5	–	2.0	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.0	–	0.0	ns

Table 2-0036/3320

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

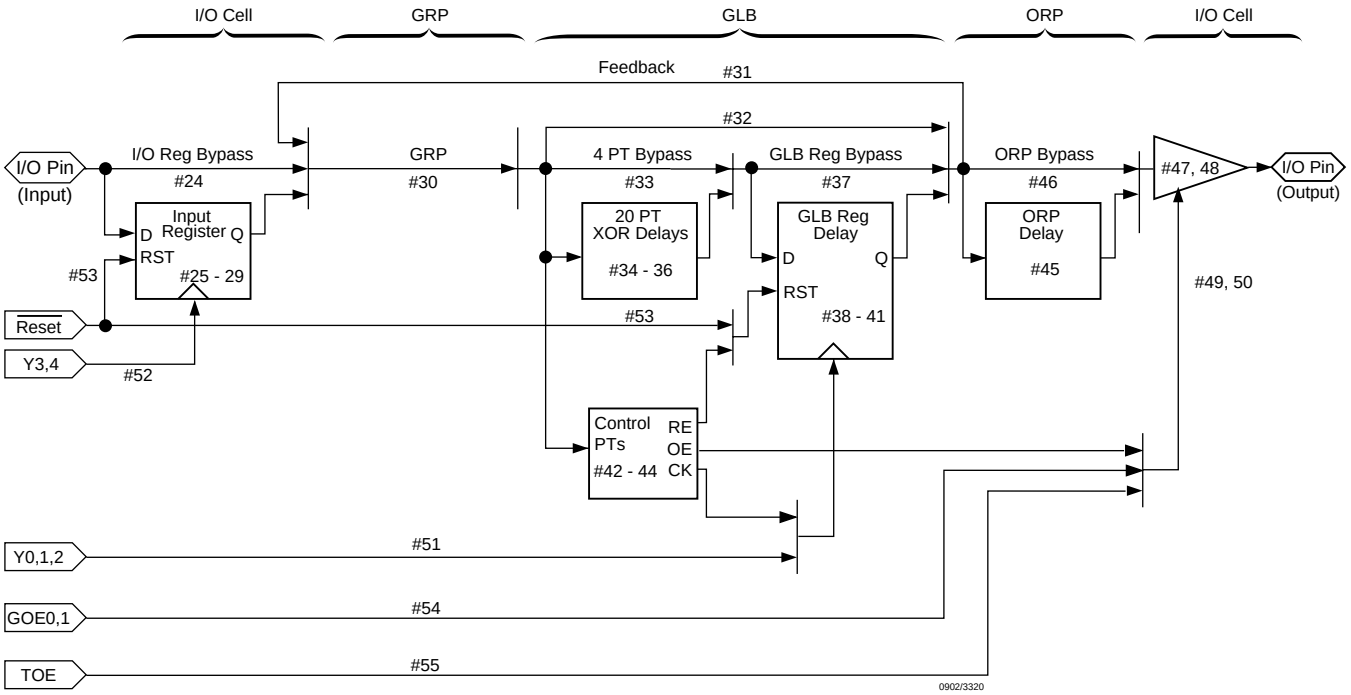
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	2.0	–	3.0	ns
t_{obs}	48	Output Buffer Delay, Slew Limited Adder	–	12.0	–	13.0	ns
t_{oen}	49	I/O Cell OE to Output Enabled	–	4.0	–	5.0	ns
t_{odis}	50	I/O Cell OE to Output Disabled	–	4.0	–	5.0	ns
Clocks							
$t_{gy0/1/2}$	51	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clock Line	3.0	3.0	4.0	4.0	ns
$t_{ioy3/4}$	52	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	3.0	3.0	4.0	4.0	ns
Global Reset							
t_{gr}	53	Global Reset to GLB and I/O Registers	–	9.0	–	9.0	ns
t_{goe}	54	Global OE Pad Buffer	–	5.0	–	7.0	ns
t_{toe}	55	Test OE Pad Buffer	–	8.0	–	10.0	ns

Table 2-0037/3320

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 3320 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
	=	(#24+ #30+ #35) + (#38) - (#24+ #30+ #44)
2.3 ns	=	(1.5 + 3.0 + 4.5) + (1.0) - (1.5 + 3.0 + 3.2)
th	=	Clock (max) + Reg h - Logic
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
	=	(#24+ #30+ #44) + (#39) - (#24+ #30+ #35)
3.6 ns	=	(1.5 + 3.0 + 3.2) + (4.9) - (1.5 + 3.0 + 4.5)
tco	=	Clock (max) + Reg co + Output
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#24 + #30 + #44) + (#40) + (#45 + #47)
11.7 ns	=	(1.5 + 3.0 + 3.2) + (0.5) + (1.5 + 2.0)

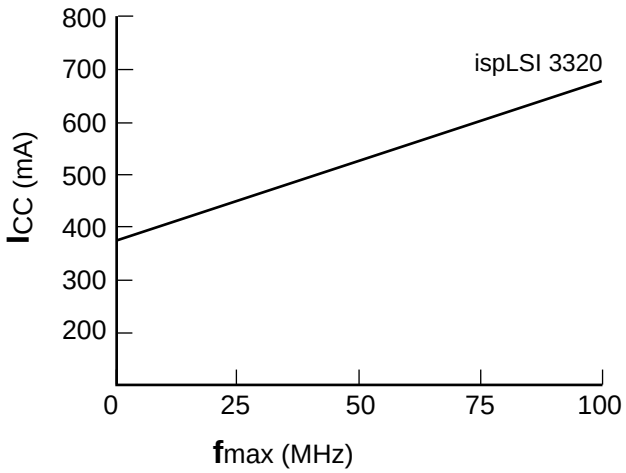
Table 2-0042/3320

Note: Calculations are based on timing specs for the ispLSI 3320-100L.

Power Consumption

Power consumption in the ispLSI 3320 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 20 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI 3320 using the following equation:

I_{CC} = 60 + (# of PTs * 0.5) + (# of nets * Max. freq * 0.0095) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

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Signal Descriptions

Signal Name	Description
GOE0, GOE1	Global Output Enable input pins.
I/O	Input/Output Pins – These are the general purpose I/O pins used by the logic array.
TOE	Test Output Enable pin – This pin tristates all I/O pins when a logic low is driven.
$\overline{\text{RESET}}$	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0, Y1, Y2	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
Y3, Y4	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells on the device.
BSCAN/$\overline{\text{ispEN}}$	Input – Dedicated in-system programming enable input pin. When this pin is high, the BSCAN TAP controller pins TMS, TDI, TDO and TCK are enabled. When this pin is brought low, the ISP State Machine control pins MODE, SDI, SDO and SCLK are enabled. High-to-low transition of this pin will put the device in the programming mode and put all I/O pins in the high-Z state.
TDI/SDI	Input – This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the ISP State Machine.
TCK/SCLK	Input – This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
TMS/MODE	Input – This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the ISP State Machine.
$\overline{\text{TRST}}$	Input – Test Reset, active low to reset the Boundary Scan State Machine.
TDO/SDO	Output – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the ISP data. When $\overline{\text{ispEN}}$ is high, it functions as Test Data Out.
GND	Ground (GND)
VCC	Vcc
NC[1]	No Connect.

1. NC pins are not to be connected to any active signals, VCC or GND.

Signal Locations

Signal	208-Pin PQFP	320-Ball BGA
GOE0, GOE1	133, 134	AD12, AC11
TOE	30	B14
$\overline{\text{RESET}}$	28	D13
Y0, Y1, Y2, Y3, Y4	132, 130, 129, 128, 127	AA12, AC13, AB13, AA13, AD13
BSCAN/$\overline{\text{ispEN}}$	27	B12
TDI/SDI	25	C12
TCK/SCLK	24	D12
TMS/MODE	23	A12
$\overline{\text{TRST}}$	29	A13
TDO/SDO	185	M4
GND	11, 26, 42, 53, 65, 78, 92, 104, 115, 131, 146, 157, 169, 183, 196, 208	A16, B13, C8, D6, D19, F4, F21, H22, J1, M2, N23, T24, U3, W4, W21, AA6, AA19, AB17, AC12, AD9
VCC	14, 39, 58, 80, 99, 118, 143, 162, 181, 203	B10, B18, C3, D4, D21, G2, K23, R2, V23, AA4, AA21,AC7, AC15
NC[1]	76, 77, 79, 81, 180, 182, 184	A1, A2, A3, A6, A9, A11, A14, A20, A23, A24, B1, B2, B5, B8, B9, B16, B17, B20, B23, B24, C5, C13, C17, C20, C24, D7, D11, D14, D17, D20, E1, E2, E3, E4, E22, E23, F24, G21, G23, H2, H3, H4, H23, J2, J23, J24, K3, L1, L4, L21, L24, M3, M21, M22, M23, N2, N3, N4, N21, N22, N24, P1, P4, P21, P24, R22, T1, T2, T23, U2, U21, U22, U23, V2, V4, W1, Y2, Y3, Y21, Y22, Y23, Y24, AA5, AA8, AA11, AA14, AA18, AB1, AB5, AB8, AB12, AB20, AC1, AC2, AC5, AC8, AC9, AC16, AC17, AC20, AC23, AC24, AD1, AD2, AD5, AD11, AD14, AD16, AD19, AD22, AD23, AD24

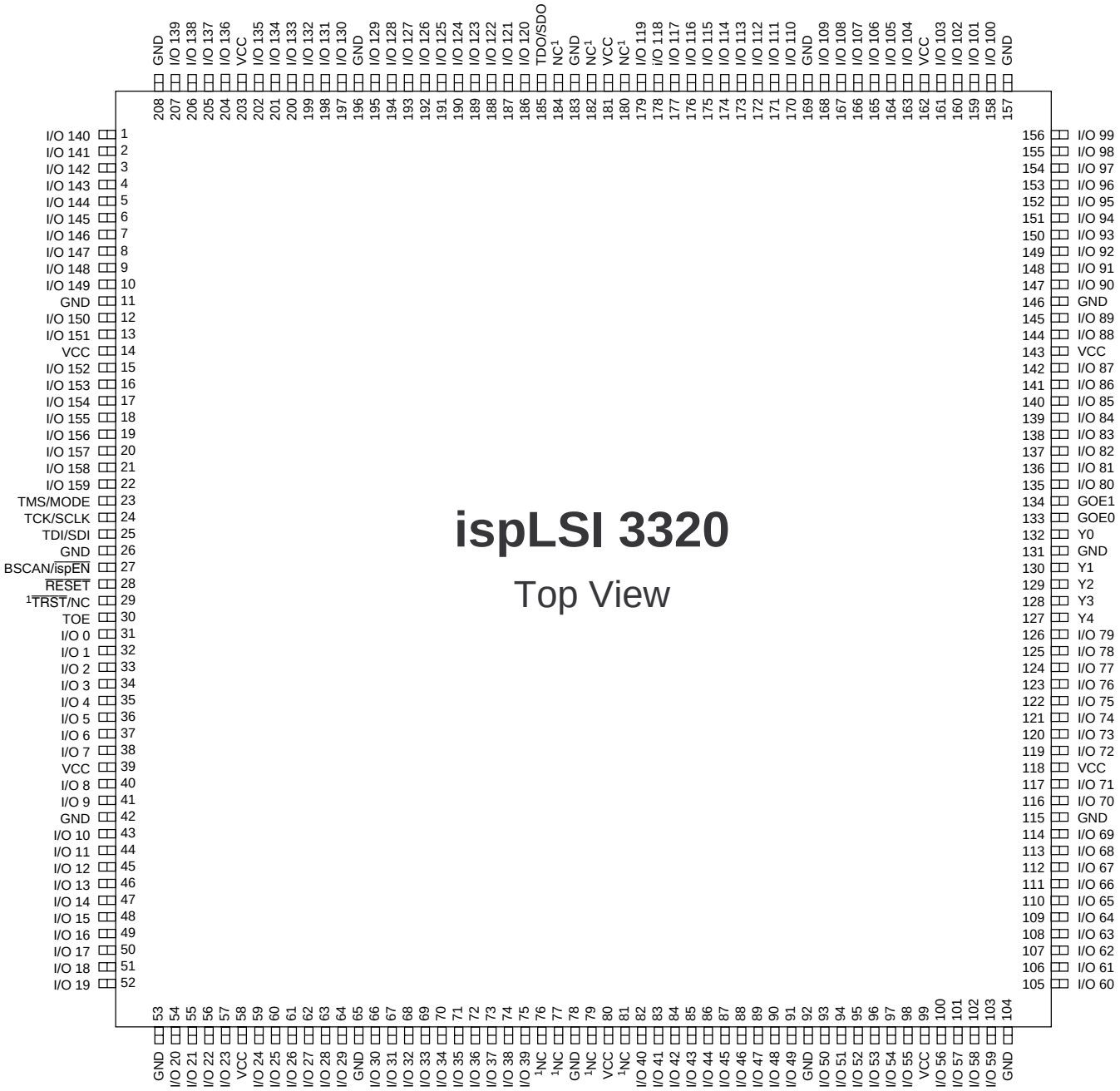
1. NC pins are not to be connected to any active signals, VCC or GND.

I/O Locations

Signal	PQFP	BGA	Signal	PQFP	BGA	Signal	PQFP	BGA	Signal	PQFP	BGA
I/O 0	31	C14	I/O 40	82	P23	I/O 80	135	AB11	I/O 120	186	M1
I/O 1	32	A15	I/O 41	83	P22	I/O 81	136	AD10	I/O 121	187	L2
I/O 2	33	B15	I/O 42	84	R24	I/O 82	137	AC10	I/O 122	188	L3
I/O 3	34	C15	I/O 43	85	R23	I/O 83	138	AB10	I/O 123	189	K1
I/O 4	35	D15	I/O 44	86	R21	I/O 84	139	AA10	I/O 124	190	K2
I/O 5	36	A17	I/O 45	87	U24	I/O 85	140	AD8	I/O 125	191	K4
I/O 6	37	C16	I/O 46	88	T22	I/O 86	141	AB9	I/O 126	192	H1
I/O 7	38	D16	I/O 47	89	T21	I/O 87	142	AA9	I/O 127	193	J3
I/O 8	40	A18	I/O 48	90	V24	I/O 88	144	AD7	I/O 128	194	J4
I/O 9	41	A19	I/O 49	91	W24	I/O 89	145	AD6	I/O 129	195	G1
I/O 10	43	C18	I/O 50	93	V22	I/O 90	147	AB7	I/O 130	197	F1
I/O 11	44	B19	I/O 51	94	W23	I/O 91	148	AC6	I/O 131	198	G3
I/O 12	45	D18	I/O 52	95	V21	I/O 92	149	AA7	I/O 132	199	F2
I/O 13	46	C19	I/O 53	96	W22	I/O 93	150	AB6	I/O 133	200	G4
I/O 14	47	A21	I/O 54	97	AA24	I/O 94	151	AD4	I/O 134	201	F3
I/O 15	48	B21	I/O 55	98	AA23	I/O 95	152	AC4	I/O 135	202	D1
I/O 16	49	A22	I/O 56	100	AB24	I/O 96	153	AD3	I/O 136	204	D2
I/O 17	50	C21	I/O 57	101	AA22	I/O 97	154	AB4	I/O 137	205	C1
I/O 18	51	B22	I/O 58	102	AB23	I/O 98	155	AC3	I/O 138	206	D3
I/O 19	52	C22	I/O 59	103	AB22	I/O 99	156	AB3	I/O 139	207	C2
I/O 20	54	C23	I/O 60	105	AC22	I/O 100	158	AB2	I/O 140	1	B3
I/O 21	55	D22	I/O 61	106	AB21	I/O 101	159	AA3	I/O 141	2	C4
I/O 22	56	E21	I/O 62	107	AA20	I/O 102	160	Y4	I/O 142	3	D5
I/O 23	57	D23	I/O 63	108	AC21	I/O 103	161	AA2	I/O 143	4	B4
I/O 24	59	D24	I/O 64	109	AD21	I/O 104	163	AA1	I/O 144	5	A4
I/O 25	60	F22	I/O 65	110	AB19	I/O 105	164	W3	I/O 145	6	C6
I/O 26	61	E24	I/O 66	111	AD20	I/O 106	165	Y1	I/O 146	7	A5
I/O 27	62	F23	I/O 67	112	AC19	I/O 107	166	W2	I/O 147	8	B6
I/O 28	63	G22	I/O 68	113	AB18	I/O 108	167	V3	I/O 148	9	C7
I/O 29	64	H21	I/O 69	114	AA17	I/O 109	168	U4	I/O 149	10	D8
I/O 30	66	G24	I/O 70	116	AC18	I/O 110	170	V1	I/O 150	12	B7
I/O 31	67	J21	I/O 71	117	AD18	I/O 111	171	T4	I/O 151	13	A7
I/O 32	68	J22	I/O 72	119	AA16	I/O 112	172	T3	I/O 152	15	D9
I/O 33	69	H24	I/O 73	120	AB16	I/O 113	173	U1	I/O 153	16	C9
I/O 34	70	K21	I/O 74	121	AD17	I/O 114	174	R4	I/O 154	17	A8
I/O 35	71	K22	I/O 75	122	AA15	I/O 115	175	R3	I/O 155	18	D10
I/O 36	72	K24	I/O 76	123	AB15	I/O 116	176	R1	I/O 156	19	C10
I/O 37	73	L22	I/O 77	124	AD15	I/O 117	177	P3	I/O 157	20	A10
I/O 38	74	L23	I/O 78	125	AB14	I/O 118	178	P2	I/O 158	21	C11
I/O 39	75	M24	I/O 79	126	AC14	I/O 119	179	N1	I/O 159	22	B11

Pin Configuration

ispLSI 3320 208-Pin PQFP (with Heat Spreader) Pinout Diagram

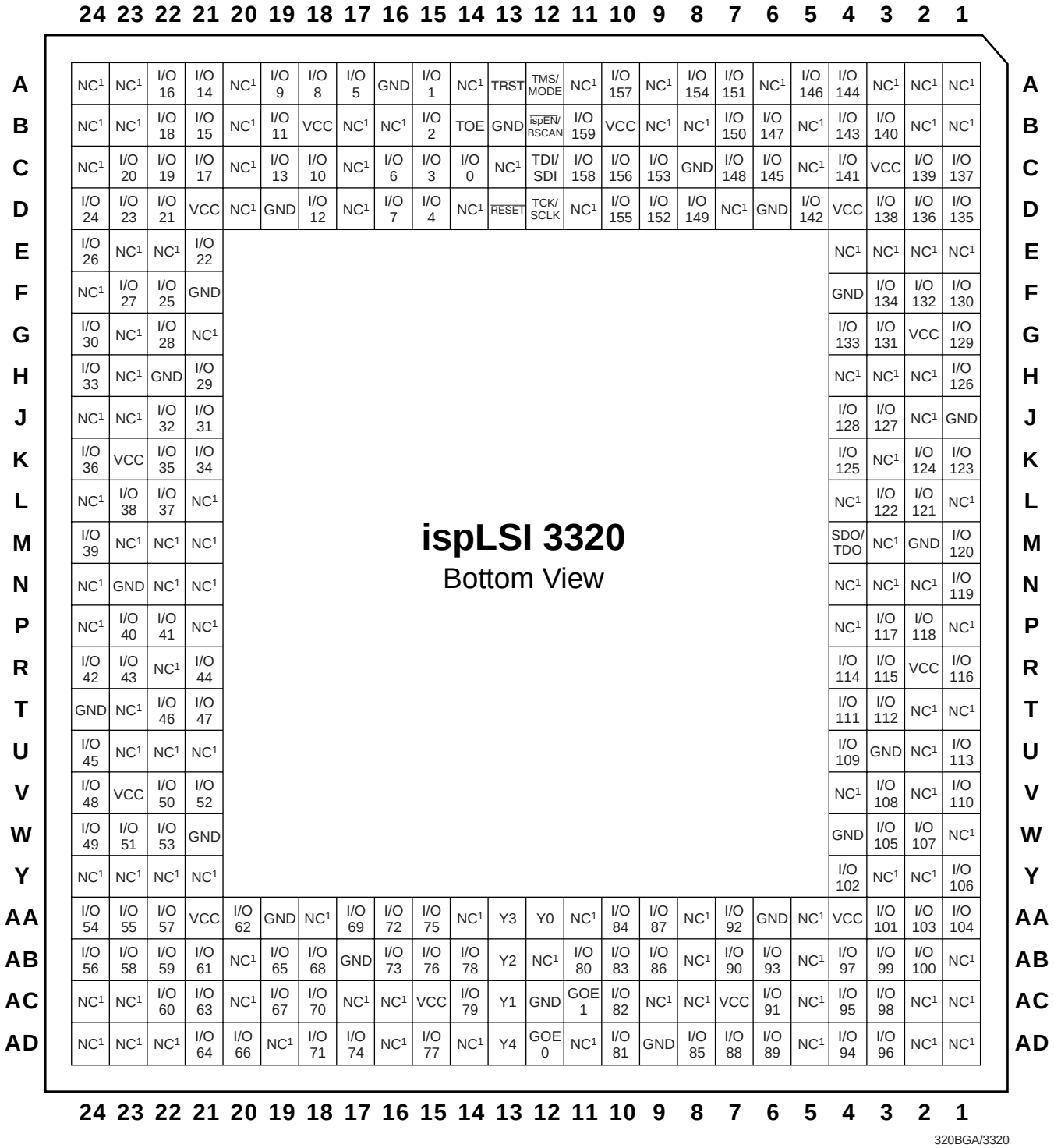


1. NC pins are not to be connected to any active signal, VCC or GND.

208MQUAD/3320

Signal Configuration

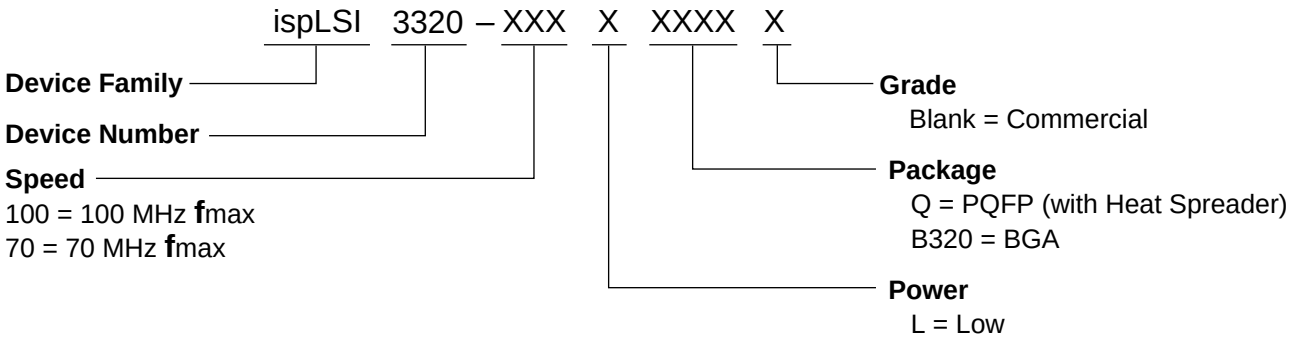
ispLSI 3320 320-Ball BGA Signal Diagram



1. NCs are not to be connected to any active signals, Vcc or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212A/3320

Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	100	10	ispLSI 3320-100LQ	208-Pin PQFP
	100	10	ispLSI 3320-100LB320	320-Ball BGA
	70	15	ispLSI 3320-70LQ	208-Pin PQFP
	70	15	ispLSI 3320-70LB320	320-Ball BGA

Table 2-0041A/3320