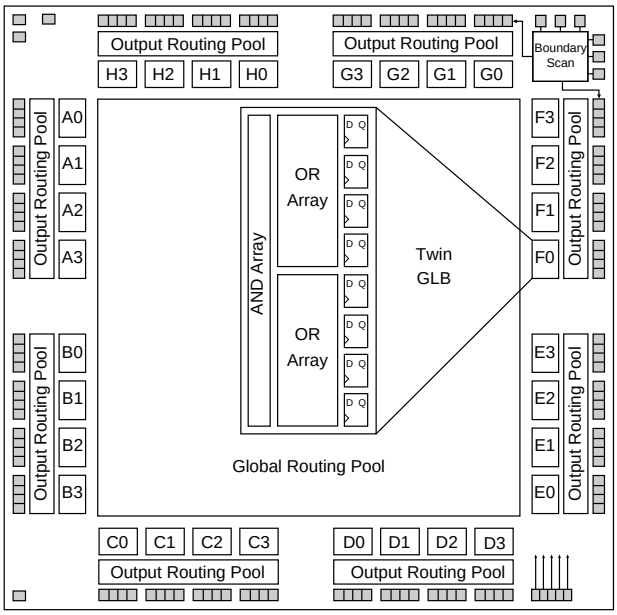
ispLSI® 3256A

In-System Programmable High Density PLD

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 128 I/O Pins**
  - **— 11000 PLD Gates**
  - **— 384 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH-PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 90 MHz Maximum Operating Frequency**
  - **— t_{pd} = 12 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **— 5V In-System Programmable (ISP™) using Lattice ISP or Boundary Scan Test (IEEE 1149.1) Protocol**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Five Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispDesignEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **— Superior Quality of Results**
  - **— Tightly Integrated with Leading CAE Vendor Tools**
  - **— Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **— PC and UNIX Platforms**

Functional Block Diagram



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Description

The ispLSI 3256A is a High-Density Programmable Logic Device containing 384 Registers, 128 Universal I/O pins, five Dedicated Clock Input Pins, eight Output Routing Pools (ORP) and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3256A features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 3256A offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 3256A device is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...H3. There are a total of 32 Twin GLBs in the ispLSI 3256A device. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

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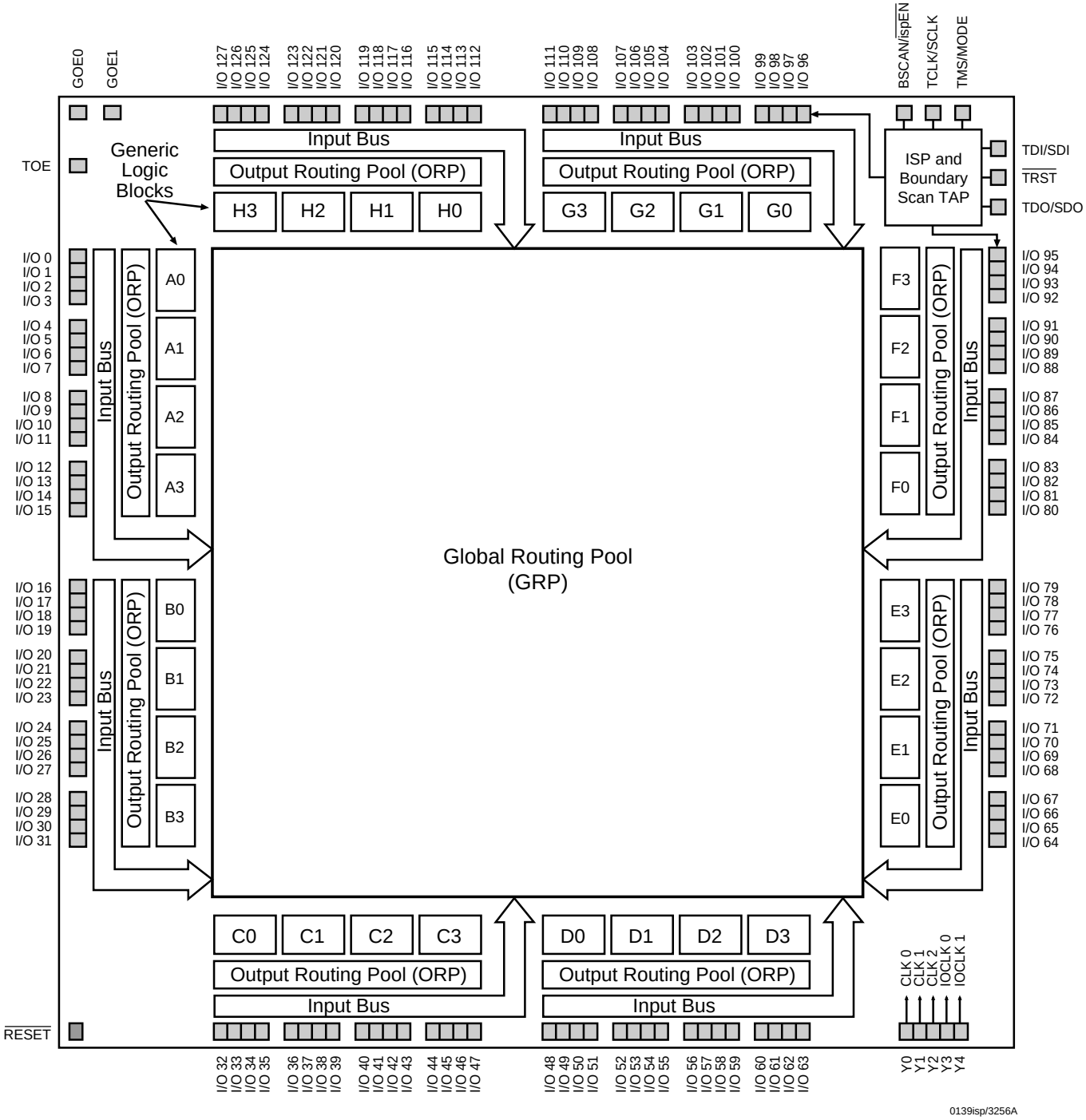
Functional Block Diagram

Figure 1. ispLSI 3256A Functional Block Diagram



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Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 128 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 128 I/O cells are grouped into eight sets of 16 bits. Each of these I/O groups is associated with a logic Megablock through the use of the ORP. These groups of 16 I/O cells share one Product Term Output Enable which is associated with a specific pair of Megablocks and two Global Output Enables.

Four Twin GLBs, 16 I/O cells and one ORP are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI 3256A device contains eight of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI 3256A device are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table at right lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI 3256A is its Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI 3256A supports the full boundary scan IEEE 1149.1 specification for ISP programming and board-level tests via the TAP controller port. It is also fully backward compatible to the Lattice ISP interface. While fully JEDEC file and functionally compatible with the earlier ispLSI 3256 devices, the 3256A requires a modified Boundary Scan Description Library (BSDL) model to support boundary scan test and programming. As a result, existing 3256 test programs that use the boundary scan test feature must be updated to use the 3256A. Please contact Lattice Applications for the new model.

The ispLSI 3256A supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI 3256A

Attribute	Quantity
Twin GLBs	32
Registers	384
I/O Pins	128
Global Clocks	5
Global OE	2
Test OE	1

Table 1-0003A/3256

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Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V

Table 2-0005/3256A

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance (Commercial/Industrial)	9	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	11	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2-0006/3256A

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/3256A

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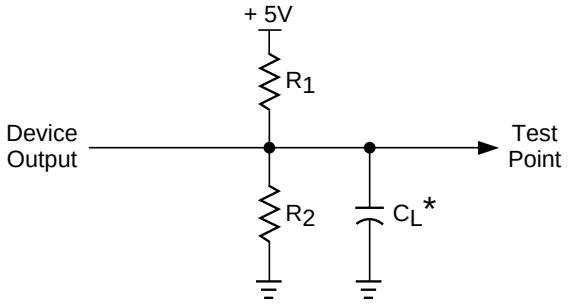
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

Table 2-0003/3256A

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

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Output Load conditions (See Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V	Commercial	–	200	–	mA
		f_{CLOCK} = 1 MHz	Industrial	–	200	–	mA

Table 2-0007/3256A

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using 16 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

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External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-90		-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	–	12.0	–	15.0	–	20.0	ns
t_{pd2}	A	2	Data Prop. Delay	–	15.0	–	18.0	–	24.5	ns
f_{max}	A	3	Clk Frequency with Internal Feedback[3]	90.0	–	77.0	–	57.0	–	MHz
f_{max} (Ext.)	–	4	Clk Frequency with Ext. Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	61.0	–	50.0	–	37.0	–	MHz
f_{max} (Tog.)	–	5	Clk Frequency, Max. Toggle[4]	125	–	83.0	–	63.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clk, 4 PT Bypass	8.0	–	9.5	–	12.5	–	ns
t_{co1}	A	7	GLB Reg. Clk to Output Delay, ORP Bypass	–	7.5	–	9.0	–	12.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clk, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clk	9.0	–	11.0	–	15.0	–	ns
t_{co2}	–	10	GLB Reg. Clk to Output Delay	–	9.0	–	10.5	–	14.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clk	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	15.0	–	20.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	10.0	–	13.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	16.0	–	18.0	–	24.5	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	16.0	–	18.0	–	24.5	ns
t_{goeen}	B	16	Global OE Output Enable	–	10.0	–	11.0	–	13.5	ns
t_{goedis}	C	17	Global OE Output Disable	–	10.0	–	11.0	–	13.5	ns
t_{toeen}	B	18	Test OE Output Enable	–	10.0	–	17.0	–	23.0	ns
t_{toedis}	C	19	Test OE Output Disable	–	10.0	–	17.0	–	23.0	ns
t_{wh}	–	20	Ext. Synchronous Clk Pulse Duration, High	4.0	–	6.0	–	8.0	–	ns
t_{wl}	–	21	Ext. Synchronous Clk Pulse Duration, Low	4.0	–	6.0	–	8.0	–	ns
t_{su3}	–	22	I/O Reg Setup Time before Ext. Sync Clk (Y3, Y4)	5.0	–	5.0	–	7.0	–	ns
t_{h3}	–	23	I/O Reg Hold Time after Ext. Sync Clk (Y3, Y4)	0.0	–	0.0	–	0.0	–	ns

Table 2-0030C/3256A

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

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Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-90		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{iobp}	24	I/O Register Bypass	–	1.9	–	2.4	–	3.3	ns
t_{iolat}	25	I/O Latch Delay	–	10.9	–	12.4	–	15.8	ns
t_{iosu}	26	I/O Register Setup Time before Clock	5.7	–	6.2	–	8.6	–	ns
t_{ioh}	27	I/O Register Hold Time after Clock	-3.7	–	-5.2	–	-7.0	–	ns
t_{ioco}	28	I/O Register Clock to Out Delay	–	4.2	–	4.2	–	5.3	ns
t_{ior}	29	I/O Register Reset to Out Delay	–	2.8	–	3.6	–	4.9	ns
GRP									
t_{grp}	30	GRP Delay	–	2.4	–	3.0	–	4.1	ns
GLB									
t_{4ptbp}	31	4 Product Term Bypass Path Delay (Comb.)	–	4.8	–	5.9	–	7.6	ns
t_{4ptbp}	32	4 Product Term Bypass Path Delay (Reg.)	–	4.8	–	5.9	–	7.6	ns
t_{1ptxor}	33	1 Product Term/XOR Path Delay	–	5.4	–	6.4	–	8.8	ns
$t_{20ptxor}$	34	20 Product Term/XOR Path Delay	–	6.4	–	7.4	–	10.1	ns
t_{xoradj}	35	XOR Adjacent Path Delay[3]	–	6.9	–	8.1	–	11.1	ns
t_{gbp}	36	GLB Register Bypass Delay	–	0.1	–	0.1	–	0.1	ns
t_{gsu}	37	GLB Register Setup Time before Clock	1.0	–	1.8	–	2.4	–	ns
t_{gh}	38	GLB Register Hold Time after Clock	4.8	–	6.0	–	8.2	–	ns
t_{gco}	39	GLB Register Clock to Output Delay	–	1.6	–	1.8	–	2.2	ns
t_{gro}	40	GLB Register Reset to Output Delay	–	2.6	–	2.8	–	3.8	ns
t_{ptre}	41	GLB Product Term Reset to Register Delay	–	8.6	–	10.5	–	14.2	ns
t_{ptoe}	42	GLB Product Term Output Enable to I/O Cell Delay	–	4.9	–	5.4	–	7.3	ns
t_{ptck}	43	GLB Product Term Clock Delay	2.8	5.3	3.2	6.3	4.3	8.5	ns
ORP									
t_{orp}	44	ORP Delay	–	2.3	–	2.7	–	3.6	ns
t_{orpbp}	45	ORP Bypass Delay	–	0.9	–	1.2	–	1.6	ns

Table 2-0036C/3256A

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

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Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-90		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t_{ob}	46	Output Buffer Delay	–	1.9	–	2.4	–	3.3	ns
t_{obs}	47	Output Buffer Delay, Slew Limited Adder	–	11.9	–	12.4	–	13.3	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.8	–	7.2	–	9.8	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.8	–	7.2	–	9.8	ns
Clocks									
$t_{gy0/1/2}$	50	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clock Line	2.7	2.7	3.6	3.6	4.9	4.9	ns
$t_{ioy3/4}$	51	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	0.7	3.7	1.2	5.2	1.6	7.0	ns
Global Reset									
t_{gr}	52	Global Reset to GLB and I/O Registers	–	6.7	–	7.1	–	9.6	ns
t_{goe}	53	Global OE Pad Buffer	–	2.3	–	2.8	–	3.7	ns
t_{toe}	54	Test OE Pad Buffer	–	3.2	–	9.8	–	13.2	ns

Table 2-0037C/3256A

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

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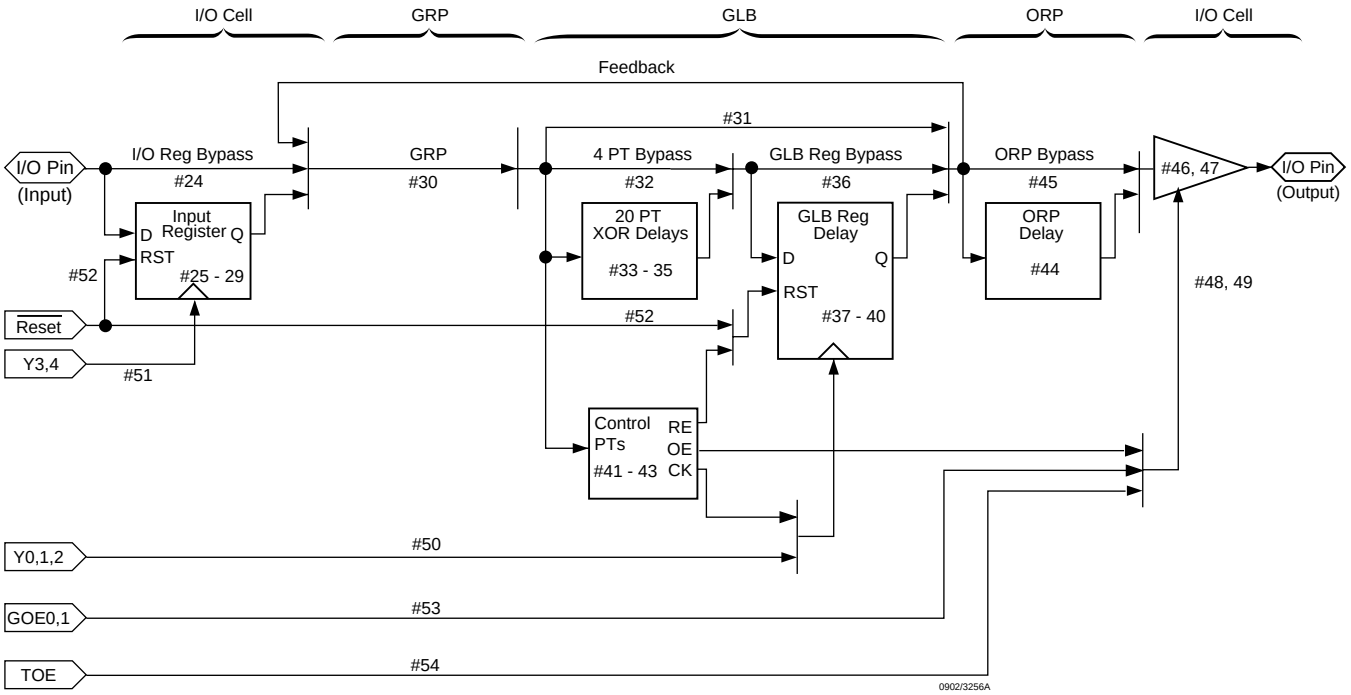
ispLSI 3256A Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
	=	(#24+ #30+ #34) + (#37) - (#24+ #30+ #43)
4.6 ns	=	(1.9 + 2.4 + 6.4) + (1.0) - (1.9 + 2.4 + 2.8)
th	=	Clock (max) + Reg h - Logic
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
	=	(#24+ #30+ #43) + (#38) - (#24+ #30+ #34)
3.7 ns	=	(1.9 + 2.4 + 5.3) + (4.8) - (1.9 + 2.4 + 6.4)
tco	=	Clock (max) + Reg co + Output
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#24 + #30 + #43) + (#39) + (#44 + #46)
15.4 ns	=	(1.9 + 2.4 + 5.3) + (1.6) + (2.3 + 1.9)

Table 2-0042/3256A

Note: Calculations are based on timing specs for the ispLSI 3256A-90L.

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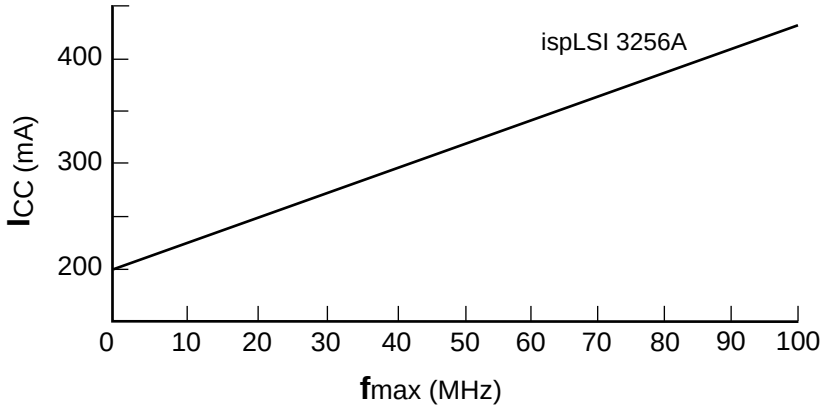
Power Consumption

Power consumption in the ispLSI 3256A device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 16 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI 3256A using the following equation:

I_{CC} = 40 + (# of PTs * 0.31) + (# of nets * Max. freq * 0.0094) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

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Pin Description

NAME	PQFP/MQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 4 I/O 5 - I/O 9 I/O 10 - I/O 14 I/O 15 - I/O 19 I/O 20 - I/O 24 I/O 25 - I/O 29 I/O 30 - I/O 34 I/O 35 - I/O 39 I/O 40 - I/O 44 I/O 45 - I/O 49 I/O 50 - I/O 54 I/O 55 - I/O 59 I/O 60 - I/O 64 I/O 65 - I/O 69 I/O 70 - I/O 74 I/O 75 - I/O 79 I/O 80 - I/O 84 I/O 85 - I/O 89 I/O 90 - I/O 94 I/O 95 - I/O 99 I/O 100 - I/O 104 I/O 105 - I/O 109 I/O 110 - I/O 114 I/O 115 - I/O 119 I/O 120 - I/O 124 I/O 125 - I/O 127	25, 26, 28, 29, 30, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 46, 47, 48, 49, 50, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 64, 65, 66, 67, 68, 69, 70, 72, 73, 74, 75, 76, 77, 78, 79, 80, 82, 83, 84, 85, 86, 87, 88, 89, 90, 92, 93, 94, 95, 96, 105, 106, 108, 109, 110, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 126, 127, 128, 129, 130, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 144, 145, 146, 147, 148, 149, 150, 152, 153, 154, 155, 156, 157, 158, 159, 160, 2, 3, 4, 5, 6, 7, 8, 9, 11, 13, 14, 15, 16, 17	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1 TOE	100 and 99 98	Global Output Enable input pins. Test output enable pin - This pin tristates all I/O pins when a logic low is driven
$\overline{\text{RESET}}$ Y0, Y1 and Y2 Y3 and Y4	20 18, 19, 103 102, 101	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/$\overline{\text{ispEN}}$ TDI/SDI TCK/SCLK TMS/MODE $\overline{\text{TRST}}$ TDO/SDO	21 22 23 24 97 104	Input – Dedicated in-system programming enable input pin. When this pin is high, the BSCAN TAP controller pins TMS, TDI, TDO and TCK are enabled. When this pin is brought low, the ISP state machine control pins MODE, SDI, SDO and SLCK are enabled. High-to-low transition of this pin will put the device in the programming mode and put all I/O pins in high-Z state. Input – This pin performs two functions depending on the state of the BSCAN/$\overline{\text{ispEN}}$ pin. It is the Test Data input to the TAP Controller when the $\overline{\text{ispEN}}$ is logic high. TDI is used to load BSCAN test data or programming data. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the ISP state machine. Input – This pin performs two functions, depending on the state of the BSCAN/$\overline{\text{ispEN}}$ pin. It is the Test Clock input pin when BSCAN/$\overline{\text{ispEN}}$ is logic high. When BSCAN/$\overline{\text{ispEN}}$ is logic low, it functions as the clock for the ISP state machine. Input – This pin performs two functions, depending on the state of the BSCAN/$\overline{\text{ispEN}}$ pin. It is the Test Mode Select input pin when BSCAN/$\overline{\text{ispEN}}$ is logic high. When BSCAN/$\overline{\text{ispEN}}$ is logic low, it functions to control the operation of the ISP state machine. Input – Test Reset, active low to reset the Boundary Scan state machine. Output – This pin performs two functions, depending on the state of the BSCAN/$\overline{\text{ispEN}}$ pin. It is the Test Data Output pin when BSCAN/$\overline{\text{ispEN}}$ is logic high, and either BSCAN test data or programming data is shifted out. When BSCAN/$\overline{\text{ispEN}}$ is logic low, it is the Serial Data Output of the ISP state machine.
GND VCC	1, 10, 27, 45, 63, 81, 107, 125, 143 12, 31, 51, 71, 91, 111, 131, 151	Ground (GND) V_{CC}

Table 2-0002/3256A.a

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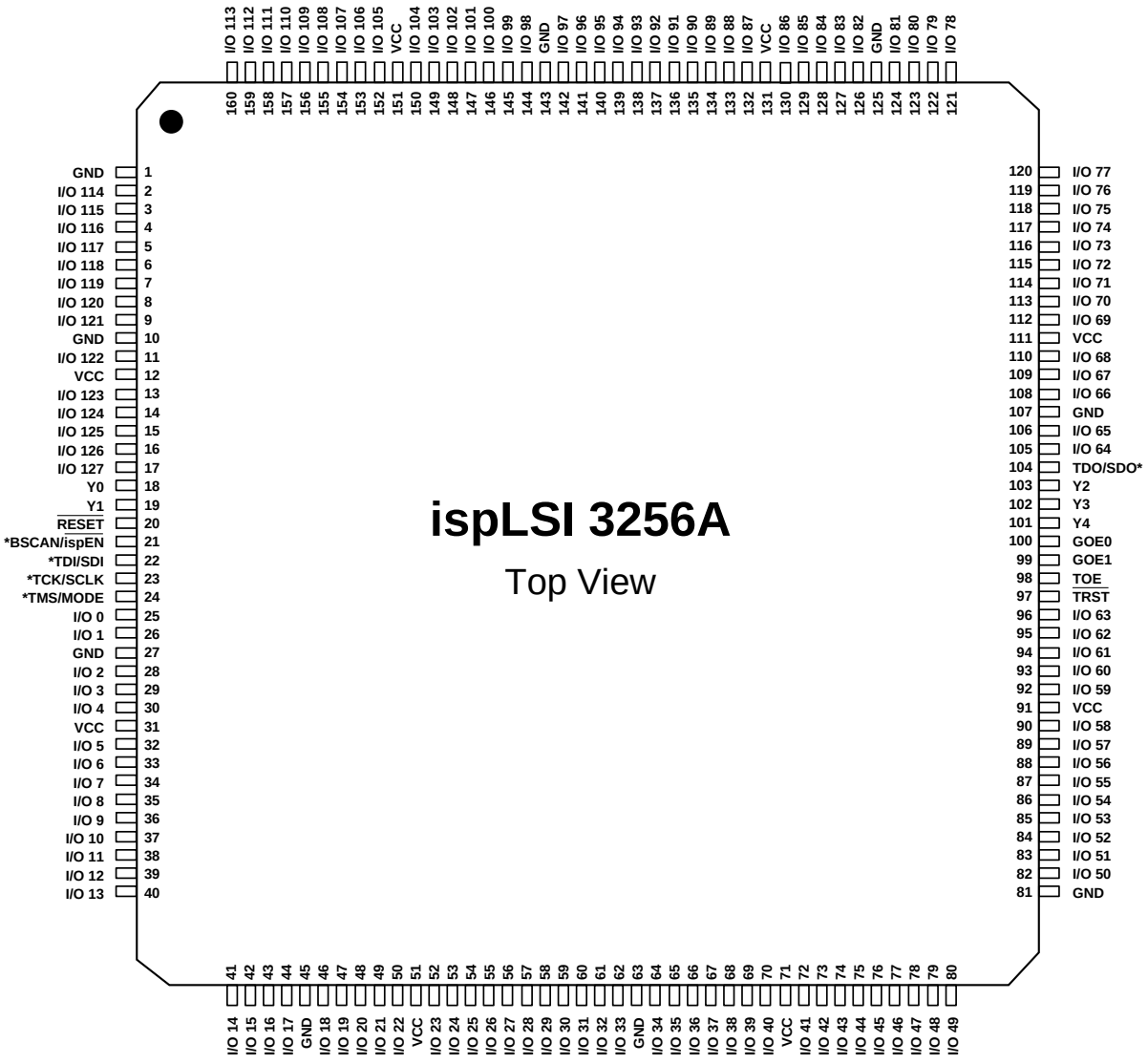
Pin Configuration

ispLSI 3256A 160-Pin MQFP and 160-Pin PQFP Pinout Diagram



*Pins have dual function capability.

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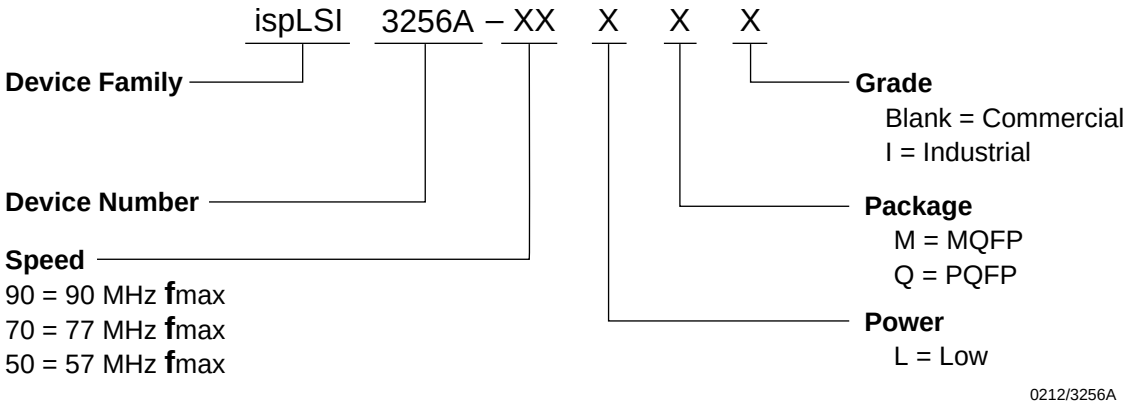
Part Number Description



Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	90	12	ispLSI 3256A-90LM*	160-Pin MQFP
	90	12	ispLSI 3256A-90LQ	160-Pin PQFP
	77	15	ispLSI 3256A-70LM*	160-Pin MQFP
	77	15	ispLSI 3256A-70LQ	160-Pin PQFP
	57	20	ispLSI 3256A-50LM**	160-Pin MQFP

Table 2-0041B/3256A

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	77	15	ispLSI 3256A-70LQI	160-Pin PQFP
	57	20	ispLSI 3256A-50LMI**	160-Pin MQFP

Table 2-0041C/3256A

*Use ispLSI 3256A in PQFP package for all new designs.
**Use ispLSI 3256A-70LQ/I for all new designs.

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