Advance Product Information

VSC7186

Quad Transceiver for Gigabit Ethernet

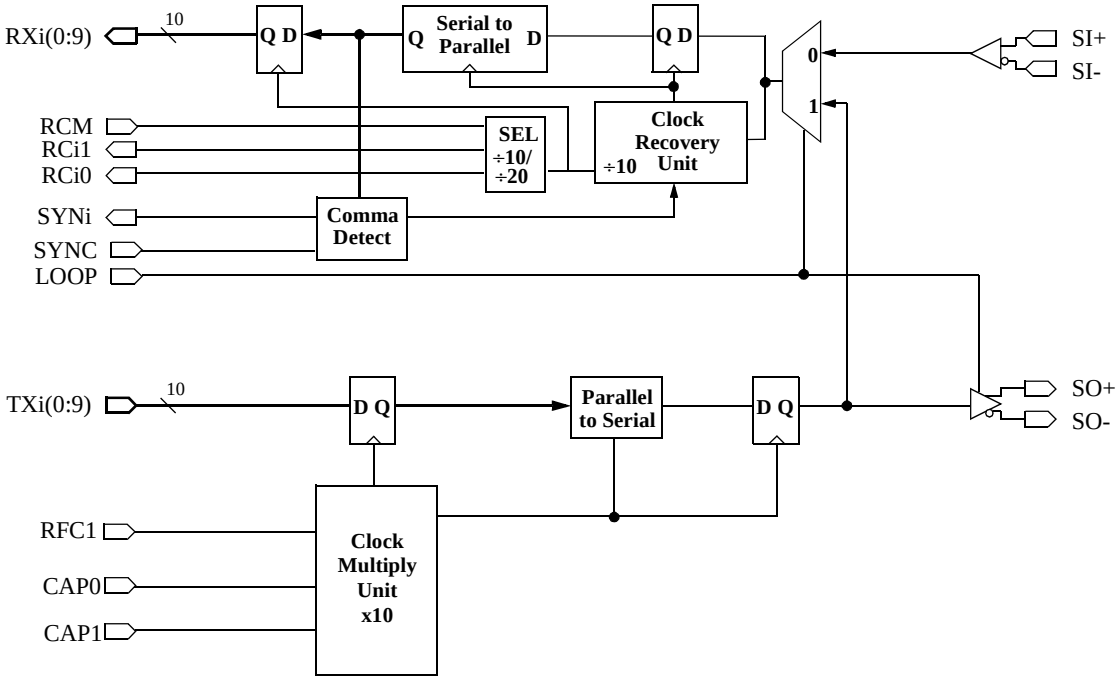
Features

- Four Complete Transceiver Functions in One IC
- Full Gigabit Ethernet (IEEE 802.3z) Compliance
- Pin-Compatible With Agilent HDMP-1686A
- 5-Volt Tolerant TTL Inputs
- Uses Reference Clock to Latch Tx Data
- 1/10th or 1/20th Baud Rate Recovered Clocks
- Common Local Loopback Control
- Single Comma Detect Enable
- Cable Equalization in Receivers
- Automatic Lock-to-Reference
- JTAG Access Port
- 2kV ESD Protection on All Pins
- 3.3V Power Supply, 2.67 W Max Dissipation
- 208 pin, 23 mm BGA Packaging

General Description

The VSC7186 is a Quad Gigabit Ethernet Transceiver IC. Each of the four transmitters has a 10-bit wide bus, running at 125 MHz, which accepts 8b/10b encoded transmit characters and serializes the data onto high speed differential outputs at rates between 1.05 and 1.36 Gb/s. The transmit data must be synchronous to the reference clock. Each receiver samples serial receive data, recovers the clock and data, deserializes it into 10-bit receive characters, outputs a recovered clock and detects “Comma” characters. The VSC7186 contains on-chip PLL circuitry for synthesis of the baud-rate transmit clock and extraction of the clocks from the received serial streams.

VSC7186 Block Diagram (1 of 4 Channels)



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Functional Description

Notation

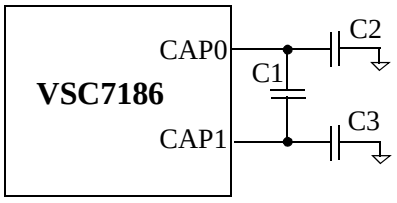
In this document, each of the four channels are identified as Channel 0, 1, 2 or 3. When discussing a signal on any specific channel, the signal will have the Channel number embedded in the name, i.e. "T**3**(0:9)". When referring to the common behavior of a signal which is used on each of the four channels, the notation "i" is used. Differential signals, i.e. SOi+ and SOi-, may be referred to as a single signal, i.e. SOi, by dropping reference to the "+" and "-".

Clock Synthesizer

The VSC7186 Clock Multiplier Unit (CMU) multiplies the reference frequency provided on the RFC1 input by 10 to achieve a baud rate clock between 1.05 and 1.36 GHz. The RFC1 input is TTL. The on-chip PLL uses a single external 0.1uF capacitor, connected between CAP0 and CAP1, to control the Loop Filter. This capacitor should be a multilayer ceramic dielectric, or better, with at least a 5V working voltage rating and a good temperature coefficient, i.e., NPO is preferred but X7R may be acceptable. These capacitors are used to minimize the impact of common mode noise on the Clock Multiplier Unit, especially power supply noise. Higher value capacitors provide better robustness in systems. NPO is preferred because if an X7R capacitor is used, the power supply noise sensitivity will vary with temperature.

For best noise immunity, the designer may use a three capacitor circuit with one differential capacitor between CAP0 and CAP1, C1, a capacitor from CAP0 to ground, C2, and a capacitor from CAP1 to ground, C3. Larger values are better but 0.1uF is adequate. However, if the designer cannot use a three capacitor circuit, a single differential capacitor, C1, is adequate. These components should be isolated from noisy traces.

Figure 1: Loop Filter Capacitors (Best Circuit)



C1=C2=C3= >0.1uF
MultiLayer Ceramic
Surface Mount
NPO (Prefered) or X7R
5V Working Voltage Rating

Serializer

The VSC7186 accepts TTL input data as four parallel 10 bit characters on the Ti(0:9) buses which are latched into the input registers on the rising edge of RFC1. The 10-bit parallel transmission character will be serialized and transmitted on the SOi+/- PECL differential outputs at the baud rate with bit Ti0 (bit a) transmitted first. User data should be encoded using 8b/10b or an equivalent code. The mapping to 10b encoded bit nomenclature and transmission order is illustrated below, along with the recognized comma pattern.

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Table 1: Transmission Order and Mapping of a 10b Character

Data Bit	*T9*	*T8*	*T7*	*T6*	*T5*	*T4*	*T3*	*T2*	*T1*	*T0*
10B Bit Position	j	h	g	f	i	e	d	c	b	a
Comma Character	x	x	x	1	1	1	1	1	0	0

Clock Recovery

The VSC7186 accepts differential high speed serial input from the selected source (either the PECL SIi+/- pins or the internal SOi+/- data), extracts the clock and retimes the data. Equalizers are included in the receiver to open the data eye and compensate for Intersymbol Interference (ISI) which may be present in the incoming data. The serial bit stream should be encoded so as to provide DC balance and limited run length by an 8b/10b encoding scheme. The digital Clock Recovery Unit (CRU) is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within $\pm$200 ppm of ten times the REF frequency. For example, Gigabit Ethernet systems use 125 MHz oscillators with a +/-100ppm accuracy resulting in +/-200 ppm between VSC7186 pairs.

Deserializer

The recovered serial bit stream is converted into a 10-bit parallel output character. The VSC7186 provides complementary TTL recovered clocks, RCi0 and RCi1, at one-twentieth of the serial baud rate if RCM=LOW, or a single clock at one-tenth the serial baud rate, on RCi1 only, if RCM=HIGH. The clocks are generated by dividing down the high-speed recovered clock which is phase locked to the serial data. The serial data is retimed, deserialized and output on Ri(0:9).

If serial input data is not present, or does not meet the required baud rate, the VSC7186 will continue to produce a recovered clock so that downstream logic may continue to function. The RCi0/RCi1 output frequency under these circumstances will differ from its expected frequency by no more than $\pm$1%.

Word Alignment

The VSC7186 provides 7-bit comma character recognition and data word alignment. Word synchronization is enabled on all channels by asserting SYNC HIGH. When synchronization is enabled, the receiver examines the recovered serial data for the presence of the “Comma” pattern. This pattern is “0011111XXX”, where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8b/10b coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5 and K28.7, which are defined for synchronization purposes. Improper comma alignment is defined as any of the following conditions:

1) The comma is not aligned within the 10-bit transmission character such that Ri(0..6) = “0011111”.
2) The comma straddles the boundary between two 10-bit transmission characters.
3) The comma is properly aligned but occurs in the received character presented during the rising edge of RCi0 rather than RCi1.

When an improperly aligned comma is encountered, the recovered clock is stretched, never slivered, so that the comma character and recovered clocks are aligned properly to Ri(0:9). This results in proper character and word alignment. When the parallel data alignment changes in response to a improperly aligned comma pattern,

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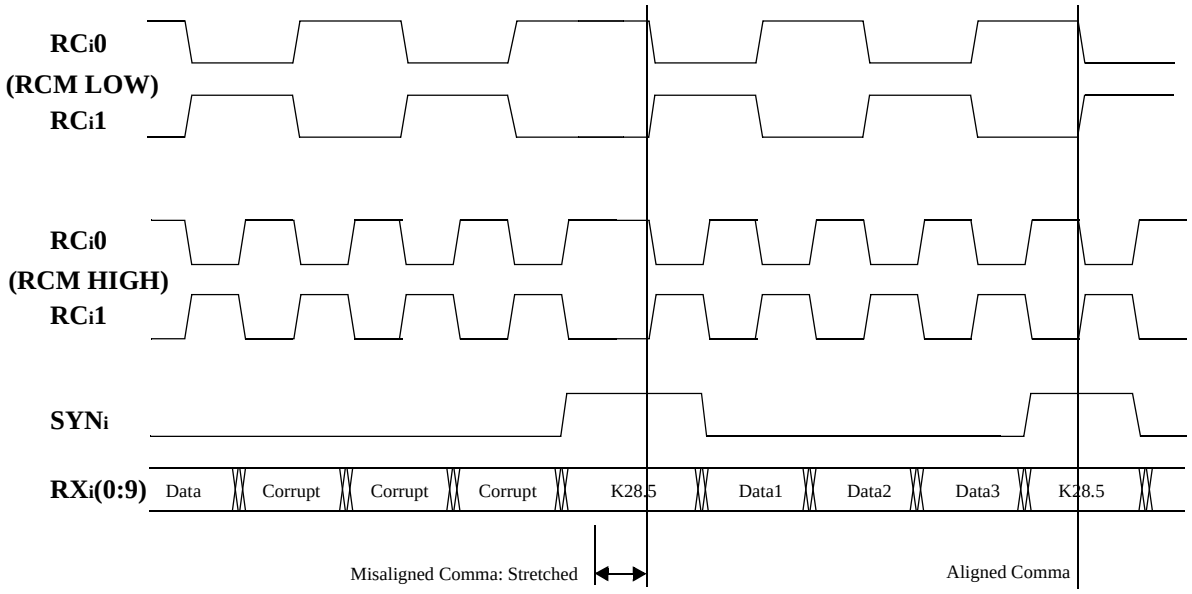
data which would have been presented on the parallel output port prior to the comma character, and possibly the comma character itself, may be lost. Possible loss of the comma character is data dependent, according to the relative change in alignment. Data subsequent to the comma character will always be output correctly and properly aligned.

On encountering a comma character, SYNi is driven HIGH. The SYNi pulse is presented simultaneously with the comma character and has a duration equal to the data. The SYNi signal is timed such that it can be captured by the adjoining protocol logic on the rising edge of RCi1. Functional waveforms for synchronization are given in Figure 1. The first K28.5 shows the case where the comma is detected, but it is misaligned so a change in the output data alignment is required. Note that up to three characters prior to the comma character may be corrupted by the realignment process. The second K28.5 shows the case when a comma is detected and no phase adjustment is necessary. It illustrates the position of the SYNi pulse in relation to the comma character on Ri(0:9).

Figure 2: Misaligned and Aligned K28.5 Characters



Loopback Operation

Loopback operation is controlled by the LOOP line. When this line is HIGH, the outgoing high-speed serial data on each of the four channels is internally looped back into that channel's high-speed serial receiver section. This provides for in-circuit testing capability independent of the transmission medium.

JTAG Access Port

A JTAG access port is provided to assist in board-level testing. Through this port most pins can be accessed or controlled and all TTL outputs can be tri-stated. A full description of the JTAG functions on this device is available in "VSC7186 JTAG Access Port Functionality". Circuits designed exclusively for the HDMP-1686A will automatically disable the JTAG port. The pinout table in this data sheet shows the proper connections for either HDMP-1686A emulation or for JTAG functionality (in parentheses).

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AC Characteristics

Figure 3: Transmit Timing Waveforms

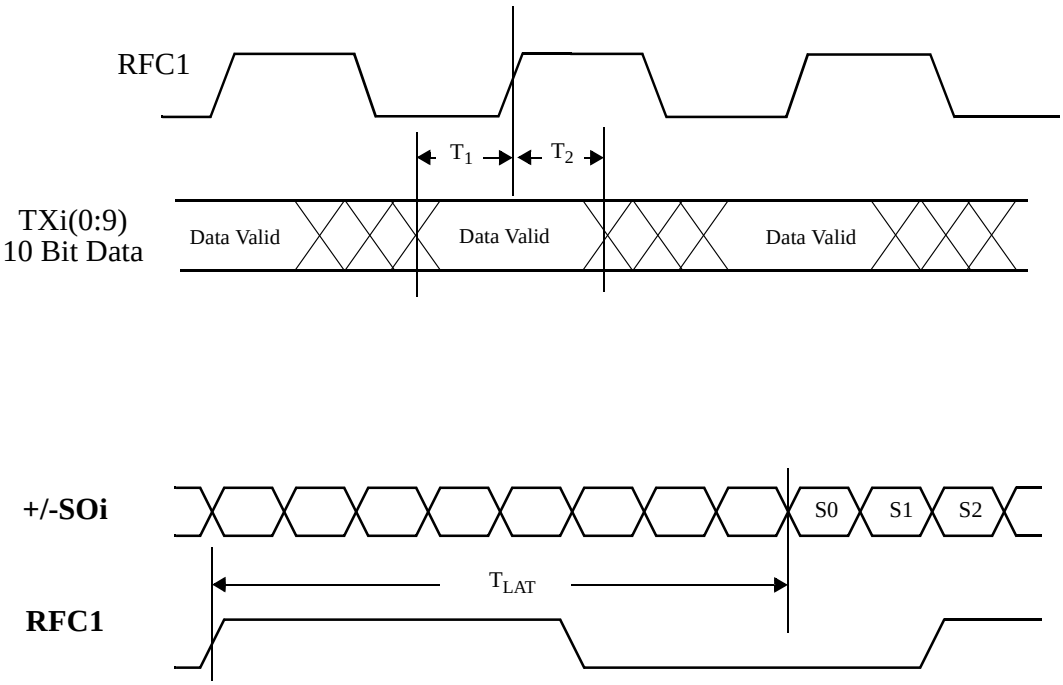

Table 2: Transmitter AC Characteristics

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_1	Ti(0:9) Setup time to the rising edge of RFC1	1.5	—	—	ns.	Measured between the valid data level of Ti(0:9) to the 1.4V point of RFC1
T_2	Ti(0:9) hold time after the rising edge of RFC1	1.0	—	—	ns.	
T_{SDR},T_{SDF}	Ti+/Ti- rise and fall time	—	—	300	ps.	20% to 80%, 75 Ohm load to Vdd/2, Tested on a sample basis
T_{LAT}	Latency from rising edge of RFC1 to Ti0 appearing on SO bit 0i	7bc + 0.66ns	—	7bc + 1.46ns	Note:	bc = bit clocks ns = nanoseconds
Transmitter Output Jitter						
RJ	Random jitter (RMS)	—	5	8	ps.	Measured at SO+/-, 1 sigma deviation of 50% crossing pt
DJ	Serial data output deterministic jitter (pk-pk)	—	35	80	ps.	IEEE 802.3Z Clause 38.68, Tested on a sample basis

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Figure 4: Receive Timing Waveforms

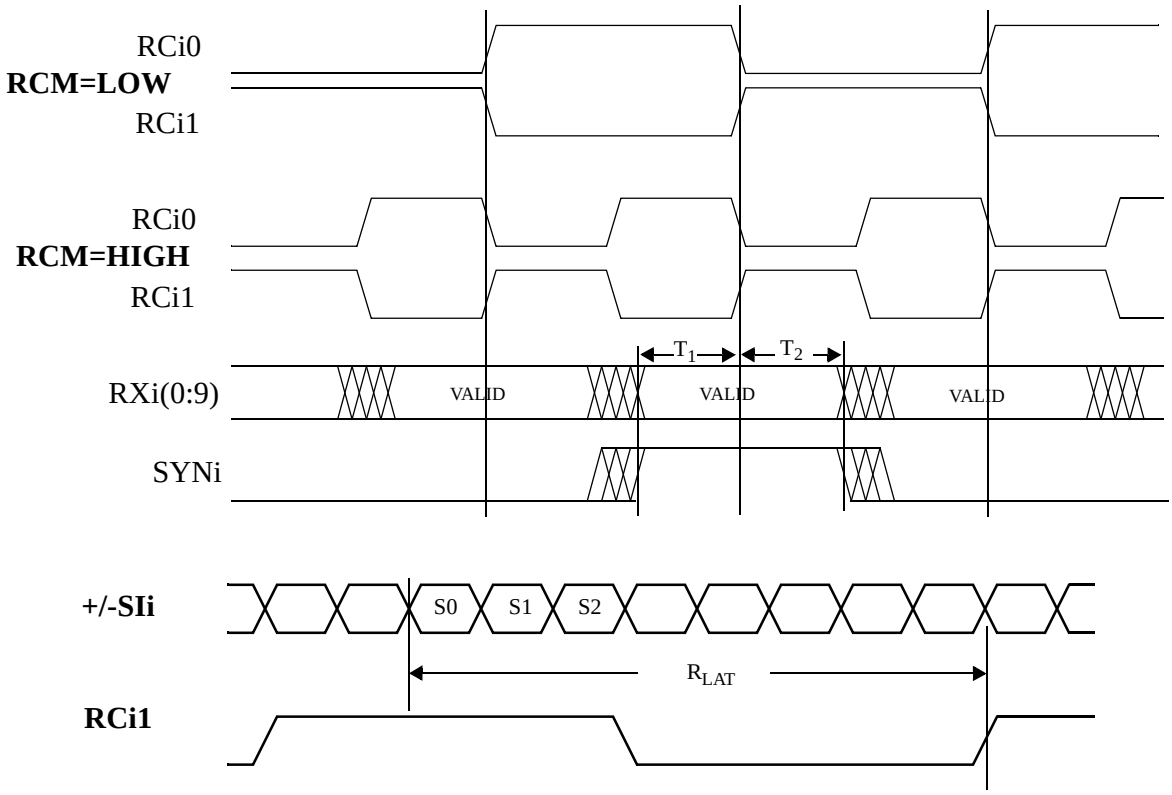

Table 3: Receive AC Characteristics—

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_1	TTL Outputs Valid prior to RCi1/RCi0 rise	3.0	—	ns.	@ 1.25Gb/s
T_2	TTL Outputs Valid after RCi1 or RCi0 rise	2.0	—	ns.	@ 1.25Gb/s
T_3	Delay between rising edge of RCi1 to rising edge of RCi0	10 x T_{Ri} -500	10 x T_{Ri} +500	ps.	T_{Ri} is the bit period of the incoming data on Ri.
T_4	Period of RCi1 and RCi0	1.98 x T_{REF}	2.02 x T_{REF}	ps.	Whether or not locked to serial data.
T_R, T_F	TTL Output rise and fall time	—	2.4	ns.	Between $V_{IL(max)}$ and $V_{IH(min)}$, into 10 pf. load.
T_{LOCK}	Data acquisition lock time*	—	1400	bit times	8b/10b IDLE pattern. Tested on a sample basis
R_{LAT}	Latency from bit 0 of RXi0 appearing on SI to rising edge of RCi1	12bc + 2.77ns	13bc + 7.28	Note:	bc = bit clocks ns = nanoseconds.
** Note: Probability of recovery for data acquisition is 95% per Section 5.3 of FC-PH rev. 4.3*					

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Figure 5: RFC1 Waveform

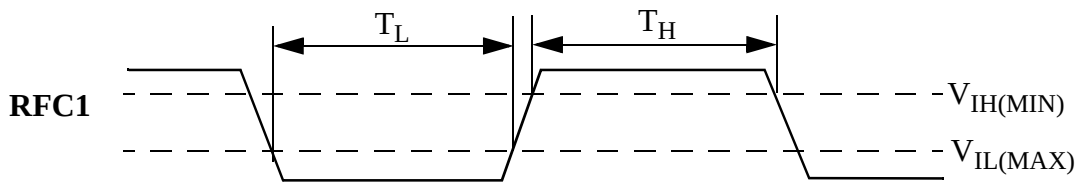

Table 4: Reference Clock Requirements

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
FR	Frequency Range	105	136	MHz	Range over which both transmit and receive reference clocks on any link may be centered
FO	Frequency Offset	-200	200	ppm.	Maximum frequency offset between transmit and receive reference clocks on one link
DC	RFC1 duty cycle	35	65	%	Measured at 1.4V
T_{RCR},T_{RCF}	RFC1 rise and fall time	—	1.5	ns.	Between $V_{IL(max)}$ and $V_{IH(min)}$

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DC Characteristics

Parameters	*Description*	*Min.*	*Typ*	*Max.*	*Units*	*Conditions*
TTL Outputs						
V_{OH}	TTL output HIGH voltage	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	TTL output LOW voltage	—	—	0.5	V	I_{OL} = +1.0mA
I_{OZ}	TTL output Leakage current	—	—	50	µA	When set to high-impedance state through JTAG.
TTL Inputs						
V_{IH}	TTL input HIGH voltage	2.0	—	5.5	V	5V Tolerant Inputs
V_{IL}	TTL input LOW voltage	0	—	0.8	V	
I_{IH}	TTL input HIGH current	—	50	500	µA	V_{IN} =2.4V
I_{IL}	TTL input LOW current	—	—	-500	µA	V_{IN} =0.5V
High Speed Outputs						
ΔV_{OUT75}(1)	TX Output differential peak-to-peak voltage swing	1200	—	2200	mVp-p	75Ω to V_{DD} – 2.0 V (Ti+) - (Ti-)
ΔV_{OUT50}(1)	Ti Output differential peak-to-peak voltage swing	1000	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V (Ti+) - (Ti-)
High Speed Inputs						
ΔV_{IN}(1)	PECL differential peak-to-peak input voltage swing	200	—	2600	mV	Ri+ - Ri-
Miscellaneous						
V_{DD}	Power supply voltage	3.14	—	3.47	V	3.3V ± 5%
P_D	Power dissipation	—	2.2	2.67	W	Maximum at 3.47V, Outputs Open, 25°C, 136MHz Ck, PRBS 2^7-1 parallel input pattern
I_{DD}	Supply current (All Supplies)	—	—	770	mA	
I_{DDA}	Supply current on V_{DDA}	—	100	—	mA	

Note: (1) Refer to Application Note, AN-37, for differential measurement techniques.

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Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD}) ..... -0.5V to +4V
DC Input Voltage (PECL inputs) ..... -0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to 5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (PECL Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^{o} to $+125^{o}$C
Storage Temperature ..... -65^{o}C to $+150^{o}$C
Maximum Input ESD (Human Body Model) ..... 2000 V

Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) ..... +3.3V±5%
Operating Temperature Range ..... 0^{o}C Ambient to $+100^{o}$C Case Temperature

Notes:

(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

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Table 5: Pin Table

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	GNDT	VCC	GNDT	SYN1	RC10	RX10	RX14	RX16	VCCT	VCC	GNDT	RX21	VCCT	RX28	GNDT	VCCT	GNDT
B	RX07	RX08	RX09	GNDT	RC11	RX11	VCCT	RX17	GND	SYN2	RX20	RX22	RX25	RX29	SYN3	RC30	RC31
C	RX04	RX05	RX06	VCCT	VCCT	RX12	GNDT	RX18	NC	RC20	VCCT	RX23	RX26	VCC	VCCT	GNDT	RX30
D	RX00	RX01	VCCT	GNDT	GND	RX13	RX15	RX19	NC (TMS)	RC21	GNDT	RX24	RX27	RX31	RX32	RX33	RX34
E	RC00	RC01	RX02	RX03										VCCT	GNDT	RX35	RX36
F	NC	SYN0	VCCT	GNDT										RX37	RX38	RX39	GND
G	TX18	TX19	GND	VCC										TX22	TX21	TX20	VCCT
H	TX14	TX15	TX16	TX17										TX26	TX25	TX24	TX23
J	TX10	TX11	TX12	TX13										VCC	TX29	TX28	TX27
K	NC	NC (TDO)	GND	GND										GND	GND	VCC	NC
L	TX08	TX09	GND	VCC										TX33	TX32	TX31	TX30
M	TX04	TX05	TX06	TX07										TX37	TX36	TX35	TX34
N	TX00	TX01	TX02	TX03										LOOP	VCC	TX39	TX38
P	NC	NC	NC	GND	SO0-	GND	SO1-	GND	CAP0	GND	SO2+	GND	SO3+	GND	NC (TDI)	NC	NC
R	RFC1	NC	GND	VCC	SO0+	GND	SO1+	GNDA	CAP1	GND	SO2-	GND	SO3-	VCC	GND (TRSTN)	VCCTR	SYNC
T	RCM0	GND	VCC	VCC	VCCP0	GND	VCCP1	GND	VCCA	GND	VCCP2	GND	VCCP3	VCC	GND	GNDTR	NC (TCK)
U	GND	GND	SI0-	SI0+	VCC	SI1-	SI1+	GND	GND	SI2-	SI2+	GND	SI3-	SI3+	GND	GND	GND

NOT POPULATED

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Table 6: Pin Description

Pin	Name	Description
N1, N2, N3 N4, M1, M2, M3, M4, L1 L2	TX0-0, TX0-1, TX0-2 TX0-3, TX0-4, TX0-5, TX0-6, TX0-7, TX0-8 TX0-9	INPUT - TTL: 10-bit Transmit bus for Channel 0. Parallel data on this bus is latched on the rising edge of REF. TX0-0 is transmitted first.
J1, J2, J3 J4, H1, H2 H3, H4, G1 G2	TX1-0, TX1-1, TX1-2 TX1-3, TX1-4, TX1-5, TX1-6, TX1-7, TX1-8, TX1-9	INPUT - TTL: 10-bit Transmit bus for Channel 1. Parallel data on this bus is latched on the rising edge of REF. TX1-0 is transmitted first.
G16, G15, G14 H17, H16, H15 H14, J17, J16 J15	TX2-0, TX2-1, TX2-2 TX2-3, TX2-4, TX2-5, TX2-6, TX2-7, TX2-8, TX2-9	INPUT - TTL: 10-bit Transmit bus for Channel 2. Parallel data on this bus is latched on the rising edge of REF. TX2-0 is transmitted first.
L17, L16, L15 L14, M17, M16 M15, M14, N17 N16	TX3-0, TX3-1, TX3-2, TX3-3, TX3-4, TX3-5, TX3-6, TX3-7, TX3-8, TX3-9	INPUT - TTL: 10-bit Transmit bus for Channel 3. Parallel data on this bus is latched on the rising edge of REF. TX3-0 is transmitted first.
R1	RFC1	INPUT - TTL: TTL Reference clock. This rising edge of RFC1 provides the reference clock, at 1/10th of the baud rate to the Clock Multiplying PLL. The rising edge of RFC1 will latch TXi(0:9) on all four channels
R5, P5 R7, P7 P11, R11 P13, R13	SO0+, SO0- SO1+, SO1- SO2+, SO2- SO3+, SO3-	OUTPUT - Differential PECL (AC Coupling recommended) These pins output the serialized transmit data for Channels 0-3 when LOOP is LOW. When LOOP is HIGH, SOi+ is HIGH and SOi- is LOW.
D1, D2, E3 E4, C1, C2 C3, B1, B2 B3	RX0-0, RX0-1, RX0-2, RX0-3, RX0-4, RX0-5, RX0-6, RX0-7, RX0-8, RX0-9	OUTPUT - TTL: 10-bit Receive bus for Channel 0. Parallel data on this bus is synchronous to RC0-0 and RC0-1. RX0-0 is the first bit received.
A6, B6, C6 D6, A7, D7 A8, B8, C8 D8	RX1-0, RX1-1, RX1-2, RX1-3, RX1-4, RX1-5, RX1-6, RX1-7, RX1-8, RX1-9	OUTPUT - TTL: 10-bit Receive bus for Channel 1. Parallel data on this bus is synchronous to RC1-0 and RC1-1. RX1-0 is the first bit received.
B11, A12, B12 C12, D12, B13 C13, D13, A14 B14	RX2-0, RX2-1, RX2-2, RX2-3, RX2-4, RX2-5, RX2-6, RX2-7, RX2-8, RX2-9	OUTPUT - TTL: 10-bit Receive bus for Channel 2. Parallel data on this bus is synchronous to RC2-0 and RC2-1. RX2-0 is the first bit received.

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Pin	Name	Description
C17, D14, D15 D16, D17, E16 E17, F14, F15 F16	RX3-0, RX3-1, RX3-2, RX3-3, RX3-4, RX3-5, RX3-6, RX3-7, RX3-8, RX3-9	OUTPUT - TTL: 10-bit Receive bus for Channel 3. Parallel data on this bus is synchronous to RC3-0 and RC3-1. RX3-0 is the first bit received.
T1	RCM0	INPUT - TTL: Recovered clock MODE control. When LOW, RCi0/RCi1 is 1/20th of the incoming baud rate. When HIGH, RCi0/RCi1 is 1/10th the incoming baud rate.
E1 E2	RC00 RC01	OUTPUT - Complementary TTL: Recovered complementary clocks for Channel 0 at 1/10th the incoming baud rate (RCM=HIGH) or 1/20th (RCM=LOW). Synchronous to the RX0(0:9) bus and SYN0.
A5 B5	RC10 RC11	OUTPUT - Complementary TTL: Recovered complementary clocks for Channel 1 at 1/10th the incoming baud rate (RCM=HIGH) or 1/20th (RCM=LOW). Synchronous to the RX1(0:9) bus and SYN1.
C10 D10	RC20 RC21	OUTPUT - Complementary TTL: Recovered complementary clocks for Channel 2 at 1/10th the incoming baud rate (RCM=HIGH) or 1/20th (RCM=LOW). Synchronous to the RX20:9) bus and SYN2.
B16 B17	RC30 RC31	OUTPUT - Complementary TTL: Recovered complementary clocks for Channel 3 at 1/10th the incoming baud rate (RCM=HIGH) or 1/20th (RCM=LOW). Synchronous to the RX3(0:9) bus and SYN3.
U4, U3 U7, U6 U11, U10 U14, U13	SI0+, SI0- SI1+, SI1- SI2+, SI2- SI3+, SI3-	INPUT - Differential PECL (AC Coupling recommended): Serial receive data inputs for Channels 0-3 which are selected when LOOP is LOW. [Internally biased to VDD/2]
N14	LOOP	INPUT - TTL: Parallel Loopback Enable input. SIi is input to the CRU for Channel i (normal operation) when LOOP is LOW. When HIGH, internal loopback paths from SOi to SIi are enabled.
R17	SYNC	INPUT - TTL: Enables SYNi and word alignment when HIGH. When LOW, keeps current word alignment and disables SYNi (always LOW).
F2 A4 B10 B15	SYN0 SYN1 SYN2 SYN3	OUTPUT - TTL: Comma Detect for Channel i. This output goes HIGH for half of an RCi1 period to indicate that RXi(0:9) contains a Comma Character (‘0011111XXX’). SYNi will go HIGH only during a cycle when RCi0 is rising. SYNi is enabled when SYNC is HIGH.
P9 R9	CAP0 CAP1	ANALOG: Loop Filter capacitor for the Clock Multiply Unit. Typically 0.1 uF connected between CAP0 and CAP1. Amplitude is less than 3.3V.
T17	NC (TCK)	(INPUT - TTL: JTAG Test Clock)
D9	NC (TMS)	(INPUT - TTL: JTAG Test Mode Select)
R15	GND (TRSTN)	(INPUT - TTL: JTAG Test Reset, Active Low)
P15	NC (TDI)	(INPUT - TTL: JTAG Test Data Input)

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Pin	Name	Description
K2	NC (TDO)	(OUTPUT - TTL: JTAG Test Data Output)
T9	VCCA	Analog Power Supply
R8	GNDA	Analog Ground. Tie to common ground plane with GND.
A2,A10,C14 G4,J14,K16 L4,N15,R4 R14,R16,T3 T4,T14,U5	VCC	Digital Logic Power Supply
C4, D3,F3 A9, B7, C5 A13, A16, C11 C15, E14, G17	VCCT	TTL Output Power Supply.
T5 T7 T11 T13	VCCP0 VCCP1 VCCP2 VCCP3	PECL I/O Power Supply for Channel i.
A1,A3,A11,A15 A17,B4,C7 C16,D4,D11 E15,F4	GNDT	Ground for TTL Outputs
B9,F17,G3,K3, K14,K15,L3,P6, P8,P10,P12,P14 R6,R10,R12,T2 T6,T8,T10,T12 T15,T16,U1,U2, U8,U9,U12,U15 U16, U17	GND	Ground

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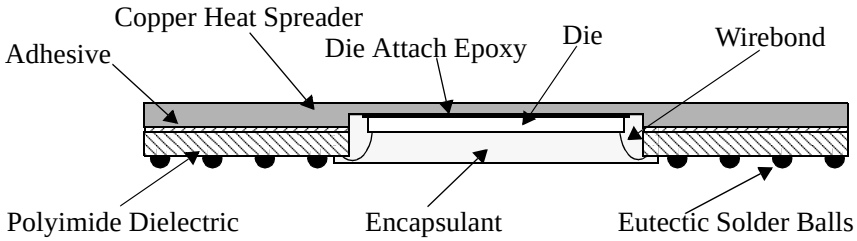
Package Thermal Characteristics

The VSC7186 is packaged in a 23 mm BGA package with 1.27mm eutectic ball spacing. The construction of the package is shown below.

Figure 6: Package Cross Section



The VSC7186 is designed to operate with a case temperature up to 100°C. In order to comply with this target, the user must guarantee that the case temperature specification of 100°C is not violated. With the Thermal Resistances shown below, the VSC7186 can operate in still air ambient temperatures of 40°C [40°C = 100°C - 2.5W * 24°C/W]. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided.

Table 7: Thermal Resistance

Symbol	*Description*	*Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	4.3	°C/W
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads.	24	°C/W
θ_{ca-100}	Thermal resistance from case to ambient with 100 LFM airflow	21	°C/W
θ_{ca-200}	Thermal resistance from case to ambient with200 LFM airflow	18.5	°C/W
θ_{ca-400}	Thermal resistance from case to ambient with 400 LFM airflow	17	°C/W
θ_{ca-600}	Thermal resistance from case to ambient with 600 LFM airflow	15	°C/W

Moisture Sensitivity Level

This device is rated at with a Moisture Sensitivity Level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

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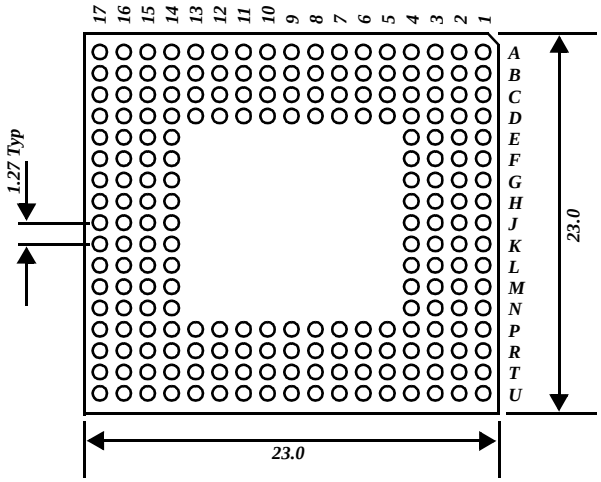
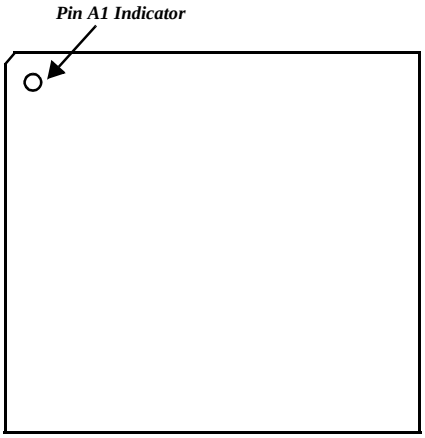
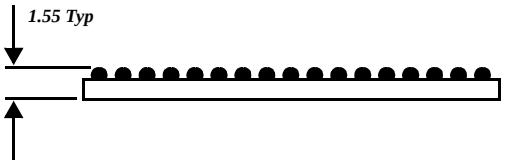
Package Information



BOTTOM VIEW



TOP VIEW



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Ordering Information

The part number for this product is formed by a combination of the device number and the package style:

VSC7186TW

Device Type:

VSC7186: Quad Gigabit Transceiver

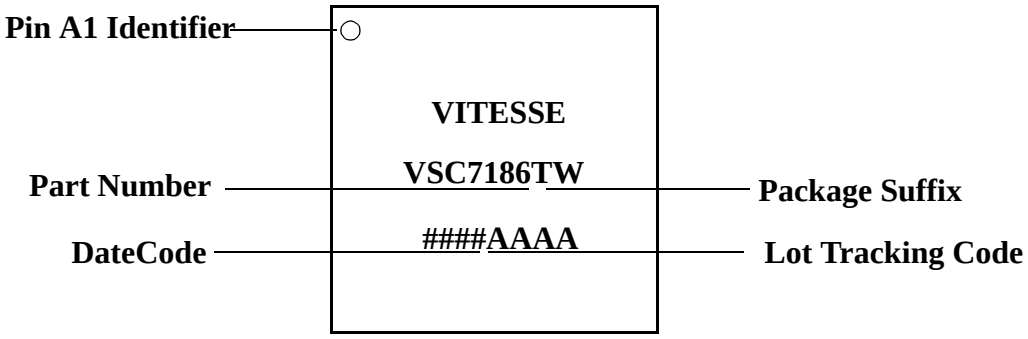
Package Style

TW: 208 pin, 23 mm BGA

Marking Information

The package is marked with three lines of text as shown below.

Figure 7: Package Marking Information



Notice

This document contains information about a product during its fabrication or early sampling phase of development. The information contained in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this data sheet is current prior to design or order placement.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without written consent is prohibited.

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