

SED1600F

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

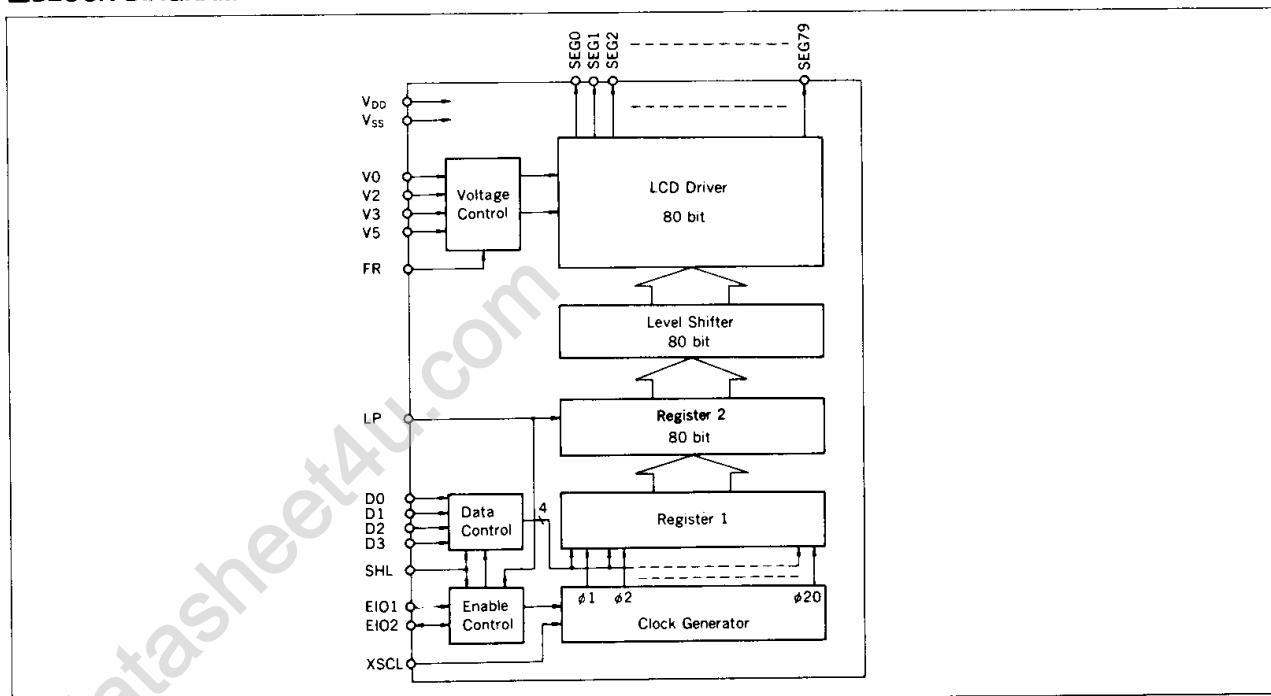
DESCRIPTION

The SED1600F is an 80 output segment (column) driver, used to driver large-capacity dot matrix LCD panels with a duty ratio of 1/300 (from 1/100). It is used in conjunction with the SED1610F or SED1630F common (row) drivers. The SED1600F has a wide range of drive voltages. The maximum voltage V_0 is isolated from V_{DD} to enable the application of any external LCD driving bias voltage from outside to the SED1600F. These unique features enable the SED1600F to operate with a wide variety of LCD panels. The SED1600F requires no enable signal to implement an enable chain technology which provides low power dissipation. This offers simpler interface with the LCD controller SED1330F/SED1341F or a microprocessor.

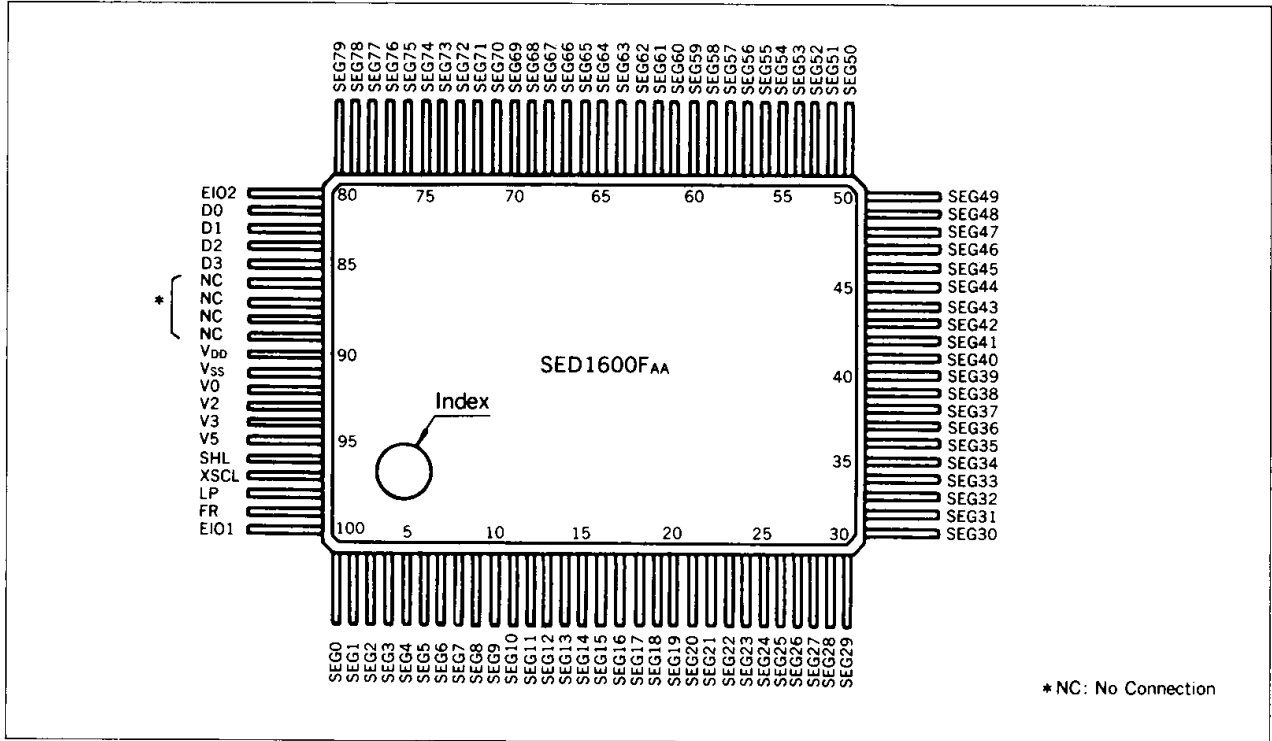
FEATURES

- 80 LCD driving outputs
- Display capacity 640 × 200 × 3 dots when combined with SED1610F (SED1630F)
- Wide range of LCD driving voltages 12 to 28V
(Absolute maximum voltage 30V)
- High-speed, low-power data transfer by 4-bit bus enable chain technology
Shift clock 6MHz Max
- Enable auto-transfer function to allow cascade connection and low power dissipation (requiring no enable signal to be furnished by a controller)
- Output shift direction pin selectable
- Ability to adjust offset bias of LCD source from V_{DD}
- Power supply for the logic $-5V \pm 10\%$
- Si gate CMOS process
- Package 100-pin QFP (plastic)

BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin name	I/O	Functions																																																														
SEG0 to SEG79	O	LCD driving segment (column) outputs. Each output changes at the falling edge of LP.																																																														
D0 to D3	I	Display data inputs.																																																														
XSCL	I	Shift clock of display data (falling edge trigger).																																																														
LP	I	Latch pulse of display data (falling edge trigger).																																																														
EIO1, EIO2	I/O	Enable I/O, which is controlled by SHL input. Output is reset by LP, and automatically falls when 80 bits of data are taken in.																																																														
SHL	I	Shift direction selection and EIO pin I/O control. When data (a, b, c, d) (e, f, g, h).....(w, x, y, z) are input to pins (D3, D2, D1, D0) respectively, the following relation is established between the data and segment outputs:																																																														
		<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">SHL</th> <th colspan="12">SEG</th> <th colspan="2">EIO</th> </tr> <tr> <th>79</th><th>78</th><th>77</th><th>76</th><th>75</th><th>74</th><th>73</th><th>72</th><th>.....</th><th>3</th><th>2</th><th>1</th><th>0</th><th>1</th><th>2</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>.....</td><td>w</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td> </tr> <tr> <td>H</td> <td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>u</td><td>t</td><td>s</td><td>.....</td><td>d</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td> </tr> </tbody> </table>	SHL	SEG												EIO		79	78	77	76	75	74	73	72	3	2	1	0	1	2	L	a	b	c	d	e	f	g	h	w	x	y	z	Output	Input	H	z	y	x	w	v	u	t	s	d	c	b	a	Input	Output
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FR	I	AC signal of LCD driving outputs.																																																														
V _{DD} , V _{SS}	Power supplies	Logic circuit power. V _{DD} : 0V (GND) V _{SS} : -5.0V																																																														
V0, V2, V3, V5	Power supplies	LCD driving power. V5: -12 to -28V V _{DD} ≥ V0 ≥ V2 > V3 ≥ V5																																																														

■ ABSOLUTE MAXIMUM RATINGS

(V_{DD} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V _{SS}	-7.0 to +0.3	V
Supply voltage (2)	V5	-30.0 to +0.3	V
Supply voltage (2)	V0, V2, V3*	V5 - 0.3 to +0.3	V
Input voltage (1)	V _I	V _{SS} - 0.3 to +0.3	V
Output voltage (1)	V _O	V _{SS} - 0.3 to +0.3	V
Output current (1)	I _O	20	mA
Output current (2)	I _{OSEG}	20	mA
Allowable power dissipation	P _D	300	mW
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-65 to +150	°C
Soldering temperature·time	T _{sol}	260°C, 10s (at lead)	—

*V0, V2 and V3 must always satisfy the condition: V_{DD} ≥ V0 ≥ V2 ≥ V3 ≥ V5.

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(Unless otherwise specified, V_{DD} = V0 = 0V, V_{SS} = -5.0V ± 10%, and Ta = -20 to 75°C)

Parameter	Symbol	Conditions	Pin	Min	Typ	Max	Unit
Operating voltage (1)	V _{SS}		V _{SS}	-5.5	-5.0	-4.5	V
Recommended operating voltage Minimum operating voltage	V5		V5	-28.0	—	-12.0 -8.0	V
Operating voltage (2)	—	Recommended value	V0	-2.5	—	0	V
Operating voltage (3)	V2	Recommended value	V2	3/9·V5	—	V0	V
Operating voltage (4)	V3	Recommended value	V3	V5	—	6/9·V5	V
“H” input voltage	V _{IH}		EIO1, EIO2, XSCL, LP, D0 to D3, FR, SHL	0.2V _{SS}	—	—	V
“L” input voltage	V _{IL}			—	—	0.8V _{SS}	V
“H” output voltage	V _{OH}	I _{OH} = -0.6mA	EIO1, EIO2	-0.4	—	—	V
“L” output voltage	V _{OL}	I _{OL} = 0.6mA		—	—	V _{SS} + 0.4	V
Input leakage current	I _{LI}	V _{SS} ≤ V _I ≤ 0V	D0 to D3, XSCL, LP, SHL, FR	—	—	2.0	μA
	I _{LI/O}	V _{SS} ≤ V _I ≤ 0V	EIO1, EIO2	—	—	5.0	μA
Stand-by current	I _{DDs}	V5 = -12.0 to -28.0V V _{IH} = V _{DD} , V _{IL} = V _{SS}	V _{DD}	—	—	25	μA
Output resistance	R _{SEG}	ΔV _{on} = 0.5V	V5	-20.0V	SEG0 to SEG79	1.5	kΩ
				-14.0V		2.0	
				-8.0V		3.0	
Current dissipation (1)	I _{SS01}	V _{SS} = -5.0V, V _{IH} = V _{DD} , V _{IL} = V _{SS} , f _{XsCL} = 1.92MHz f _{LP} = 12kHz, Frame period = 60Hz Input data: Inverted bit by bit No-load	V _{SS}	—	120	500	μA
Current dissipation (2)	I _{SS02}	V _{SS} = -5.0V, V2 = -4.0V V3 = -16.0V, V5 = -20.0V All other conditions are same as I _{SS01} .	V5	—	20	100	μA
Input capacitance	C _I	Ta = 25°C	D0 to D3, XSCL, LP, FR, SHL	—	—	8.0	pF
	C _{I/O}		EIO1, EIO2	—	—	15.0	pF

● AC Electrical Characteristics

(V_{SS} = -5.0 ± 10%, T_a = -20 to 75°C)

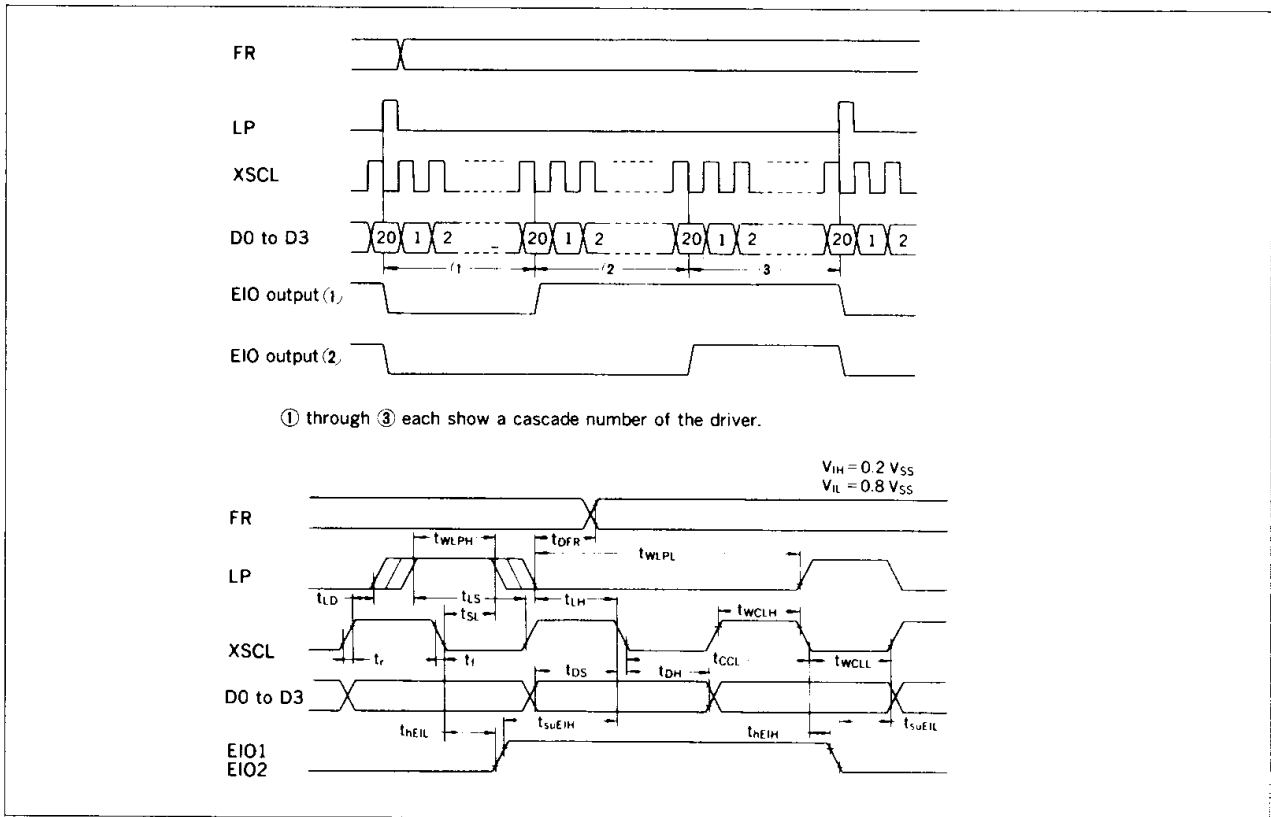
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
XSCL period	t _{CCL}	t _r , t _f ≤ 10ns	166	—	—	ns
XSCL "H" pulse width	t _{WCLH}		70	—	—	ns
XSCL "L" pulse width	t _{WCLL}		70	—	—	ns
Data setup time	t _{DS}		60	—	—	ns
Data hold time	t _{DH}		40	—	—	ns
XSCL-rise to LP-rise time	t _{LD}		0	—	—	ns
XSCL-fall to LP-fall time	t _{SL}		70	—	—	ns
LP-rise to XSCL-rise time	t _{LS}		70	—	—	ns
LP-fall to XSCL-fall time	t _{LH}		70	—	—	ns
LP "H" pulse width	t _{WLPH}		70	—	—	ns
LP "L" pulse width	t _{WLPL}		230	—	—	ns
Alloable FR delay time	t _{DFR}		-500	—	500	ns
Enable "H" setup time	t _{SUEIH}		40	—	—	ns
Enable "H" hold time	t _{HEIH}		0	—	—	ns
Enable "L" setup time	t _{SUEIL}		0	—	—	ns
Enable "L" hold time	t _{HEIL}		0	—	—	ns
Input signal rise time	t _r		—	—	50*	ns
Input signal fall time	t _f		—	—	50*	ns

*The specifications for t_r and t_f are provided to prevent a malfunction which may occur when noise is mixed with a slow-down signal. To assure high-speed XSCL, both t_r and t_f must satisfy the following relation:

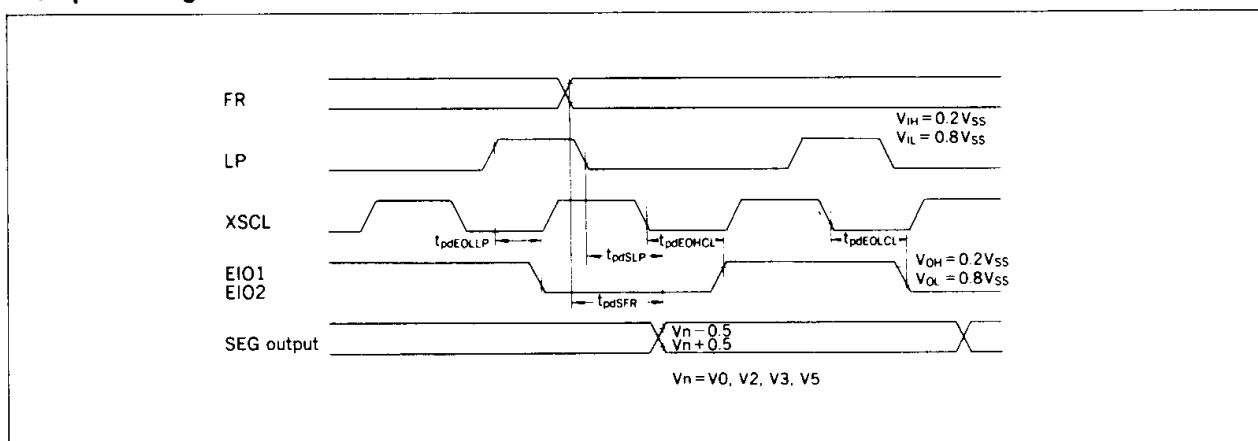
$$t_r, t_f < \frac{t_{CCL} - (t_{WCLH} + t_{WCLL})}{2}$$

● Timing Chart

○ Input Timing



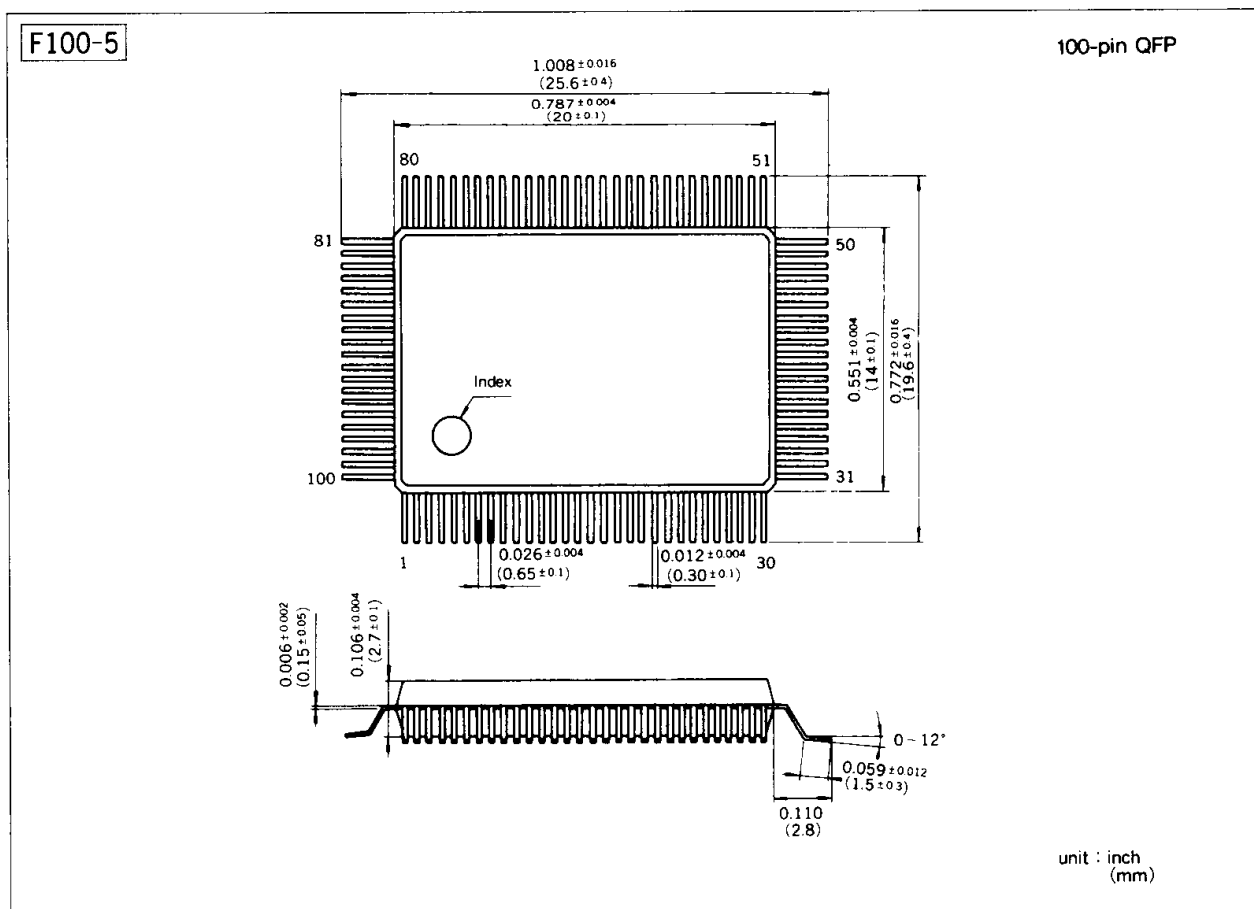
○ Output Timing



($V_{SS} = -5.0 \pm 10\%$, $T_a = -20$ to 75°C)

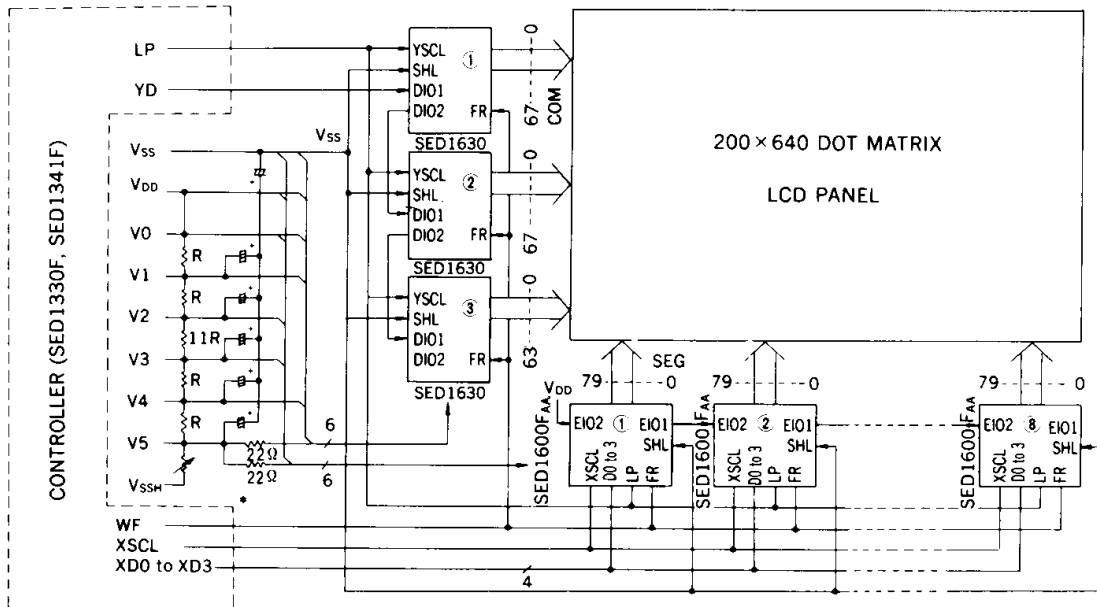
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(LP-rise to disable) time	$t_{pdEOLLP}$	XSCL = "L"	—	—	70	ns
(XSCL-fall to disable) time	$t_{pdEOLCL}$	LP = "H"	—	—	70	ns
(XSCL-fall to enable) time	$t_{pdEOHCL}$		—	—	100	ns
(LP-fall to SEG output) time	t_{pdSLP}	$V_5 = -12.0$ to -28.0V	—	—	4.5	μS
(FR to SEG output) delay time	t_{pdSFR}	$C_L = 100\text{pF}$	—	—	4.5	μS

■ PACKAGE DIMENSIONS



EXAMPLE OF APPLICATION (SED1600F_{AA})

for 200×640 DOT MATRIX LCD



*Be sure to connect a current limiter resistor. Also, connect decoupling capacitors (0.01μF) near pins V_{SS} and V₅ of each LSI for noise protection.