Data Sheet

VSC7140

1.0625 Gb/s Fibre Channel
Dual Repeater / Hub Node

Features

- Supports ANSI X3T11 1.0625Gb/s, FC-AL Disk Attach for Resiliency
- Dual Digital Clock Recovery Units
- Dual Digital Signal Detect Units
- Dual Port Bypass Circuits
- 106.25 or 53.125 MHz Reference Clock
- Implements 2 Hub Nodes
- Provides Bi-directional Signal Clean-up.
- 1.2 W Typical Power Dissipation
- 3.3V Power Supply
- 52-Pin, 10mm PQFP

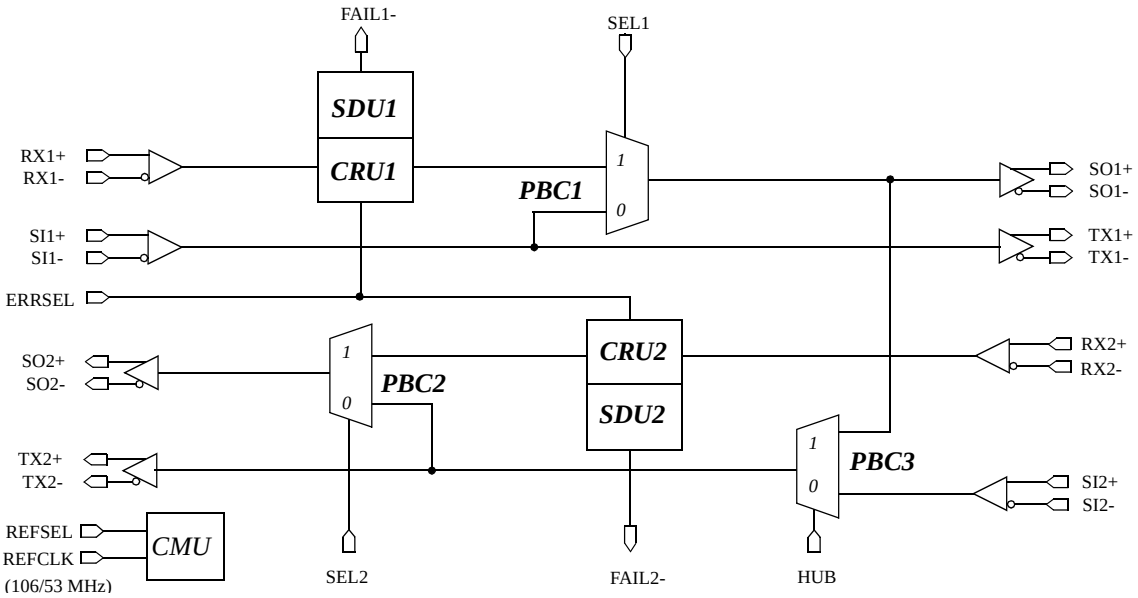
General Description

The VSC7140 is a dual Fibre Channel repeater which can be used in Hubs, JBODs or any Fibre Channel Subsystem requiring clean incoming and outgoing signals at a bulkhead connector. The digital Clock Recovery Unit (CRU) recovers incoming data from an external device, amplifies it and attenuates jitter. A digital Signal Detect Unit (SDU) determines whether the incoming signal contains invalid Fibre Channel data. A 2:1 multiplexer forms a Port Bypass Circuit (PBC) to route either recovered incoming data or SI to SO.

Fibre Channel subsystems requiring signal cleanup at the bulkhead would connect RX1 to the incoming signal and SO1 to the internal subsystem's input. RX2 would connect to the output of the subsystem and SO2 would connect to the bulkhead.

For Hub applications, SI would connect to the previous Hub Node and output data to the external device on TX. Incoming data from the external device on RX is recovered and cleaned up and passed to the next Hub node on SO. If the external device is not functional, SI is passed to SO.

VSC7140 Block Diagram



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Functional Description

The VSC7140 contains two fully integrated repeaters to improve signal quality and determine whether the input to the repeater contains invalid Fibre Channel data. Each repeater consists of a Clock Recovery Unit (CRU) and a digital Signal Detect Unit (SDU). The CRU locks onto the incoming signal, generates a recovered clock (nominally 1.0625 GHz) and uses this clock to resynchronize the incoming signal. The recovered data has improved signal quality due to amplification and jitter attenuation. Recovered data is retimed to the recovered clock, not to the reference clock, REFCLK. The design of the CRU eliminates the need for any Lock-to-Reference signal since, in the absence of data, the CRU locks onto REFCLK automatically which eliminates the need for any external control.

The Signal Detect Units (SDUs) test the recovered data from the CRUs for invalid Fibre Channel data by looking for run length errors (more than 5 consecutive 1's or 0's) and the absence of a seven bit pattern found in the K28.5 character of either disparity ('0000101' or '1111010'). This K28.5 pattern should occur between all valid Fibre Channel frames. The maximum length of a Fibre Channel frame is 2148 bytes (or 21,480 encoded bits) and the SDU divides time into 1-1/2 maximum frames with a 15-bit counter (~31 microseconds). At the end of each interval, any run length or K28.5 errors which occured during the interval are stored internally for use by the state machine which drives the SDU output, FAILn-.

The ERRSEL input controls both SDUs while the FAILn- outputs provide the status of each SDU. ERRSEL selects two different modes generated by the SDU; Single Frame (LOW) or Multiple Frame (HIGH) error modes. In Single Frame Error Mode, any error condition that occurs within the 1-1/2 frame interval causes FAILn- to be asserted LOW immediately after that interval. FAILn- remains asserted until immediately after an error free interval. In Multiple Frame Error Mode, FAILn- is asserted after four consecutive intervals containing errors and remains asserted until after four consecutive error-free intervals occur. The intent of the Multiple Frame Error Mode is to allow FAIL1- or FAIL2- to be directly connected to the Port Bypass Circuit controls, SEL1 or SEL2, in order to configure the part to isolate RX1 or RX2 whenever invalid data is present. Single Frame Error Mode allows the user to develop their own algorithm for monitoring data and controlling SEL1 or SEL2.

A TTL reference clock, REFCLK, is used by the internal Clock Multiplier Unit (CMU) to generate a baud rate clock (nominally 1.0625 GHz). If REFSEL is HIGH, the CMU multiplies REFCLK (nominally 106.25 MHz) by a factor of 10. If REFSEL is LOW, the CMU multiplies REFCLK (nominally 53.125 MHz) by a factor of 20. The user must ensure that REFSEL is properly set in order to match the frequency of REFCLK.

Three Port Bypass Circuits (PBC) contain differential 2:1 muxes operating at 1.0625 Gb/s for routing serial data. SEL1 configures PBC1 to select either the output of CRU1 (HIGH) or SI1 (LOW) to drive SO1. SEL2 configures PBC2 to select either the output of CRU2 (HIGH) or the output of PBC3 (LOW) to drive SO2. HUB configures PBC3 to select either the output of PBC1 (HIGH) or SI2 (LOW) to drive the input to PBC2.

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Application Examples

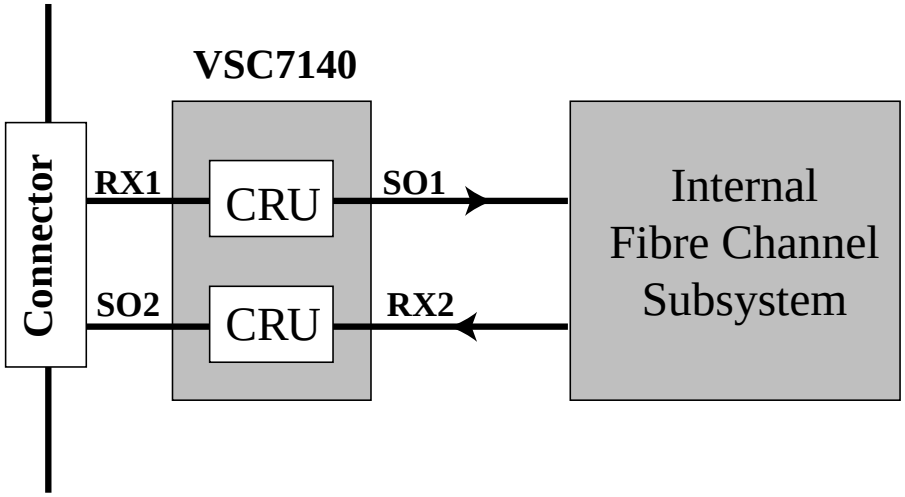
The VSC7140 is intended for two applications, Dual Repeater or Dual Hub, as configured by HUB. Users needing to retime both incoming and outgoing signals at the bulkhead of a Fibre Channel system would use the part in Dual Repeater Mode (HUB is LOW). Users building Fibre Channel Hubs would use the part in Dual Hub mode (HUB is HIGH) to fully handle the functions of two Hub Nodes.

Dual Repeater Mode

In this example, the VSC7140 forms a dual repeater in a complex Fibre Channel system, such as a JBOD (Just a Bunch Of Disks) RAID (Redundant Array of Independent Disks) subsystem, which requires the incoming Fibre Channel signal to be retimed to ensure adequate signal quality to the input of the subsystem. Likewise, the output of the JBOD subsystem requires retiming to ensure that the outgoing signal from the system meets the amplitude and jitter requirements of Fibre Channel. For this application, the dual CRUs are the only circuits required although the SDUs may be used for reporting signal status. Therefore, the VSC7140 would be configured as follows:

HUB is LOW to select Dual Repeater Mode.
RX1 connects to the external input from the bulkhead.
SO1 connects to the input to the JBOD subsystem.
RX2 connects to the output of the JBOD subsystem.
SO2 connects to the output to the bulkhead.
SI1 and SI2 are not used. Pull up SI1+ and SI2+ to V_{DD} with 22k Ohms to prevent input oscillations.
TX1 and TX2 are not used. Leave unconnected.
SEL1 and SEL2 are driven HIGH.
FAIL1- and FAIL2- may be used for status. ERRSEL is selected as desired by the user.

Figure 1: Block Diagram: Use of VSC7140 in Dual Repeater Mode



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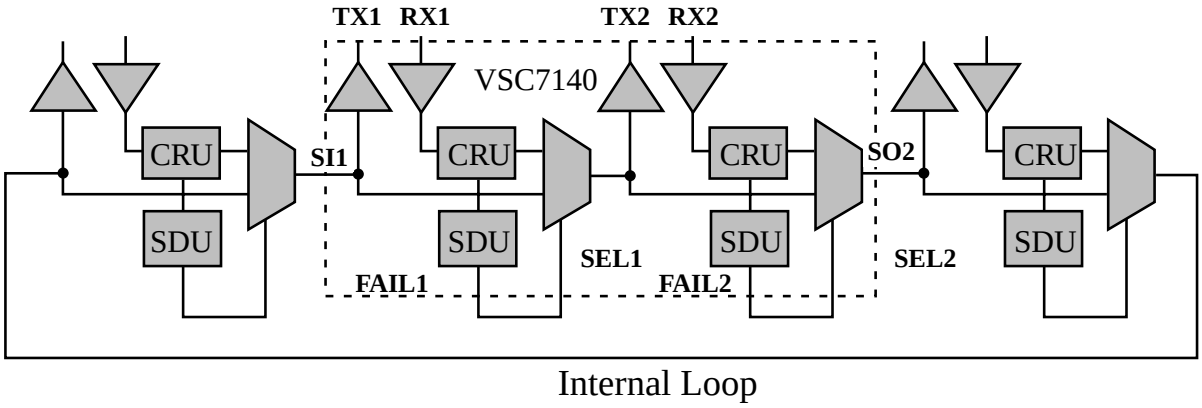
Dual Hub Mode

In this example, the VSC7140 is used to fully implement two adjacent nodes in a Fibre Channel Hub. Incoming external signals on RX require retiming to improve amplitude and eliminate jitter before being used by the Hub. The TX outputs drive the external device. A serial loop is formed by daisy chaining the SI to SO paths of each node. The SDUs are required to configure the Hub to include external devices on the SI/SO loop if they produce valid Fibre Channel data or to exclude them from the loop if they are not operational.

HUB is HIGH to select Hub Mode.
RX1 connects to the external output from Device #1. TX1 connects to the external input to Device #1.
RX2 connects to the external output from Device #2. TX2 connects to the external input to Device #2.
SI1 is connected to the SO2 output of the previous VSC7140. SI2 is pulled up SI2+ with 22k Ohms.
SO2 is connected to the SI1 input of the next VSC7140. SO1 is left unconnected.
If ERRSEL is HIGH, FAIL1- connects to SEL1 and FAIL2- connects to SEL2.
If ERRSEL is LOW, FAIL1- and FAIL2- are used by off-chip circuits to control SEL1 and SEL2.

Figure 2: Block Diagram: Use of VSC7140 in Hub Mode



Note: SO1 and SI2 not used.

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AC Characteristics

Figure 3: AC Timing Diagrams

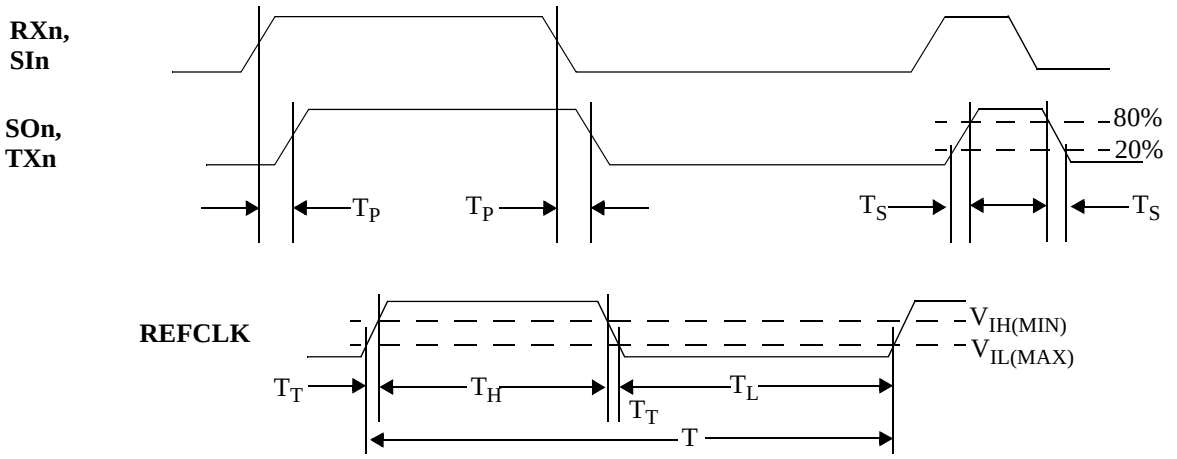

Table 1: AC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
	Differential Inputs/Outputs				
T_P	Latency from Serial Input (RXn/ SIn) to Serial Output (TXn/SOn)	0.25	7.0	ns	
T_S	Differential Output Rise/Fall time	—	300	ps	Between 20% and 80%
	Reference Clock Requirements				
T_T	REFCLK input rise/fall times	—	2.0	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$
F	REFCLK Frequency	105 52.5	108 54	MHz	106.25 MHz Nom.; REFSEL is HIGH 53.125 MHz Nom.; REFSEL is LOW
F_O	Frequency Offset	-200	+200	ppm	Maximum frequency offset between 10 or 20 times REFCLK and the datarate of the serial input to the CRU.
DC	REFCLK Duty Cycle	35	65	%	Measured at 1.5V
T_H , T_L	REFCLK Input HIGH/LOW time	2.5	—	ns	From $V_{IH(MIN)}$ to $V_{IH(MIN)}$ or $V_{IL(MAX)}$ to $V_{IL(MAX)}$

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DC Characteristics *(Over recommended operating conditions).*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	Output LOW Voltage (TTL)	—	—	0.5	V	I_{OL}= +1.0mA
V_{DD}	Supply voltage	3.14	—	3.47	V	V_{DD} = 3.3V $\pm$ 5%
P_D	Power Dissipation	—	1.2	1.7	W	Outputs open, V_{DD} = V_{DD} max
I_{DD}	Supply current	—	365	490	mA	Outputs open, V_{DD} = V_{DD} max
ΔV_{IN}	PECL input swing: SIn, RXn	300	—	2600	mVp-p	AC Coupled. Internally biased at $V_{DD}/2$
ΔV_{OUT75}	PECL output swing: TXn, SOn	1200	—	2200	mVp-p	75Ω to V_{DD} – 2.0 V
ΔV_{OUT50}	PECL output swing: TXn, SOn	1200	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{DD}) .....-0.5V to +4V
PECL DC Input Voltage ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage..... -0.5V to 5.5V
DC Voltage Applied to TTL Outputs ..... -0.5V to V_{DD} + 0.5V
TTL Output Current .....+/-50mA
PECL Output Current .....+/-50mA
Case Temperature Under Bias .....-55° to +125°C
Storage Temperature.....-65° to + 150°C
Maximum Input ESD (Human Body Model)..... 1500 V

Recommended Operating Conditions

Power Supply Voltage..... ....3.3V +/- 5%
Ambient Operating Temperature Range.....0 °C Ambient to +95°C Case

Notes:

1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

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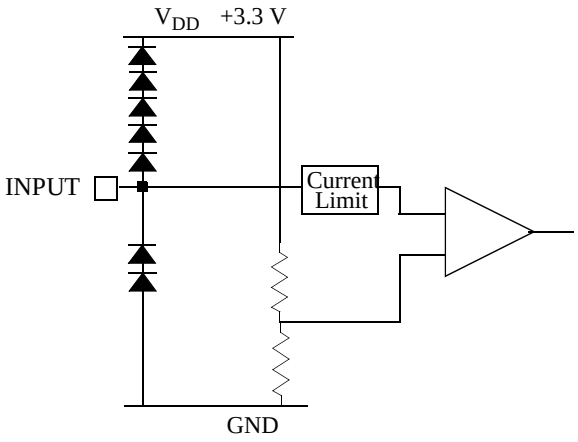
Input Structures

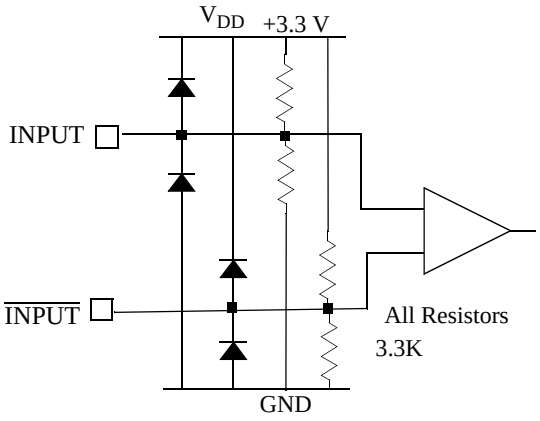
Two input structures exists in this part; TTL and High Speed, Differential Inputs. The TTL Inputs will interface with any TTL or 3.3V or 5V CMOS outputs. The High Speed, Differential Inputs are intended to be AC Coupled per the FC-PH specification. Being AC Coupled, the High Speed, Differential Input buffers are biased at $V_{DD}/2$. Refer to Figure 4, Input structures.

Figure 4: Input Structures



REFCLK and TTL Inputs

A



High Speed Differential Input
(RXn+/-, SIn+/-)

B

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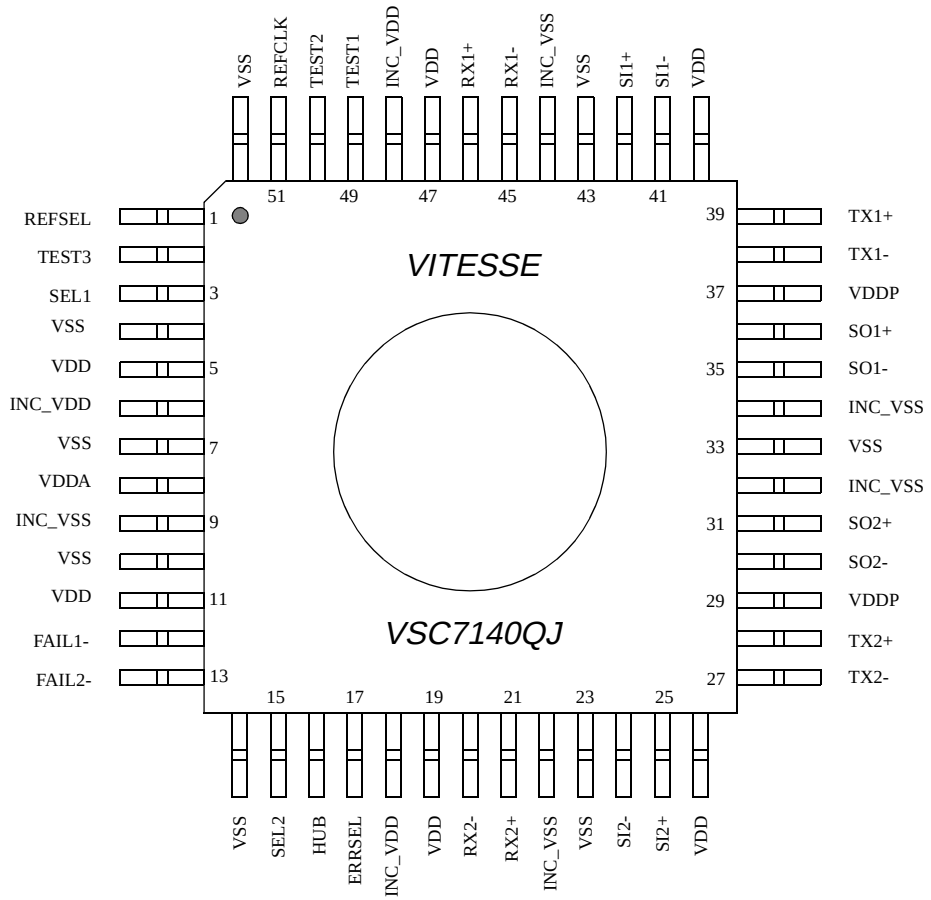
Package Pin Descriptions

Figure 5: Pin Diagram



(TOP VIEW)

NOTE: Heat spreader is not internally connected electrically.
It should not be connected electrically by the user.

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Table 2: Pin Identification

Pin #	*Name*	*Description*
46, 45 21, 20	RX1+, RX1- RX2+, RX2-	INPUT - Differential. Serial input to CRU1/CRU2. (AC Coupling recommended) (Biased internally at $V_{DD}/2$)
39, 38 28, 27	TX1+, TX1- TX2+, TX2-	OUTPUT - Differential. Serial output from PBC1/PBC2. (AC Coupling recommended)
42, 41 25, 24	SI1+, SI1-SI2+, SI2-	INPUT - Differential. Serial input. (AC Coupling recommended) (Biased internally at $V_{DD}/2$)
36, 35 31, 30	SO1+, SO1- SO2+, SO2-	OUTPUT - Differential. Serial output from PBCx to disk drive 'x'. (AC Coupling recommended).
3	SEL1	INPUT - TTL. SEL1 configures PBC1 to select either the output of CRU1 (HIGH) or SI1 (LOW) to drive SO1.
15	SEL2	INPUT - TTL. SEL2 configures PBC2 to select either the output of CRU2 (HIGH) or the output of PBC3 (LOW) to drive SO2.
16	HUB	INPUT - TTL. HUB configures PBC3 to select either the ouput of PBC1 (HIGH) or SI2 (LOW) to drive the input to PBC2.
51	REFCLK	INPUT - TTL. REFerence CLocK at 1/10th or 1/20th the baud rate (Nominally 53.125 or 106.25 MHz) as determined by REFSEL. Used for internal clock multiplier unit.
1	REFSEL	INPUT - TTL. REFclk SELect. When HIGH, REFCLK is 1/10th the baud rate and would normally be 106.25 MHz. When LOW, REFCLK is 1/20th the baud rate (53.125 MHz)
12, 13	FAIL1- FAIL2-	OUTPUT - TTL. When LOW, indicates that the output of CRU1/2 contains invalid Fibre Channel data.
17	ERRSEL	INPUT - TTL. Selects the algorithm to drive the FAIL1-/FAIL2- outputs. When HIGH, the "Multiple Frame Error Mode" is used. When LOW, the "Single Frame Error Mode" is selected.
49, 50, 2	TEST1 TEST2 TEST3	INPUT - TTL. LOW for factory test, HIGH for normal operation.
5, 11, 19, 26 40, 47	VDD	Power Supply. 3.3V Supply.
29, 37	VDDP	High-Speed Output Power Supply. 3.3V Supply for PECL drivers.
8	VDDA	Analog Power Supply. 3.3V for Clock Multiplier PLL. Bypass to pin 7.
4, 7, 10, 14 23, 33, 43, 52	VSS	Ground.
6,18,48	INC_VDD	Internally Not Connected. Connect these pins to VDD for compatibility with future versions of the VSC7140.
9,22,32, 34, 44	INC_VSS	Internally Not Connected. Connect these pins to VSS for compatibility with future versions of the VSC7140.

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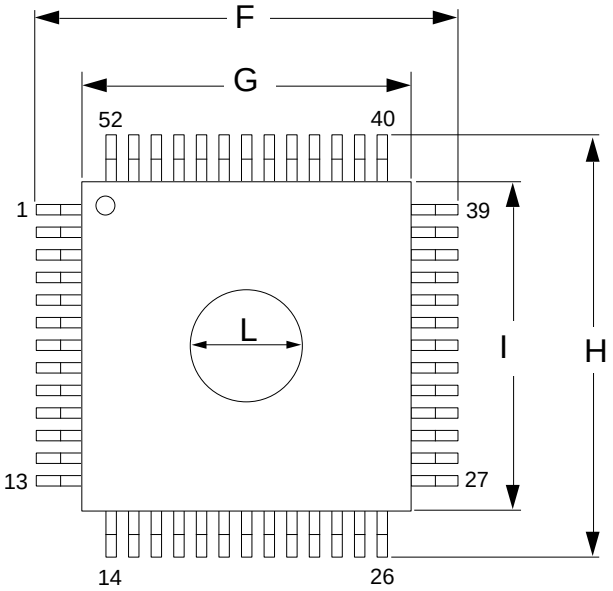
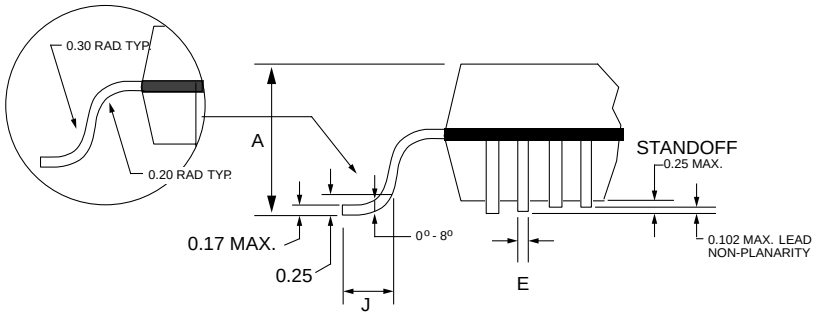
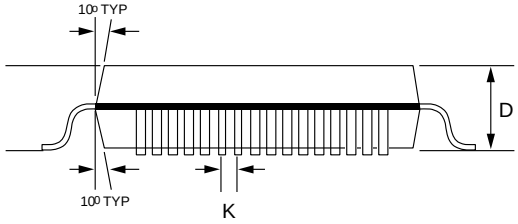
Package Information

52 (QJ) PQFP Package Drawing



Item	*mm*	*Tolerance*
A	2.45	MAX
D	2.00	+0.15/-0.10
E	0.30	±0.05
F	13.20	±0.25
G	10.00	±0.10
H	13.20	±0.25
I	10.00	±0.10
J	0.88	+0.15/-0.10
K	0.65	BASIC
L	3.56	±0.50 DIA





Notes:
Heat spreader up
All units in mm unless otherwise noted
Drawings not to scale.
Package Drawing #101-224-5 Issue #1

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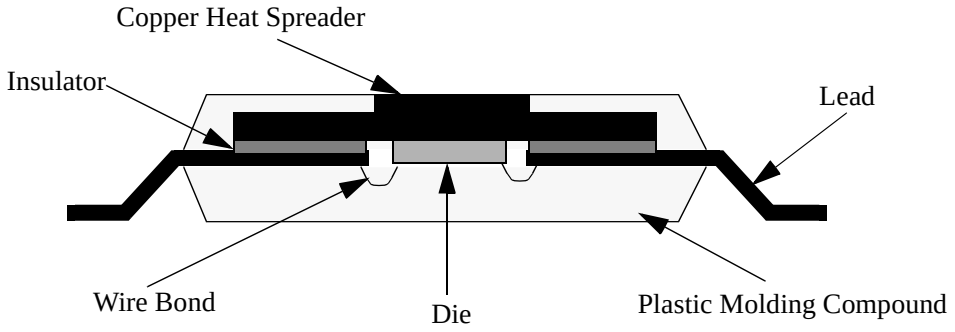
Package Thermal Characteristics

The VSC7140 is packaged into a thermally-enhanced plastic quad flatpack. This package adheres to the industry-standard EIAJ footprint for a 10x10mm body but has been enhanced to improve thermal dissipation with the inclusion of an exposed copper heat spreader. The package construction is as shown in Figure 6.

Figure 6: Package Cross Section



The thermal resistance for the VSC7140 package is improved through low thermal resistance paths from the die to the exposed surface of the heat spreader and from the die to the leadframe through the heat spreader overlap of the leadframe.

Table 3: 52 PQFP Thermal Resistance

Symbol	*Description*	*Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	2.5	^{o}C/W
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads for a non-thermally saturated board.	37.0	^{o}C/W
θ_{ca-100}	Thermal resistance from case to ambient in 100 LFPM air.	31.0	^{o}C/W
θ_{ca-200}	Thermal resistance from case to ambient in 200 LFPM air.	28.0	^{o}C/W
θ_{ca-400}	Thermal resistance from case to ambient in 400 LFPM air.	24.0	^{o}C/W
θ_{ca-600}	Thermal resistance from case to ambient in 600 LFPM air.	22.0	^{o}C/W

The user must ensure that the maximum case temperature specification (95^{o} C) is not exceeded. Given the thermal resistance of the package in still air, the user may operate the VSC7140 in still air if the ambient temperature does not exceed 32^{o} C (95^{o} C - 1.7W * 37^{o} C/W = 32^{o} C). If operation above this ambient temperature is required, an appropriate heatsink must be used with the part or adequate airflow must be provided.

Moisture Sensitivity Level

This device is rated with a moisture sensitivity level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

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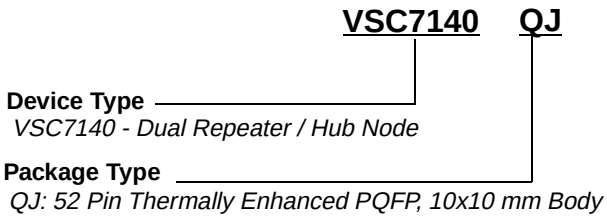
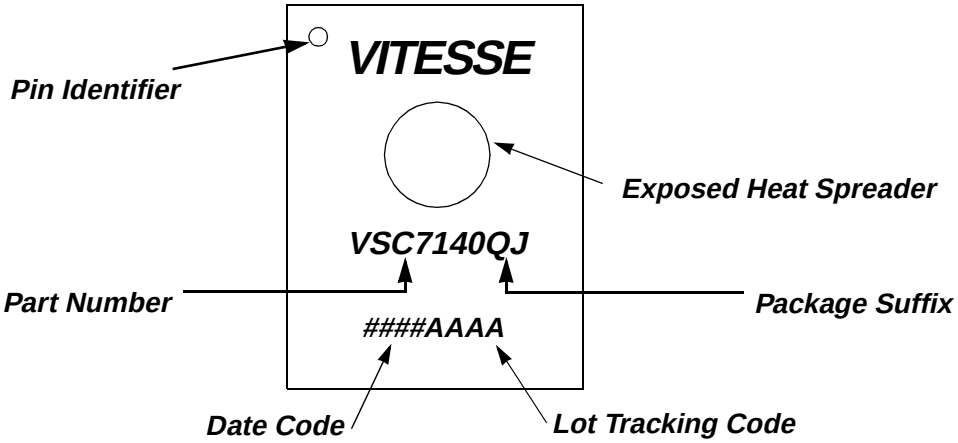
Ordering Information

The order number for this product is formed by a combination of the device number and package type.



Marking Information

The package is marked with three lines of text as shown below (QJ Package):



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