

## BCM3116 QAMLINK® RECEIVER

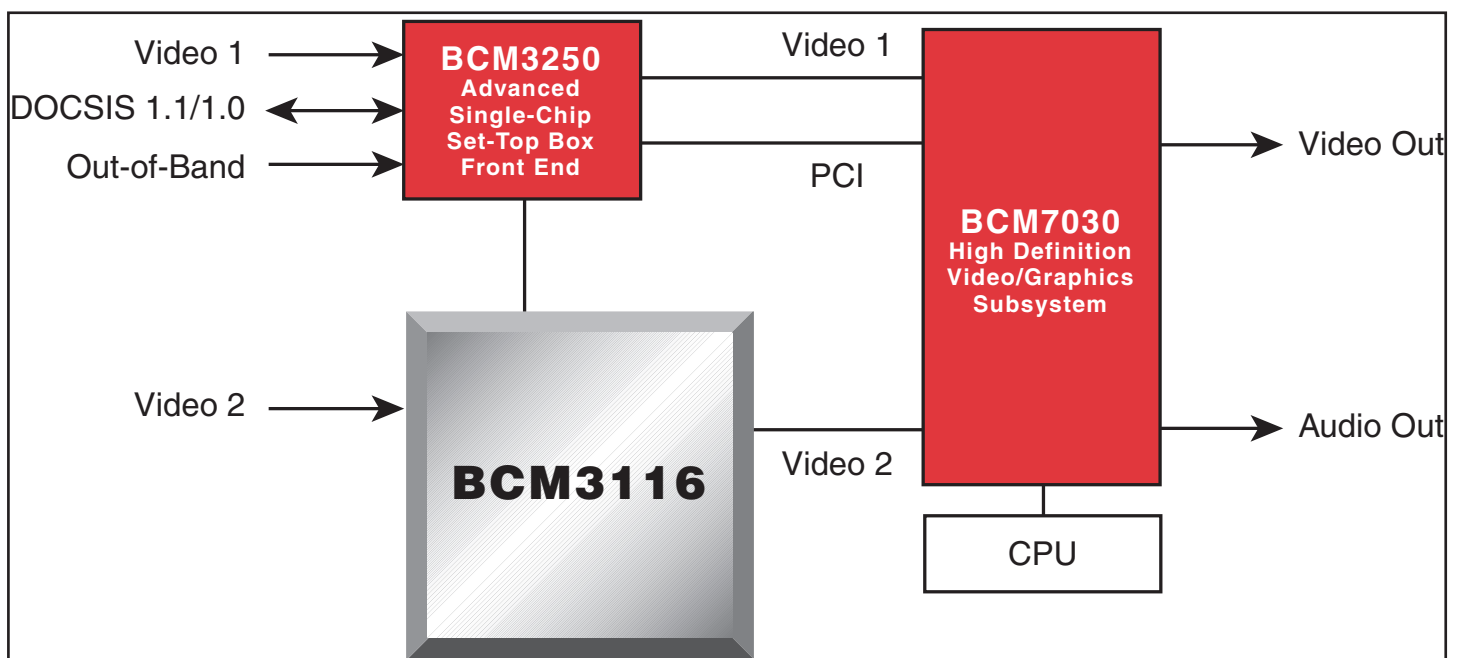
### BCM3116 FEATURES

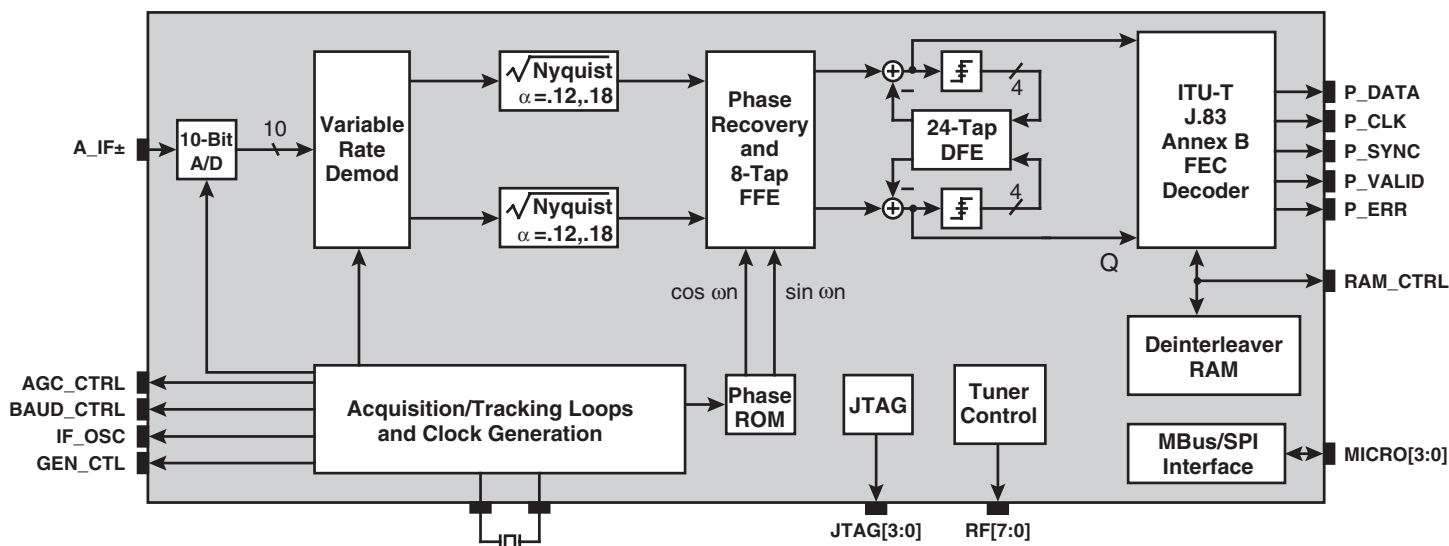
- Downstream QAM Receiver for North American set-top box and DOCSIS cable modem applications.
- Integrated QAMLink® receiver with forward error correction (FEC)
  - 5.059641/5.360537 MBaud variable symbol rate
  - Supports 64 and 256-QAM
  - Digital demodulator, Nyquist filters, tracking loops, and 32-tap adaptive decision feedback equalizer
  - Digital derotator for wideband carrier phase tracking
- ITU-T J.83 Annex B-compliant FEC decoder
  - 16-state trellis decoder
  - Reed-Solomon (n,k) = (128,122); t = 3
  - Programmable convolutional deinterleaver, I\*J < 128 with internal RAM, I\*J > 128 with external RAM
- IC or SPI-compatible microcontroller interface
- On-chip generation of all clock and control signals
- 3.3V operation
- JTAG Test Interface
- 100-pin PQFP

### SUMMARY OF BENEFITS

- Fully integrated, DOCSIS-based solution for cable modems and cable-TV set-top boxes
  - Enables the industry's lowest cost, least complex system
  - Simplifies system, board and software design through the integration of analog components
  - Reduces power consumption
- Enhanced digital adaptive equalization
  - Robust performance in the presence of multipath at high order QAM constellations
  - Superior echo cancellation capability for both wired and wireless applications

### Interactive Set-top Box with DOCSIS and Watch and Record Dual Video Channels





The **BCM3116** QAMLink Receiver is a fully asynchronous design with an integrated FEC and 10-bit analog-to-digital converter. It provides a complete digital transmission solution for cable modems, cable-TV set-top boxes and digital microwave radios. Its bandwidth-efficient feature set expands the existing potential bandwidth of a standard analog network and provides operators with reliable, error-free transmission.

The **BCM3116** accepts a modulated data stream at up to 38.8 Mbps and delivers a demodulated, equalized and error-corrected output data stream. The receiver integrates a 10-bit A/D converter, a 256-QAM demodulator with square-root raised-cosine receive filters, a 32-tap adaptive equalizer with an embedded phase recovery derotator, acquisition and tracking loops, and a forward error correction (FEC) decoder. The FEC is ITU-T J.83 Annex B, DOCSIS, DigiCipher II<sup>®</sup>, IEEE 802.14, and SCTE DVS-031-compliant.

The analog IF waveform is fed into the chip, where it is sampled by the integrated A/D converter, digitally mixed to baseband and filtered by dual square-root Nyquist filters. Inter-symbol interference is then removed by the adaptive decision feedback equalizer (DFE). A decision slicer, which supports constellations up to 256-QAM, formats the equalized data which is then fed into a trellis decoder, derandomizer, deinterleaver, and Reed-Solomon decoder. The final error-corrected output is delivered in non-MPEG or in MPEG-2 transport format.

Optimized for high-volume manufacturing, the **BCM3116** represents a highly integrated solution that reduces the system-level chip count, the cost and the complexity associated with manufacturing RF receivers.

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