CY7C006
CY7C016

16K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **True dual-ported memory cells which allow simultaneous reads of the same memory location**
- **16K x 8 organization (CY7C006)**
- **16K x 9 organization (CY7C016)**
- **0.65-micron CMOS for optimum speed/power**
- **High-speed access: 15 ns**
- **Low operating power: I_{CC} = 140 mA (typ.)**
- **Fully asynchronous operation**
- **Automatic power-down**
- **TTL compatible**
- **Expandable data bus to 16/18 bits or more using Master/Slave chip select when using more than one device**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **INT flag for port-to-port communication**
- **Available in 68-pin PLCC (7C006), 64-pin (7C006) and 80-pin (7C016) TQFP**
- **Pin compatible and functional equivalent to IDT7006/IDT7016**

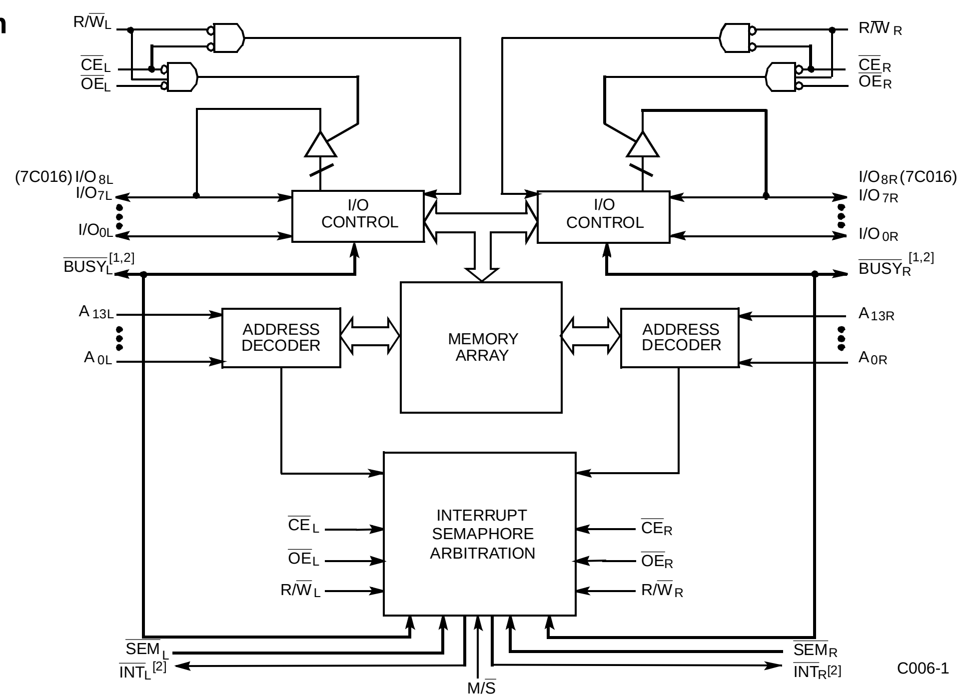
Functional Description

The CY7C006 and CY7C016 are high-speed CMOS 16K x 8 and 16K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7C006/016 to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C006/016 can be utilized as a standalone 128-/144-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16-/18-bit or wider master/slave dual-port static RAM. An M/S pin is provided for implementing 16-/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable (CE), Read or Write Enable (R/W), and Output Enable (OE). Two flags, BUSY and INT, are provided on each port. BUSY signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag (INT) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a Chip Enable (CE) pin or SEM pin.

The CY7C006 and CY7C016 are available in 68-pin PLCC (CY7C006), 64-pin (CY7C006) TQFP, and 80-pin (CY7C016) TQFP.

Logic Block Diagram



Notes:
1. BUSY is an output in master mode and an input in slave mode.
2. Interrupt: push-pull output and requires no pull-up resistor.

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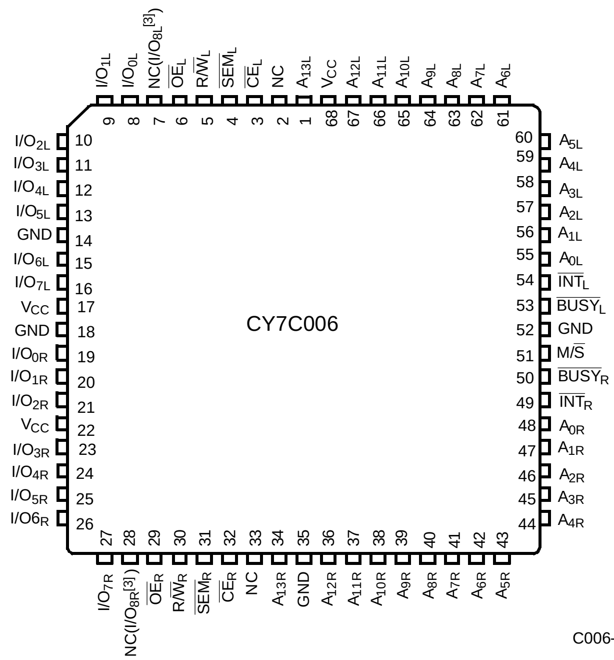
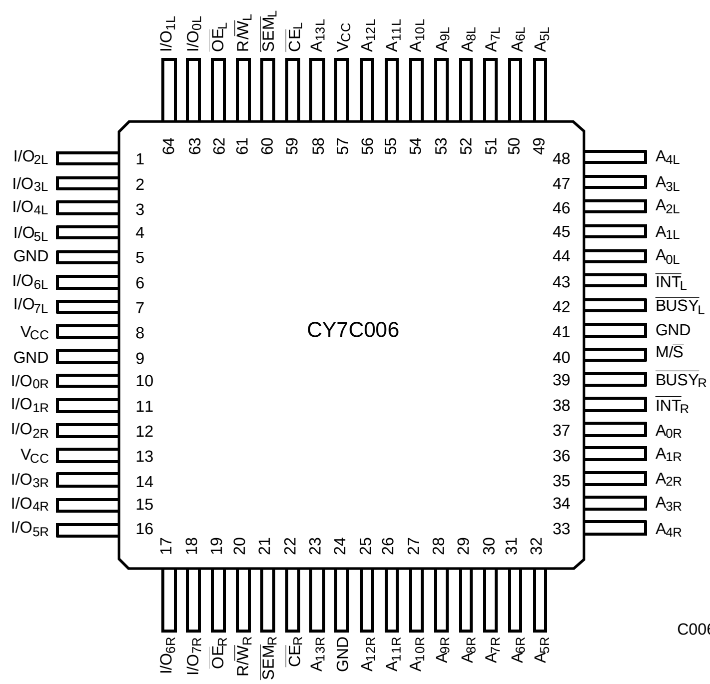
Pin Configurations

68-Pin PLCC
Top View



64-Pin TQFP
Top View

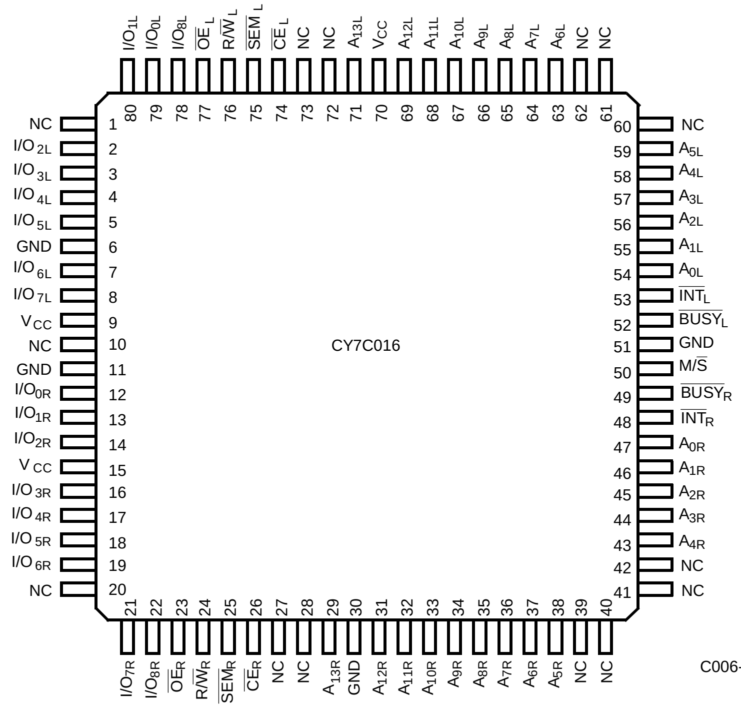


Note:

3. I/O for CY7C016 only.

Pin Configurations (continued)

80-Pin TQFP
Top View



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Pin Definitions

Left Port	Right Port	Description
$I/O_{0L–7L(8L)}$	$I/O_{0R–7R(8R)}$	Data Bus Input/Output
$A_{0L–13L}$	$A_{0R–13R}$	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 3FFE and is cleared when left port reads location 3FFE. $\overline{INT}_R$ is set when left port writes location 3FFF and is cleared when right port reads location 3FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

	7C006-15 7C016-15	7C006-25 7C016-25	7C006-35 7C016-35	7C006-55 7C016-55
Maximum Access Time (ns)	15	25	35	55
Maximum Operating Current (mA)	260	220	210	200
Maximum Standby Current for I_{SB1} (mA)	70	60	50	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... –55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... –0.5V to +7.0V

DC Input Voltage[4].. –0.5V to +7.0V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current.. >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C006-15 7C016-15 Min.	Typ.	Max.	7C006-25 7C016-25 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}				2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10		+10	–10		+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		–10		+10	–10		+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com’l		170	260		160	220	mA
			Ind					160	270	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com’l		50	70		40	60	mA
			Ind					40	75	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com’l		110	170		90	130	mA
			Ind					90	150	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Com’l		3	15		3	15	mA
			Ind					3	15	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≥ 0.2V, Active Port Outputs, f = f_{MAX}[5]	Com’l		100	150		80	120	mA
			Ind					80	130	

Notes:

4. Pulse width < 20 ns.
5. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

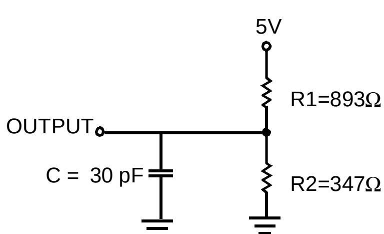
Electrical Characteristics (continued)

Parameter	Description	Test Conditions		7C006-35 7C016-35 Min.	Typ.	Max.	7C006-55 7C016-55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}				2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10		+10	–10		+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		–10		+10	–10		+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		150	210		140	200	mA
			Ind		150	250		140	240	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l		30	50		20	40	mA
			Ind		30	65		20	55	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l		80	120		70	100	mA
			Ind		80	130		70	115	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Com'l		3	15		3	15	mA
			Ind		3	15		3	15	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[5]	Com'l		70	100		60	90	mA
			Ind		70	110		60	95	

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



(a) Normal Load (Load 1)

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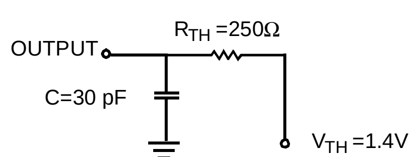
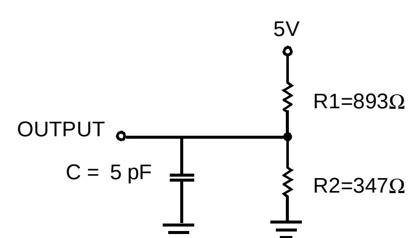


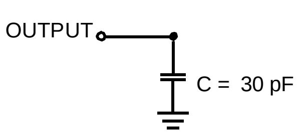
(b) Thévenin Equivalent (Load)

C006-6



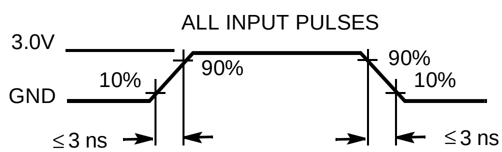
(c) Three-State Delay (Load 3)

C006-7



Load (Load 2)

C006-8



C006-9

Note:

6. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C006-15 7C016-15		7C006-25 7C016-25		7C006-35 7C016-35		7C006-55 7C016-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		13		20		25	ns
t_{LZOE}[8, 9, 10]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[8, 9, 10]	$\overline{OE}$ HIGH to High Z		10		15		15		25	ns
t_{LZCE}[8, 9, 10]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[8, 9, 10]	$\overline{CE}$ HIGH to High Z		10		15		15		25	ns
t_{PU}[10]	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}[10]	$\overline{CE}$ HIGH to Power-Down		15		25		35		55	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		45		ns
t_{AW}	Address Set-Up to Write End	12		20		30		45		ns
t_{HA}	Address Hold From Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		40		ns
t_{SD}	Data Set-Up to Write End	10		15		15		25		ns
t_{HD}[11]	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[9, 10]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[9, 10]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[12]	Write Pulse to Data Delay		30		50		60		80	ns
t_{DDD}[12]	Write Data Valid to Read Data Valid		25		30		35		60	ns
BUSY TIMING[13]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		17		25		30	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		17		25		30		ns
t_{BDD}[14]	$\overline{BUSY}$ HIGH to Data Valid		Note 13		Note 13		Note 13		Note 13	ns

Notes:

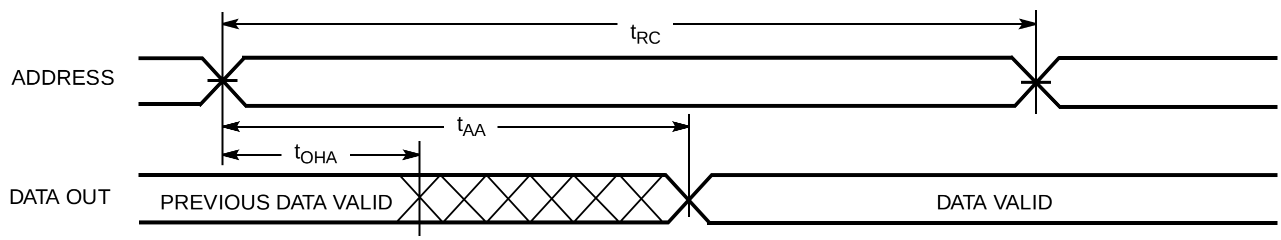
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
9. Test conditions used are Load 3.
10. This parameter is guaranteed but not tested.
11. Must be met by the device writing to the RAM under all operating conditions.
12. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
13. Test conditions used are Load 2.
14. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).

Switching Characteristics Over the Operating Range[7] (continued)

Parameter	Description	7C006-15 7C016-15		7C006-25 7C016-25		7C006-35 7C016-35		7C006-55 7C016-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
INTERRUPT TIMING[13]										
t_{INS}	$\overline{INT}$ Set Time		15		25		25		30	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25		30	ns
SEMAPHORE TIMING										
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns

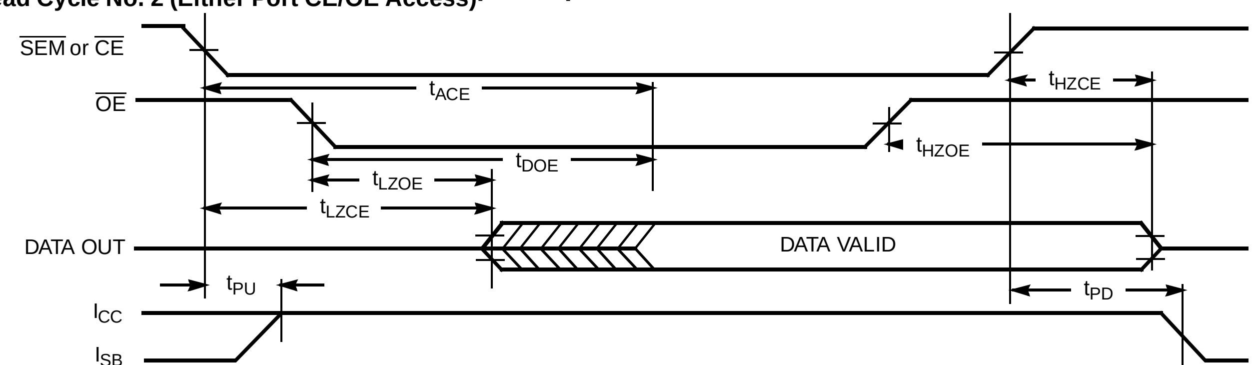
Switching Waveforms

Read Cycle No. 1 (Either Port Address Access)[15, 16]



C006-10

Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)[15, 17, 18]

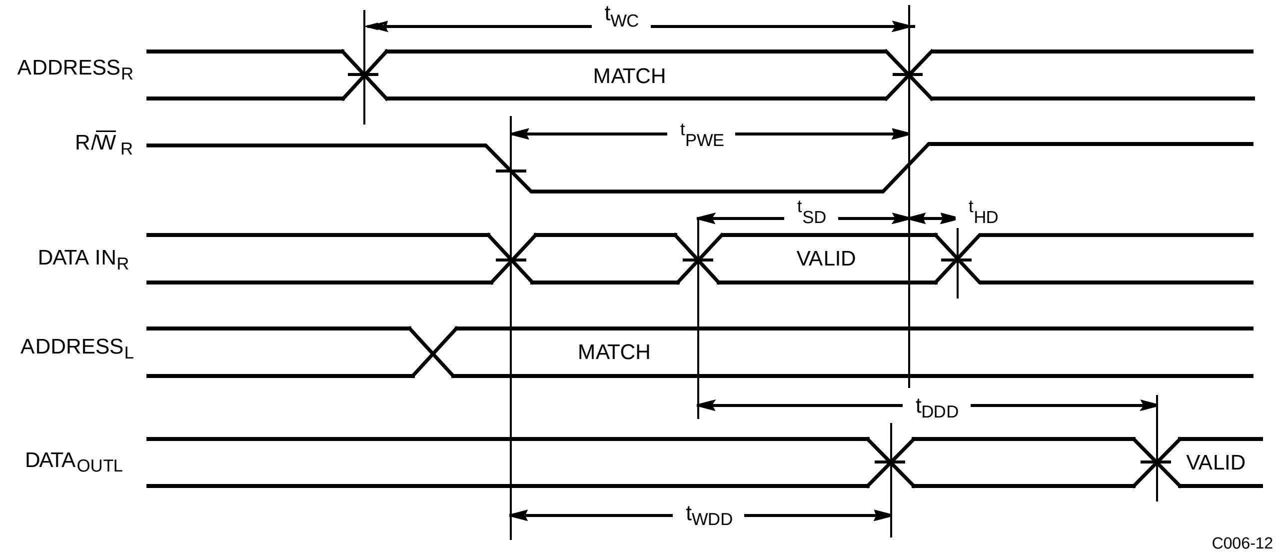


C006-11

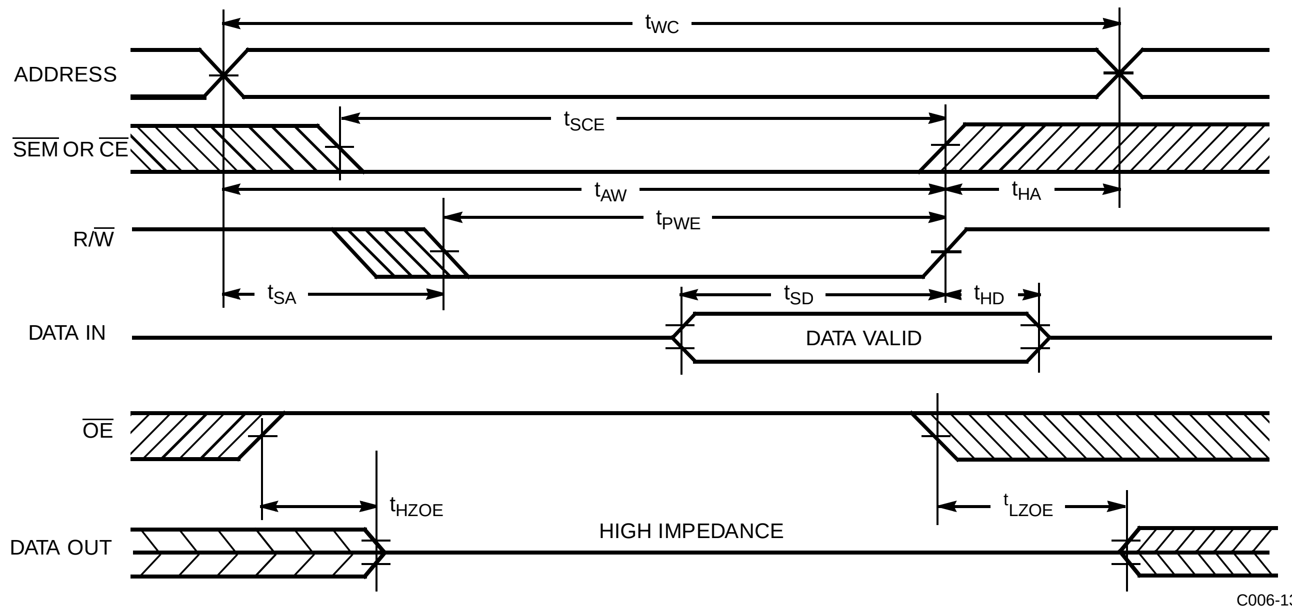
Notes:
15. R/$\overline{W}$ is HIGH for read cycle.
16. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. $\overline{CE_L}$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.

Switching Waveforms (continued)

Read Timing with Port-to-Port Delay (M/$\overline{S}$=L)[19, 20]



Write Cycle No. 1: $\overline{OE}$ Three-State Data I/Os (Either Port)[21, 22, 23]

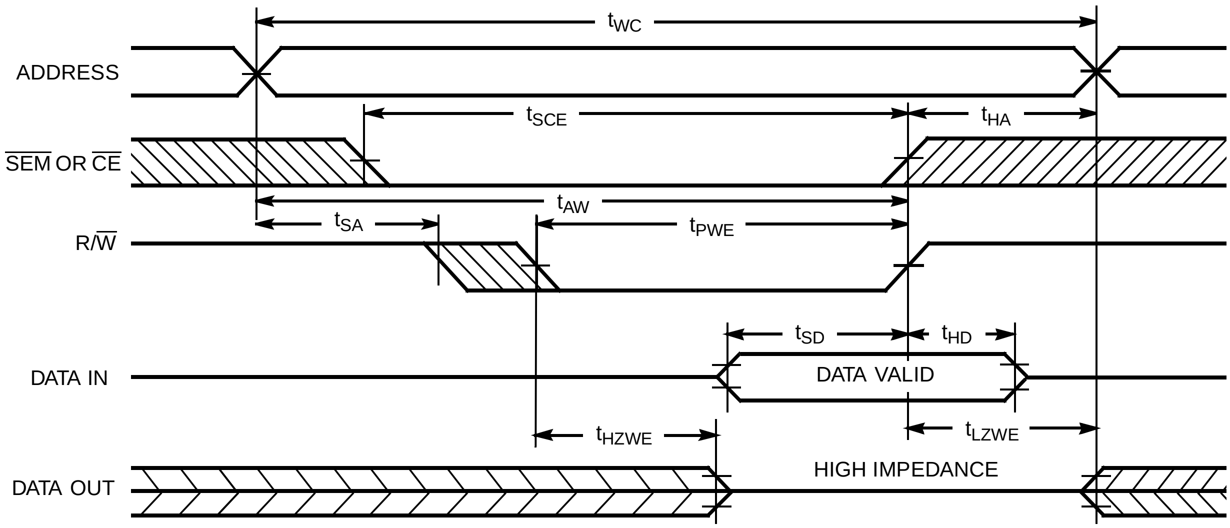


Notes:

19. $\overline{BUSY}$ = HIGH for the writing port.
20. $\overline{CE}_L = \overline{CE}_R$ = LOW.
21. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or ($t_{HZWE} + t_{SD}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
23. R/$\overline{W}$ must be HIGH during all address transitions.

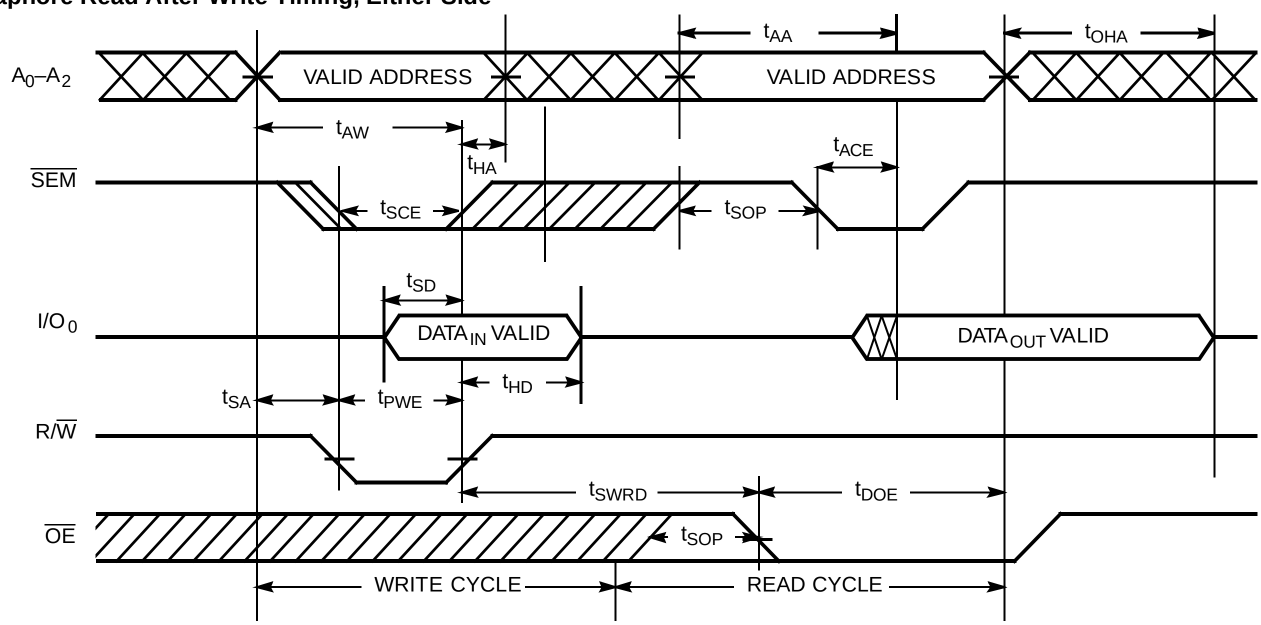
Switching Waveforms (continued)

Write Cycle No. 2: R/$\overline{W}$ Three-State Data I/Os (Either Port)[20, 22, 24]



C006-14

Semaphore Read After Write Timing, Either Side[25]



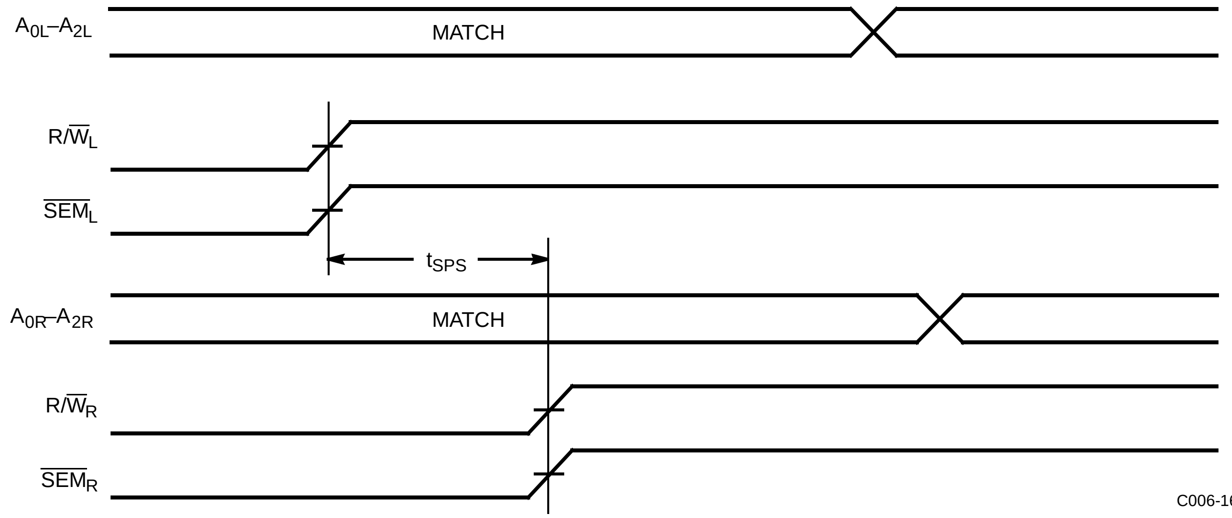
C006-15

Notes:

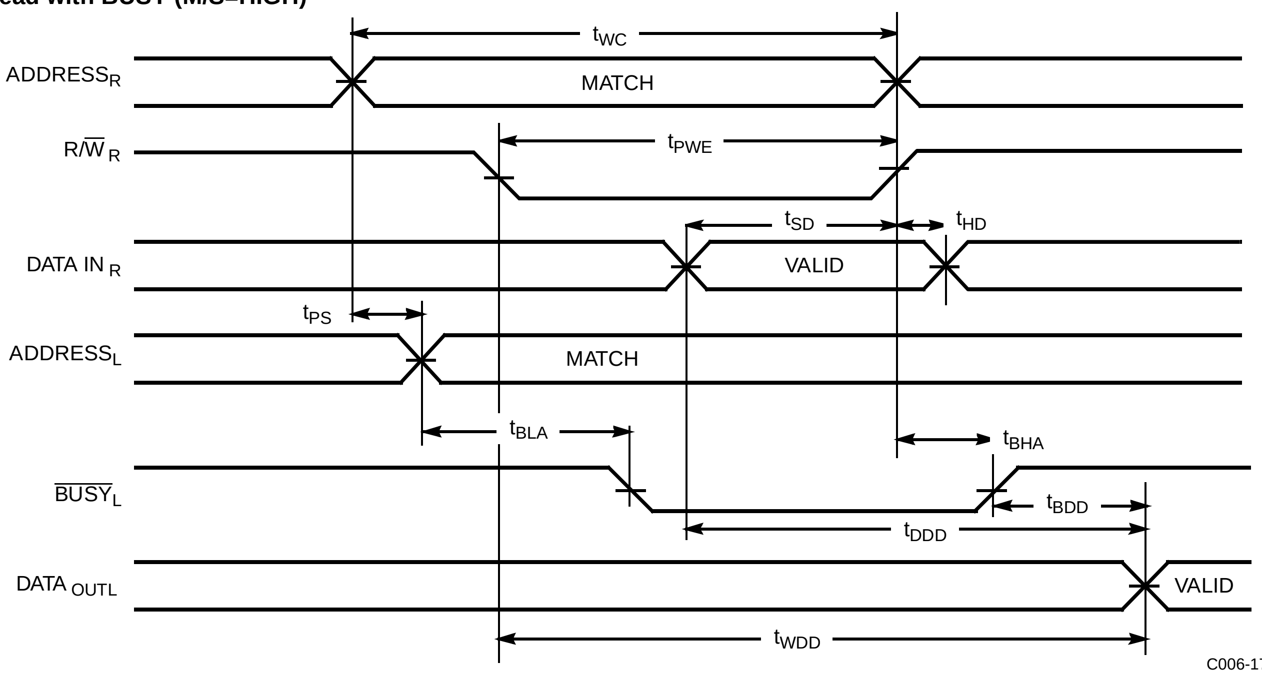
24. Data I/O pins enter high-impedance when $\overline{OE}$ is held LOW during write.
25. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).

Switching Waveforms (continued)

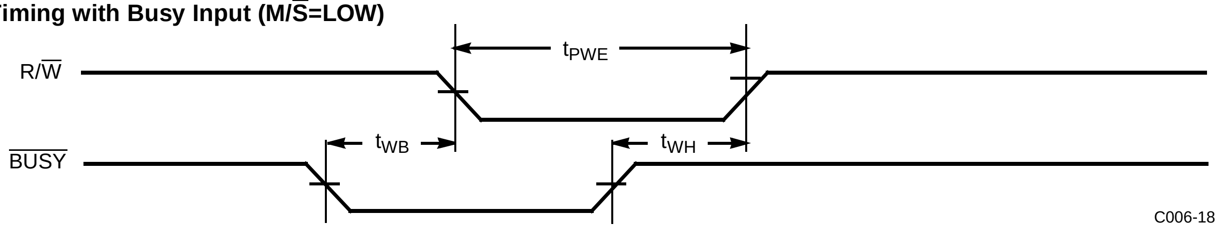
Semaphore Contention [26, 27, 28]



Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[19]



Write Timing with Busy Input (M/$\overline{S}$=LOW)



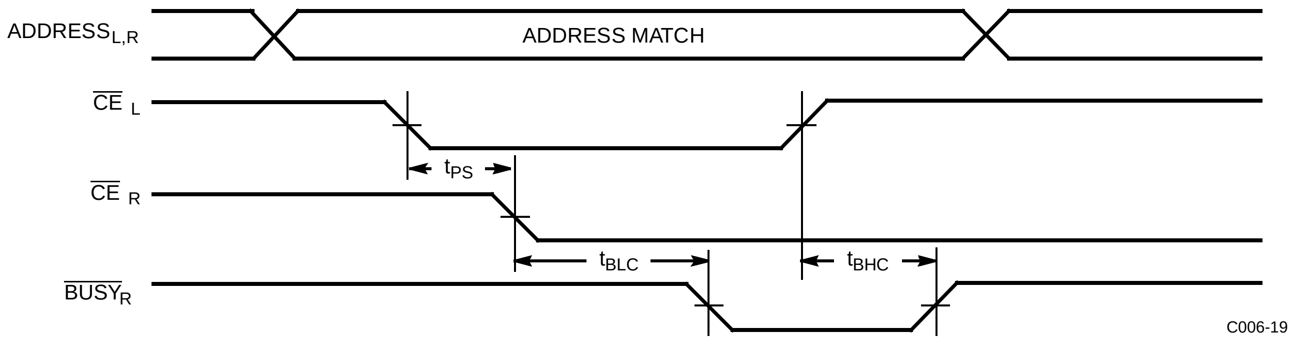
Notes:

26. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
27. Semaphores are reset (available to both ports) at cycle start.
28. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

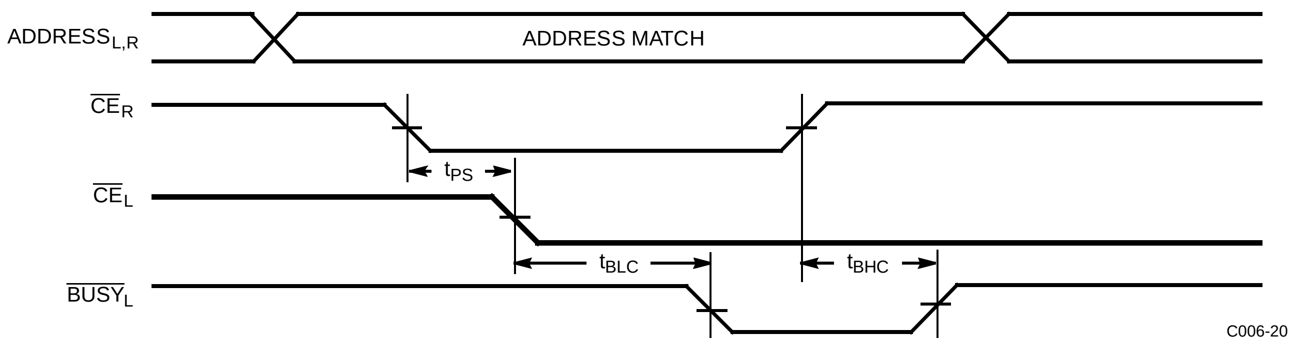
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[29]

$\overline{CE}_L$ Valid First:

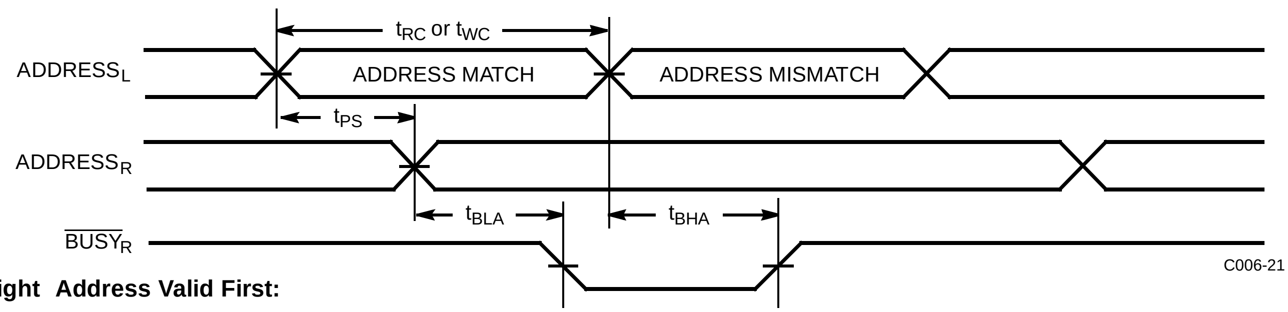


$\overline{CE}_R$ Valid First:

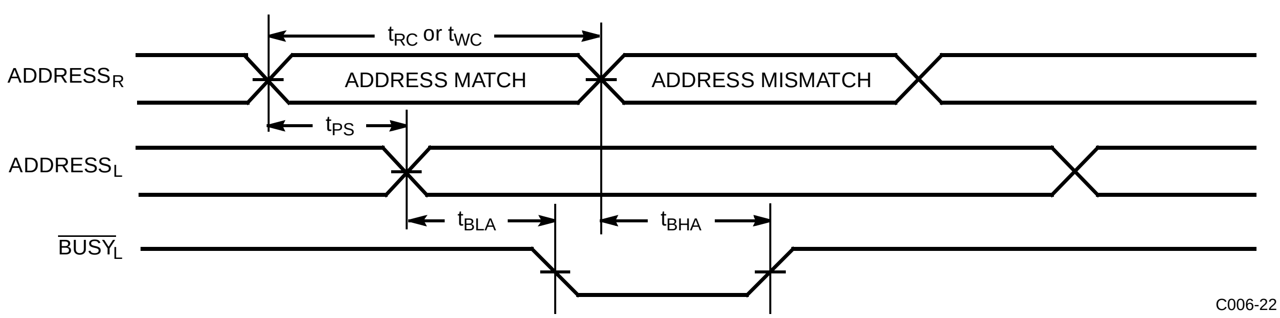


Busy Timing Diagram No. 2 (Address Arbitration)[28]

Left Address Valid First:



Right Address Valid First:



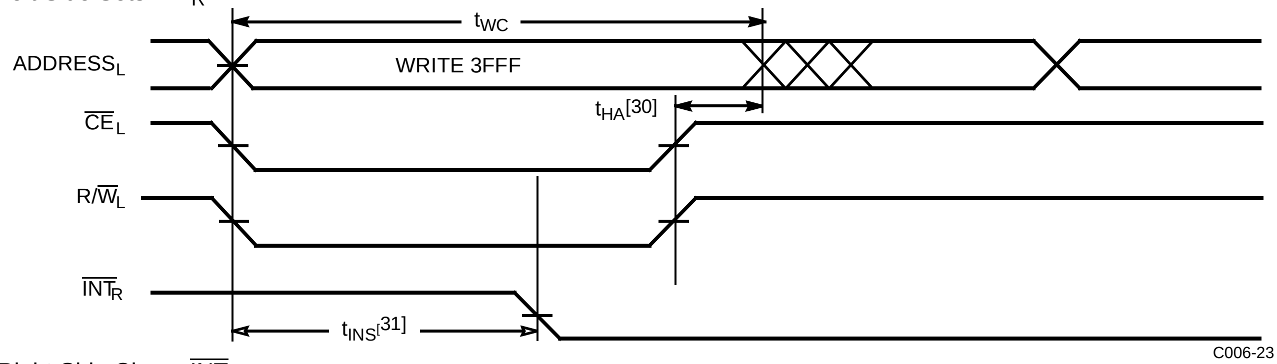
Notes:

29. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.
30. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
31. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

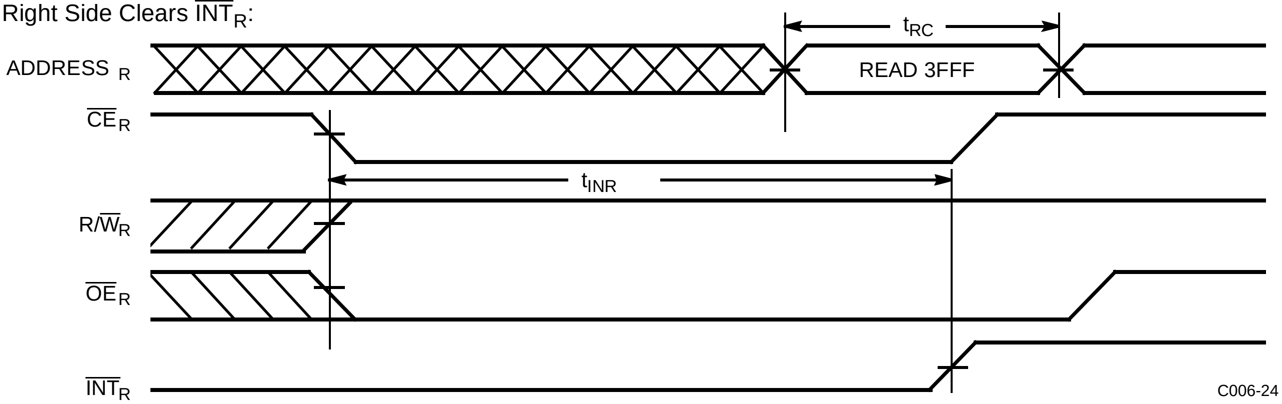
Switching Waveforms (continued)

Interrupt Timing Diagrams

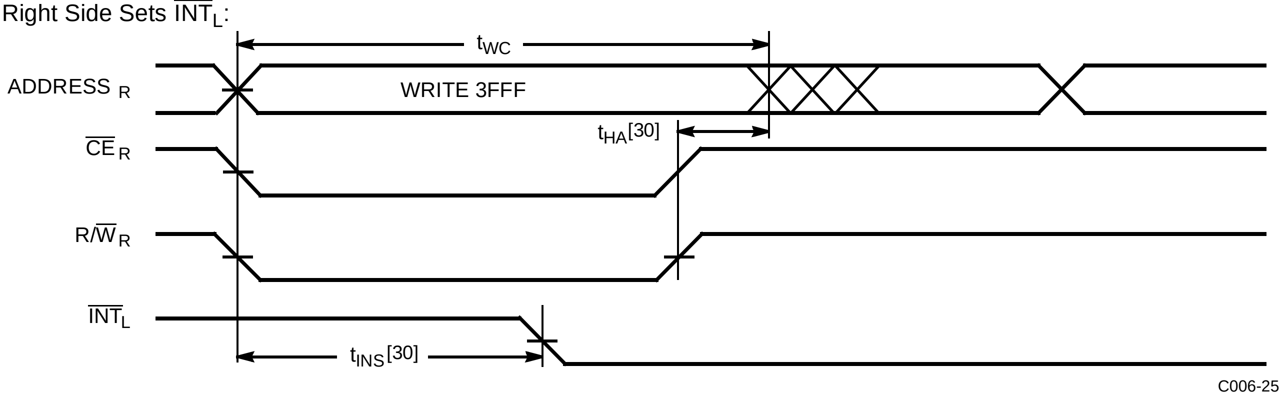
Left Side Sets $\overline{INT}_R$:



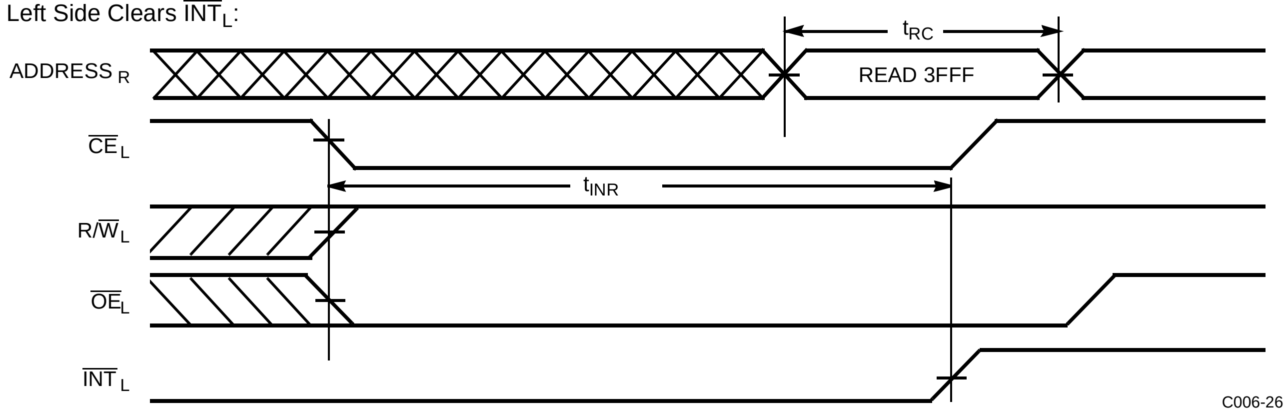
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



Architecture

The CY7C006/016 consists of a an array of 16K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{\text{CE}}$, $\overline{\text{OE}}$, R/$\overline{\text{W}}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{\text{BUSY}}$ pin is provided on each port. Two Interrupt ($\overline{\text{INT}}$) pins can be utilized for port-to-port communication. Two Semaphore ($\overline{\text{SEM}}$) control pins are used for allocating shared resources. With the M/$\overline{\text{S}}$ pin, the CY7C006/016 can function as a Master ($\overline{\text{BUSY}}$ pins are outputs) or as a slave ($\overline{\text{BUSY}}$ pins are inputs). The CY7C006/016 has an automatic power-down feature controlled by $\overline{\text{CE}}$. Each port is provided with its own Output Enable control ($\overline{\text{OE}}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{\text{W}}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{\text{OE}}$ pin (see Write Cycle No.1 waveform) or the R/$\overline{\text{W}}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{\text{OE}}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{\text{W}}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{\text{CE}}$	R/$\overline{\text{W}}$	$\overline{\text{OE}}$	$\overline{\text{SEM}}$	$I/O_{0–7/8}$	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	↑	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Read Operation

When reading the device, the user must assert both the $\overline{\text{OE}}$ and $\overline{\text{CE}}$ pins. Data will be available t_{ACE} after $\overline{\text{CE}}$ or t_{DOE} after $\overline{\text{OE}}$ are asserted. If the user of the CY7C006/016 wishes to access a semaphore flag, then the $\overline{\text{SEM}}$ pin must be asserted instead of the $\overline{\text{CE}}$ pin.

Interrupts

The interrupt flag ($\overline{\text{INT}}$) permits communications between ports. When the left port writes to location 3FFF(HEX), the right port's interrupt flag ($\overline{\text{INT}}_R$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{\text{INT}}_L$) is accomplished when the right port writes to location 3FFE(HEX). This flag is cleared when the left port reads location 3FFE(HEX). The message at 3FFE(HEX) and 3FFF(HEX) is user-defined. See *Table 2* for input requirements for $\overline{\text{INT}}$. $\overline{\text{INT}}_R$ and $\overline{\text{INT}}_L$ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7C006/016 provides on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{\text{CE}}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{\text{BUSY}}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{\text{CE}}$ is taken LOW. $\overline{\text{BUSY}}_L$ and $\overline{\text{BUSY}}_R$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/$\overline{\text{S}}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{\text{BUSY}}$ output of the master is connected to the $\overline{\text{BUSY}}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{\text{BUSY}}$ input has settled (t_{BLA}). Otherwise, the slave chip may begin a write cycle during a contention situation. When presented a HIGH input, the M/$\overline{\text{S}}$ pin allows the device to be used as a master and therefore the $\overline{\text{BUSY}}$ line is an output. $\overline{\text{BUSY}}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C006/016 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports.The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{\text{SEM}}$ or $\overline{\text{OE}}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore.When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Table 2. Interrupt Operation Example (assumes $\overline{\text{BUSY}}_L$=$\overline{\text{BUSY}}_R$=HIGH)

	Left Port					Right Port				
Function	R/$\overline{\text{W}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$A_{0L–13L}$	$\overline{\text{INT}}$	R/$\overline{\text{W}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$A_{0R–13R}$	$\overline{\text{INT}}$
Set Left $\overline{\text{INT}}$	X	X	X	X	L	L	L	X	3FFE	X
Reset Left $\overline{\text{INT}}$	X	L	L	3FFE	H	X	L	L	X	X
Set Right $\overline{\text{INT}}$	L	L	X	3FFF	X	X	X	X	X	L
Reset Right $\overline{\text{INT}}$	X	X	X	X	X	X	L	L	3FFF	H

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access.When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All Semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 3. Semaphore Operation Example

Function	$I/O_{0-7/8}$ Left	$I/O_{0-7/8}$ Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Ordering Information

16K x8 Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C006-15AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C006-25AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006-25AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006-25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C006-35AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006-35AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006-35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C006-55AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006-55AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006-55JI	J81	68-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

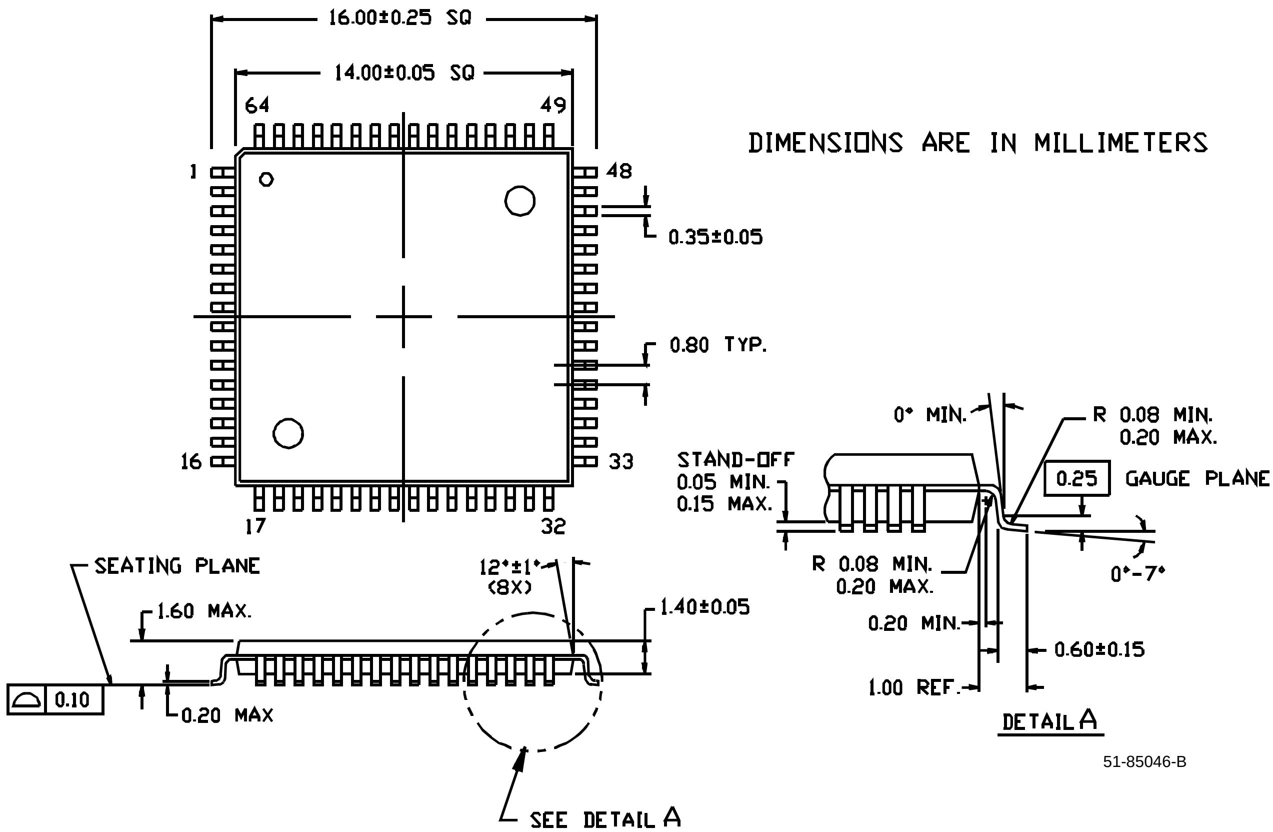
16K x9 Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C016-15AC	A80	80-Lead Thin Quad Flat Package	Commercial
25	CY7C016-25AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-25AI	A80	80-Lead Thin Quad Flat Package	Industrial
35	CY7C016-35AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-35AI	A80	80-Lead Thin Quad Flat Package	Industrial
55	CY7C016-55AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-55AI	A80	80-Lead Thin Quad Flat Package	Industrial

Document #: 38-00416-B

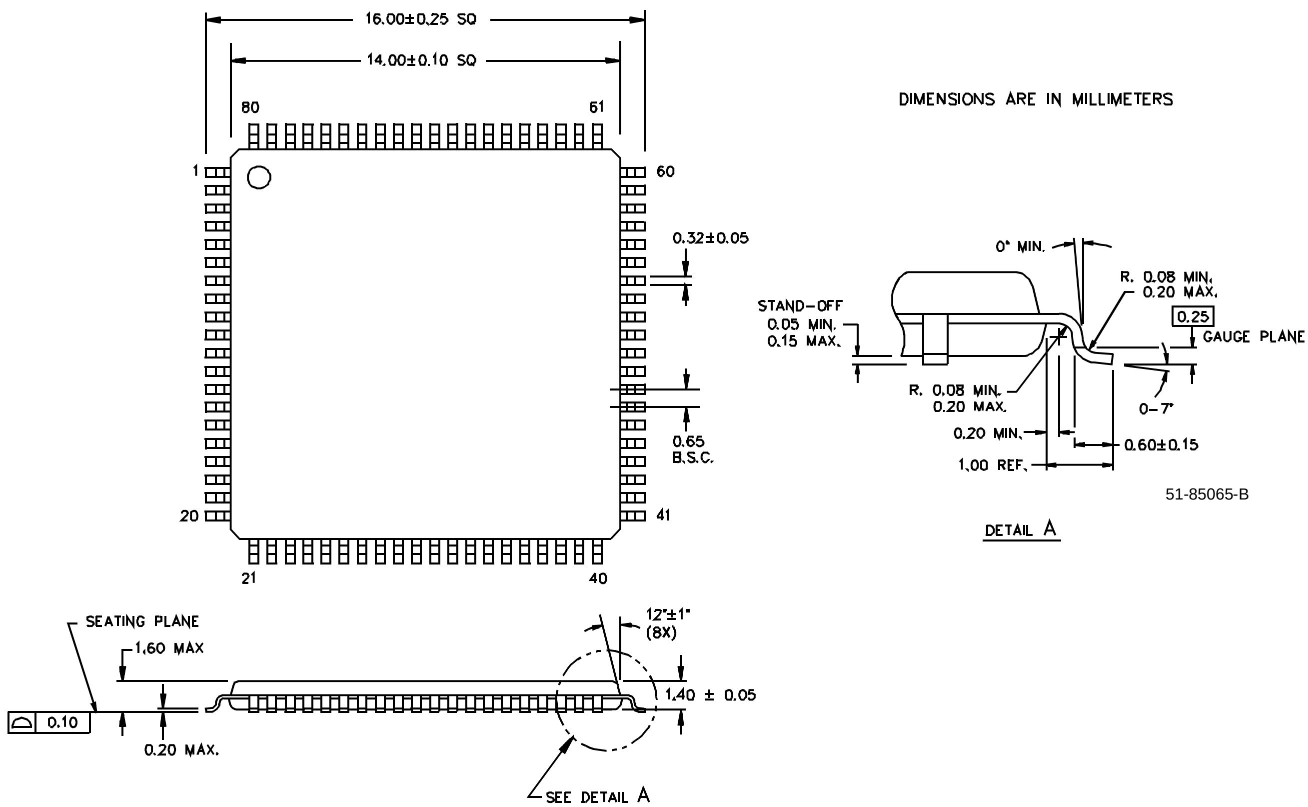
Package Diagrams

64-Lead Thin Plastic Quad Flat Pack (14 x 14 x 1.4 mm) A65

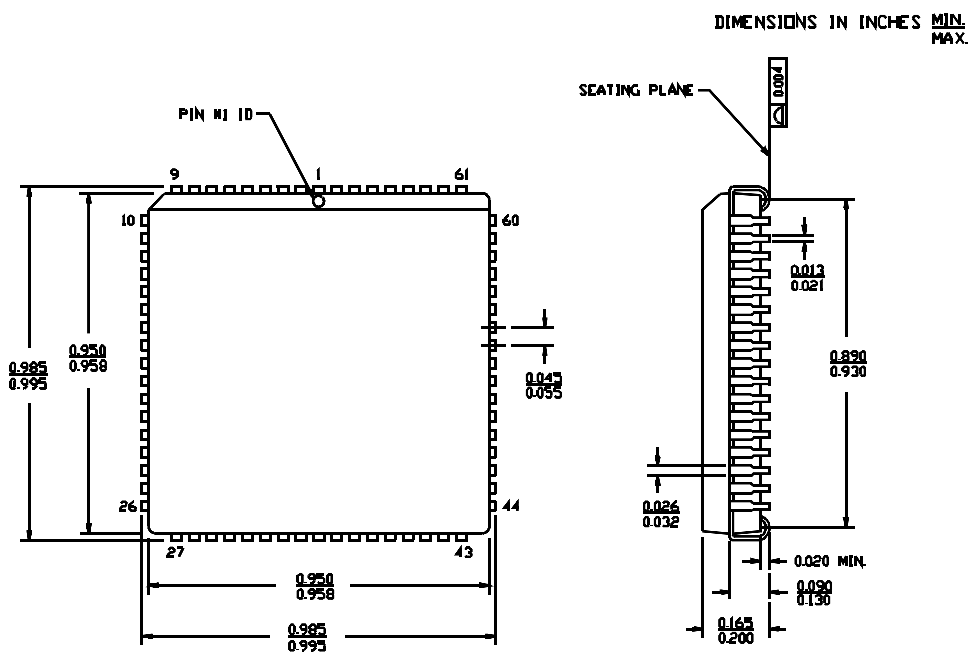


Package Diagrams (continued)

80-Pin Thin Plastic Quad Flat Pack A80



68-Lead Plastic Leaded Chip Carrier J81



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