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MCF5206

Product Brief

MCF5206 Integrated Microprocessor

The MCF5206 integrated microprocessor combines a ColdFire™ processor core with several peripheral functions such as a DRAM controller, timers, parallel and serial interfaces, and system integration. Designed for embedded control applications, the ColdFire core delivers enhanced performance while maintaining low system costs. To speed program execution, the on-chip instruction cache and SRAM provide one-cycle access to critical code and data. The MCF5206 processor greatly reduces the time required for system design and implementation by packaging common system functions on chip and providing glueless interfaces to 8-, 16-, and 32-bit DRAM, SRAM, ROM, and I/O devices.

The revolutionary ColdFire microprocessor architecture gives cost-sensitive, high-volume markets new levels of price and performance. Based on the concept of variable-length RISC technology, ColdFire combines the architectural simplicity of conventional 32-bit RISC with a memory-saving, variable-length instruction set. In defining the ColdFire architecture for embedded processing applications, Motorola incorporated RISC architecture for peak performance and a simplified version of the variable-length instruction set found in the M68000 Family for code density.

By using a variable-length instruction set architecture, embedded processor designers using ColdFire RISC processors will enjoy significant system-level advantages over conventional fixed-length RISC architectures. The denser binary code for ColdFire processors consumes less valuable memory than any fixed-length instruction set RISC processor available. This improved code density means more efficient system memory use for a given application, and requires slower, less costly memory to help achieve a target performance level.

The integrated peripheral functions provide high performance and flexibility. The DRAM controller supports up to 512 Mbytes of DRAM. The MCF5206 processor supports both page-mode and extended-data-out DRAMs. The serial interfaces consist of a programmable full duplex DUART and a separate I^2C[1]-compatible Motorola bus (M-Bus interface). The two 16-bit general-purpose multimode timers provide separate input and output signals. For system protection, the processor includes a programmable 16-bit software watchdog timer and several bus monitors. In addition, common system functions such as chip-selects, interrupt control, bus arbitration, and IEEE 1149.1 Test (JTAG) support are included.

A sophisticated debug interface supports both background-debug mode and real-time trace. This interface is common to all ColdFire-based processors and allows common emulator support across the entire ColdFire Family.

ColdFire is a trademark of Motorola.

1. I^2C bus is a proprietary Philips interface bus.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

SEMICONDUCTOR PRODUCT INFORMATION

The primary features of the MCF5206 integrated processor include the following:

- ColdFire Processor Core
  - — Variable-length RISC
  - — 32-bit internal address bus with up to 256 Mbytes of off-chip linear address space
  - — 32-bit data bus
  - — 16 user-visible 32-bit wide registers
  - — Supervisor / User modes for system protection
  - — Vector base register to relocate exception-vector table
  - — Optimized for high-level language constructs
  - — 17 MIPS at 33Mhz
- 512-Byte Direct-Mapped Instruction Cache
- 512-Byte On-Chip SRAM
  - — Provides one-cycle access to critical code and data
- DRAM Controller
  - — Supports up to 32 Mbytes of memory using 4M x 1 DRAMs, 128 Mbytes using 16M x 1 DRAMs, 256 Mbytes using 32x1 DRAMS
  - — Programmable refresh timer provides CAS-before-RAS refresh
  - — Support for 2 separate memory banks
  - — Support for page-mode DRAMs and extended-data-out (EDO) DRAMs
  - — Allows external bus master access
- Dual Universal Synchronous/Asynchronous Receiver/Transmitter (DUART)
  - — Full duplex operation
  - — Flexible baud-rate generator
  - — Modem control signals available ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$)
  - — Processor-interrupt capability
  - — Compatible with MC68681 DUART programming model
- Dual 16-Bit General-Purpose Multimode Timers
  - — 8-bit prescaler
  - — Timer input and output pins
  - — 30ns resolution with 33MHz system clock
  - — Processor-interrupt capability
- Motorola Bus (M-Bus) Module
  - — Interchip bus interface for EEPROMs, LCD controllers, A/D converters, keypads
  - — Compatible with industry-standard I^2C Bus
  - — Master or slave modes support multiple masters
  - — Automatic interrupt generation with programmable level
- System Interface
  - — Glueless bus interface to 8-, 16-, and 32-bit DRAM, SRAM, ROM, and I/O devices
  - — 8 programmable chip-select signals
  - — Programmable wait states and port sizes
  - — Allows external bus masters to access chip-selects
  - —System protection
    - 16-bit software watchdog timer with prescaler
    - Double bus fault monitor
    - Bus timeout monitor
    - Spurious interrupt monitor
  - — Programmable interrupt controller
    - Low interrupt latency
    - 3 external interrupt inputs
    - Programmable interrupt priority and autovector generator
  - — IEEE 1149.1 test (JTAG) support
  - — 8-Bit General-Purpose I/O Interface
- System Debug Support
  - — Real-time trace
  - — Background debug interface
- Fully Static 5.0-Volt Operation
- 160 Pin QFP Package

OVERVIEW

Figure 1 is a block diagram of the MCF5206 processor. The paragraphs that follow provide an overview of the integrated processor.

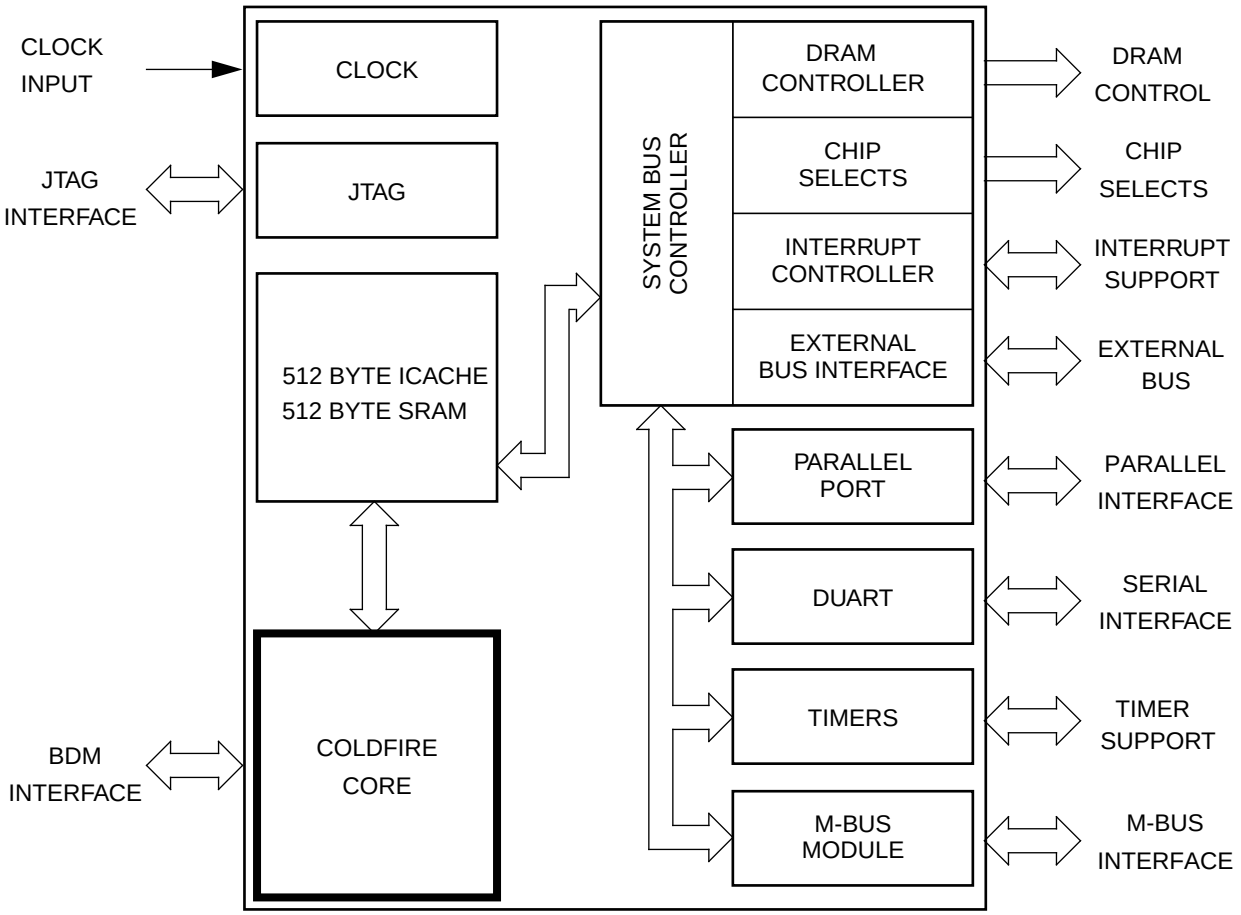

Figure 1. MCF5206 Block Diagram

ColdFire Processor Core

The ColdFire processor core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size.The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, thereby minimizing time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC datapath with a dual-read-ported register file feeding an arithmetic/logic unit.

Instruction Cache

The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock. The MCF5206 processor uses a 512-byte, direct-mapped instruction cache to achieve 17 MIPS at 33 Mhz.The cache is accessed by physical addresses, where each 16-byte line consists of an address tag and a valid bit.

The instruction cache also includes a bursting interface for 32-, 16-, and 8-bit port sizes to quickly fill cache lines.

Internal SRAM

The 512-byte on-chip SRAM provides one clock-cycle access for the ColdFire core. This SRAM can store processor stack and critical code or data segments to maximize performance.

DRAM Controller

The MCF5206 DRAM controller provides a glueless interface for up to 2 banks of DRAM, each of which can be from 128 Kbytes up to 256 Mbytes in size. The controller supports an 8-, 16-, or 32-bit data bus. A unique addressing scheme allows for increases in system memory size without rerouting address lines and rewiring boards. The controller operates in full-page mode, burst-page mode, or in regular mode, and supports extended-data-out (EDO) DRAMs. At 33Mhz, the DRAM controller supports DRAMs with access times as fast as 60ns.

DUART Module

A full duplex DUART module contains independent receivers and transmitters that can be clocked by the DUART internal timer. This timer is clocked by the system clock or an external clock supplied by the TIN pin. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity, and up to 2 stop bits in 1/16 increments. Four-byte receive buffers and two-byte transmit buffers minimize CPU service calls. The DUART module also provides several error-detection and maskable-interrupt capabilities. Modem support includes request-to-send ($\overline{RTS}$) and clear-to-send ($\overline{CTS}$) lines.

The system clock provides the clocking function via a programmable prescaler. Users can select full duplex, autoecho loopback, local loopback, and remote loopback modes. The programmable DUART can interrupt the CPU on various normal or error-condition events.

Timer Module

The timer module includes 2 general-purpose timers, each of which contains a free-running 16-bit timer for use in any of 3 modes. One mode captures the timer value with an external event. Another mode triggers an external signal or interrupts the CPU when the timer reaches a set value, while a third mode counts external events. The timer unit has an 8-bit prescaler that allows programming of the clock input frequency, which is derived from the system clock. The programmable timer-output pin generates either an active-low pulse or toggles the output.

Motorola Bus (M-Bus) Module

The M-Bus interface is a two-wire, bidirectional serial bus that exchanges data between devices and is compatible with the I^2C Bus standard. The M-Bus minimizes the interconnection between devices in the end system and is best suited for applications that need occasional bursts of rapid communication over short distances among several devices. Bus capacitance and the number of unique addresses limit the maximum communication length and the number of devices that can be connected.

System Interface

The MCF5206 processor provides a glueless interface to 8-, 16-, and 32-bit port size SRAM, ROM, and peripheral devices with independent programmable control of the assertion and negation of chip-selects and write-enables. Programmable address and data-hold times can be extended for a compatible interface to external devices and memory. The MCF5206 also supports bursting ROMs.

External Bus Interface. The bus interface controller transfers information between the ColdFire core and memory, peripherals, or other masters on the external bus. The external bus interface provides up to 28 bits of address bus space, a 32-bit data bus, and all associated control signals. This interface implements an extended synchronous protocol that supports bursting operations. For nonsynchronous external memory and peripherals, the MCF5206 processor provides an alternate asynchronous bus transfer acknowledgment signal.

Simple two-wire request/acknowledge bus arbitration between the MCF5206 processor and another bus master, such as a DMA device, is glueless with arbitration handled internal to the MCF5206 processor. Alternately, an external bus arbiter can control more complex three-wire (request, grant, busy) multiple-master bus arbitration, allowing overlapped bus arbitration with one clock-bus handovers.

Chip-Selects. Eight programmable chip-select outputs provide signals that enable external memory and

peripheral circuits for automatic wait-state insertion. These signals also interface to 8-, 16-, or 32-bit ports. In addition, other external bus masters can access chip-selects. The upper 4 chip-selects are multiplexed with A[27:24] of the address bus and the 4 write-enable signals. The base address, access permissions, and timing waveforms are all programmable with configuration registers.

Except for full-page mode, all operations are available to other external bus masters. The DRAM controller can generate $\overline{CAS}$ and $\overline{RAS}$ for an external master and can continue to manage refresh requests.

8-Bit General-Purpose Interface. An 8-bit general-purpose programmable parallel port serves as either an input or an output on a bit-by-bit basis. The parallel port is multiplexed with PST[3:0] and DDATA[3:0] debug signals.

Interrupt Controller. The interrupt controller provides user-programmable control of 3 or 7 external interrupt and 5 internal peripheral interrupts. Users can program each internal interrupt to any one of 7 interrupt levels and 4 priority levels within each of these levels. The 3 external interrupt signals can be configured as either fixed interrupt levels 1, 4, and 7, or as a 7-level encoded interrupt. Users can program the external interrupts to any one of the 4 priority levels within the respective interrupt levels.

System Protection. The MCF5206 processor contains a 16-bit software watchdog timer with an 8-bit prescaler. The programmable software watchdog timer provides either a level 7 interrupt or a hardware reset on timeout. The MCF5206 processor also contains a reset status register that indicates the cause of the last reset.

JTAG. To help with system diagnostics and manufacturing testing, the MCF5206 processor includes dedicated user-accessible test logic that complies with the IEEE 1149.1 standard for boundary scan testability, often referred to as Joint Test Action Group, or JTAG. For more information, refer to the IEEE 1149.1 standard.

System Debug Interface

The ColdFire processor core debug interface supports real-time trace and background-debug mode. A four-pin background debug mode (BDM) interface provides system debug. The BDM is a proper subset of the BDM interface provided on Motorola's 683XX Family of parts.

In real-time trace, 4 status lines provide information on processor activity in real time (PST pins). A 4-bit wide debug data bus (DDATA) displays operand data, which helps track the machine's dynamic execution path as the change-of-flow instructions execute. These signals are multiplexed with an 8-bit parallel port for application development, which does not use real-time trace.

Pinout and Package

The MCF5206 device is supplied in a 160-pin plastic quad flat pack package with the pinout shown in Figure 2.

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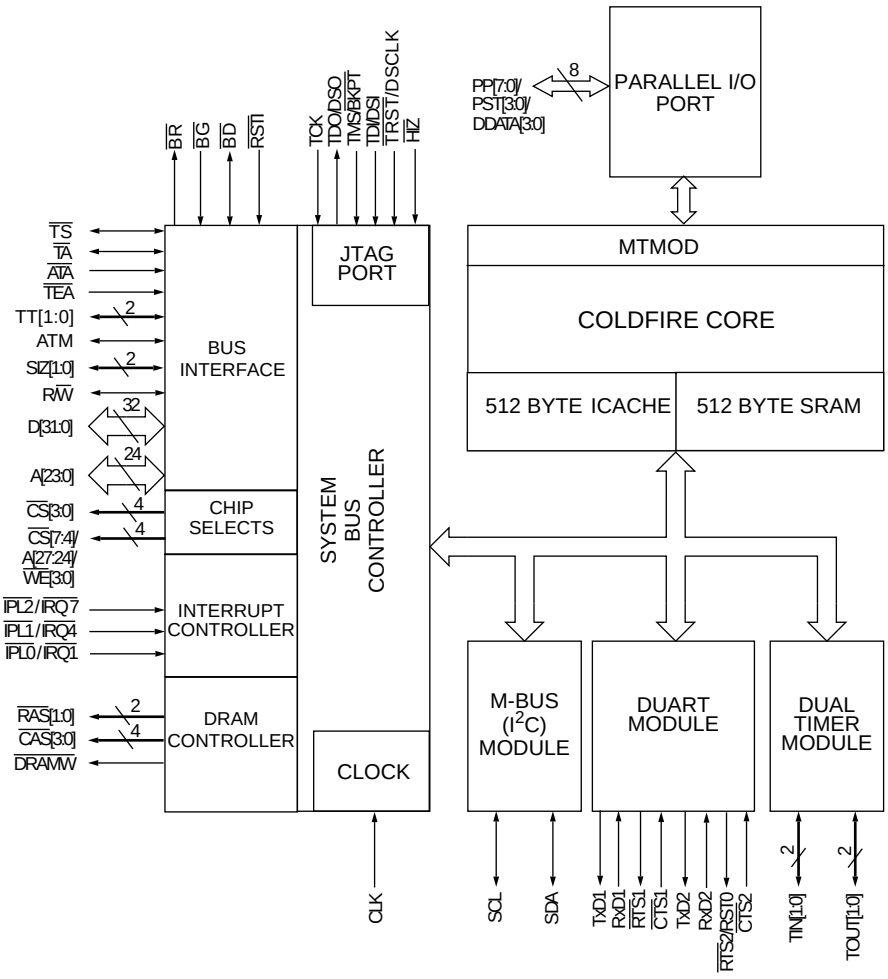

MORE INFORMATION

The table below identifies the packages and operating frequencies currently available for the MCF5206 processor.

MCF5206 Package/Frequency Availability

PACKAGE	FREQUENCY
Plastic Quad Flat Pack 160 lead	16, 25, and 33Mhz

Documentation

Additional and detailed information is available from Motorola literature distribution centers.

DOCUMENT NUMBER	DOCUMENT TITLE	AVAILABILITY
MCF5206UM/AD	MCF5206 User's Manual	1Q97 WWW 1Q97
MCF5200PRM/AD	MCF5200 ColdFire Family Programmer's Reference Manual	now

DEVELOPMENT TOOLS AND EVALUATION SYSTEMS

For information on third-party development tools support, refer to the *High Performance Embedded Systems Source* (BR729/D).

ColdFire evaluation boards are available. Contact your local Motorola sales office for technical details and additional information on these boards.

Visit the Motorola web site at http://www.mot.com/coldfire for additional information on any ColdFire family product.

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036
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