CMOS MT9123

Dual Voice Echo Canceller

Data Sheet

November 2005

Features

- Dual channel 64 ms or single channel 128 ms echo cancellation
- Conforms to ITU-T G.165 requirements
- Narrow-band signal detection
- Programmable double-talk detection threshold
- Non-linear processor with adaptive suppression threshold and comfort noise insertion
- Offset nulling of all PCM channels
- Controllerless mode or Controller mode with serial interface
- ST-BUS or variable-rate SSI PCM interfaces
- Selectable μ/A-Law ITU-T G.711; μ/A-Law Sign Mag; linear 2's complement
- Per channel selectable 12 dB attenuator
- Transparent data transfer and mute option
- 19.2 MHz master clock operation

Applications

- Wireless Telephony
- Trunk echo cancellers

Ordering Information

MT9123AP	28 Pin PLCC	Tubes
MT9123AE	28 Pin PDIP	Tubes
MT9123APR	28 Pin PLCC	Tape & Reel
MT9123AP1	28 Pin PLCC*	Tubes
MT9123APR1	28 Pin PLCC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

Description

The MT9123 Voice Echo Canceller implements a cost effective solution for telephony voice-band echo cancellation conforming to ITU-T G.165 requirements. The MT9123 architecture contains two echo cancellers which can be configured to provide dual channel 64 millisecond echo cancellation or single channel 128 millisecond echo cancellation.

The MT9123 operates in two major modes: Controller or Controllerless. Controller mode allows access to an array of features for customizing the MT9123 operation. Controllerless mode is for applications where default register settings are sufficient.

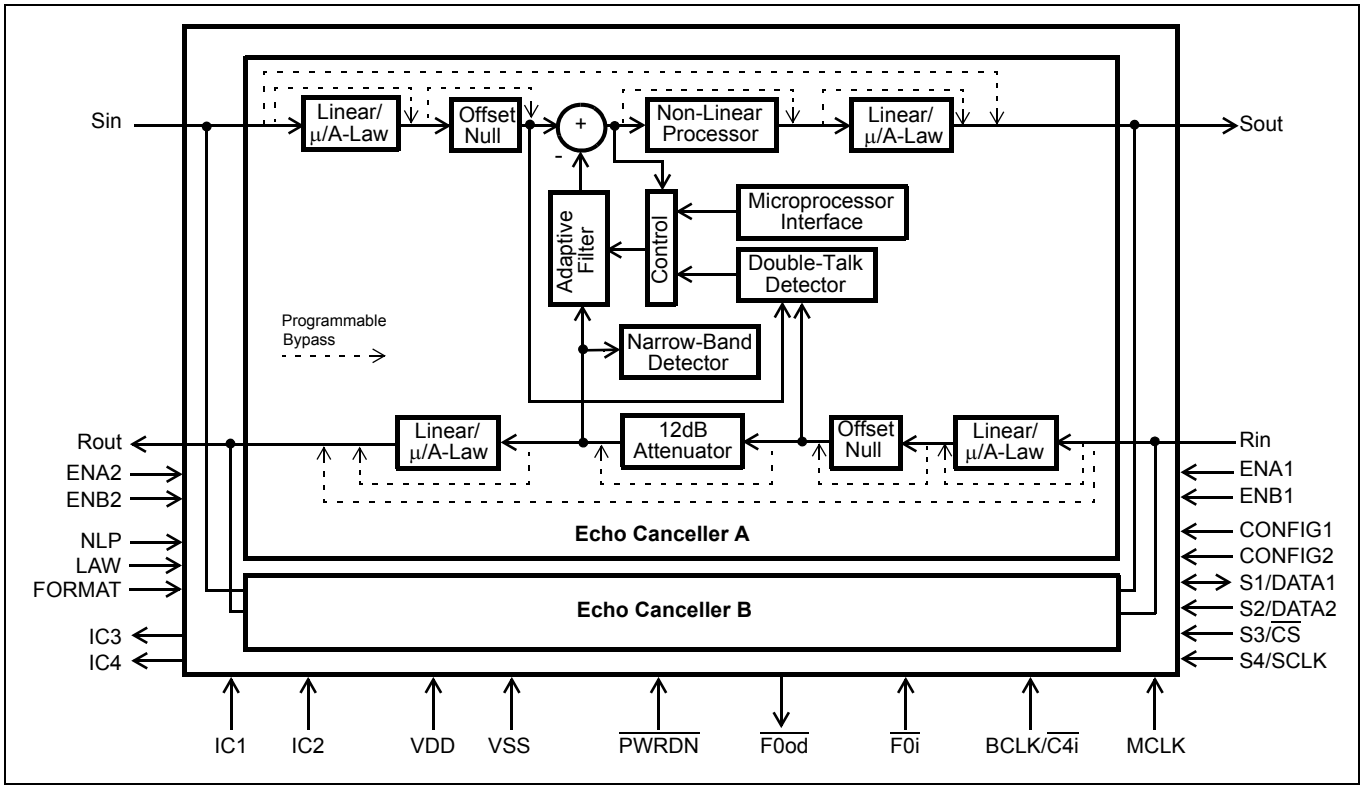


Figure 1 - Functional Block Diagram

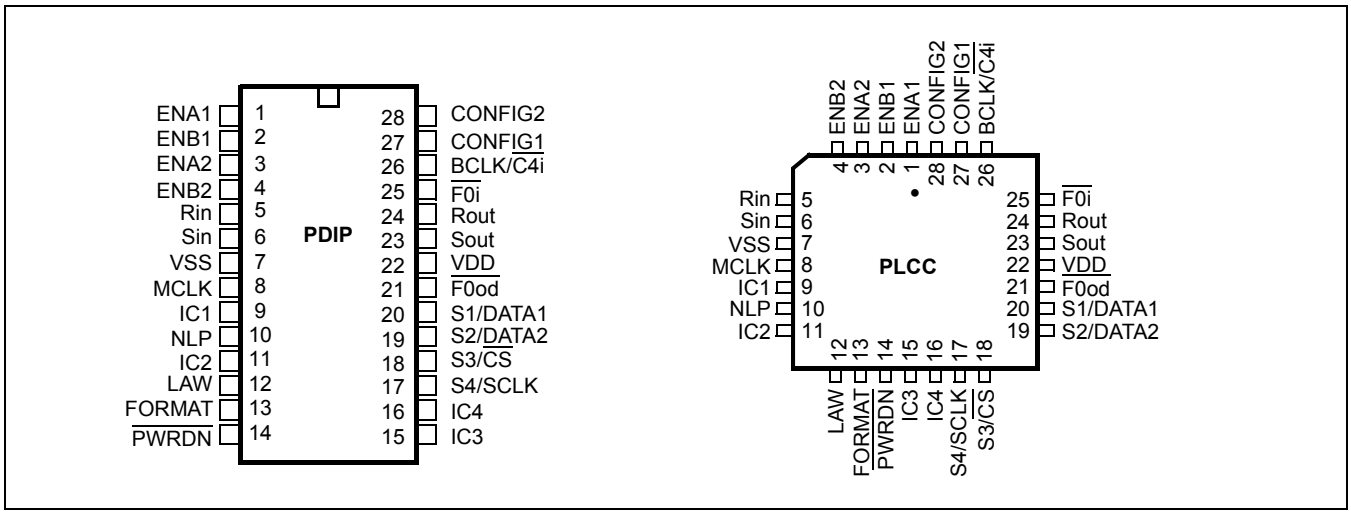


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	ENA1	**SSI Enable Strobe / ST-BUS Mode for Rin/Sout (Input)**. This pin has dual functions depending on whether SSI or ST-BUS is selected. For SSI, this strobe must be present for frame synchronization. This is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer for Echo Canceller A on Rin/Sout pins. Strobe period is 125 microseconds. For ST-BUS, this pin, in conjunction with the ENB1 pin, will select the proper ST-BUS mode for Rin/Sout pins (see ST-BUS Operation description). The selected mode applies to both Echo Canceller A and B.
2	ENB1	**SSI Enable Strobe / ST-BUS Mode for Rin/Sout (Input)**. This pin has dual functions depending on whether SSI or ST-BUS is selected. For SSI, this is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer for Echo Canceller B on Rin/Sout pins. Strobe period is 125 microseconds. For ST-BUS, this pin, in conjunction with the ENA1 pin, will select the proper ST-BUS mode for Rin/Sout pins (see ST-BUS Operation description). The selected mode applies to both Echo Canceller A and B.
3	ENA2	**SSI Enable Strobe / ST-BUS Mode for Sin/Rout (Input)**. This pin has dual functions depending on whether SSI or ST-BUS is selected. For SSI, this is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer for Echo Canceller A on Sin/Rout pins. Strobe period is 125 microseconds. For ST-BUS, this pin, in conjunction with the ENB2 pin, will select the proper ST-BUS mode for Sin/Rout pins (see ST-BUS Operation description). The selected mode applies to both Echo Canceller A and B.

Pin Description (continued)

Pin #	Name	Description
4	ENB2	**SSI Enable Strobe / ST-BUS Mode for Sin/Rout (Input)**. This pin has dual functions depending on whether SSI or ST-BUS is selected. For SSI, this is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer for Echo Canceller B on Sin/Rout pins. Strobe period is 125 microseconds. For ST-BUS, this pin, in conjunction with the ENA2 pin, will select the proper ST-BUS mode for Sin/Rout pins (see ST-BUS Operation description). The selected mode applies to both Echo Canceller A and B.
5	Rin	**Receive PCM Signal Input (Input).** 128 kbit/s to 4096 kbit/s serial PCM input stream. Data may be in either companded or 2's complement linear format. Two PCM channels are time-multiplexed on this pin. These are the Receive Input reference channels for Echo Cancellers A and B. Data bits are clocked in following SSI or ST-BUS timing requirements.
6	Sin	**Send PCM Signal Input (Input).** 128 kbit/s to 4096 kbit/s serial PCM input stream. Data may be in either companded or 2's complement linear format. Two PCM channels are time-multiplexed on this pin. These are the Send Input channels (after echo path) for Echo Cancellers A and B. Data bits are clocked in following SSI or ST-BUS timing requirements.
7	VSS	**Digital Ground.** Nominally 0 volts.
8	MCLK	**Master Clock (Input).** Nominal 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.
9	IC1	**Internal Connection 1 (Input).** Must be tied to Vss.
10	NLP	**Non-Linear Processor Control (Input).** Controllerless Mode: An active high enables the Non-Linear Processors in Echo Cancellers A and B. Both NLP's are disabled when low. Intended for conformance testing to G.165 and it is usually tied to Vdd for normal operation. Controller Mode: This pin is ignored (tie to Vdd or Vss). The non-linear processor operation is controlled by the NLPDis bit in Control Register 2. Refer to the Register Summary.
11	IC2	**Internal Connection 2 (Input).** Must be tied to Vss.
12	LAW	**A/$\overline{\mu}$ Law Select (Input).** An active low selects μ–Law companded PCM. When high, selects A-Law companded PCM. This control is for both echo cancellers and is valid for both controller and controllerless modes.
13	FORMAT	**ITU-T/$\overline{\text{Sign Mag}}$ (Input).** An active low selects sign-magnitude PCM code. When high, selects ITU-T (G.711) PCM code. This control is for both echo cancellers and is valid for both controller and controllerless modes.
14	PWRDN	**Power-down (Input).** An active low resets the device and puts the MT9123 into a low-power stand-by mode.
15	IC3	**Internal Connection 3 (Output).** Must be left unconnected.
16	IC4	**Internal Connection 4 (Output).** Must be left unconnected.

Pin Description (continued)

Pin #	Name	Description
17/18	S4/S3	**Selection of Echo Canceller B Functional States (Input).** Controllerless Mode: Selects Echo Canceller B functional states according to Table 2. Controller Mode: S4 and S3 pins become SCLK and $\overline{CS}$ pins respectively.
17	SCLK	**Serial Port Synchronous Clock (Input).** Data clock for the serial microport interface.
18	CS	Chip Select (Input). Enables serial microport interface data transfers. Active low.
19/20	S2/S1	**Selection of Echo Canceller A Functional States (Input).** Controllerless Mode: Selects Echo Canceller A functional states according to Table 2. Controller Mode: S2 and S1 pins become DATA2 and DATA1 pins respectively.
19	DATA2	**Serial Data Receive (Input).** In Motorola/National serial microport operation, the DATA2 pin is used for receiving data. In Intel serial microport operation, the DATA2 pin is not used and must be tied to Vss or Vdd.
20	DATA1	**Serial Data Port (Bidirectional).** In Motorola/National serial microport operation, the DATA1 pin is used for transmitting data. In Intel serial microport operation, the DATA1 pin is used for transmitting and receiving data.
21	F0od	**Delayed Frame Pulse Output (Output).** In ST-BUS operation, this pin generates a delayed frame pulse after the 4th channel time slot and is used for daisy-chaining multiple ST-BUS devices. See Figures 4 to 7. In SSI operation, this pin outputs logic low.
22	VDD	**Positive Power Supply.** Nominally 5 volts.
23	Sout	**Send PCM Signal Output (Output).** 128 kbit/s to 4096 kbit/s serial PCM output stream. Data may be in either companded or 2's complement linear PCM format. Two PCM channels are time-multiplexed on this pin. These are the Send Out signals after echo cancellation and Non-linear processing. Data bits are clocked out following SSI or ST-BUS timing requirements.
24	Rout	**Receive PCM Signal Output (Output).** 128 kbit/s to 4096 kbit/s serial PCM output stream. Data may be in either companded or 2's complement linear PCM format. Two PCM channels are time-multiplexed on this pin. This output pin is provided for convenience in some applications and may not always be required. Data bits are clocked out following SSI or ST-BUS timing requirements.
25	F0i	**Frame Pulse (input).** In ST-BUS operation, this is a frame alignment low going pulse. SSI operation is enabled by connecting this pin to Vss.
26	BCLK/$\overline{C4i}$	**Bit Clock/ST-BUS Clock (Input).** In SSI operation, BCLK pin is a 128 kHz to 4.096 MHz bit clock. This clock must be synchronous with ENA1, ENA2, ENB1 and ENB2 enable strobes. In ST-BUS operation, $\overline{C4i}$ pin must be connected to the 4.096 MHz ($\overline{C4}$) system clock.

Pin Description (continued)

Pin #	Name	Description
27/28	CONFIG1/ CONFIG2	**Device Configuration Pins (Inputs).** When CONFIG1 and CONFIG2 pins are both logic 0, the MT9123 serial microport is enabled. This configuration is defined as Controller Mode. When CONFIG1 and CONFIG2 pins are in any other logic combination, the MT9123 is configured in Controllerless Mode. See Table 3.

Notes:

1. All unused inputs should be connected to logic low or high unless otherwise stated. All outputs should be left open circuit when not used.
2. All inputs have TTL compatible logic levels except for MCLK, Sin and Rin pins which have CMOS compatible logic levels and $\overline{\text{PWRDN}}$ pin which has Schmitt trigger compatible logic levels.
3. All outputs are CMOS pins with CMOS logic levels.

Functional Description

The MT9123 architecture contains two individually controlled echo cancellers (Echo Canceller A and B). They can be set in three distinct configurations: Normal, Back-to-Back and Extended Delay (see Figure 3). Under Normal configuration, the two echo cancellers are positioned in parallel providing 64 millisecond echo cancellation in two channels simultaneously. In Back-to-Back configuration, the two echo cancellers are positioned to cancel echo coming from both directions in a single channel. In Extended-Delay configuration, the two echo cancellers are internally cascaded into one 128 millisecond echo canceller.

Each echo canceller contains the following main elements (see Figure 1).

- Adaptive Filter for estimating the echo channel
- Subtracter for cancelling the echo
- Double-Talk detector for disabling the filter adaptation during periods of double-talk
- Non-Linear Processor for suppression of residual echo
- Narrow-Band Detector for preventing Adaptive Filter divergence caused by narrow-band signals
- Offset Null filters for removing the DC component in PCM channels
- 12 dB attenuator for signal attenuation
- Serial controller interface compatible with Motorola, National and Intel microcontrollers
- PCM encoder/decoder compatible with μ/A-Law ITU-T G.711, μ/A-Law Sign-Mag or linear 2's complement coding

The MT9123 has two modes of operation: *Controllerless* and *Controller*. Controllerless mode is intended for applications where customization is not required. Controller mode allows access to all registers for customizing the MT9123 operation. Refer to Table 7 for a complete list. Controller mode is selected when CONFIG1 and CONFIG2 pins are both connected to Vss.

Each echo canceller in the MT9123 has four functional states: *Mute*, *Bypass*, *Disable Adaptation* and *Enable Adaptation*. These are explained in the section entitled Echo Canceller Functional States.

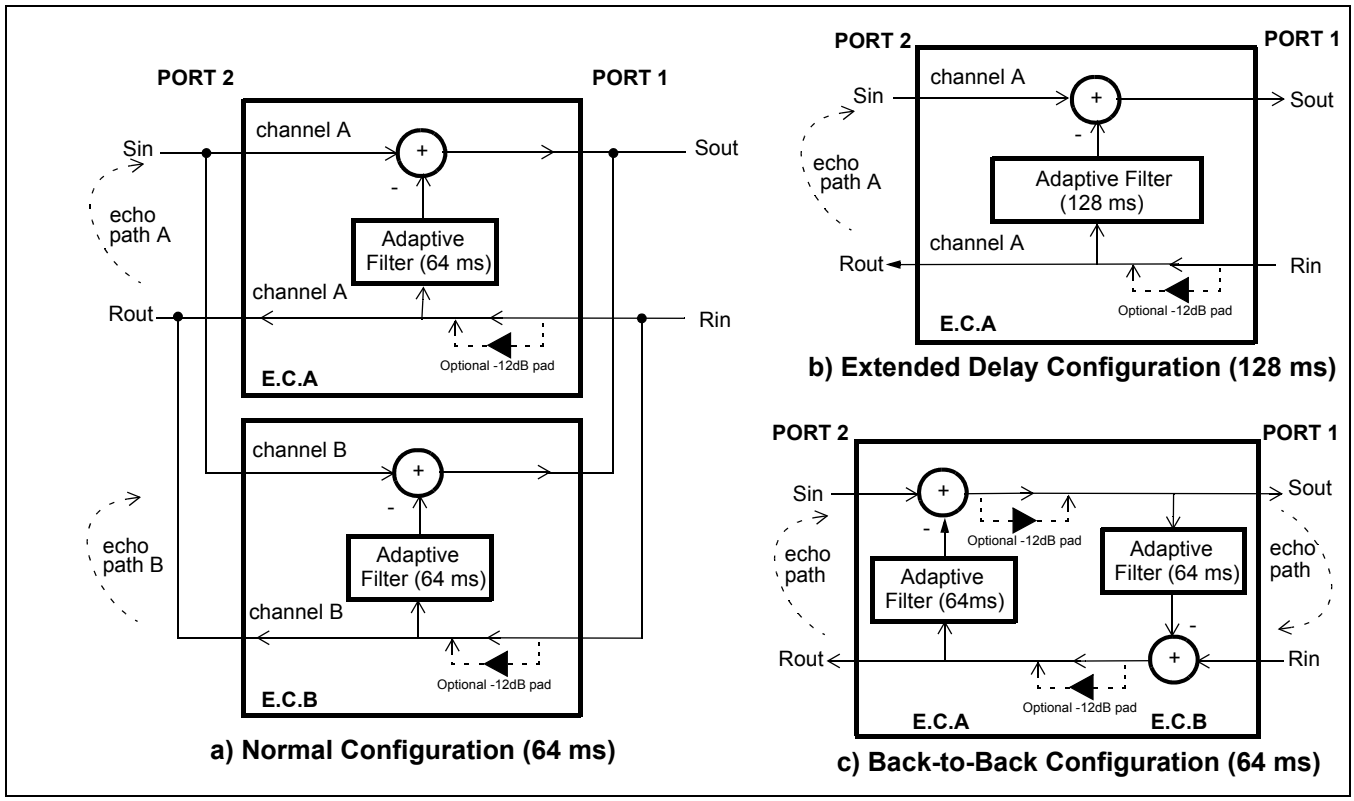


Figure 3 - Device Configuration

Adaptive Filter

The adaptive filter is a 1024 tap FIR filter which is divided into two sections. Each section contains 512 taps providing 64 ms of echo estimation. In Normal configuration, the first section is dedicated to channel A and the second section to channel B. In Extended Delay configuration, both sections are cascaded to provide 128 ms of echo estimation in channel A.

Double-Talk Detector

Double-Talk is defined as those periods of time when signal energy is present in both directions simultaneously. When this happens, it is necessary to disable the filter adaptation to prevent divergence of the adaptive filter coefficients. Note that when double-talk is detected, the adaptation process is halted but the echo canceller continues to cancel echo.

A double-talk condition exists whenever the Sin signal level is greater than the expected return echo level. The relative signal levels of Rin (Lrin) and Sin (Lsin) are compared according to the following expression to identify a double-talk condition:

$$Lsin > Lrin + 20log_{10}(DTDT)$$

where DTDT is the Double-Talk Detection Threshold. Lsin and Lrin are the relative signal levels expressed in dBm0.

A different method is used when it is uncertain whether Sin consists of a low level double-talk signal or an echo return. During these periods, the adaptation process is slowed down but it is not halted.

Controllerless Mode

In G.165 standard, the echo return loss is expected to be at least 6 dB. This implies that the Double-Talk Detector Threshold (DTDT) should be set to 0.5 (-6 dB). However, in order to get additional guardband, the DTDT is set internally to 0.5625 (-5 dB). In controllerless mode, the Double-Talk Detector is always active.

Controller Mode

In some applications the return loss can be higher or lower than 6 dB. The MT9123 allows the user to change the detection threshold to suit each application's need. This threshold can be set by writing the desired threshold value into the DTDT register.

The DTDT register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$DTDT_{(hex)} = hex(DTDT_{(dec)} * 32768)$$

where $0 < DTDT_{(dec)} < 1$

Example: For DTDT = 0.5625 (-5 dB), the hexadecimal value becomes
$hex($0.5625 * 32768$)$ = 4800h

Non-Linear Processor (NLP)

After echo cancellation, there is always a small amount of residual echo which may still be audible. The MT9123 uses an NLP to remove residual echo signals which have a level lower than the Adaptive Suppression Threshold (TSUP in G.165). This threshold depends upon the level of the Rin (Lrin) reference signal as well as the programmed value of the Non-Linear Processor Threshold register (NLPTHR). TSUP can be calculated by the following equation:

$$TSUP = Lrin + 20log_{10}(NLPTHR)$$

where NLPTHR is the Non-Linear Processor Threshold register value and Lrin is the relative power level expressed in dBm0.

When the level of residual error signal falls below TSUP, the NLP is activated further attenuating the residual signal to less than -65 dBm0. To prevent a perceived decrease in background noise due to the activation of the NLP, a spectrally-shaped comfort noise, equivalent in power level to the background noise, is injected. This keeps the perceived noise level constant. Consequently, the user does not hear the activation and de-activation of the NLP.

Controllerless Mode

The NLP processor can be disabled by connecting the NLP pin to Vss.

Controller Mode

The NLP processor can be disabled by setting the NLPDis bit to 1 in Control Register 2.

The NLPTHR register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$NLPTHR_{(hex)} = hex(NLPTHR_{(dec)} * 32768)$$

where $0 < NLPTHR_{(dec)} < 1$

The comfort noise injection can be disabled by setting the INJDis bit to 1 in Control Register 1.

It should be noted that the NLPTHR is valid and the comfort noise injection is active only when the NLP is enabled.

Narrow Band Signal Detector (NBSD)

Single or dual frequency tones (e.g., DTMF tones) present in the reference input (Rin) of the echo canceller for a prolonged period of time may cause the adaptive filter to diverge. The Narrow Band Signal Detector (NBSD) is designed to prevent this divergence by detecting single or dual tones of arbitrary frequency, phase, and amplitude. When narrow band signals are detected, the adaptation process is halted but the echo canceller continues to cancel echo.

Controllerless Mode

The NBSD is always active and automatically disables the filter adaptation process when narrow band signals are detected.

Controller Mode

The NBSD can be disabled by setting the NBDis bit to 1 in Control Register 2.

Offset Null Filter

Adaptive filters in general do not operate properly when a DC offset is present on either the reference signal (Rin) or the echo composite signal (Sin). To remove the DC component, the MT9123 incorporates Offset Null filters in both Rin and Sin inputs.

Controllerless Mode

The Offset Null filters are always active.

Controller Mode

The offset null filters can be disabled by setting the HPFDis bit to 1 in Control Register 2.

Echo Canceller Functional States

Each echo canceller has four functional states: Mute, Bypass, Disable Adaptation and Enable Adaptation.

Mute:

The Mute state forces the echo canceller to transmit quiet code and halts the filter adaptation process.

In Normal configuration, the PCM output data on Rout is replaced with the quiet code according to the following table.

	LINEAR 16 bits 2's complement	SIGN/ MAGNITUDE μ-Law A-Law	CCITT (G.711)	
			μ-Law	A-Law
+Zero (quiet code)	0000h	80h	FFh	D5h

Table 1 - Quiet PCM Code Assignment

In Back-to-Back configuration, both echo cancellers are combined to implement a full duplex echo canceller. Therefore muting Echo Canceller A causes quiet code to be transmitted on Rout, while muting Echo Canceller B causes quiet code to be transmitted on Sout.

In Extended Delay configuration, both echo cancellers are cascaded to make one 128 ms echo canceller. In this configuration, muting Echo Canceller A causes quiet code to be transmitted on Rout.

Bypass:

The Bypass state directly transfers PCM codes from Rin to Rout and from Sin to Sout. When Bypass state is selected, the adaptive filter coefficients are reset to zero.

Disable Adaptation:

When the Disable Adaptation state is selected, the adaptive filter coefficients are frozen at their current value. In this state, the adaptation process is halted however the MT9123 continues to cancel echo.

Enable Adaptation:

In Enable Adaptation state, the adaptive filter coefficients are continually updated. This allows the echo canceller to model the echo return path characteristics in order to cancel echo. This is the normal operating state.

Controllerless Mode

The four functional states can be selected via S1, S2, S3, and S4 pins as shown in the following table.

Echo Canceller A S2/S1	Functional State	Echo Canceller B S4/S3
00	Mute(1)	00
01	Bypass(2)	01
10	Disable Adaptation(1,3)	10
11	Enable Adaptation(3)	11

Table 2 - Functional States Control Pins

(1) Filter coefficients are frozen (adaptation disabled)
(2) The adaptive filter coefficients are reset to zero
(3) The MT9123 cancels echo

Controller Mode

The echo canceller functions are selected in Control Register 1 and Control Register 2 through four control bits: MuteS, MuteR, Bypass and AdaptDis. See Register Summary for details.

MT9123 Throughput Delay

The throughput delay of the MT9123 varies according to the data path and the device configuration. For all device configurations, except for Bypass state, Rin to Rout has a delay of two frames and Sin to Sout has a delay of three frames. In Bypass state, the Rin to Rout and Sin to Sout paths have a delay of two frames. In ST-BUS operation, the D and C channels have a delay of one frame.

Power Down

Forcing the $\overline{\text{PWRDN}}$ pin to logic low, will put the MT9123 into a power down state. In this state all internal clocks are halted, the DATA1, Sout and Rout pins are tristated and the F0od pin output high.

The device will automatically begin the execution of its initialization routines when the $\overline{\text{PWRDN}}$ pin is returned to logic high and a clock is applied to the MCLK pin. The initialization routines execute for one frame and will set the MT9123 to default register values.

Device Configuration

The MT9123 architecture contains two individually controlled echo cancellers (Echo Canceller A and B). They can be set in three distinct configurations: Normal, Back-to-Back, and Extended Delay. See Figure 3.

Normal Configuration:

In this configuration, the two echo cancellers (Echo Canceller A and B) are positioned in parallel, as shown in Figure 3a, providing 64 milliseconds of echo cancellation in two channels simultaneously.

In SSI operation, both channels are available in different timeslots on the same TDM (Time Division Multiplexing) bus. For Echo Canceller A, the ENA1 enable strobe pin defines the Rin/Sout (PORT1) time slot while the ENA2 enable strobe pin defines the Sin/Rout (PORT2) time slot. The ENB1 and ENB2 enable strobes perform the same function for Echo Canceller B.

In ST-BUS operation, the ENA1, ENA2, ENB1 and ENB2 pins are used to determine the PCM data format and the channel locations. See Table 4.

Back-to-Back Configuration:

In this configuration, the two echo cancellers are positioned to cancel echo coming from both directions in a single channel providing full duplex 64 millisecond echo-cancellation. See Figure 3c. This configuration uses only one timeslot on PORT1 and PORT2, allowing a no-glue interface for applications where bidirectional echo cancellation is required.

In SSI operation, ENA1 and ENA2 enable pins are used to strobe data on Rin/Sout and Sin/Rout respectively. In ST-BUS operation, ENA1, ENA2, ENB1 and ENB2 inputs are used to select the ST-BUS mode according to Table 4.

Examples of Back-to-Back configuration include positioning the MT9123 between a codec and a transmission device or between two codecs for echo control on analog trunks.

Extended Delay configuration:

In this configuration, the two echo cancellers are internally cascaded into one 128 millisecond echo canceller. See Figure 3b. In SSI operation, ENA1 and ENA2 enable pins are used to strobe data on Rin/Sout and Sin/Rout respectively. In ST-BUS operation, ENA1, ENA2, ENB1 and ENB2 inputs are used to select the ST-BUS mode according to Table 4.

Controllerless Mode

The three configurations can be selected through the CONFIG1 and CONFIG2 pins as shown in the following table.

CONFIG1	CONFIG2	CONFIGURATION
0	0	*(selects Controller Mode)*
0	1	Extended Delay Mode
1	0	Back-to-Back Mode
1	1	Normal Mode

Table 3 - Configuration in Controllerless Mode

Controller Mode

In Control Register 1, the Normal configuration can be programmed by setting both BBM and Extended-Delay bits to 0. Back-to-Back configuration can be programmed by setting the BBM bit to 1 and Extended-Delay bit to 0.

Extended-Delay configuration can be programmed by setting the Extended-Delay bit to 1 and BBM bit to 0. Both BBM and Extended-Delay bits in Control Register 1 can not be set to 1 at the same time.

PCM Data I/O

The PCM data transfer for the MT9123 is provided through two PCM ports. PORT1 consists of Rin and Sout pins while PORT2 consists of Sin and Rout Pins. The Data is transferred through these ports according to either ST-BUS or SSI conventions. The device determines the mode of operation by monitoring the signal applied to the F0i pin. When a valid ST-BUS frame pulse is applied to the F0i pin, the MT9123 will assume ST-BUS operation. If F0i is tied continuously to Vss the MT9123 will assume SSI operation.

ST-BUS Operation

The ST-BUS PCM interface conforms to Zarlink's ST-BUS standard and it is used to transport 8 bit companded PCM data (using one timeslot) or 16 bit 2's complement linear PCM data (using two timeslots). Pins ENA1 and ENB1 select timeslots on PORT1 while pins ENA2 and ENB2 select timeslots on PORT2. See Table 4 and Figures 5 to 8.

PORT1 Rin/Sout		ST-BUS Mode Selection	PORT2 Sin/Rout	
Enable Pins			Enable Pins	
ENB1	ENA1		ENB2	ENA2
0	0	Mode 1. 8 bit companded PCM I/O on timeslots 0 & 1.	0	0
0	1	Mode 2. 8 bit companded PCM I/O on timeslots 2 & 3.	0	1
1	0	Mode 3. 8 bit companded PCM I/O on timeslots 2 & 3. Includes D & C channel bypass in timeslots 0 & 1.	1	0
1	1	Mode 4. 16 bit 2's complement linear PCM I/O on timeslots 0 - 3.	1	1

Table 4 - ST-BUS Mode Select

Note that if the device is in back-to-back or extended delay configurations, the second timeslot in any ST-BUS Mode contains undefined data. This means that the following timeslots contain undefined data: timeslot 1 in ST-BUS Mode 1; timeslot 3 in ST-BUS Modes 2 & 3 and timeslots 2 and 3 in ST-BUS Mode 4.

SSI Operation

The SSI PCM interface consists of data input pins (Rin, Sin), data output pins (Sout, Rout), a variable rate bit clock (BCLK), and four enable pins (ENA1,ENB1, ENA2 and ENB2) to provide strobes for data transfers. The active high enable may be either 8 or 16 BCLK cycles in duration. Automatic detection of the data type (8 bit companded or 16 bit 2's complement linear) is accomplished internally. The data type cannot change dynamically from one frame to the next.

In SSI operation, the frame boundary is determined by the rising edge of the ENA1 enable strobe (see Figure 9). The other enable strobes (ENB1, ENA2 and ENB2) are used for parsing input/output data and they must pulse within 125 microseconds of the rising edge of ENA1. If they are unused, they must be tied to Vss.

In SSI operation, the enable strobes may be a mixed combination of 8 or 16 BCLK cycles allowing the flexibility to mix 2's complement linear data on one port (e.g., Rin/Sout) with companded data on the other port (e.g., Sin/Rout).

Enable Strobe Pin	Echo Canceller	Port
ENA1	A	1
ENB1	B	1
ENA2	A	2
ENB2	B	2

Table 5 - SSI Enable Strobe Pins

PCM Law and Format Control (LAW, FORMAT)

The PCM companding/coding law used by the MT9123 is controlled through the LAW and FORMAT pins. ITU-T G.711 companding curves for μ-Law and A-Law are selected by the LAW pin. PCM coding ITU-T G.711 and Sign-Magnitude are selected by the FORMAT pin. See Table 6.

PCM Code	Sign-Magnitude FORMAT=0	ITU-T (G.711) FORMAT=1	
	μ/A-LAW LAW = 0 or 1	μ-LAW LAW = 0	A-LAW LAW =1
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
- Zero	0000 0000	0111 1111	0101 0101
- Full Scale	0111 1111	0000 0000	0010 1010

Table 6 - Companded PCM

Linear PCM

The 16-bit 2's complement PCM linear coding permits a dynamic range beyond that which is specified in ITU-T G.711 for companded PCM. The echo-cancellation algorithm will accept 16 bits 2's complement linear code which gives a dynamic range of +15 dBm0.

Linear PCM data must be formatted as 14-bit, 2's complement data with three bits of sign extension in the most significant positions (i.e.: S,S,S,12,11, ...1,0) for a total of 16 bits where "S" is the extended sign bit. When A-Law is converted to 2's complement linear format, it must be scaled up by 6 dB (i.e., left shifted one bit) with a zero inserted into the least significant bit position. See Figure 7.

Bit Clock (BCLK/$\overline{\text{C4i}}$)

The BCLK/$\overline{\text{C4i}}$ pin is used to clock the PCM data in both SSI (BCLK) and ST-BUS ($\overline{\text{C4i}}$) operations.

In SSI operation, the bit rate is determined by the BCLK frequency. This input must contain either eight or sixteen clock cycles within the valid enable strobe window. BCLK may be any rate between 128 KHz to 4.096 MHz and can be discontinuous outside of the enable strobe windows defined by ENA1, ENB1, ENA2 and ENB2 pins. Incoming PCM data (Rin, Sin) are sampled on the falling edge of BCLK while outgoing PCM data (Sout, Rout) are clocked out on the rising edge of BCLK. See Figure 17.

In ST-BUS operation, connect the system $\overline{\text{C4}}$ (4.096 MHz) clock to the $\overline{\text{C4i}}$ pin.

Master Clock (MCLK)

A nominal 20 MHz master clock (MCLK) is required for execution of the MT9123 algorithms. The MCLK input may be asynchronous with the 8 KHz frame. If only one channel operation is required, (Echo Canceller A only) the MCLK can be as low as 9.6 MHz.

Microport

The serial microport provides access to all MT9123 internal read and write registers and it is enabled when CONFIG1 and CONFIG2 pins are both set to logic 0. This microport is compatible with Intel MCS-51 (mode 0), Motorola SPI (CPOL=0, CPHA=0), and National Semiconductor Microwire specifications. The microport consists of a transmit/receive data pin (DATA1), a receive data pin (DATA2), a chip select pin ($\overline{CS}$) and a synchronous data clock pin (SCLK).

The MT9123 automatically adjusts its internal timing and pin configuration to conform to Intel or Motorola/National requirements. The microport dynamically senses the state of the SCLK pin each time $\overline{CS}$ pin becomes active (i.e., high to low transition). If SCLK pin is high during $\overline{CS}$ activation, then Intel mode 0 timing is assumed. In this case DATA1 pin is defined as a bi-directional (transmit/receive) serial port and DATA2 is internally disconnected. If SCLK is low during $\overline{CS}$ activation, then Motorola/National timing is assumed and DATA1 is defined as the data transmit pin while DATA2 becomes the data receive pin. The MT9123 supports Motorola half-duplex processor mode (CPOL=0 and CPHA=0). This means that during a write to the MT9123, by the Motorola processor, output data from the DATA1 pin must be ignored. This also means that input data on the DATA2 pin is ignored by the MT9123 during a valid read by the Motorola processor.

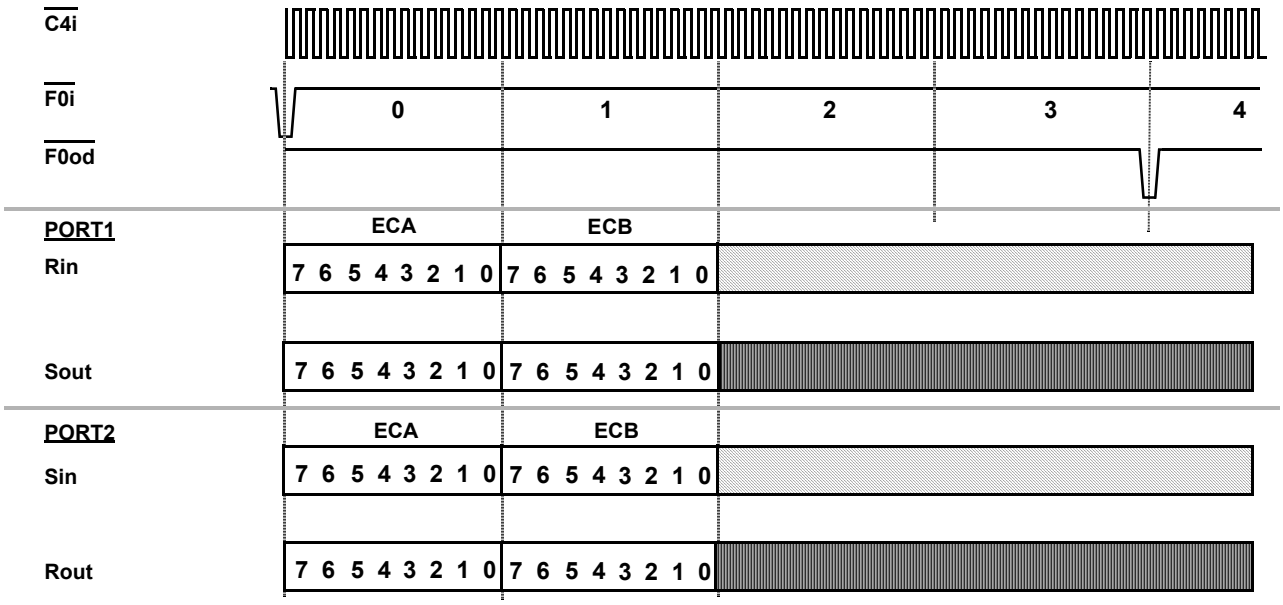
All data transfers through the microport are two bytes long. This requires the transmission of a Command/Address byte followed by the data byte to be written or read from the addressed register. $\overline{CS}$ must remain low for the duration of this two-byte transfer. As shown in Figures 9 and 10, the falling edge of $\overline{CS}$ indicates to the MT9123 that a microport transfer is about to begin. The first 8 clock cycles of SCLK after the falling edge of $\overline{CS}$ are always used to receive the Command/Address byte from the microcontroller. The Command/Address byte contains information detailing whether the second byte transfer will be a read or a write operation and at what address. The next 8 clock cycles are used to transfer the data byte between the MT9123 and the microcontroller. At the end of the two-byte transfer, $\overline{CS}$ is brought high again to terminate the session. The rising edge of $\overline{CS}$ will tri-state the DATA1 pin. The DATA1 pin will remain tri-stated as long as $\overline{CS}$ is high.

Intel processors utilize Least Significant Bit (LSB) first transmission while Motorola/National processors use Most Significant Bit (MSB) first transmission. The MT9123 microport automatically accommodates these two schemes for normal data bytes. However, to ensure timely decoding of the R/$\overline{W}$ and address information, the Command/Address byte is defined differently for Intel and Motorola/National operations. Refer to the relative timing diagrams of Figures 9 and 10.

Receive data is sampled on the rising edge of SCLK while transmit data is clocked out on the falling edge of SCLK. Detailed microport timing is shown in Figure 18 and Figure 19.

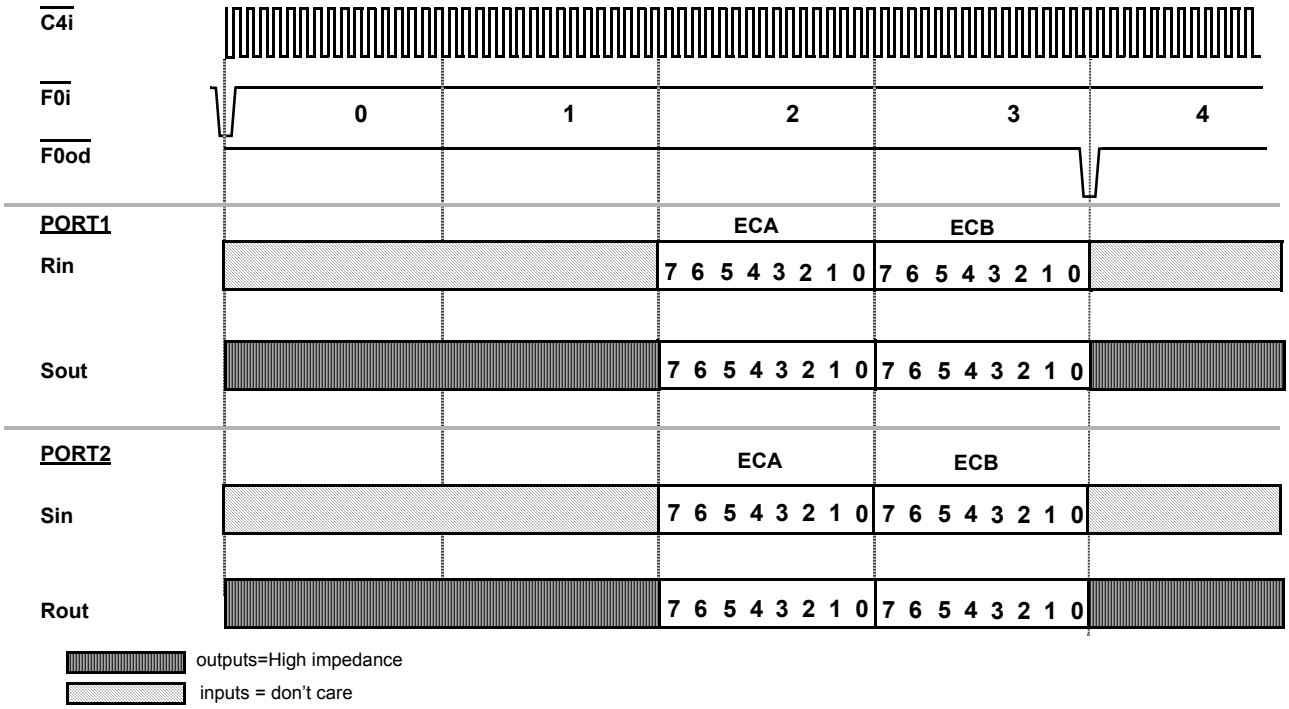
Function	Controllerless selected when pins CONFIG1 & 2 ≠ 00	Controller selected when pins CONFIG1 & 2 = 00
Normal Configuration	Set pins CONFIG1 to 1 and CONFIG2 1 to select this configuration.	Set bits Extended-Delay to 0 and BBM to 0 in Control Register 1 to select.
Back-to-Back Configuration	Set pins CONFIG1 to 1 and CONFIG2 to 0 to select this configuration.	Set bit BBM to 1 in Control Register 1 to select.
Extended Delay Configuration	Set pins CONFIG1 to 0 and CONFIG2 to 1 to select this configuration.	Set bit Extended-Delay to 1 in Control Register 1 to select.
Mute	Set pins S2/S1 to 00 and S4/S3 to 00 to select for Echo Canceller A and Echo Canceller B respectively.	Set bit MuteR to 1 or MuteS to 1 in Control Register 2 to select.
Bypass	Set pins S2/S1 to 01 and S4/S3 to 01 to select for Echo Canceller A and Echo Canceller B, respectively.	Set bit Bypass to 1 in Control Register 1 to select.
Disable Adaptation	Set pins S2/S1 to 10 and S4/S3 to 10 to select for Echo Canceller A and Echo Canceller B, respectively.	Set bit AdaptDis to 1 in Control Register 1 to select.
Enable Adaptation	Set pins S2/S1 to 11 and S4/S3 to 11 to select for Echo Canceller A and Echo Canceller B, respectively.	Set bits AdaptDis to 0 and Bypass to 0 in Control Register 1 to select.
SSI	Tie pin $\overline{F0i}$ to VSS to select.	Tie pin $\overline{F0i}$ to VSS to select.
ST-BUS	Apply a valid ST-BUS frame pulse to $\overline{F0i}$ pin to select.	Apply a valid ST-BUS frame pulse to $\overline{F0i}$ pin to select.
12dB Attenuator	Always disabled.	Set bit PAD to 1 in Control Register 1 to enable.
Double-Talk Detector	Continuously enabled which disables filter adaptation when double-talk is detected.	The detection threshold can be controlled via Double-Talk Detection Threshold Register 1 and 2.
Non-Linear Processor	Set pin NLP to 1 to enable.	Set bit NLPDis to 1 to disable.
PCM Law	Set pin LAW to 1 or 0 to select A-Law or μ-Law respectively.	Set pin LAW to 1or 0 to select A-Law or μ-Law respectively.
PCM Format	Set pin FORMAT to 0 or 1 to select Sign-Magnitude or ITU-T format respectively.	Set pin FORMAT to 0 or 1 to select Sign-Magnitude or ITU-T format respectively.
Narrow-Band Signal Detector	Continuously enabled which disables the filter adaptation when narrow band signal is detected.	Set bit NBDis to 1 in Control Register 2 to disable.
Offset Null Filter	Continuously enabled which removes the DC component in the PCM input.	Set bit HPFDis to 1 in Control Register 2 to disable.

Table 7 - MT9123 Function Control Summary



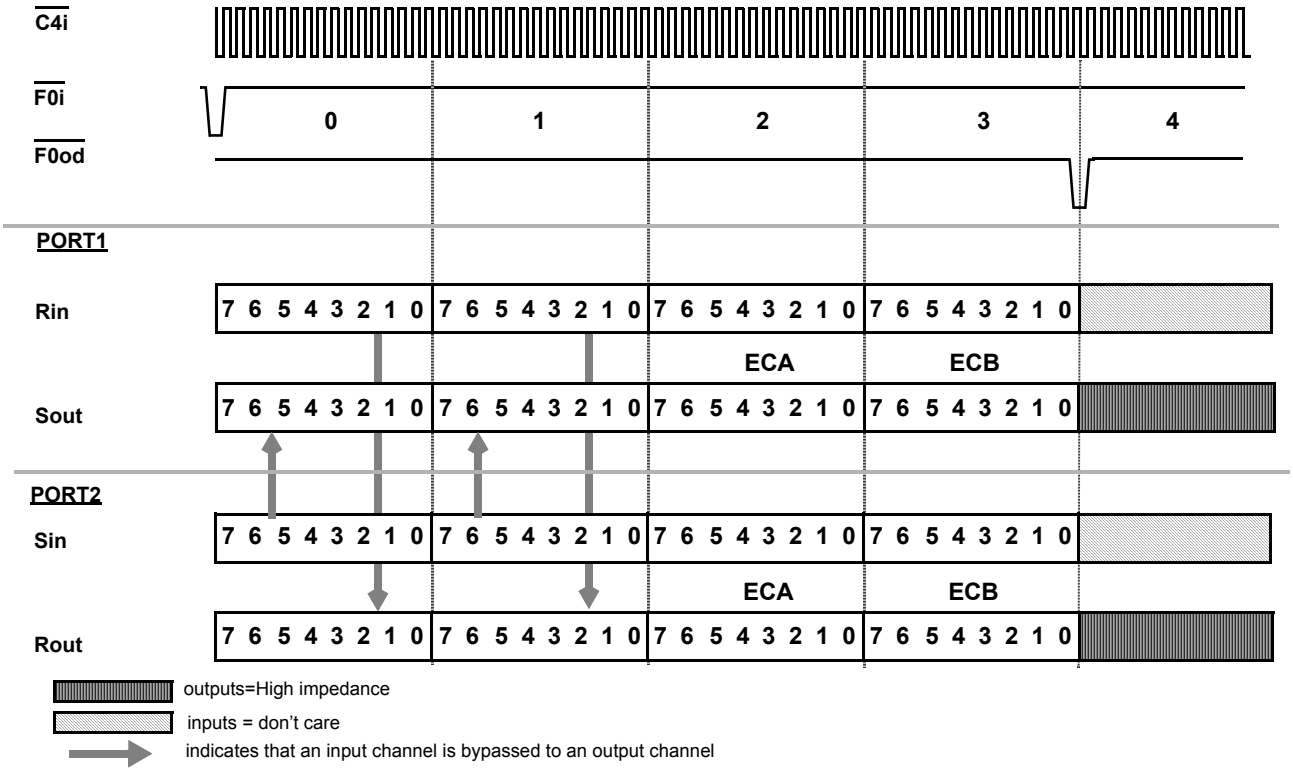
In ST-BUS Mode 1, both echo canceller I/O channels are assigned to ST-BUS timeslots 0 and 1. Note that the user could configure PORT1 and PORT2 into different ST-BUS modes. The pin F0od is always delayed 4 time slots to permit a more flexible interleave of ST-BUS modes.

Figure 4 - ST-BUS 8 Bit Companded PCM I/O on Timeslots 0 & 1 (Mode 1)



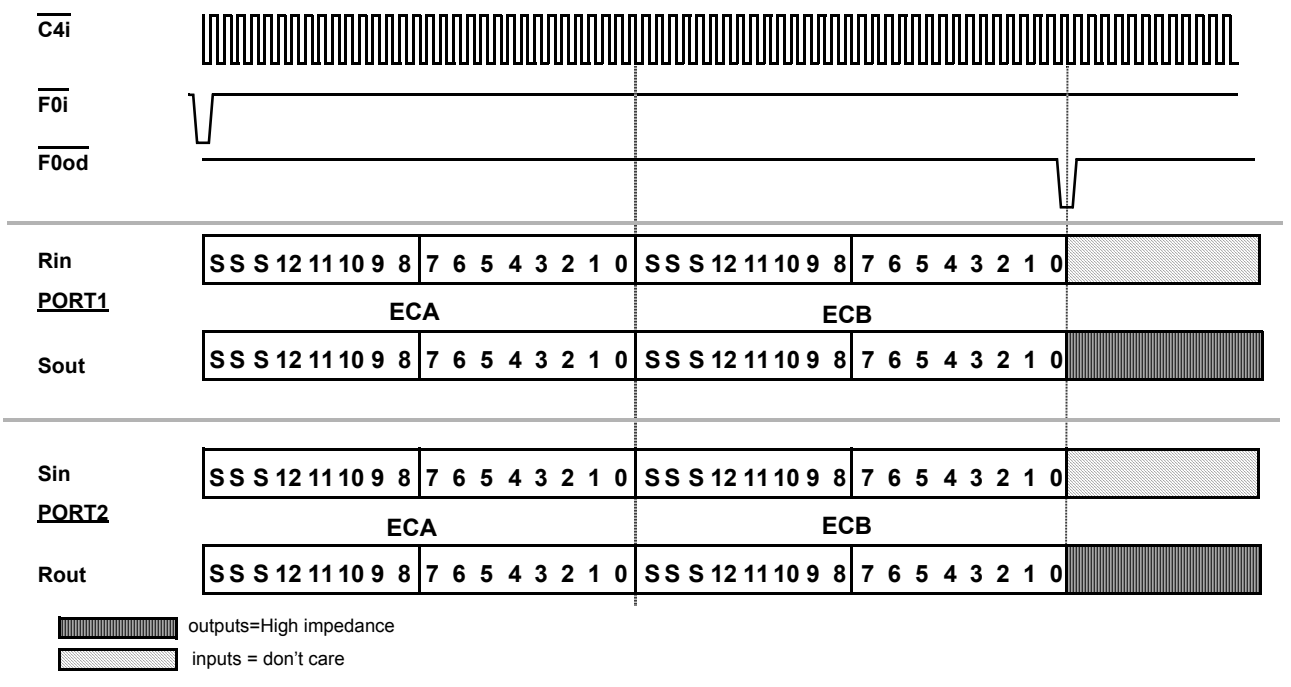
In ST-BUS Mode 2, both echo canceller I/O channels are assigned to ST-BUS timeslots 2 and 3. Note that the user could configure PORT1 and PORT2 into different ST-BUS modes. The pin F0od is always delayed 4 time slots to permit a more flexible interleave of ST-BUS modes.

Figure 5 - ST-BUS 8 Bit Companded PCM I/O on Timeslots 2 & 3 (Mode 2)



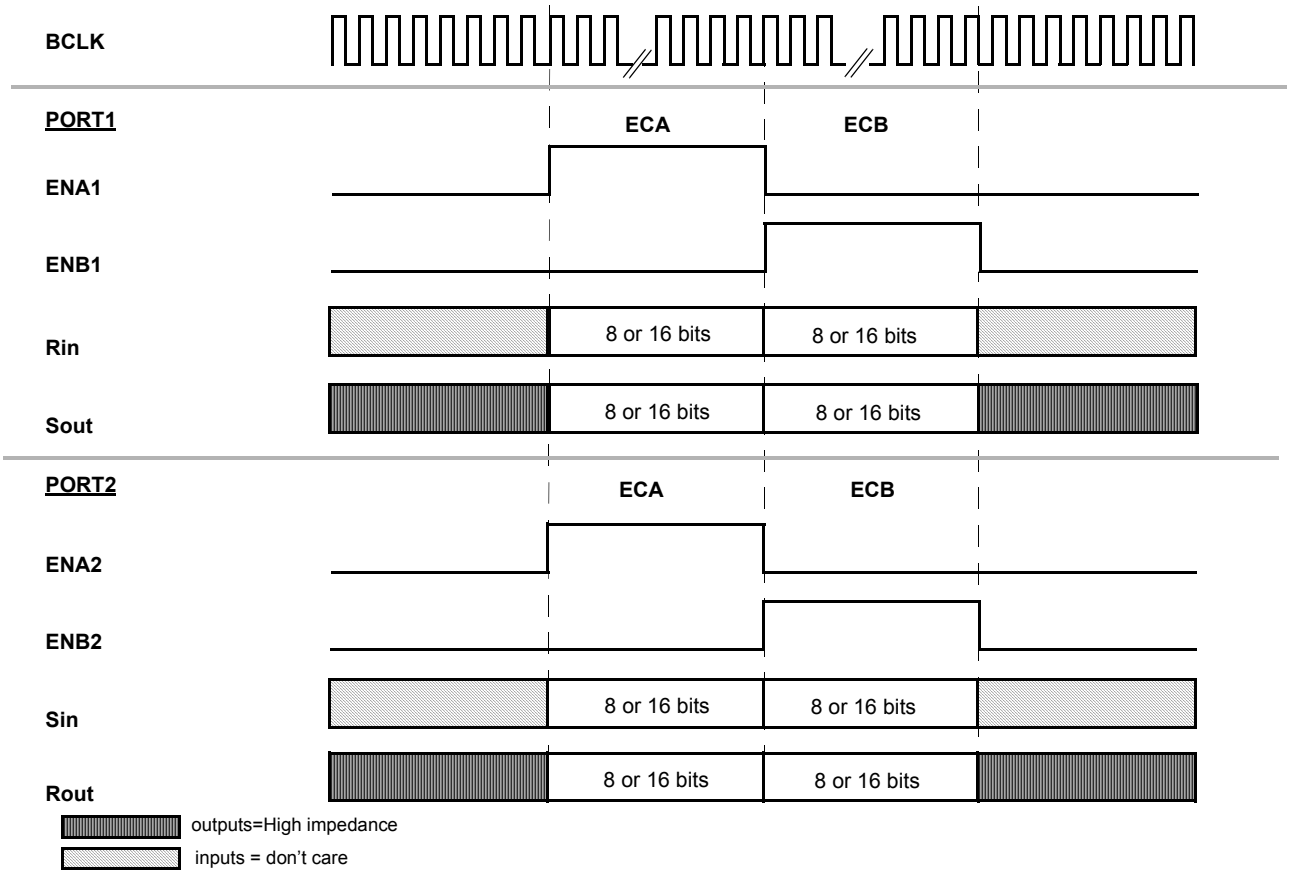
ST-BUS Mode 3 supports connection to 2B+D devices where timeslots 0 and 1 transport D and C channels and both echo canceller I/O channels are assigned to ST-BUS timeslots 2 and 3. Both PORT1 and PORT2 must be configured in ST-BUS Mode 3.

Figure 6 - ST-BUS 8 Bit Companded PCM I/O with D and C channels (Mode 3)



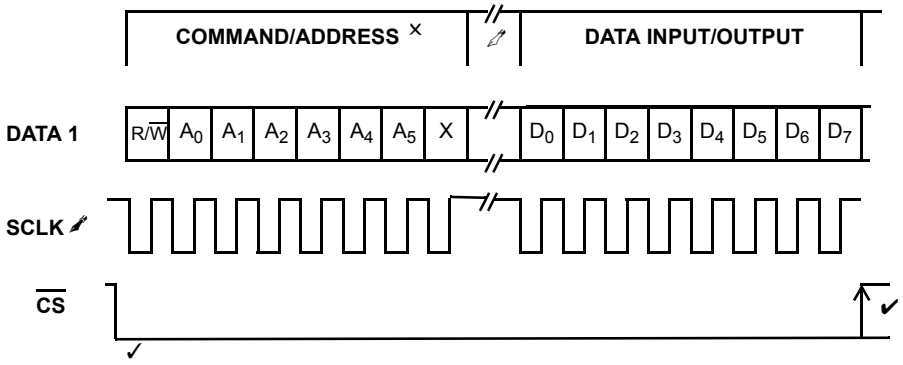
ST-BUS Mode 4 allows 16 bits 2's complement linear data to be transferred using ST-BUS I/O timing. Note that PORT1 and PORT2 need not necessarily both be in mode 4.

Figure 7 - ST-BUS 16 Bit 2's Complement Linear PCM I/O (Mode 4)



Note that the two ports are independent so that, for example, PORT1 can operate with 8 bit enable strobes and PORT2 can operate with 16 bit enable strobes.

Figure 8 - SSI Operation



Delays due to internal processor timing which are transparent to the MT9123.

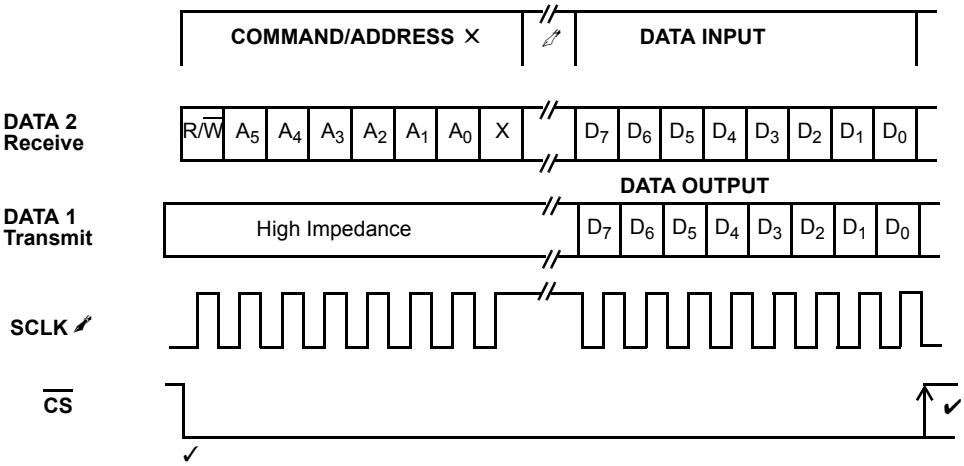
The MT9123: latches receive data on the rising edge of SCLK
outputs transmit data on the falling edge of SCLK

✓ The falling edge of $\overline{CS}$ indicates that a COMMAND/ADDRESS byte will be transmitted from the microprocessor. The subsequent byte is always data followed by $\overline{CS}$ returning high.

✔ A new COMMAND/ADDRESS byte may be loaded only by $\overline{CS}$ cycling high then low again.

× The COMMAND/ADDRESS byte contains: 1 bit - Read/$\overline{Write}$
6 bits - Addressing Data
1 bit - Unused

Figure 9 - Serial Microport Timing for Intel Mode 0



Delays due to internal processor timing which are transparent to the MT9123.

The MT9123: latches receive data on the rising edge of SCLK
outputs transmit data on the falling edge of SCLK

✓ The falling edge of $\overline{CS}$ indicates that a COMMAND/ADDRESS byte will be transmitted from the microprocessor. The subsequent byte is always data followed by $\overline{CS}$ returning high.

✔ A new COMMAND/ADDRESS byte may be loaded only by $\overline{CS}$ cycling high then low again.

× The COMMAND/ADDRESS byte contains: 1 bit - Read/$\overline{Write}$
6 bits - Addressing Data
1 bit - Unused

Figure 10 - Serial Microport Timing for Motorola Mode 00 or National Microwire

Register Summary

Echo Canceller A, Control Register 1 ADDRESS = 00h WRITE/READ VERIFY

CRA1

7	6	5	4	3	2	1	0
Reset	INJDis	BBM	PAD	Bypass	AdaptDis	0	Extended Delay

Power Reset Value 0000 0000

Echo Canceller B, Control Register 1 ADDRESS = 20h WRITE/READ VERIFY

CRB1

7	6	5	4	3	2	1	0
Reset	INJDis	BBM	PAD	Bypass	AdaptDis	1	0

Power Reset Value 0000 0010

Extended-Delay	When high, Echo Cancellers A and B are internally cascaded into one 128ms echo canceller. When low, Echo Cancellers A and B operate independently. Do not enable both Extended-Delay and BBM configurations at the same time.
AdaptDis	When high, echo canceller adaptation is disabled. When low, the echo canceller dynamically adapts to the echo path characteristics.
Bypass	When high, Sin data is by-passed to Sout and Rin data is by-passed to Rout. When low, output data on both Sout and Rout is a function of the echo canceller algorithm.
PAD	When high, 12 dB of attenuation is inserted into the Rin to Rout path. When low the Rin to Rout path gain is 0 dB.
BBM	When high the Back to Back configuration is enabled. When low the Normal configuration is enabled. Do not enable Extended-Delay and BBM configurations at the same time. Always set both BBM bits of the two echo cancellers to the same logic value to avoid conflict.
INJDis	When high, the noise injection process is disabled. When low noise injection is enabled.
Reset	When high, the power-up initialization is executed presetting all register bits including this bit.

Note: Bits marked as "1" or "0" are reserved bits and should be written as indicated.

Echo Canceller A, Control Register 2 ADDRESS = 01h WRITE/READ VERIFY
Echo Canceller B, Control Register 2 ADDRESS = 21h WRITE/READ VERIFY

CR2

7	6	5	4	3	2	1	0
0	0	NLPDis	0	NBDis	HPFDis	MuteS	MuteR

Power Reset Value 0000 0000

MuteR	When high, data on Rout is muted to quiet code. When low, Rout carries active code.
MuteS	When high, data on Sout is muted to quiet code. When low, Sout carries active code.
HPFDis	When high, the offset nulling high pass filters are bypassed in the Rin and Sin paths. When low, the offset nulling filters are active and will remove DC offsets on PCM input signals.
NBDis	When high, the narrow-band detector is disabled. When low, the narrow-band detector is enabled.
NLPDis	When high, the non-linear processor is disabled. When low, the non-linear processors function normally. Useful for G.165 conformance testing.

Note: Bits marked as "0" are reserved bits and should be written as indicated.

Echo Canceller A, Status Register ADDRESS = 02h READ
Echo Canceller B, Status Register ADDRESS = 22h READ

SR

		DTDet	Conv	Down	Active		NB
7	6	5	4	3	2	1	0

Power Reset Value
0000 0000

NB	Logic high indicates the presence of a narrow-band signal on Rin.
Active	Logic high indicates that the power level on Rin is above the threshold level (i.e., low power condition).
Down	Decision indicator for the non-linear processor gain adjustment.
Conv	Decision indicator for rapid adaptation convergence. Logic high indicates a rapid convergence state.
DTDet	Logic high indicates the presence of a double-talk condition.

Echo Canceller A, Flat Delay Register ADDRESS = 04h WRITE/READ VERIFY
Echo Canceller B, Flat Delay Register ADDRESS = 24h WRITE/READ VERIFY

FD

FD_7	FD_6	FD_5	FD_4	FD_3	FD_2	FD_1	FD_0
7	6	5	4	3	2	1	0

Power Reset Value 00h

Echo Canceller A, Decay Step Number Register ADDRESS = 07h WRITE/READ VERIFY
Echo Canceller B, Decay Step Number Register ADDRESS = 27h WRITE/READ VERIFY

NS

NS_7	NS_6	NS_5	NS_4	NS_3	NS_2	NS_1	NS_0
7	6	5	4	3	2	1	0

Power Reset Value 00h

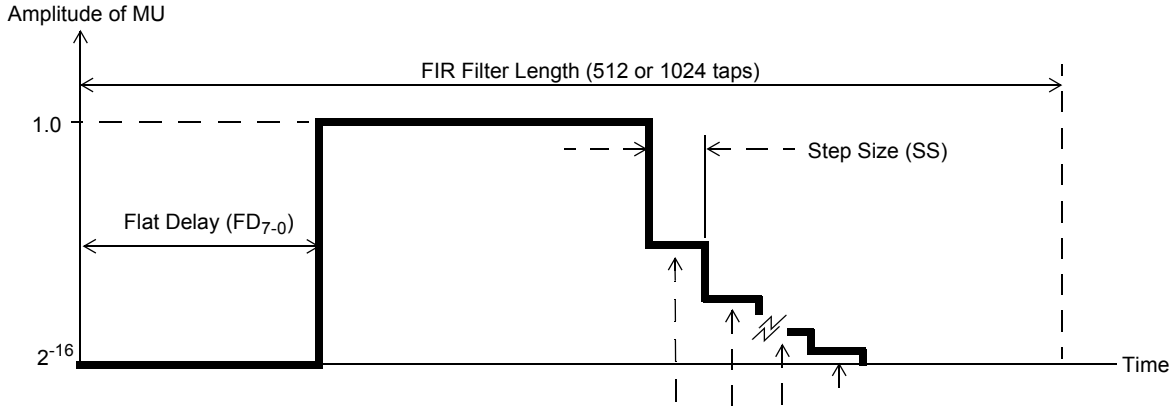
Echo Canceller A, Decay Step Size Control Register ADDRESS = 06h WRITE/READ VERIFY
Echo Canceller B, Decay Step Size Control Register ADDRESS = 26h WRITE/READ VERIFY

SSC

0	0	0	0	0	SSC_2	SSC_1	SSC_0
7	6	5	4	3	2	1	0

Power Reset Value 04h

Note: Bits marked with "0" are reserved bits and should be written "0".



The Exponential Decay registers (Decay Step Number and Decay Step Size) and Flat Delay register allow the LMS adaptation step-size (MU) to be programmed over the length of the FIR filter. A programmable MU profile allows the performance of the echo canceller to be optimized for specific applications. For example, if the characteristic of the echo response is known to have a flat delay of several milliseconds and a roughly exponential decay of the echo impulse response, then the MU profile can be programmed to approximate this expected impulse response thereby improving the convergence characteristics of the adaptive filter. Note that in the following register descriptions, one tap is equivalent to 125 μs (64 ms/512 taps).

FD_{7-0} **Flat Delay**: This register defines the flat delay of the MU profile, (i.e., where the MU value is 2^{-16}). The delay is defined as FD_{7-0} x 8 taps. For example; if FD_{7-0} = 5, then MU=2^{-16} for the first 40 taps of the echo canceller FIR filter. The valid range of FD_{7-0} is: 0 <= FD_{7-0} <= 64 in normal mode and 0 <= FD_{7-0} <= 128 in extended-delay mode. **The default value of FD_{7-0} is zero.**

SSC_{2-0} **Decay Step Size Control**: This register controls the step size (SS) to be used during the exponential decay of MU. The decay rate is defined as a decrease of MU by a factor of 2 every SS taps of the FIR filter, where **SS = 4 x$2^{SSC_{2-0}}$**. For example; If SSC_{2-0} = 4, then MU is reduced by a factor of 2 every 64 taps of the FIR filter. **The default value of SSC_{2-0} is 04h.**

NS_{7-0} **Decay Step Number**: This register defines the number of steps to be used for the decay of MU where each step has a period of SS taps (see SSC_{2-0}). The start of the exponential decay is defined as:
Filter Length (512 or 1024) - [Decay Step Number (NS_{7-0}) x Step Size (SS)] where **SS = 4 x$2^{SSC_{2-0}}$**.
For example, if NS_{7-0}=4 and SSC_{2-0}=4, then the exponential decay start value is **512 - [NS_{7-0} x SS] = 512 - [4 x (4x2^4)] = 256** taps for a filter length of 512 taps.

Echo Canceller A, Rin Peak Detect Register 2 ADDRESS = 0Dh READ
Echo Canceller B, Rin Peak Detect Register 2 ADDRESS = 2Dh READ

Power Reset Value
N/A

RP

RP_{15}	RP_{14}	RP_{13}	RP_{12}	RP_{11}	RP_{10}	RP_9	RP_8
7	6	5	4	3	2	1	0

Echo Canceller A, Rin Peak Detect Register 1 ADDRESS = 0Ch READ
Echo Canceller B, Rin Peak Detect Register 1 ADDRESS = 2Ch READ

Power Reset Value
N/A

RP

RP_7	RP_6	RP_5	RP_4	RP_3	RP_2	RP_1	RP_0
7	6	5	4	3	2	1	0

These peak detector registers allow the user to monitor the receive in signal (Rin) peak signal level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.

Echo Canceller A, Sin Peak Detect Register 2 ADDRESS = 0Fh READ
Echo Canceller B, Sin Peak Detect Register 2 ADDRESS = 2Fh READ

Power Reset Value
N/A

SP

SP_{15}	SP_{14}	SP_{13}	SP_{12}	SP_{11}	SP_{10}	SP_9	SP_8
7	6	5	4	3	2	1	0

Echo Canceller A, Sin Peak Detect Register 1 ADDRESS = 0Eh READ
Echo Canceller B, Sin Peak Detect Register 1 ADDRESS = 2Eh READ

Power Reset Value
N/A

SP

SP_7	SP_6	SP_5	SP_4	SP_3	SP_2	SP_1	SP_0
7	6	5	4	3	2	1	0

These peak detector registers allow the user to monitor the send in signal (Sin) peak signal level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.

Echo Canceller A, Error Peak Detect Register 2 ADDRESS = 11h READ
Echo Canceller B, Error Peak Detect Register 2 ADDRESS = 31h READ

Power Reset Value
N/A

EP

EP_{15}	EP_{14}	EP_{13}	EP_{12}	EP_{11}	EP_{10}	EP_9	EP_8
7	6	5	4	3	2	1	0

Echo Canceller A, Error Peak Detect Register 1 ADDRESS = 10h READ
Echo Canceller B, Error Peak Detect Register 1 ADDRESS = 30h READ

Power Reset Value
N/A

EP

EP_7	EP_6	EP_5	EP_4	EP_3	EP_2	EP_1	EP_0
7	6	5	4	3	2	1	0

These peak detector registers allow the user to monitor the error signal peak level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.

Echo Canceller A, Double-Talk Detection Threshold Register 2 ADDRESS = 15h WRITE/READ VERIFY
Echo Canceller B, Double-Talk Detection Threshold Register 2 ADDRESS = 35h WRITE/READ VERIFY

DTDT

$DTDT_{15}$	$DTDT_{14}$	$DTDT_{13}$	$DTDT_{12}$	$DTDT_{11}$	$DTDT_{10}$	$DTDT_{9}$	$DTDT_{8}$
7	6	5	4	3	2	1	0

Power Reset Value
48h

Echo Canceller A, Double-Talk Detection Threshold Register 1 ADDRESS = 14h WRITE/READ VERIFY
Echo Canceller B, Double-Talk Detection Threshold Register 1 ADDRESS = 34h WRITE/READ VERIFY

DTDT

$DTDT_{7}$	$DTDT_{6}$	$DTDT_{5}$	$DTDT_{4}$	$DTDT_{3}$	$DTDT_{2}$	$DTDT_{1}$	$DTDT_{0}$
7	6	5	4	3	2	1	0

Power Reset Value
00h

This register allows the user to program the level of Double-Talk Detection Threshold (DTDT). The 16 bit 2's complement linear value **defaults** to 4800h= 0.5625 or -5 dB. The maximum value is 7FFFh = 0.9999 or 0 dB. The high byte is in Register 2 and the low byte is in Register 1.

Echo Canceller A, Non-Linear Processor Threshold Register 2 ADDRESS = 19h WRITE/READ VERIFY
Echo Canceller B, Non-Linear Processor Threshold Register 2 ADDRESS = 39h WRITE/READ VERIFY

NLPTHR

NLP_{15}	NLP_{14}	NLP_{13}	NLP_{12}	NLP_{11}	NLP_{10}	NLP_{9}	NLP_{8}
7	6	5	4	3	2	1	0

Power Reset Value
08h

Echo Canceller A, Non-Linear Processor Threshold Register 1 ADDRESS = 18h WRITE/READ VERIFY
Echo Canceller B, Non-Linear Processor Threshold Register 1 ADDRESS = 38h WRITE/READ VERIFY

NLPTHR

NLP_{7}	NLP_{6}	NLP_{5}	NLP_{4}	NLP_{3}	NLP_{2}	NLP_{1}	NLP_{0}
7	6	5	4	3	2	1	0

Power Reset Value
00h

This register allows the user to program the level of the Non-Linear Processor Threshold (NLPTHR). The 16 bit 2's complement linear value **defaults** to 0800h = 0.0625 or -24.1 dB. The maximum value is 7FFFh = 0.9999 or 0 dB. The high byte is in Register 2 and the low byte is in Register 1.

Echo Canceller A, Adaptation Step Size (MU) Register 2 ADDRESS = 1Bh WRITE/READ VERIFY
Echo Canceller B, Adaptation Step Size (MU) Register 2 ADDRESS = 3Bh WRITE/READ VERIFY

MU

MU_{15}	MU_{14}	MU_{13}	MU_{12}	MU_{11}	MU_{10}	MU_{9}	MU_{8}
7	6	5	4	3	2	1	0

Power Reset Value
40h

Echo Canceller A, Adaptation Step Size (MU) Register 1 ADDRESS = 1Ah WRITE/READ VERIFY
Echo Canceller B, Adaptation Step Size (MU) Register 1 ADDRESS = 3Ah WRITE/READ VERIFY

MU

MU_{7}	MU_{6}	MU_{5}	MU_{4}	MU_{3}	MU_{2}	MU_{1}	MU_{0}
7	6	5	4	3	2	1	0

Power Reset Value
00h

This register allows the user to program the level of MU. MU is a 16 bit 2's complement value which defaults to 4000h = 1.0
The high byte is in Register 2 and the low byte is in Register 1.

Applications

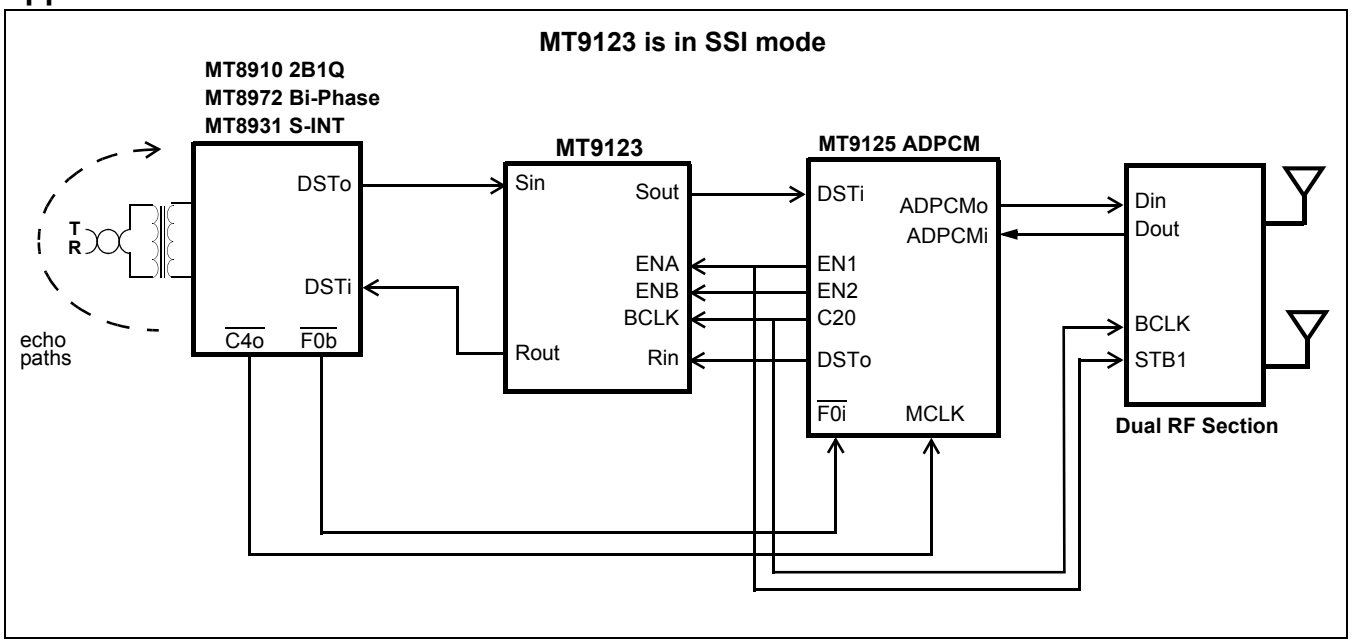


Figure 11 - (Basic Rate ISDN) Wireless Application Diagram

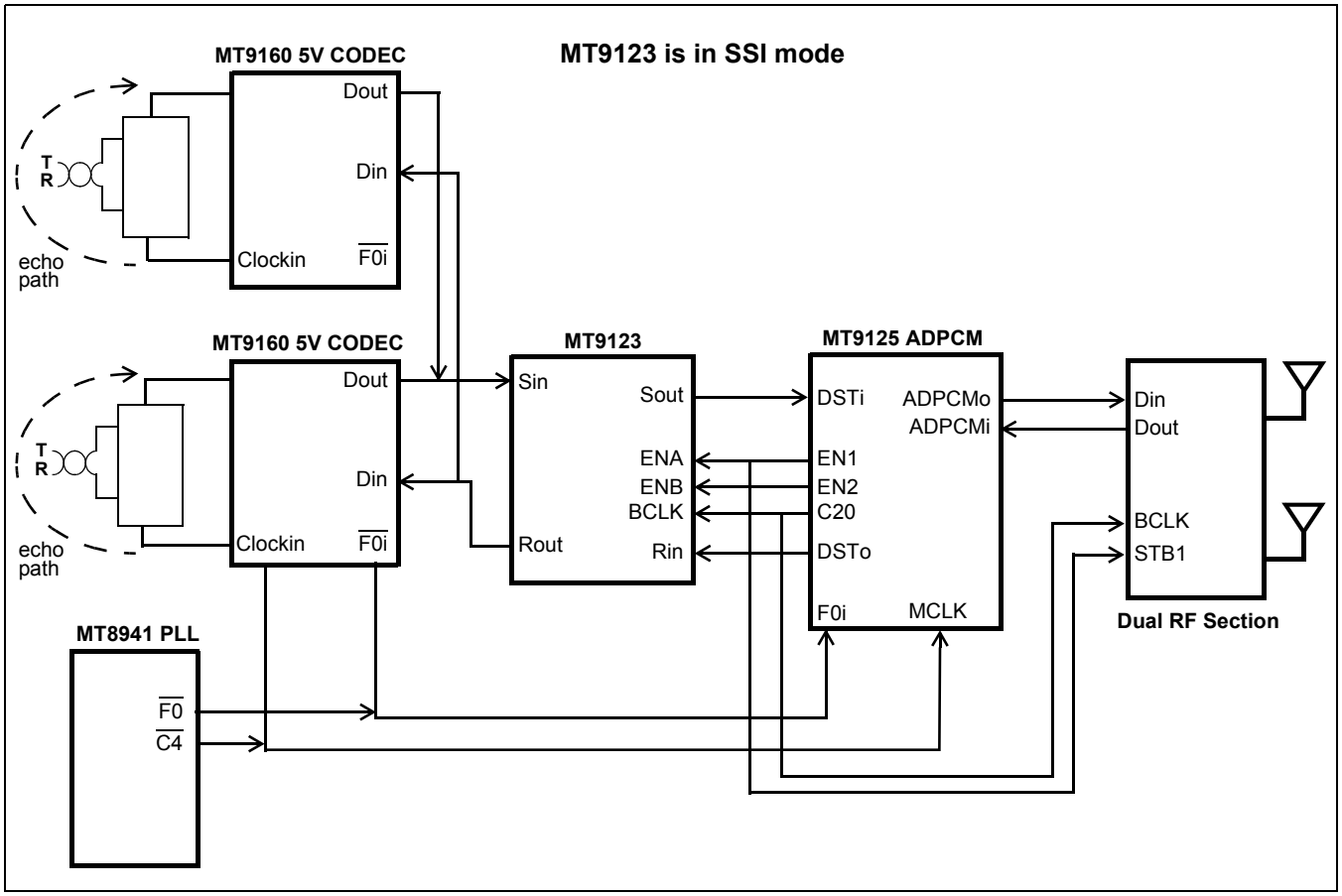


Figure 12 - (Analog Trunk) Wireless Application Diagram

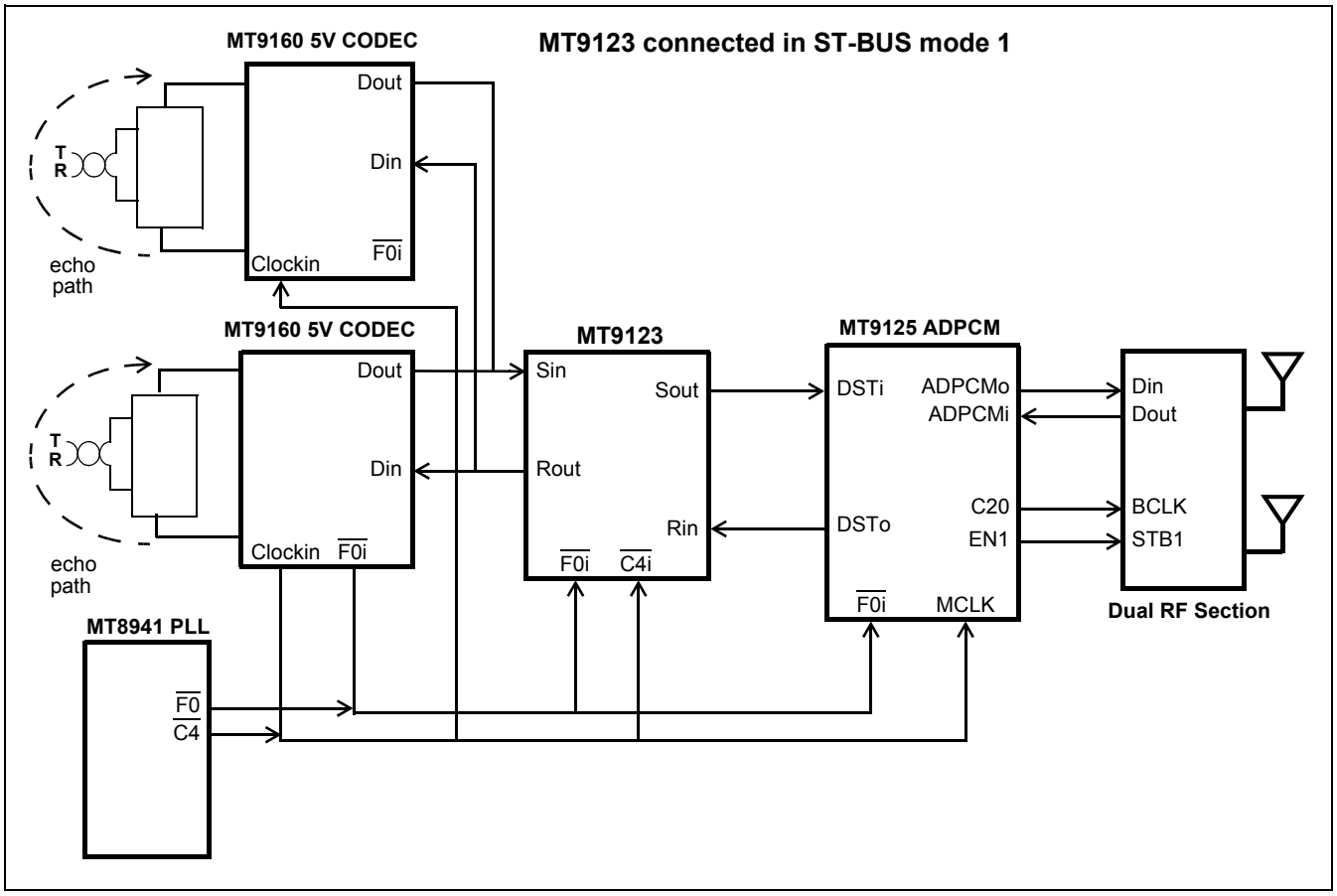


Figure 13 - (Analog Trunk) Wireless Application Diagram

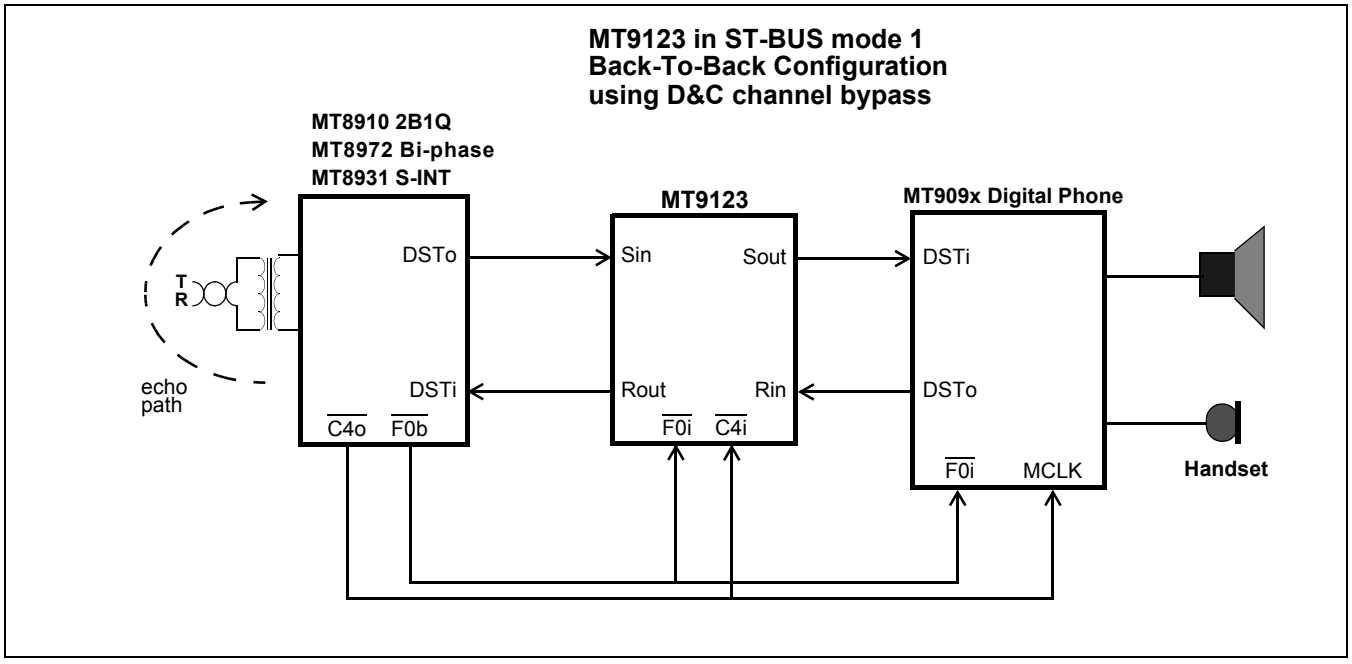


Figure 14 - (Basic Rate ISDN) Wired Telephone Application Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD}-V_{SS}	-0.3	7.0	V
2	Voltage on any digital pin	$V_{i/o}$	V_{SS}-0.3	V_{DD}+ 0.3	V
3	Continuous Current on any digital pin	$I_{i/o}$		±20	mA
4	Storage Temperature	T_{ST}	-65	150	°C
5	Package Power Dissipation	P_D		500	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
2	TTL Input High Voltage		2.4		V_{DD}	V	400mV noise margin
3	TTL Input Low Voltage		V_{SS}		0.4	V	400mV noise margin
4	CMOS Input High Voltage		4.5		V_{DD}	V	
5	CMOS Input Low Voltage		V_{SS}		0.5	V	
6	Operating Temperature	T_A	-40		+85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions/Notes
1	Supply Current	I_{CC} I_{DD}		 50	100	µA mA	$\overline{PWRDN}$ = 0 $\overline{PWRDN}$ = 1, clocks active
2	Input HIGH voltage (TTL)	V_{IH}	2.0			V	All except MCLK,Sin,Rin
3	Input LOW voltage (TTL)	V_{IL}			0.8	V	All except MCLK,Sin,Rin
4	Input HIGH voltage (CMOS)	V_{IHC}	3.5			V	MCLK,Sin,Rin
5	Input LOW voltage (CMOS)	V_{ILC}			1.5	V	MCLK,Sin,Rin
6	Input leakage current	I_{IH}/I_{IL}		0.1	10	µA	V_{IN}=V_{SS} to V_{DD}
7	High level output voltage	V_{OH}	0.9V_{DD}			V	I_{OH}=2.5mA
8	Low level output voltage	V_{OL}			0.1V_{DD}	V	I_{OL}=5.0mA
9	High impedance leakage	I_{OZ}		1	10	µA	V_{IN}=V_{SS} to V_{DD}
10	Output capacitance	C_o		10		pF	
11	Input capacitance	C_i		8		pF	
12	$\overline{PWRDN}$ Positive Threshold Voltage Hysteresis Negative Threshold Voltage	 V+ V_H V-	 3.75	 1.0	 1.25	 V V V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* DC Electrical Characteristics are over recommended temperature and supply voltage.

AC Electrical Characteristics† - Serial Data Interfaces (see Figures 16 and 17)
Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Max.	Units	Test Notes
1	MCLK Clock High	t_{MCH}	20		ns	
2	MCLK Clock Low	t_{MCL}	20		ns	
3	MCLK Frequency Dual Channel Single Channel	 f_{DCLK} f_{SCLK}	 19.15 9.58	 20.5	 MHz MHz	
4	BCLK/$\overline{C4i}$ Clock High	t_{BCH}, t_{C4H}	90		ns	
5	BCLK/$\overline{C4i}$ Clock Low	t_{BLL}, t_{C4L}	90		ns	
6	BCLK/$\overline{C4i}$ Period	t_{BCP}	240	7900	ns	
7	SSI Enable Strobe to Data Delay (first bit)	t_{SD}		80	ns	C_L=150pF
8	SSI Data Output Delay (excluding first bit)	t_{DD}		80	ns	C_L=150pF
9	SSI Output Active to High Impedance	t_{AHZ}		80	ns	C_L=150pF
10	SSI Enable Strobe Signal Setup	t_{SSS}	10	t_{BCP} -15	ns	
11	SSI Enable Strobe Signal Hold	t_{SSH}	15	t_{BCP} -10	ns	
12	SSI Data Input Setup	t_{DIS}	10		ns	
13	SSI Data Input Hold	t_{DIH}	15		ns	
14	$\overline{F0i}$ Setup	t_{F0iS}	20	150	ns	
15	$\overline{F0i}$ Hold	t_{F0iH}	20	150	ns	
16	ST-BUS Data Output delay	t_{DSD}		80	ns	C_L=150pF
17	ST-BUS Output Active to High Impedance	t_{ASHZ}		80	ns	C_L=150pF
18	ST-BUS Data Input Hold time	t_{DSH}	20		ns	
19	ST-BUS Data Input Setup time	t_{DSS}	20		ns	
20	$\overline{F0od}$ Delay	t_{DFD}		80	ns	C_L=150pF
21	$\overline{F0od}$ Pulse Width Low	t_{DFW}	200		ns	C_L=150pF

† Timing is over recommended temperature and power supply voltages.

AC Electrical Characteristics† - Microport Timing (see Figure 16)

	Characteristics	Sym.	Min.	Max.	Units	Test Notes
1	Input Data Setup	t_{IDS}	100		ns	
2	Input Data Hold	t_{IDH}	30		ns	
3	Output Data Delay	t_{ODD}		100	ns	C_L=150pF
4	Serial Clock Period	t_{SCP}	500		ns	
5	SCLK Pulse Width High	t_{SCH}	250		ns	
6	SCLK Pulse Width Low	t_{SCL}	250		ns	
7	$\overline{CS}$ Setup-Intel	t_{CSSI}	200		ns	
8	$\overline{CS}$ Setup-Motorola	t_{CSSM}	100		ns	
9	$\overline{CS}$ Hold	t_{CSH}	100		ns	
10	$\overline{CS}$ to Output High Impedance	t_{OHZ}		100	ns	C_L=150pF

† Timing is over recommended temperature range and recommended power supply voltages.

Characteristic	Symbol	TTL Pin	CMOS Pin	Units
TTL reference level	V_{TT}	1.5	-	V
CMOS reference level	V_{CT}	-	$0.5*V_{DD}$	V
Input HIGH level	V_H	2.4	$0.9*V_{DD}$	V
Input LOW level	V_L	0.4	$0.1*V_{DD}$	V
Rise/Fall HIGH measurement point	V_{HM}	2.0	$0.7*V_{DD}$	V
Rise/Fall LOW measurement point	V_{HL}	0.8	$0.3*V_{DD}$	V

Table 8 - Reference Level Definition for Timing Measurements

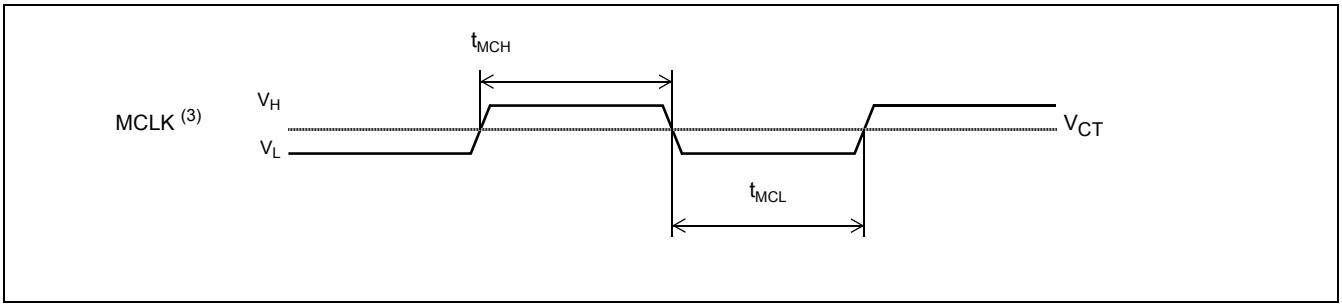


Figure 15 - Master Clock - MCLK

Notes: 1. CMOS output
2. TTL input compatible
3. CMOS input
(see Table 8 for symbol definitions)

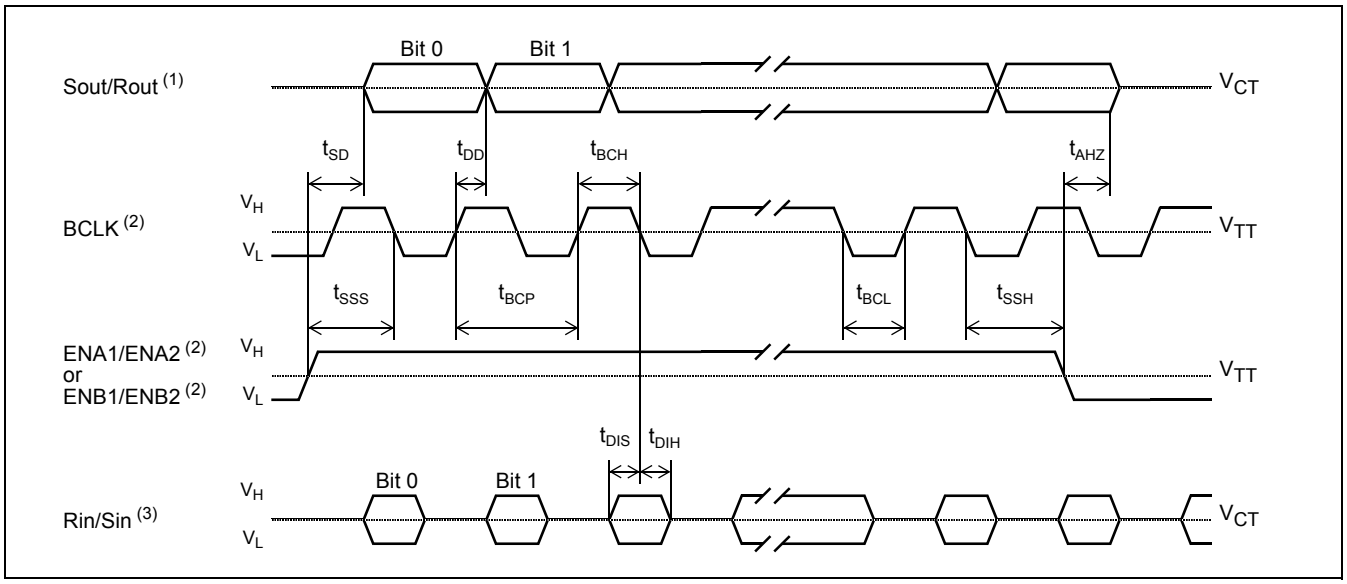


Figure 16 - SSI Data Port Timing

Notes: 1. CMOS output
2. TTL input compatible
3. CMOS input
(see Table 8 for symbol definitions)

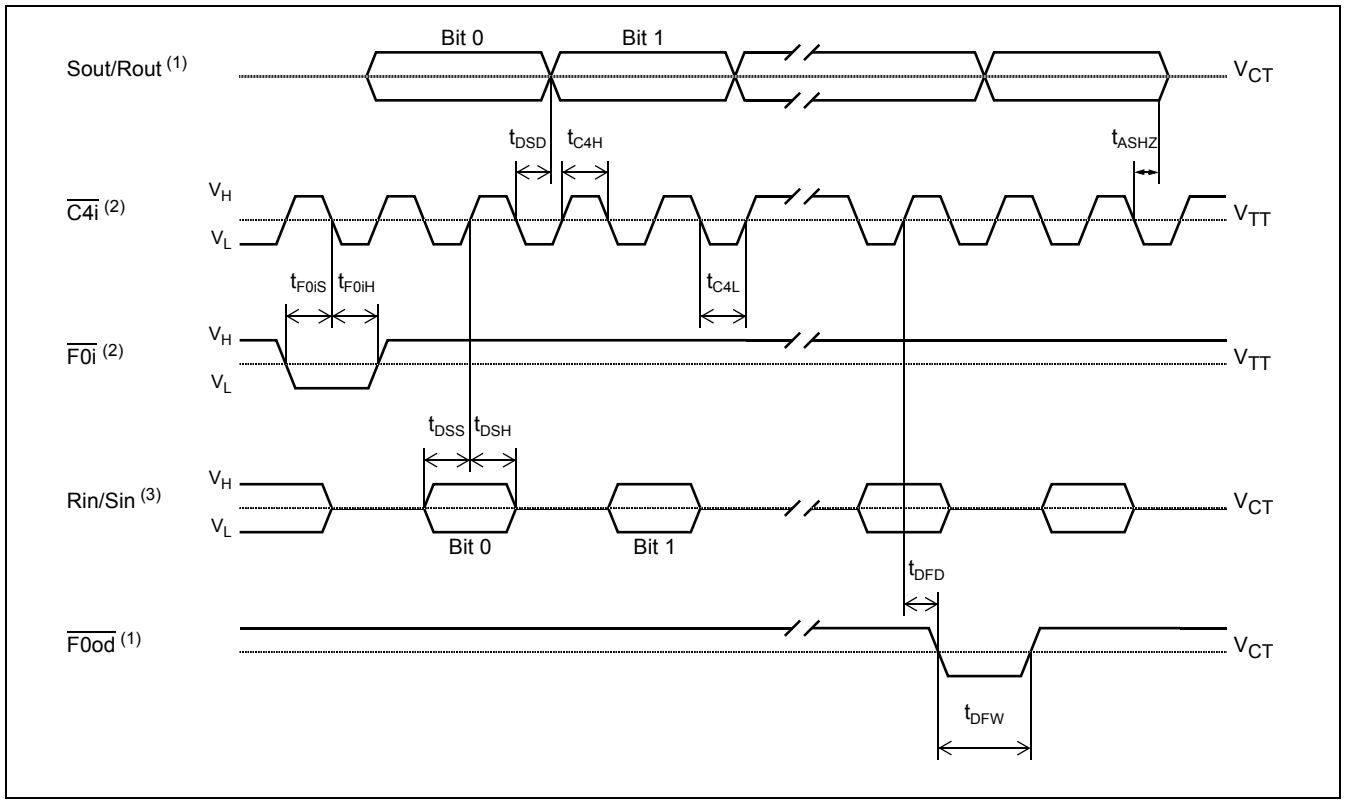


Figure 17 - ST-BUS Data Port Timing

Notes: 1. CMOS output
2. TTL input compatible
3. CMOS input
(see Table 8 for symbol definitions)

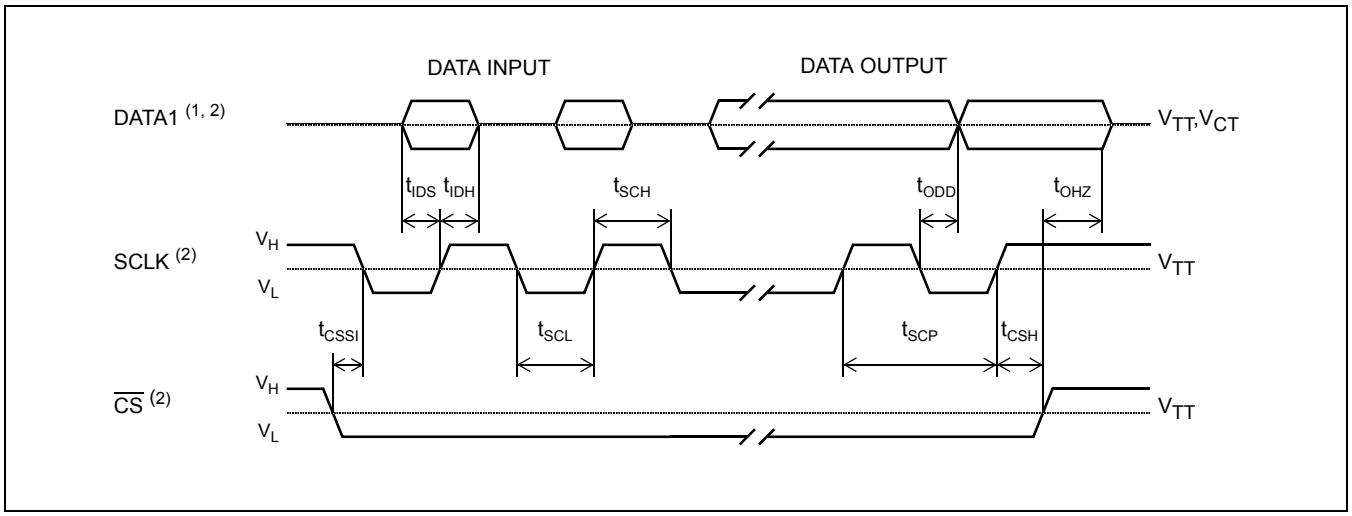


Figure 18 - INTEL Serial Microport Timing

Notes: 1. CMOS output
2. TTL input compatible
3. CMOS input
(see Table 8 for symbol definitions)

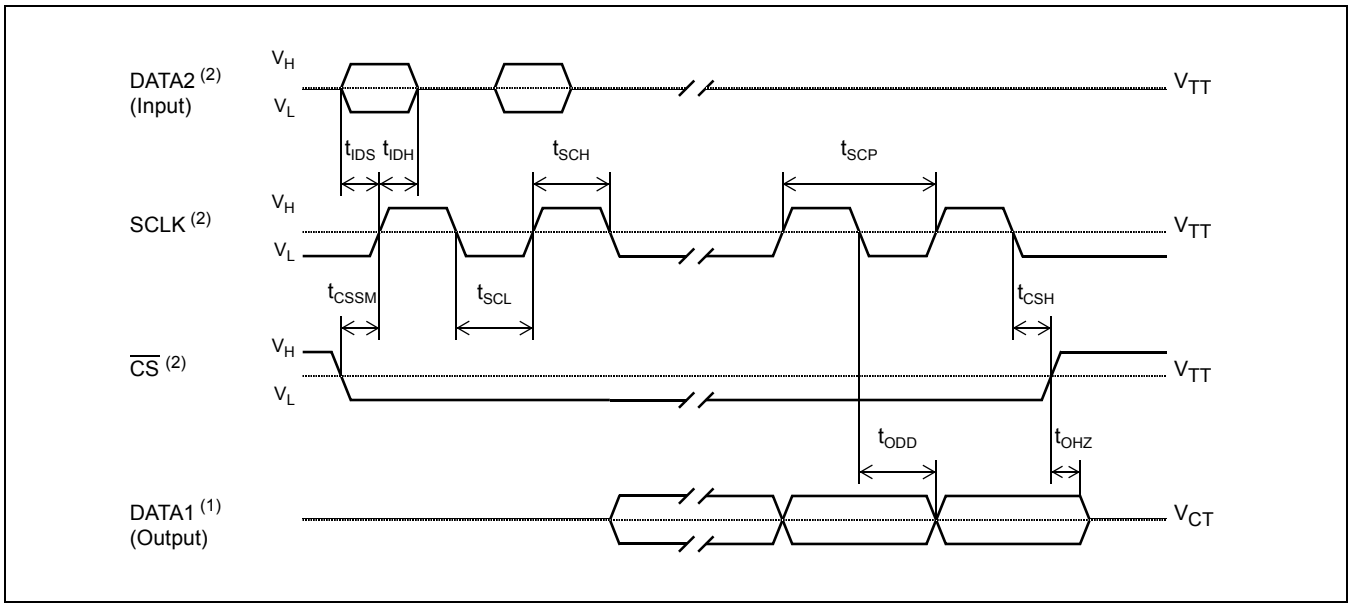
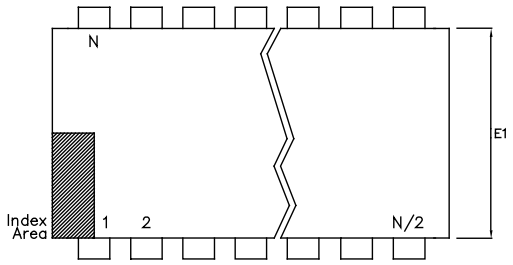
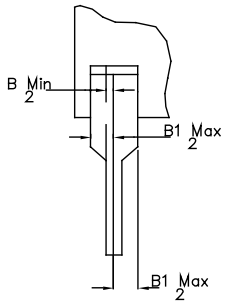
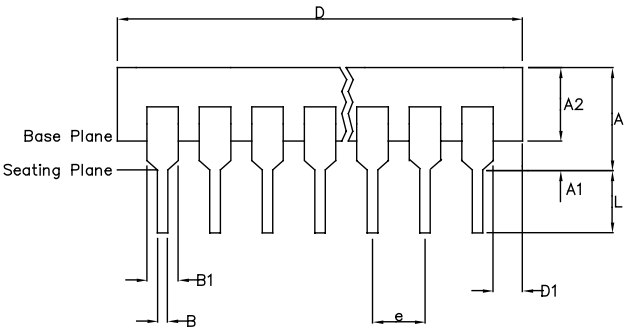


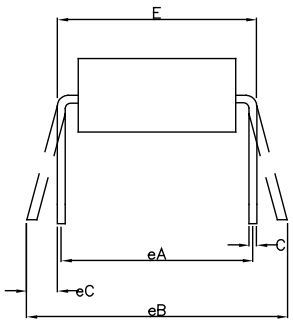
Figure 19 - MOTOROLA Serial Microport Timing

Notes: 1. CMOS output
2. TTL input compatible
3. CMOS input
(see Table 8 for symbol definitions)









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	35.05	39.75	1.380	1.565
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	28		28	
Conforms to Jedec MS-011AB ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	4
ACN	7010	203532	213102	CDCA
DATE	20Apr95	25Nov97	15Jul02	02Dec05
APPRD.				

ZARLINK SEMICONDUCTOR

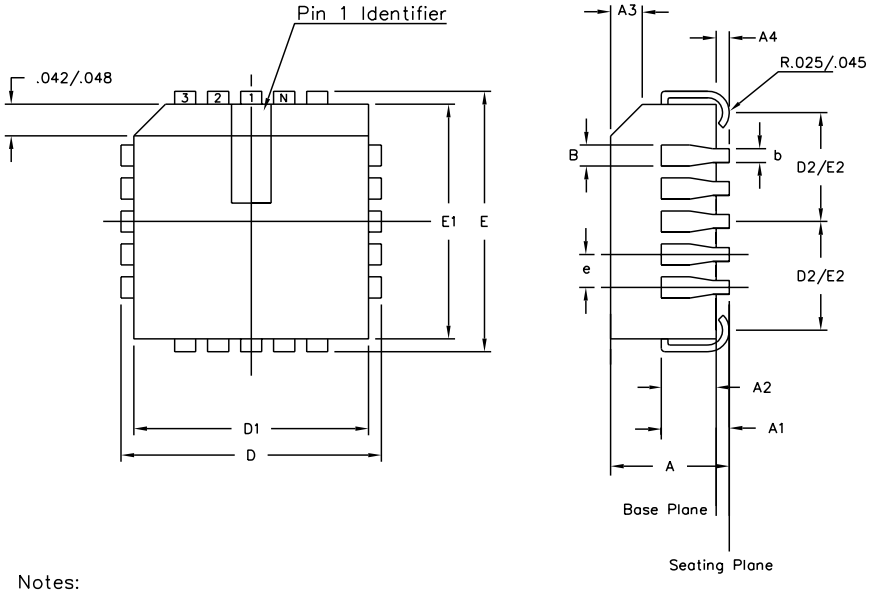
Previous package codes

DP / E

Package Code DA

Package Outline for 28 lead 600mils PDIP

GPD00072



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.43	11.58
D2	0.191	0.219	4.85	5.56
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.43	11.58
E2	0.191	0.219	4.85	5.56
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	7			
NE	7			
N	28			
Note	Square			
Conforms to JEDEC MS-018AB Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207469	212422	
DATE	15Aug94	10Sep99	22Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
HP / P

Package Code QA

Package Outline for 28 lead PLCC

GPD00002

For more information about all Zarlink products visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE