EP220 & EP224
Classic EPLDs

May 1995, ver. 1 Data Sheet

Features

- High-performance, low-power Erasable Programmable Logic Devices (EPLDs) with 8 macrocells
  - Combinatorial speeds as low as 7.5 ns
  - Counter frequencies of up to 100 MHz
  - Pipelined data rates of up to 115 MHz
  - Maximum 5.5-ns Clock-to-output time; minimum 4.5-ns setup time
- Replacement or upgrade for 16V8/20V8 PAL and GAL devices
- Up to 18 inputs (10 dedicated inputs) in EP220, 22 inputs (14 dedicated inputs) in EP224; up to 8 outputs in both EP220 and EP224
- Macrocells independently programmable for both registered and combinatorial logic
- Programmable inversion control supporting active-high or active-low outputs
- Low power consumption
  - Typical I_{CC} = 90 mA at 25 MHz (for -7A speed grades)
  - Quarter-power mode (I_{CC} = 40 mA)
  - Programmable zero-power mode with typical I_{CC} = 50 µA (for -10A and -12 speed grades)
- Programmable Security Bit for total protection of proprietary designs
- Low output skew for Clock driver applications
- 100% generically tested to provide 100% programming yield
- Software and programming support from Altera and a wide range of third-party tools
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages
  - 20-pin plastic J-lead package (PLCC)
  - 20-pin ceramic and plastic dual in-line packages (CerDIP and PDIP)
  - 24-pin PDIP
  - 28-pin PLCC

General Description

The EPROM-based EP220 and EP224 devices feature a flexible I/O architecture and implement 150 usable (300 available) gates of custom user logic functions. EP220 and EP224 devices can be used as upgrades for high-speed bipolar programmable logic devices (PLDs) or for 74-series LS and CMOS (SSI and MSI) logic devices in high-performance microcomputer systems.

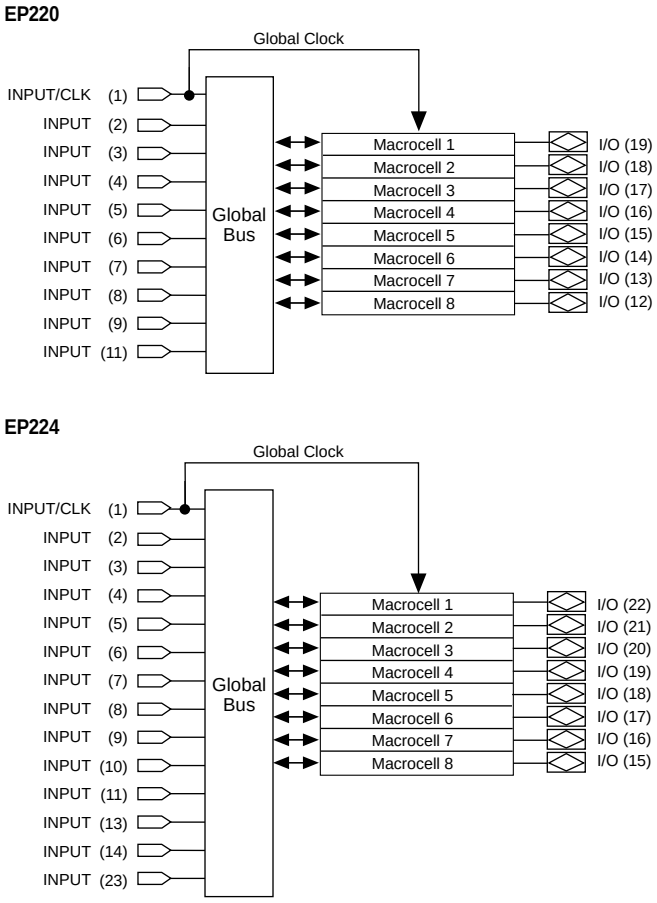
Compared to bipolar devices of equivalent speed, the EP220 and EP224 offer lower power consumption, faster input-to-non-registered-output delay (t_{PD}) in combinatorial mode, and higher counter frequencies in registered applications. This added performance supports faster state machine designs compared to bipolar devices, and provides additional timing margin for existing designs. The EP220 and EP224 are ideal for high-volume manufacturing of high-performance systems. These devices improve performance and decrease system noise, power consumption, and heat generation.

Functional Description

Figure 1 shows block diagrams of the EP220 and EP224 device architectures. The EP220 has 10 dedicated inputs and 8 I/O pins; the EP224 has 14 dedicated inputs and 8 I/O pins.

Figure 1. EP220 & EP224 Block Diagram

Numbers in parentheses refer to the pin-out number.



The EP220 and EP224 architecture is based on a sum-of-products, programmable-AND/fixed-OR structure. Each macrocell can be individually programmed for combinatorial or registered output. An inversion option allows each output to be configured for active-high or active-low operation. Each I/O pin can be programmed to function as an input, output, or bidirectional pin.

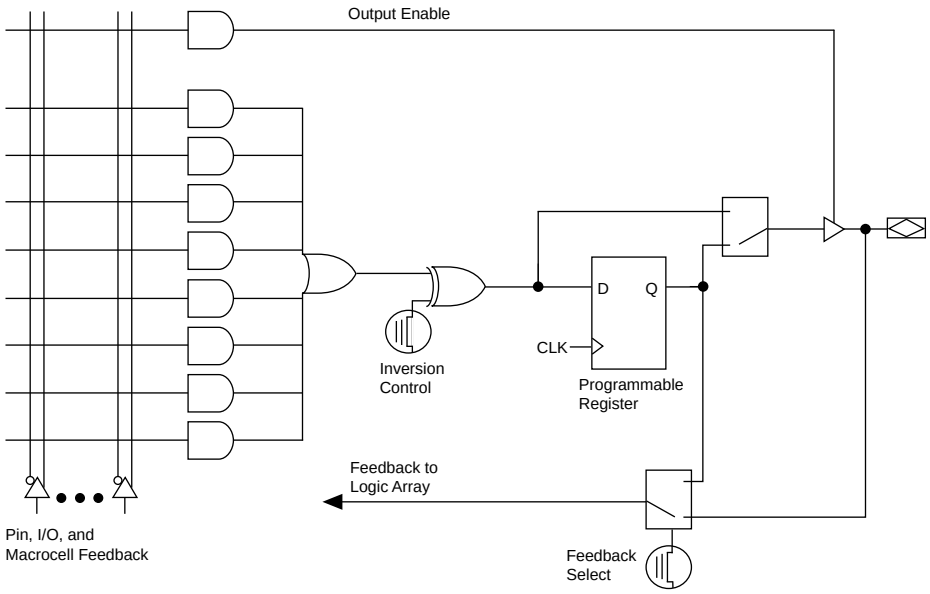
The EP220 and EP224 device architecture offers the following features:

- Macrocells
- High-frequency, low-skew global Clock

Macrocells

Each macrocell includes a product-term block with 8 AND product terms feeding an OR gate. One product term is dedicated to the Output Enable (OE) control of the tri-state buffer. The global logic array allows each product term to connect to the true or complement of each input—36 inputs for the EP220, 44 inputs for the EP224—and I/O feedback signal. See Figure 2.

Figure 2. EP220 & EP224 Macrocell



Macrocells can be individually configured for registered or combinatorial operation, providing a mixed-mode operation not available in fixed-architecture PAL devices. When registered output is selected, feedback from the register to the logic array bypasses the output buffer. When combinatorial output is selected, feedback comes from the I/O pin through the output buffer, and can be used for bidirectional I/O. Unlike PAL and GAL devices, all eight outputs on the EP220 and EP224 allow a combinatorial feedback signal from the I/O pin to feed the logic array. Data is clocked into the macrocell's D register on the rising edge of the global Clock.

The XOR gate can implement active-high or active-low logic, and can use DeMorgan's inversion to reduce the number of product terms needed to implement a function.

If the EP220 and EP224 register outputs do not require an OE signal, the internal product term can hold the output in an enabled state; if a global OE signal is required, any input can be dedicated to the task, and all eight product terms can be programmed accordingly.

High-Frequency, Low-Skew Global Clock

EP220 and EP224 devices have extremely low output-pin skew: registered output skew (t_{OCR}) is typically less than 300 ps; combinatorial output skew (t_{OSC}) is typically less than 400 ps. This low output-skew rate makes EP220 and EP224 devices ideal for high-frequency system Clock applications, including Intel Pentium microprocessors, 486-based PCs, and PCI bus designs.

PLD Compatibility

The EP220 and EP224 devices are a logical superset of most high-speed, 24-pin PAL/GAL devices. Industry-standard JEDEC Files from compatible devices can be programmed into EP220 or EP224 devices. Table 1 summarizes some of the devices that can be replaced or upgraded with EP220 and EP224 devices.

Table 1. EP220- and EP224-Compatible Devices (Part 1 of 4)

PAL/GAL Vendor	PAL/GAL Device	Altera Replacement Device	Speed Grade
Advanced Micro Devices	PAL16L8	EP220-7	-7
	PAL16R8		
	PALCE16V8		
	PAL20L8	EP224-7	
	PAL20R8		
	PALCE20V8		
	PAL16L8	EP220-10	-10
	PAL16R8		
	PALCE16V8		
	PAL20L8	EP224-10	
	PAL20R8		
	PALCE20V8		

Table 1. EP220- and EP224-Compatible Devices (Part 2 of 4)

PAL/GAL Vendor	PAL/GAL Device	Altera Replacement Device	Speed Grade
Advanced Micro Devices *(continued)*	PAL16L8D	EP220-10A	-10A
	PAL16R8D		
	PAL16R8-7		
	PALCE16V8		
	PAL20L8-10	EP224-10A	
	PAL20R8-10		
	PAL20R8-7		
	PALCE20V8		
	PAL16L8	EP220-12	-12
	PAL16R8		
	PALCE16V8		
	PAL20L8	EP224-12	
	PAL20R8		
	PALCE20V8		
Lattice Semiconductor Corp.	GAL16V8B	EP220-7	-7
	GAL20V8B	EP224-7	
	GAL16V8A	EP220-10	-10
	GAL16V8B		
	GAL20V8A	EP224-10	
	GAL20V8B		
National Semiconductor	PAL16L8	EP220-7	-7
	PAL16R8		
	PAL16L8	EP220-10	-10
	PAL16R8		
	GAL16V8A		
	PAL20L8	EP224-10	
	PAL20R8		
	GAL20V8A		
	PAL16L8D	EP220-10A	-10A
	PAL16R8D		
	GAL16V8A		
	PAL20L8D	EP224-10A	
	PAL20R8D		
	GAL20V8A		

Table 1. EP220- and EP224-Compatible Devices (Part 3 of 4)

PAL/GAL Vendor	PAL/GAL Device	Altera Replacement Device	Speed Grade
National Semiconductor *(continued)*	PAL16L8	EP220-12	-12
	PAL16R8		
	GAL16V8A		
	PAL20L8	EP224-12	
	PAL20R8		
	GAL20V8A		
Philips Semiconductor	PLUS16L8	EP220-7	-7
	PLUS16R8		
	PLUS20L8	EP224-7	
	PLUS20R8		
	PLUS16L8	EP220-10	-10
	PLUS16R8		
	PLUS20L8	EP224-10	
	PLUS20R8		
	PLUS16L8D	EP220-10A	-10A
	PLUS16R8D		
	PLUS16R8-7		
	PLUS20L8-10	EP224-10A	
	PLUS20R8-10		
	PLUS20R8-7		
	PLUS16L8	EP220-12	-12
	PLUS16R8		
	PLUS20L8	EP224-12	
	PLUS20R8-		
Texas Instruments, Inc.	TIBPAL16L8	EP220-7	-7
	TIBPAL20L8	EP224-7	
	TIBPAL16L8	EP220-10	-10
	TIBPAL20L8	EP224-10	
	TIBPAL16L8-10	EP220-10A	-10A
	TIBPAL16R8-10		
	TIBPAL16R8-7		
	TIBPAL20L8-10	EP224-10A	
	TIBPAL20R8-10		
	TIBPAL20R8-7		

Table 1. EP220- and EP224-Compatible Devices (Part 4 of 4)

PAL/GAL Vendor	PAL/GAL Device	Altera Replacement Device	Speed Grade
Texas Instruments, Inc. *(continued)*	TIBPAL16L8	EP220-12	-12
	TIBPAL16R6		
	TIBPAL16R8		
	TIBPAL20L8	EP224-12	
	TIBPAL20R6		
	TIBPAL20R8		

Power-On Characteristics

The EP220 and EP224 inputs and outputs respond a maximum of 1 µs after V_{CC} power-up (V_{CC} = 4.75 V), or after a power-loss/power-up sequence. All macrocells that are programmed as registers are set to a logic low on power-up.

Design Security

EP220 and EP224 devices contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is turned on, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when a device is erased.

Turbo Bit

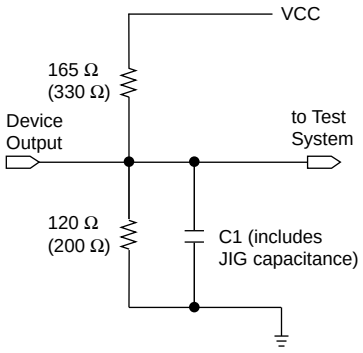
The -10A and -12 speed grades of the EP220 and EP224 devices contain a programmable Turbo Bit to control the automatic power-down feature that enables the low-standby-power mode (I_{CC}). When the Turbo Bit is turned on, the low-standby-power mode is disabled. All AC values are tested with the Turbo Bit turned on. When the device is operating with the Turbo Bit turned off (non-turbo mode), a non-turbo adder must be added to the appropriate AC parameter to determine worst-case timing. The non-turbo adder is specified in the "AC Operating Conditions" tables in this data sheet.

Generic Testing

EP220 and EP224 devices are fully functionally tested and guaranteed. Complete testing of each programmable EPROM configuration element and all internal logic elements ensures 100% programming yield. Figure 3 shows AC test conditions.

Figure 3. EP220 & EP224 AC Test Circuits

Power-supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test-system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for the EP224 device.



Test programs are used and then erased during the early stages of the device production flow. EPROM-based devices in one-time-programmable, windowless packages also contain on-board logic test circuitry to allow verification of function and AC specifications during the production flow.

Software & Programming Support

The EP220 is supported by the Altera MAX+PLUS II development software, Altera programming hardware, and third-party hardware. Both the EP220 and EP224 are supported by the Altera PLDshell Plus design software, third-party logic compilers (e.g., ABEL, CUPL, PLDesigner, LOG/IC, and iPLS II), and third-party programming hardware (e.g., Data I/O).

For more information on software support with PLDshell Plus, go to the ***PLDshell Plus/PLDasm User's Guide*** (available from the Altera Literature Department). For more information on MAX+PLUS II, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in the Altera ***1995 Data Book*** , or refer to MAX+PLUS II Help. Go to the *Programming Hardware Data Sheet* and the *Programming Hardware Manufacturers Data Sheet* in the Altera ***1995 Data Book*** for information on Altera and third-party programming hardware support.

Figure 4 shows the typical supply current (I_{CC}) versus frequency for EP220 and EP224 devices.

Figure 4. EP220 & EP224 I_{CC} vs. Frequency

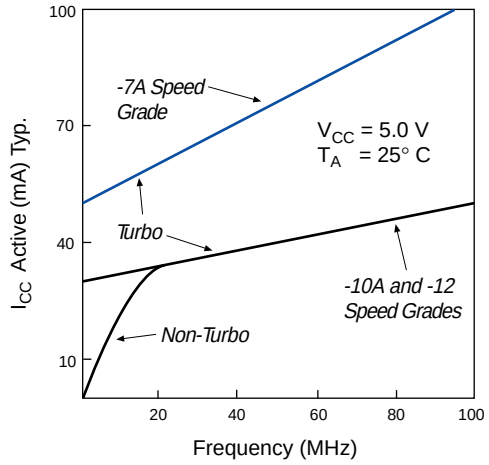
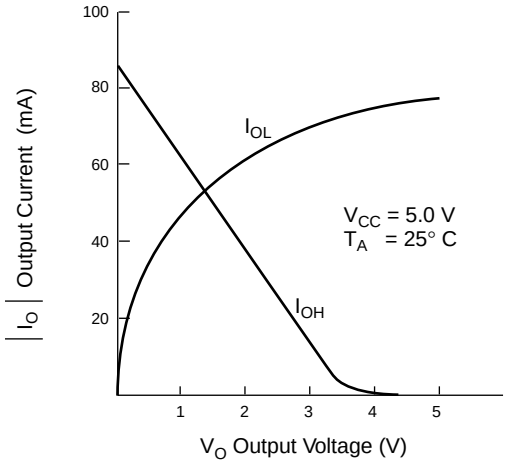


Figure 5 shows the output drive characteristics of EP220 and EP224 I/O pins.

Figure 5. EP220 & EP224 Output Drive Characteristics



Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (2)*	–2.0	7.0	V
V_I	DC input voltage	*Notes (2), (3)*	–0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature		–65	150	° C
T_{AMB}	Ambient temperature	*Note (4)*	–10	85	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	5.0-V operation	4.75	5.25	V
V_{IN}	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			500	ns
t_F	Input fall time			500	ns

DC Operating Conditions *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	*Note (6)*	2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	*Note (6)*	–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4.0 mA DC, V_{CC} = Min.	2.4		V
V_{OL}	Low-level output voltage	-7A, -7, -10: I_{OL} = 24 mA DC, V_{CC} = Min. -10A, -12: I_{OL} = 12 mA DC, V_{CC} = Min.		0.45	V
I_I	Input leakage current	V_{CC} = Max., GND < V_{IN} < V_{CC}	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_{CC} = Max., GND < V_{OUT} < V_{CC}	–10	10	µA
I_{SC}	Output short-circuit current	V_{CC} = Max., V_{OUT} = 0.5 V, *Note (7)*	–30	120	mA

Capacitance *Notes (5), (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		6	pF
C_{OUT}	I/O capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF
C_{CLK}	Clock pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF
C_{VPP}	V_{PP} pin capacitance	V_{PP} on pin 11 (EP220) and pin 13 (EP224), f = 1.0 MHz		10	pF

I_{CC} Supply Current: EP220-7A & EP224-7A *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
I_{CC3}	V_{CC} supply current	f_{IN} = 25 MHz, *Note (9)*		90	mA
		f_{IN} = 100 MHz, *Note (9)*		115	mA

I_{CC} Supply Current: EP220-10A, EP224-10A, EP220-12 & EP224-12 *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
I_{CC1}	V_{CC} supply current (non-turbo)	Standby mode, *Note (9)*		500	µA
I_{CC2}	V_{CC} supply current (non-turbo)	V_{CC} = Max., V_{IN} = V_{CC} or GND, no load, f_{IN} = 1 MHz, *Notes (9), (10)*		5	mA
I_{CC3}	V_{CC} supply current (turbo, active)	f_{IN} = 15 MHz, *Note (9)*		50	mA
		f_{IN} = 80 MHz, *Note (9)*		60	mA

I_{CC} Supply Current: EP220-7, EP224-7, EP220-10 & EP224-10 *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
I_{CC1}	V_{CC} supply current (standby)	f_{IN} = 25 MHz, *Note (9)*		90	µA
		f_{IN} = 74 MHz, *Note (9)*		105	mA
I_{CC3}	V_{CC} supply current (active)	f_{IN} = 25 MHz, *Note (9)*		115	mA
		f_{IN} = 74 MHz, *Note (9)*		135	mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in the Altera ***1995 Data Book***.
(2) Voltage with respect to ground.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(4) Under bias. Extended temperature versions are also available.
(5) Operating conditions: T_A = 0° C to 70° C, V_{CC} = 5.0 V ± 5% for commercial use.
T_A = –40° C to 85° C, V_{CC} = 5.0 V ± 10% for industrial use.
(6) Absolute values with respect to device GND; all over- and undershoots due to system or tester noise are included.
(7) For -7A, -10A, -12 speed grades for EP220 and EP224 devices: maximum DC I_{OL} (all 8 outputs) = 64 mA.
For -7, -10 speed grades for EP220 and EP224 devices: test 1 output at a time; test duration should not exceed 1 s.
(8) These values are measured during initial characterization. V_{CC} = Max., V_{IN} = V_{CC} or GND.
(9) Measured with a device programmed as an 8-bit counter.
(10) When the Turbo Bit is not set (non-turbo mode), an EP220 or EP224 device enters standby mode if no logic transitions occur for approximately 75 ns after the last transition.

AC Operating Conditions: -7A, -10A, & -12 Speed Grades *Note (1)*

Combinatorial Mode		EP220-7A EP224-7A		EP220-10A EP224-10A		EP220-12 EP224-12		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
t_{PD1}	Input to non-registered output, *Note (3)*		7.5		10		12	20	ns
t_{PD2}	I/O to non-registered output, *Note (3)*		7.5		10		12	20	ns
t_{PZX}	Input or I/O to output enable, *Note (4)*		9		12		12	20	ns
t_{PXZ}	Input or I/O to output disable, *Note (4)*		9		10		12	20	ns
t_{OSR}	Register-mode output to output skew		300		-		-	-	ps
t_{OSC}	Combinatorial-mode output to output skew		400		-		-	-	ps

Synchronous Clock Mode		EP220-7A EP224-7A		EP220-10A EP224-10A		EP220-12 EP224-12		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Units**
f_{MAX}	Maximum frequency (pipelined), no feedback, *Note (3)*	115		111		90.9		-	MHz
f_{CNT1}	Maximum counter frequency, external feedback, *Note (3)*	100		80		66		-	MHz
f_{CNT2}	Maximum counter frequency, internal feedback, *Note (3)*	115		100		83.3		-	MHz
t_{SU1}	Input or I/O setup time to global clock	4.5		7		9		20	ns
t_{H}	Input or I/O hold time from global clock	0		0		0		0	ns
t_{CO1}	Global clock to output delay, *Note (3)*		5.5		5.5		6	0	ns
t_{CO2}	Global clock to output delay through combinatorial macrocell		10		13		15	20	ns
t_{CNT}	Minimum global clock period, *Note (3)*		10		10		12	20	ns
t_{CL}	Clock low time	4		4		5		0	ns
t_{CH}	Clock high time	4		4		5		0	ns
t_{CP}	Clock period	10		9		11		0	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 5\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) If the device enters standby mode and remains inactive for approximately 75 ns, increase the time by the amount shown. For EP220-10A, EP220-12, and EP224-10A, EP224-12 devices only.

(3) Measured with all outputs switching.

(4) The t_{PZX} and t_{PXZ} parameters are measured at ± 0.5 V from steady-state voltage that is driven by the specified output load. The t_{PXZ} parameter is measured with $C_L = 5$ pF and with all eight outputs switching.

AC Operating Conditions: -7 & -10 Speed Grades *Note (1)*

Combinatorial Mode		EP220-7 EP224-7		EP220-10 EP224-10		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{PD1}	Input or I/O to non-registered output, inversion on, *Note (2)*		7.5		10	ns
t_{PD2}	Input or I/O to non-registered output, inversion off, *Note (2)*		8.5		10	ns
t_{PZX}	Input or I/O to output enable, *Note (3)*		9		10	ns
t_{PXZ}	Input or I/O to output disable, *Note (3)*		9		10	ns
t_{OSR}	Register mode output-to-output skew		300		300	ps
t_{OSC}	Combinatorial mode output-to-output skew		400		400	ps

Synchronous Clock Mode		EP220-7 EP224-7		EP220-10 EP224-10		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{MAX}	Maximum frequency (pipelined), no feedback, *Note (2)*	100		62.5		MHz
f_{CNT1}	Maximum counter frequency, external feedback, *Note (2)*	74		58.8		MHz
f_{CNT2}	Maximum counter frequency, internal feedback, *Note (2)*	100		60.6		MHz
t_{SU1}	Input or I/O setup time to global clock	7		10		ns
t_{H}	Input or I/O hold time from global clock	0		0		ns
t_{CO1}	Global clock to output delay, *Note (2)*		6.5		7	ns
t_{CO2}	Global clock to output delay through combinatorial macrocell		11		13	ns
t_{CNT}	Minimum global clock period, *Note (2)*		10		16.5	ns
t_{CL}	Clock low time	4		7		ns
t_{CH}	Clock high time	4		7		ns
t_{CP}	Clock period	10		16		ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.

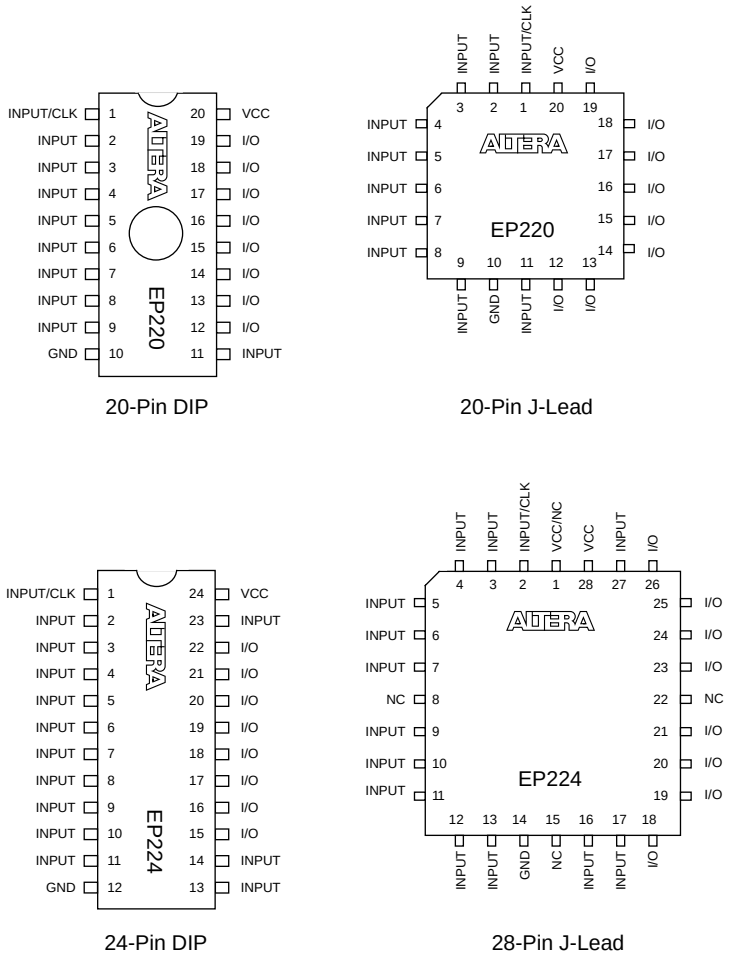
(2) Measured with three I/O outputs switching.

(3) The t_{PZX} and t_{PXZ} parameters are measured at ± 0.5 V from steady-state voltage that is driven by the specified output load. The t_{PXZ} parameter is measured with $C_L = 5$ pF and with all eight outputs switching.

Figure 6 shows the package pin-outs for EP220 and EP224 devices.

Figure 6. EP220 & EP224 Package Pin-Outs

Package outlines not drawn to scale. Windows in ceramic packages only.



Package Outlines

Refer to "Altera Device Package Outlines" in the Altera ***1995 Data Book*** for detailed information on package outlines.

Product Availability

Table 2 summarizes the availability of EP220 and EP224 devices. Altera will accept Intel ordering codes for Intel devices until June 30, 1995. After that date, only Altera ordering codes will be accepted.

Table 2. EP220 & EP224 Availability

Device	Temperature Grade	Speed Grade	Package	Altera Ordering Code	Intel Ordering Code
EP220	Commercial temperature (0° C to 70° C)	-10A	20-pin CerDIP	EP220DC-10A	D85C220-80
		-7	20-pin PDIP	EP220PC-7	P85C220-7
		-10	20-pin PDIP	EP220PC-10	P85C220-10
		-10A	20-pin PDIP	EP220PC-10A	P85C220-80
		-12	20-pin PDIP	EP220PC-12	P85C220-66
		-7A	20-pin PLCC	EP220LC-7A	N85C220-100
		-10A	20-pin PLCC	EP220LC-10A	N85C220-80
		-12	20-pin PLCC	EP220LC-12	N85C220-66
		-7	20-pin PLCC	EP220LC-7	N85C220-7
		-10	20-pin PLCC	EP220LC-10	N85C220-10
	Industrial temperature (–40° C to 85° C)	-12	20-pin PLCC	EP220LI-12	TN85C220-66
EP224	Commercial temperature (0° Cto 70° C)	-7	24-pin PDIP	EP224PC-7	P85C224-7
		-10	24-pin PDIP	EP224PC-10	P85C224-10
		-10A	24-pin PDIP	EP224PC-10A	P85C224-80
		-12	24-pin PDIP	EP224PC-12	P85C224-66
		-7A	28-pin PLCC	EP224LC-7A	N85C224-100
		-10A	28-pin PLCC	EP224LC-10A	N85C224-80
		-12	28-pin PLCC	EP224LC-12	N85C224-66
		-7	28-pin PLCC	EP224LC-7	N85C224-7
		-10	28-pin PLCC	EP224LC-10	N85C224-10

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