

100MHz DC-Restored Video Amplifier



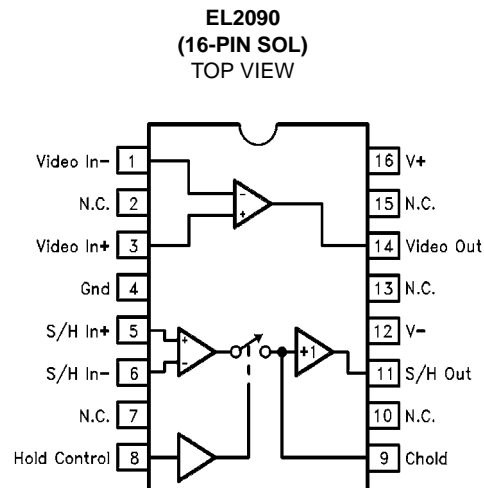
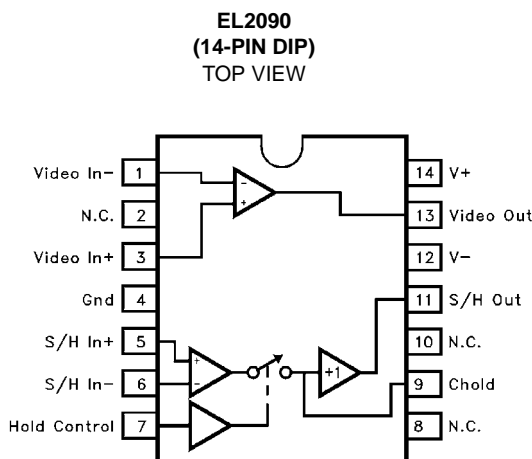
The EL2090 is the first complete DC-restored monolithic video amplifier sub-system. It contains a very high-quality video amplifier and a nulling sample-and-hold amplifier specifically designed to stabilize video performance. When the HOLD logic input is set to a logic 0 during a horizontal sync, the sample-and-hold amplifier may be used as a general-purpose op-amp to null the DC offset of the video amplifier. When the HOLD input goes to a logic 1 the sample-and-hold stores the correction voltage on the hold capacitor to maintain DC correction during the subsequent scan line.

The video amplifier is optimized for video characteristics, and performance at NTSC is nearly perfect. It is a current-feedback amplifier, so that -3dB bandwidth changes little at various closed-loop gains. The amplifier easily drives video signal levels into 75Ω loads. With 100MHz bandwidth, the EL2090 is also useful in HDTV applications.

The sample-and-hold is optimized for fast sync pulse response. The application circuit shown will restore the video DC level in five scan lines, even if the HOLD pulse is only 2μs long. The output impedance of the sample-and-hold is low and constant over frequency and load current so that the performance of the video amplifier is not compromised by connections to the DC restore circuitry.

The EL2090 is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL2090 is specified for operation over the 0°C to 75 °C temperature range.

Pinouts



Features

- Complete video level restoration system
- 0.01% differential gain and 0.02° differential phase accuracy at NTSC
- 100MHz bandwidth
- 0.1dB flatness to 20MHz
- Sample-and-hold has 15nA typical leakage and 1.5pC charge injection
- System can acquire DC correction level in 10μs, or 5 scan lines of 2μs each, to 1/2 IRE
- $V_S = \pm 5V$ to $\pm 15V$
- TTL/CMOS hold signal

Applications

- Input amplifier in video equipment
- Restoration amplifier in video mixers

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL2090CN	0°C to +75°C	14-Pin PDIP	MDP0031
EL2090CM	0°C to +75°C	16-Pin SOL	MDP0027

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Voltage between V+ and V-36V
 Voltage between V_{IN+} , S/H $_{IN+}$, S/H $_{IN-}$, C $_{HOLD}$,
 and GND pins (V+)+0.5V to (V-) -0.5V
 V_{OUT} Current 60mA

Current into V_{IN-} and HOLD Pins 5mA
 Current S/H $_{OUT}$ 16mA
 Internal Power Dissipation See Curves
 Operating Ambient Temperature Range 0°C to 75°C
 Operating Junction Temperature Plastic DIP or SOL 150°C
 Storage Temperature Range -65°C to $+15^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications $V_S = \pm 15\text{V}$; $R_L = 150\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise specified

PARAMETER	DESCRIPTION	TEMP	MIN	TYP	MAX	UNITS
I_S	Total Supply Current	Full		14	17	mA
VIDEO AMPLIFIER SECTION (NOT RESTORED)						
V_{OS}	Input Offset Voltage	Full		8	70	mV
I_{B+}	+ V_{IN} Input Bias Current	Full		2	15	μA
I_{B-}	- V_{IN} Input Bias Current	Full		30	150	μA
R_{OL}	Transimpedance	25°C		300		V/mA
A_{VOL}	Open-Loop Voltage Gain; $V_{OUT} = \pm 2\text{V}$	Full	56	65		dB
V_O	Output Voltage Swing	$V_S = \pm 15\text{V}$; $R_L = 2\text{k}\Omega$	Full	± 12	± 13	V
		$V_S = \pm 5\text{V}$; $R_L = 150\Omega$	Full	± 3.0	± 3.5	V
I_{SC}	Short-Circuit Current; + V_{IN} Set to $\pm 2\text{V}$; - V_{IN} to Ground through $1\text{k}\Omega$	25°C	± 50	± 90	± 160	mA
SAMPLE-AND-HOLD SECTION						
V_{OS}	Input Offset Voltage	Full		2	10	mV
I_B	Input Bias Current	Full		0.5	2.5	μA
I_{OS}	Input Offset Current	Full		0.05	0.5	μA
$R_{IN, DIFF}$	Input Differential Resistance	25°C		200		$\text{k}\Omega$
$R_{IN, COMM}$	Input Common-Mode Resistance	25°C		100		$\text{M}\Omega$
V_{CM}	Common-Mode Input Range	Full	± 11	± 12.5		V
SAMPLE-AND-HOLD SECTION						
A_{VOL}	Large Signal Voltage Gain	Full	15k	50k		V/V
CMRR	Common-Mode Rejection Ratio; $V_{CM} = \pm 11\text{V}$	Full	75	95		dB
PSRR	Power-Supply Rejection Ratio; $V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	Full	75	95		dB
V_{THRESH}	HOLD Pin Logic Threshold	Full	0.8	1.4	2.0	V
I_{DROOP}	Hold Mode Droop Current	Full		10	50	nA
I_{CHARGE}	Charge Current Available to Chold	Full	± 90	± 135		μA
V_O	Output Swing; $R_L = 2\text{k}$	Full	± 10	± 13		V
I_{SC}	Short-Circuit Current	25°C	± 10	± 17	± 40	mA

EL2090

Closed-Loop AC Electrical Specifications

$V_S = \pm 15V$; $C_L = 15pF$; $C_{STRAY} (-V_{IN}) = 2.5pF$; $R_F = R_G = 300\Omega$; $R_L = 150\Omega$;
 $C_{HOLD} = 100pF$; $T_A = 25^\circ C$

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
VIDEO AMPLIFIER SECTION					
SR	SlewRate; V_{OUT} from -2 to +2V		600		V/ μ s
BW	Bandwidth;	-3dB	75	100	MHz
		± 1 dB	35	60	MHz
		± 0.1 dB	10	20	MHz
dG (Peaking)	Differential Gain; V_{IN} from -0.7V to 0.7V; F = 3.58MHz		0.01		%
d θ (Peaking)	Differential Phase; V_{IN} from -0.7V to 0.7V; F = 3.58MHz		0.02		$^\circ$
SAMPLE-AND-HOLD SECTION					
BW	Gain-Bandwidth Product		1.3		MHz
Q	Sample to Hold Charge Injection (Note 1)		1.5	5	pC
T	Sample to Hold or Hold to Sample Delay Time		20		ns
T_s	Sample to Hold Settling Time to 2mV		200		ns

NOTE:

- The logic input is between 0V and 5V, with a 220 Ω resistor in series with the HOLD pin and 39pF capacitor from HOLD pin to ground.

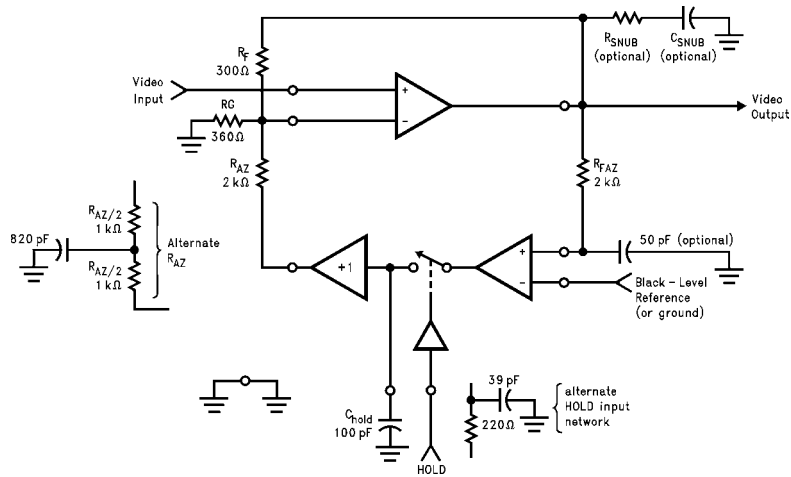
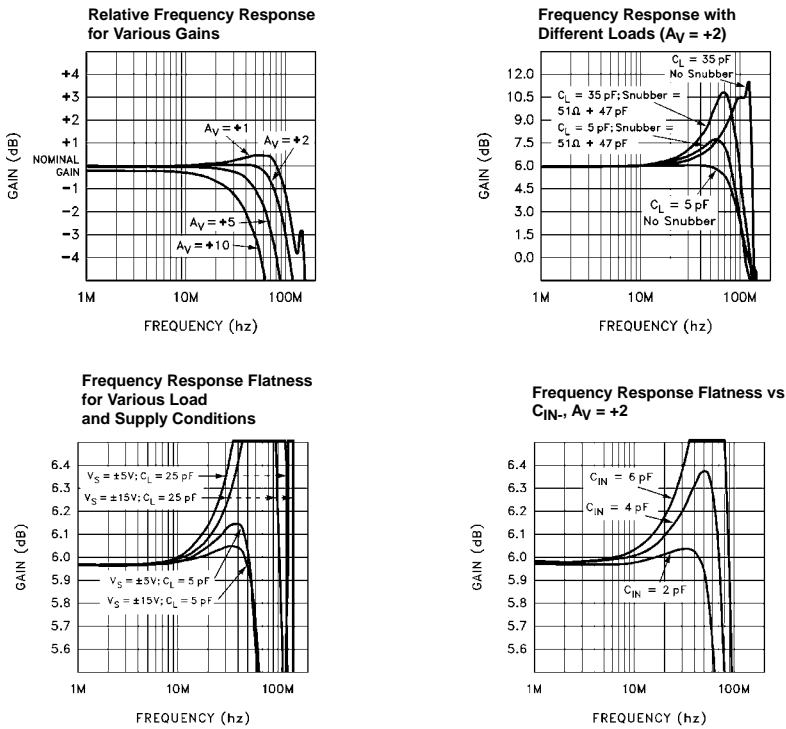
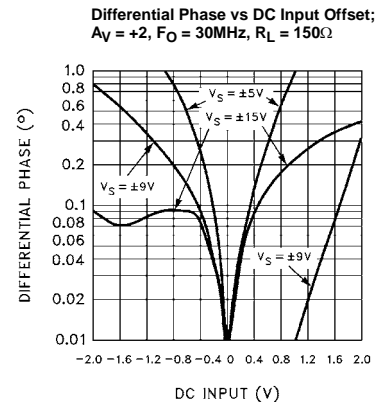
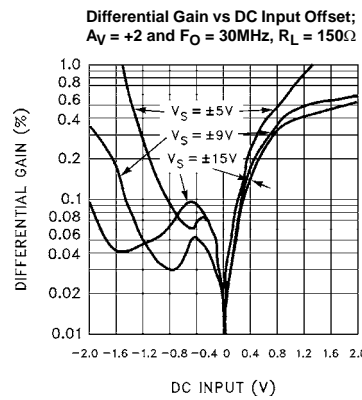
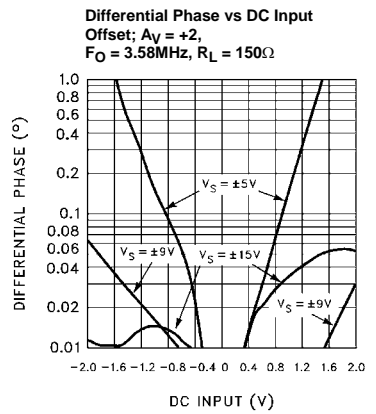
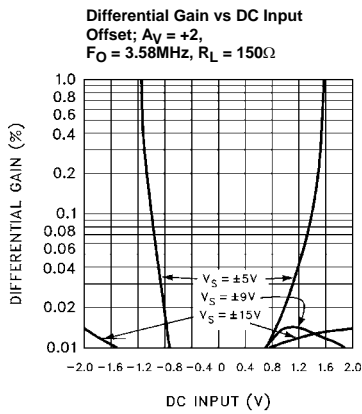
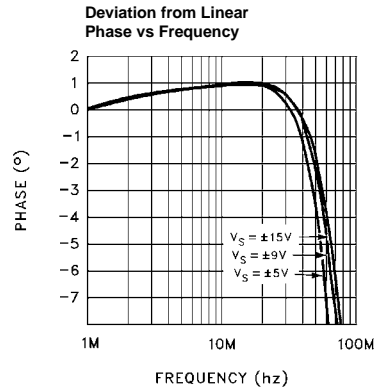
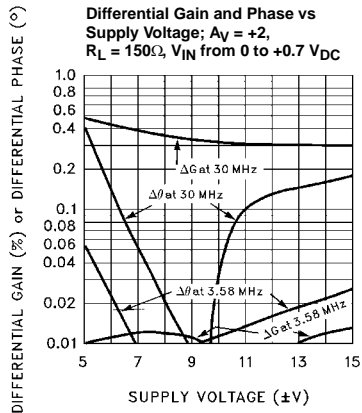


FIGURE 1. TYPICAL APPLICATION ($A_V = +2$)

Typical Performance Curves

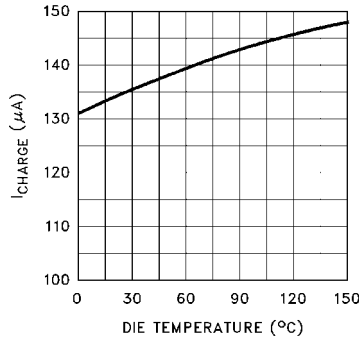


Typical Performance Curves (Continued)

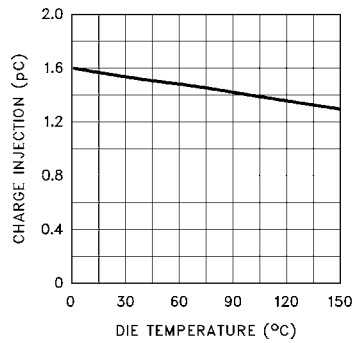


Typical Performance Curves (Continued)

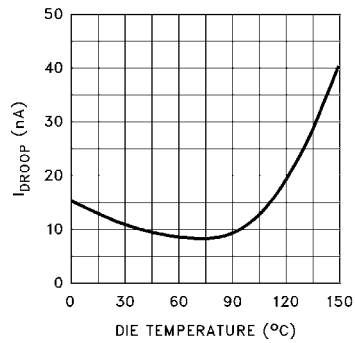
S/H Available Charge Current vs Temperature



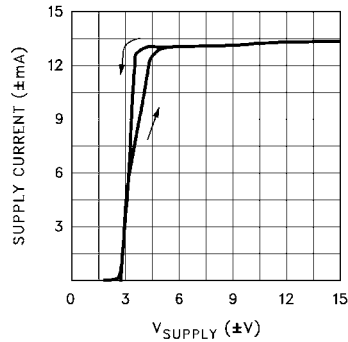
Sample-to-Hold Change Injection vs Temperature



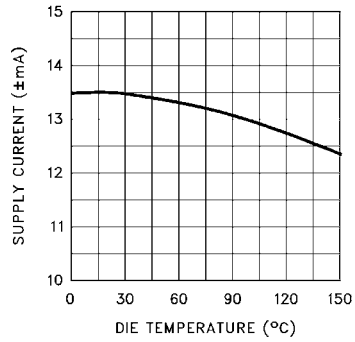
Typical Droop Current vs Temperature, V_S = ±15V



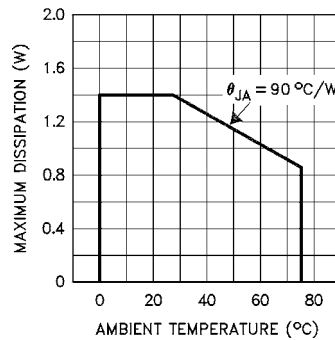
Supply Current vs Supply Voltage



Supply Current vs Temperature; V_S = ±15V



Maximum Power Dissipation vs Ambient Temperature— 14-Pin PDIP and 16-Pin SOL



Applications Information

The EL2090 is a general purpose component and thus the video amplifier and sample-and-hold pins are uncommitted. Therefore much of the ultimate performance as a DC-restored video amplifier will be set by external component values and parasitics. Some application considerations will be offered here.

The DC feedback from the sample-and-hold can be applied to either positive or negative inputs of the video amplifier (with appropriate phasing of the sample-and-hold amplifier inputs). We will consider feedback to the inverting video input. During a sample mode (the HOLD input at a logic low), the sample-and-hold acts as a simple nulling op-amp.

Ideally, the DC feedback resistor R_{az} is a high value so as not to couple a large amount of the AC signal on the video input back to the sample-and-hold amplifier output. The sample-and-hold output is a low impedance at high frequencies, but variations of the DC operating point will change the output impedance somewhat. No more than a few ohms output impedance change will occur, but this can cause gain variations in the 0.01% realm. This DC-dependent gain change is in fact a differential gain effect. Some small differential phase error will also be added. The best approach is to maximize the DC feedback resistor value so as to isolate the sample-and-hold from the video path as much as possible. Values of 1k Ω or above for R_{az} will cause little to no video degradation.

This suggests that the largest applicable power supply voltages be used so that the output swing of the sample-and-hold can still correct for the variations of DC offset in the video input with large values of R_{az} . The typical application circuit shown will allow correction of $\pm 1V$ inputs with good isolation of the sample-and-hold output. Good isolation is defined as no video degradation due to the insertion of the sample-and-hold loop. Lower supply voltages will require a smaller value of DC feedback resistor to retain correction of the full input DC variation. The EL2090 differential phase performance is optimum at $\pm 9V$ supplies, and differential gain only marginally improves above this voltage. Since all video characteristics mildly degrade with increasing die temperature, the $\pm 9V$ levels are somewhat better than $\pm 15V$ supplies. However, $\pm 15V$ supplies are quite usable.

Ultimate video performance, especially in HDTV applications, can also be optimized by setting the black-level reference such that the signal span at the video amplifier's output is set to its optimum range. For instance, setting the span to $\pm 1V$ of output is preferable to a span of 0V to +2V. The curves of differential gain and phase versus input DC offset will serve as guides.

The DC feedback resistor may be split so that a bypass capacitor is added to reduce the initially small sample-and-hold transients to even smaller levels. The corruption can be reduced to as low as 1mV peak seen at the video amplifier

output. The size of the capacitor should not be so large as to de-stabilize the sample-and-hold feedback loop, nor so small as to reduce the video amplifier's gain flatness. A resistor or some other video isolation network should be inserted between the video amplifier output and the sample-and-hold input to prevent excessive video from bleeding through the autozero section, as well as preventing spurious DC correction due to video signals confusing the sample-and-hold during autozero events. Figure 1 shows convenient component values. A full 3.58MHz trap is not necessary for suppressing NTSC chroma burst interaction with the sample-and-hold input; the simple R-C network suggested in Figure 1 suffices.

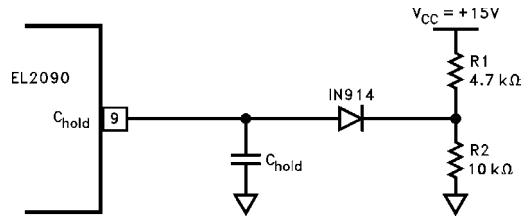
The HOLD input to the sample-and-hold has a 1.4V threshold and is clamped to a diode below ground and 6V above ground. The hold step characteristics are not sensitive to logic high nor low levels (within TTL or CMOS swings), but logic slewrates greater than 1000V/ μ s can couple noise and hold step into the sample-to-hold output waveforms. The logic slewrates should be greater than 50V/ μ s to avoid hold jitter. To avoid artificially high droop in hold mode, the Chold pin and Chold itself should be guarded with circuit board traces connected to the output of the sample-and-hold. Low-leakage hold capacitors should be used, such as mica or mylar, but not ceramic. The excellent properties of more expensive polystyrene, polypropylene, or teflon capacitors are not needed.

The user should be aware of a combination of conditions that may make the EL2090 operate incorrectly upon power-up. The fault condition can be described by noticing that the sample-and-hold output (pin 11) appears locked at a voltage close to V_{CC} . This voltage is maintained regardless of changes at the inputs to the sample-and-hold (pins 5 and 6) or to the HOLD control input (pin 7). Two conditions must occur to bring this about:

1. A large value of Chold_ usually values of 1000pF or more. This is not an unusual situation. Many users want to reduce the size of the hold step and increasing Chold is the most direct way to do this. Increasing Chold also reduces the slew rate of the sample and hold section but because of the limited size of the video signal, this is usually not a limitation.
2. A sampling interval (dictated by the HOLD pin) that is too small. By small, we mean less than 2 μ s.

For a sampling interval that is wide enough, there is enough time for the loop to close and for the amplifier to discharge whatever charge was dumped onto Chold it during the initial power spike and to then ramp up (or down) to the voltage that is proper for a balanced loop. When the sampling interval is too small, there is insufficient time for internal devices to recover from their initial saturated state from power-up because the feedback is not closed long enough. Therefore, typical recovery times for the loop are 2 μ s or greater. Summarizing, the two things that could prevent proper saturation recovery are (as mentioned above) too

large a capacitor which slows the charge and discharge rate of the stored voltage at Chold and too small a sampling interval in which the entire feedback loop is closed.



The circuit shown above prevents the fault condition from occurring by preventing the node from ever saturating. By clamping the value of Chold to some value lower than the supply voltage less a saturation voltage, we prevent this node from approaching the positive rail. The maximum voltage is set by the resistive voltage divider (between V+ and GND) R1 and R2 plus a diode. This value can be adjusted if the maximum size of the input signal is known. The diode used is an off-the-shelf 1N914 or 1N916.

As is true of all 100MHz amplifiers, good bypassing of the supplies to ground is mandatory. 1 μ F tantalums are sufficient, and 0.01 μ F leaded chip capacitors in parallel with medium value electrolytics are also good. Pins longer than 1/2 can induce a characteristic 150MHz resonance and ringing.

The V_{IN-} of the video amplifier should have the absolute minimum of parasitic capacitance. Stray capacitance of more than 3pF will cause peaking and compromise the gain flatness. The bandwidth of the amplifier is fundamentally set by the value of R_f . As demonstrated by the frequency response versus gain graph, the peaking and bandwidth is a weak function of gain. The EL2090 was designed for $R_f = 300\Omega$ giving optimum gain flatness at $A_v = +2$. Unity-gain response is flattest for $R_f = 360\Omega$; gains of +5 can use $R_f = 270\Omega$. In situations where the peaking is accentuated by load capacitance or -input capacitance the value of R_f will have to be increased, and some bandwidth will be sacrificed.

The V_{IN+} of the video amplifier should not look into an inductive source impedance. If the source is physically remote and a terminated input line is not provided, it may be necessary to connect an input "snubber" to ground. A snubber is a resistor in series with a capacitor which de-Q's the input resonance. Typical values are 100 Ω and 30pF.

The output of the video amplifier is sensitive to capacitive loads greater than 25pF, and a snubber to ground or a resistor in series with the output is useful to isolate reactive loads.

EL2090 Macromodel

* Revision A, October 1992

.param vclamp = {-0.002 * (TEMP-25)}

*

* Connections:

	Vidin+								
*		Vidin-							
*			+Vsupply						
*				-Vsupply					
*					Vid Out				
*						S/H In+			
*							S/H In-		
*								S/H Out	
*									Hold Control
*									Chold
*									

.subckt EL2090/EL 3 1 14 12 13 5 6 11 7 9

*

***** Video Amplifier *****

*

e1 20 0 3 0 1.0

vis 20 34 0V

h2 34 38 vxx 1.0

r10 1 36 25

l1 36 38 20nH

iinp 3 0 10µA

iinm 1 0 5µA

h1 21 0 vis 600

r2 21 22 1K

d1 22 0 dclamp

d2 0 22 dclamp

e2 23 0 22 0 0.00166666666

l5 23 24 0.7µH

c5 24 0 0.5pF

r5 24 0 600

g1 0 25 24 0 1.0

rol 25 0 400K

cdp 25 0 7.7pF

q1 12 25 26 qp

q2 14 25 27 qn

q3 14 26 28 qn

q4 12 27 29 qp

r7 28 13 4

r8 29 13 4

ios1 14 26 2.5mA

ios2 27 12 2.5mA

ips 14 12 7.2mA

ivos 0 33 5mA

vxx 33 0 0V

r11 33 0 1K

*

***** Sample & Hold *****

*

g40 49 0 5 6 1e-3

vcur 49 42 0v

r43 6 0 100Meg

r44 5 0 100Meg

r40 42 0 4K

d41 50 42 diode

d42 42 51 diode

v41 50 0 {vclamp}

EL2090 Macromodel (Continued)

```
v42 0 51 {vclamp}
g41 44 0 42 0 200e-6
r42 44 0 31Meg
d45 9 14 diode
d46 12 9 diode
s1 44 9 48 0 swa
e40 46 0 9 0 0.95
i40 0 9 10nA
r45 46 47 70
l40 47 11 70nH
c40 7 9 0.32pF
r47 7 48 10K
c41 48 0 3pF
*
* Models
*
.model qn npn(is=5e-15 bf=500 tf=0.1nS)
.model qp pnp(is=5e-15 bf=500 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.02 bv=2.75 n=4)
.model diode d
.model swa vswitch(von=1.2v voff=1.6v roff=1e12 ron=100)
.ends
```

EL2090 Macromodel (Continued)

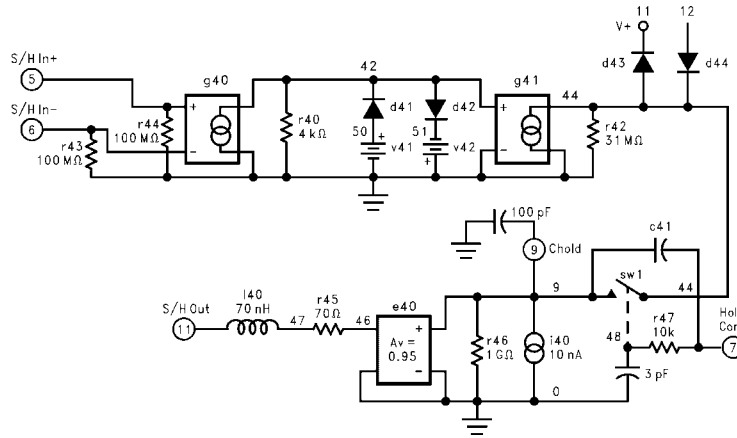


FIGURE 2. SAMPLE AND HOLD AMPLIFIER

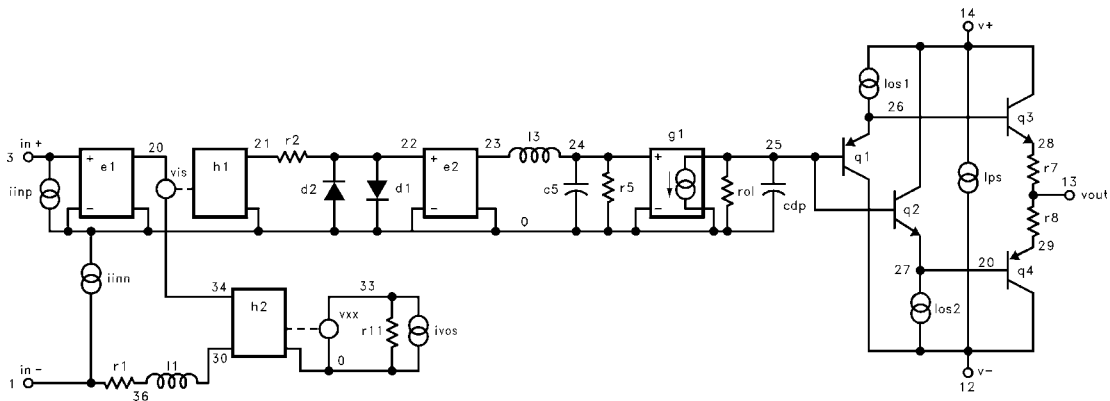


FIGURE 3. VIDEO AMPLIFIER

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com