82503
DUAL SERIAL TRANSCEIVER (DST)

82503 PRODUCT FEATURE SET OVERVIEW

- **Single Component Ethernet* Interface to Both 802.3 10BASE-T and AUI**
- **Automatic or Manual Port Selection**
- **Manchester Encoder/Decoder and Clock Recovery**
- **No Glue Interface to Industry-Standard LAN Controllers**
  - **— Intel 82586, 82590, 82593 and 82596**
  - **— AMD 7990 (LANCE*)**
  - **— National Semiconductor 8390 and 83932 (SONIC*)**
  - **— Western Digital 83C690**
  - **— Fujitsu 86950 (Etherstar*)**
- **Diagnostic Loopback**
- **Reset, Low Power Modes**
- **Network Status Indicators**
- **Defeatable Jabber Timer**
- **User Test Modes**
- **10 MHz Transmit Clock Generator**
- **One Micron CHMOS** IV (Px48) Technology**
- **Single 5-V Supply**

INTERFACE FEATURES

TPE

- **Complies with 10BASE-T, IEEE Std. 802.3i-1990 for Twisted Pair Ethernet**
- **Selectable Polarity Switching**
- **Direct Interface to TPE Analog Filters**
- **On-Chip TPE Squelch**
- **Defeatable Link Integrity (LI)**
- **Support of Cable Lengths $>$100m**

AUI

- **Complies with IEEE 802.3 AUI Standard**
- **Direct Interface to AUI Transformers**
- **On-Chip AUI Squelch**

A block diagram of a typical application is shown in Figure 1. The 82503 Dual Serial Transceiver is a high-integration CMOS device designed to simplify interfacing industry standard Ethernet LAN Controllers to IEEE 802.3 local area network applications (10BASE5, 10BASE2, and 10BASE-T). The component supports both an attachment unit interface (AUI) and a Twisted Pair Ethernet interface (TPE). It allows OEMs to design a state-of-the-art media interface that is jumperless and fully automatic. The 82503 includes on-chip AUI and TPE drivers and receivers; it offers designers a cost-effective, integrated solution for interfacing LAN controllers to the wire medium.

**CHMOS is a patented process of Intel Corporation.
*Ethernet is a registered trademark of Xerox Corporation.
LANCE is a registered trademark of Advanced Micro Devices.
Etherstar is a registered trademark of Fujitsu Electronics.
Sonic is a registered trademark of National Semiconductor Corporation.

October 1995 **Order Number: 290421-004**

82503 Dual Serial Transceiver (DST)

CONTENTS

CONTENTS

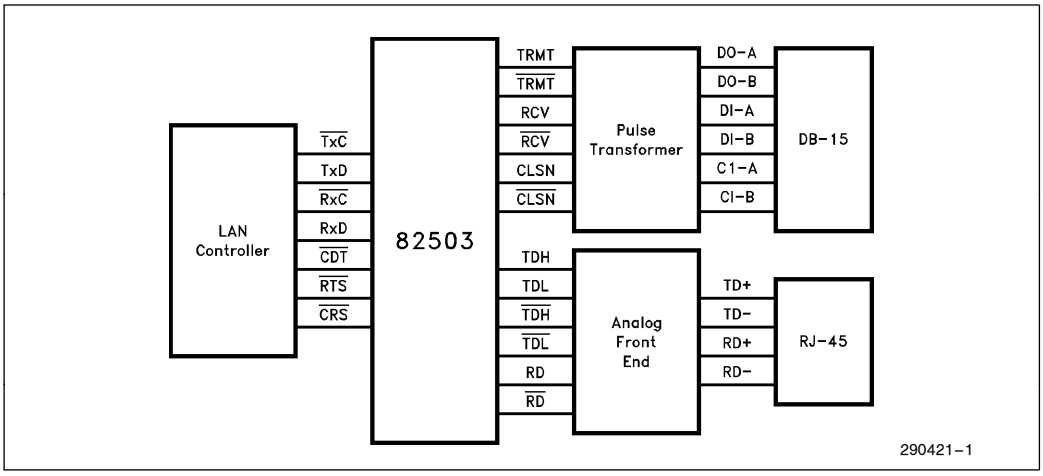

Figure 1. Application Block Diagram

1.0 82503 PRODUCT FEATURES

The 82503 incorporates all the active circuitry required to interface Ethernet controllers to 10BASE-T networks or the attachment unit interface (AUI). It supports a direct no-glue interface to Intel's family of high-performance LAN controllers (82586, 82590, 82593, and 82596). The 82503 also provides a direct no-glue interface to the National Semiconductor 8390 and 83932 (SONIC), the Western Digital 83C690, the Advanced Micro Devices 7990 (LANCE) and 79C900 (ILACC), and the Fujitsu 86950 (Etherstar) controllers.

This component includes three advanced features: jumperless two-port design capability, automatic port selection, and polarity switching. The jumperless TPE or AUI port selection capability allows designers maximum ease-of-use and network flexibility. Automatic port selection ensures complete software compatibility with existing 10BASE2 and 10BASE5 software drivers. The 82503's polarity switching feature will detect and correct polarity errors on the twisted pair—the most common wiring fault in twisted pair networks.

The 82503 contains all the circuitry needed to meet the 10BASE-T specification, including link integrity, a jabber timer and internal predistortion. Deselecting link integrity allows the component to be used in some prestandard networks. The 82503's jabber timer prevents the station from continuously transmitting and is defeatable for simple design characterization. The predistortion circuitry eliminates line overcharge and reduces jitter on 10BASE-T links.

The 82503 can also support twisted pair cable lengths of up to 200m when placed in TPE Extended Squelch Mode (XSQ).

This component incorporates six LED drivers to display transmit data, receive data, collision, link integrity, polarity faults and port selections, allowing for complete network monitoring by the user. The transmit, receive and collision LEDs indicate the rate of activity by the frequency of flashing. The 82503 also has a low power mode. During low power, many of the 82503's pins are in a high-impedance state to facilitate board-level testing.

The 82503's diagnostic loopback control enables it to route a transmission signal from the LAN controller through its Manchester encoder-decoder circuitry and back to the LAN controller. This provides effective network node fault detection and isolation capabilities. In addition, the 82503 supports diagnostic test modes that generate continuous tranmission of data through the twisted pair port, allowing designers to measure the analog performance of their design.

The 82503 is available in 44-lead PLCC and 44-lead QFP packages and is fabricated with Intel's low-power, high-speed, CHMOS IV technology using a single 5-V supply.

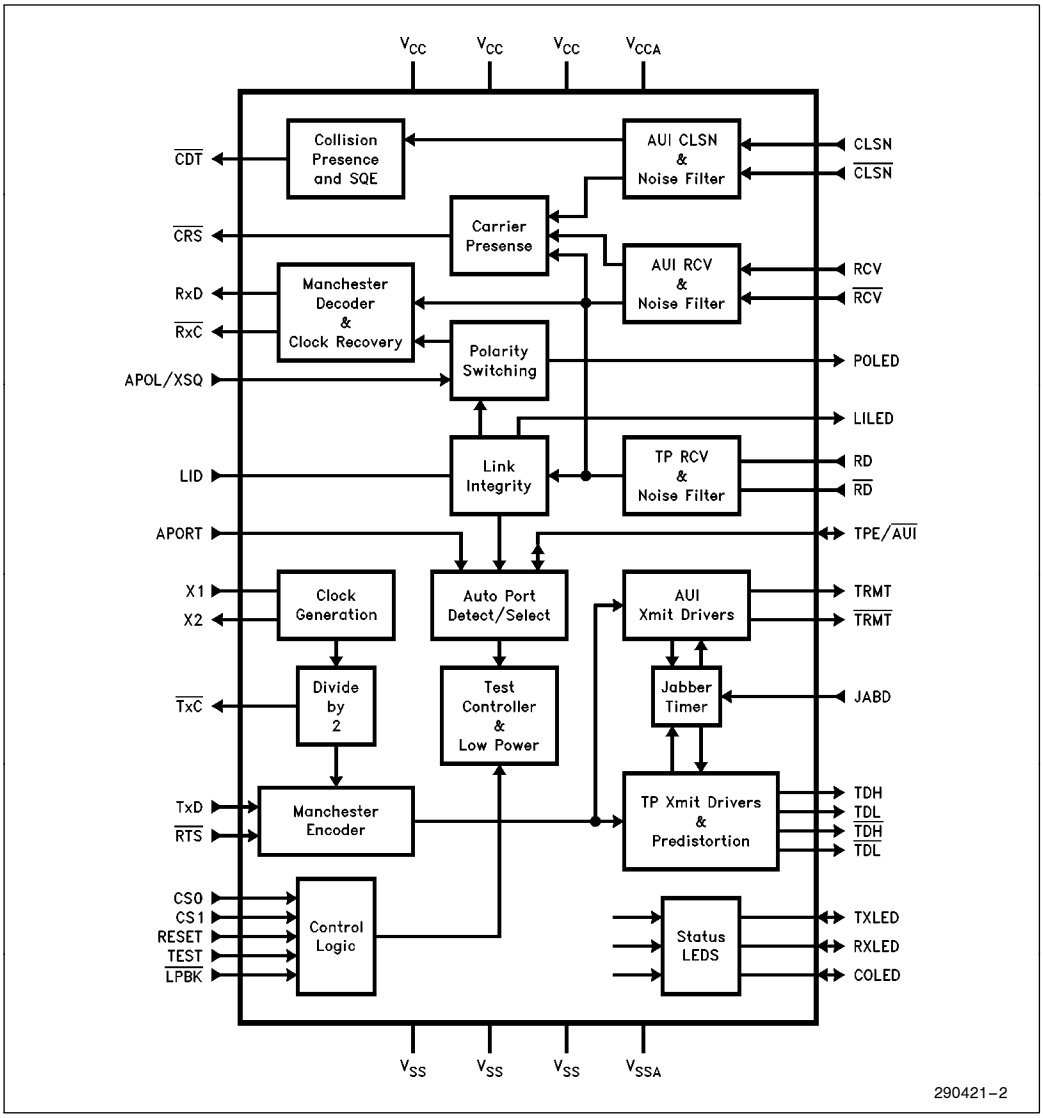

Figure 2. 82503 Functional Block Diagram

2.0 PIN DEFINITION

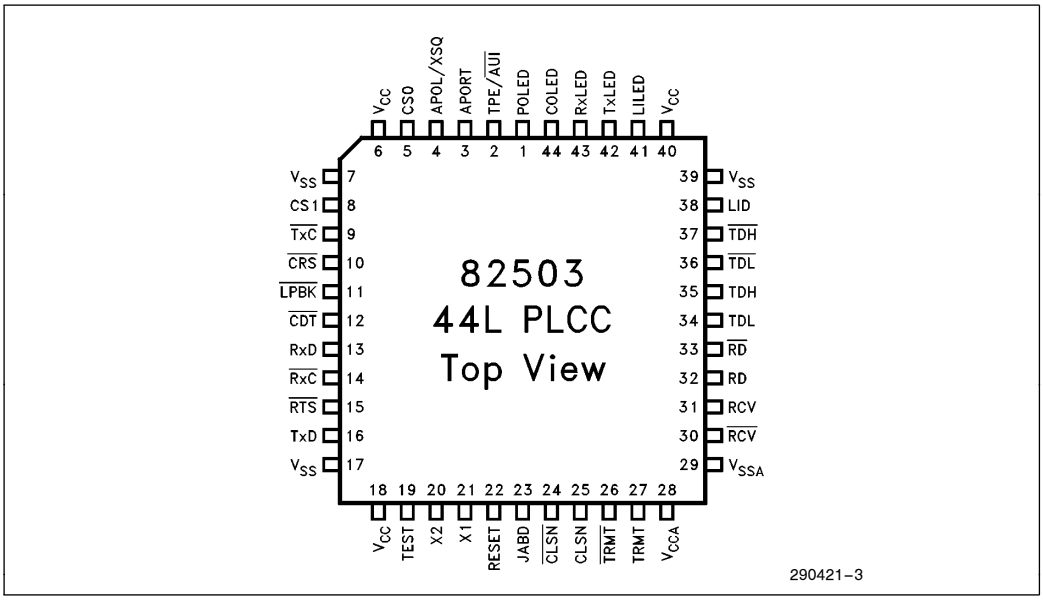

Figure 3. 44-Lead PLCC Pin Configuration

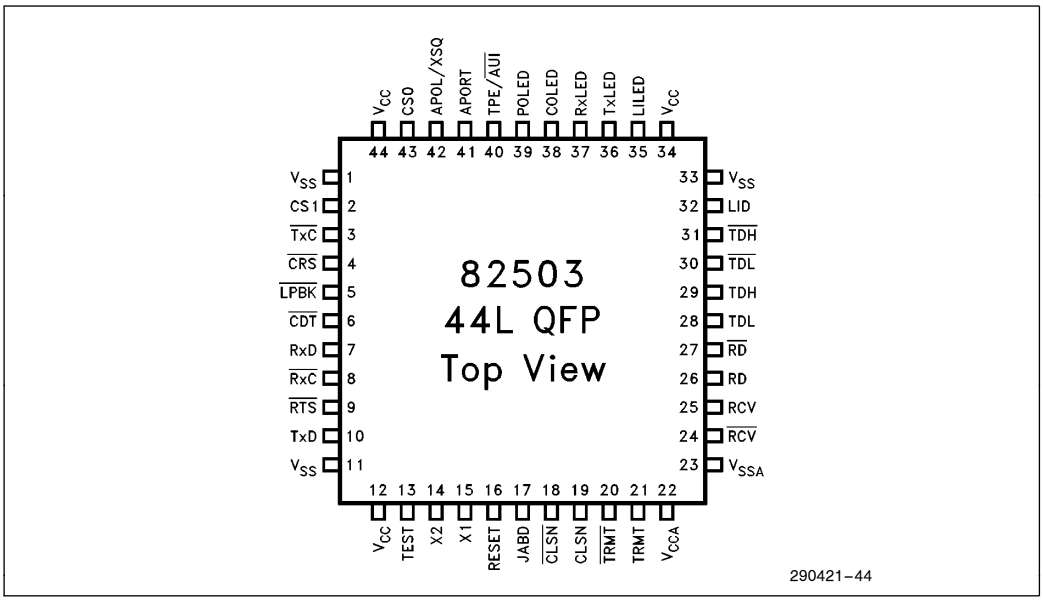

Figure 4. 44-Lead QFP Pin Configuration

2.1 Power Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
V_{SS}(1)	7, 17, 39	1, 11, 33	Supply	**Digital Ground.**
V_{CC}(1)	6, 18, 40	44, 12, 34	Supply	**Digital V_{CC}.** A 5-V ± 5% Power Supply.
V_{CCA}(1)	28	22	Supply	**Analog V_{CC}.** A 5-V ± 5% Power Supply.
V_{SSA}(1)	29	23	Supply	**Analog Ground.**

NOTE:
1. V_{CC} and V_{CCA} must be connected to the same power supply. V_{SS} and V_{SSA} must be connected to the same ground. Separate decoupling and noise conditioning (e.g., ferrite beads) should be used.

2.2 Clock Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
X1	21	15	I	**CLOCK CRYSTAL.** A 20 MHz crystal input. This pin can be driven with an external MOS level clock when X2 is left floating.
X2	20	14	O	**CLOCK CRYSTAL.** A 20 MHz crystal output. X1 can be driven with an external MOS level clock when this pin is left floating.

2.3 AUI Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TRMT $\overline{\text{TRMT}}$	27 26	21 20	O O	**TRANSMIT PAIR.** A differential output driver pair that drives the transmit pair of the transceiver cable. The output bit stream is Manchester encoded. Following the last transition, which is positive at TRMT, the differential voltage is reduced to zero volts.
RCV $\overline{\text{RCV}}$	31 30	25 24	I I	**RECEIVE PAIR.** A differentially driven input pair which is tied to the receive pair of the Ethernet transceiver cable. The first transition on RCV is negative-going to indicate the beginning of the frame. The last transition is positive-going to indicate the end of the frame. The received bit stream is assumed to be Manchester encoded.
CLSN $\overline{\text{CLSN}}$	25 24	19 18	I I	**COLLISION PAIR.** A differentially driven input pair tied to the collision presence pair of the Ethernet transceiver cable. The collision presence signal is a 10 MHz square wave. The first transition at CLSN is negative-going to indicate the beginning of the signal; the last transition is positive-going to indicate the end of the signal.

2.4 TPE Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TDH $\overline{\text{TDH}}$ TDL $\overline{\text{TDL}}$	35 37 34 36	29 31 28 30	O O O O	**TP TRANSMIT PAIR DRIVERS.** These four outputs constitute the twisted-pair drivers, which have predistortion capabilities. The TDH/$\overline{\text{TDH}}$ outputs generate the 10 Mb/s Manchester Encoded data. The TDL/$\overline{\text{TDL}}$ outputs mirror the TDH/$\overline{\text{TDH}}$ outputs except for fat bit occurrences (100 ns pulses). During the second half of a fat bit (either high or low), the TDL/$\overline{\text{TDL}}$ outputs are inverted with respect to TDH/$\overline{\text{TDH}}$ outputs. This signal behavior reduces the amount of jitter by preventing overcharge on the twisted pair medium.
RD $\overline{\text{RD}}$	32 33	26 27	I I	**TP RECEIVE PAIR.** The differential twisted pair receiver. The receiver pair is connected to the twisted pair medium and is driven with 10 Mb/s Manchester encoded data.

2.5 Controller Interface Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
$\overline{\text{TxC}}$	9	3	O	**TRANSMIT CLOCK.** A 10 MHz clock output tied directly to the transmit clock pin of the Ethernet controller. Changes sense depending on controller selected. Active low for Intel and Fujitsu controller interfaces, active high for National and AMD interfaces. Can drive one TTL load.
TxD	16	10	I	**TRANSMIT DATA.** TTL input. NRZ serial data is clocked in on TxD from the Ethernet controller. Connects directly to the transmit data pin of the Ethernet controller.
$\overline{\text{RTS}}$	15	9	I	**REQUEST TO SEND.** TTL input. An active low input signal synchronous to $\overline{\text{TxC}}$ which enables data transmission on the active port. Changes sense depending on controller selected. Active low for the Intel controller interface, active high for National, AMD, and Fujitsu interfaces.
$\overline{\text{RxC}}$	14	8	O	**RECEIVE CLOCK.** A 10 MHz clock output tied directly to the receive clock pin of the Ethernet controller. This clock is the recovered clock from incoming data on the active port. Changes sense depending on controller selected. Active low for Intel and Fujitsu controller interfaces, active high for National and AMD interfaces. Can drive one TTL load.
RxD	13	7	O	**RECEIVE DATA.** Received NRZ data (synchronous to $\overline{\text{RxC}}$) passed to the Ethernet controller. Connect directly to the receive data pin of the controller. Can drive one TTL load.
$\overline{\text{CRS}}$	10	4	O	**CARRIER SENSE.** Output that alerts the Ethernet controller that data is present on the active port. Connects directly to the carrier sense pin of the Ethernet controller. Changes sense depending on controller mode selected. Active low for Intel controller interface, active high for National, AMD, and Fujitsu interfaces. Can drive one TTL load.
$\overline{\text{CDT}}$	12	6	O	**COLLISION DETECT.** Output that indicates presence of a collision. Connects directly to the collision detect pin of the Ethernet controller. Changes sense depending on controller selected. Active low for Intel and Fujitsu controller interfaces, active high for National and AMD interfaces. Can drive one TTL load.

2.6 Mode Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TPE/$\overline{AUI}$	2	40	I/O	**PORT SELECT.** TTL input/LED output. If APORT is low, TPE/$\overline{AUI}$ is an input and selects either the TPE port (TPE/$\overline{AUI}$ high) or AUI port (TPE/$\overline{AUI}$ low). If APORT is high, the 82503 will indicate the port selected by driving TPE/$\overline{AUI}$ high (TPE) or low (AUI). TPE/$\overline{AUI}$ can drive an LED pull-up.
APORT	3	41	I	**AUTOMATIC PORT SELECTION.** TTL input. When high, 82503 will automatically select TPE or AUI port based on presence of valid link beats or frames on the TPE receive input. Mode selected will be indicated on TPE/$\overline{AUI}$.
APOL/XSQ	4	42	I	**AUTOMATIC POLARITY CORRECTION/EXTENDED SQUELCH ENABLE.** TTL input. When high, the extended squelch mode is disabled and automatic polarity correction is enabled. Both junctions (APOL and XSQ) are enabled when this pin is at a high impedance state. When low, both functions become disabled. The presence of a polarity fault on the TPE receive pair is indicated on POLED regardless of the state of APOL.
LID	38	32	I	**LINK INTEGRITY DISABLE.** TTL input. If high, link integrity function is disabled. If low, link integrity function is enabled.
CS0 CS1	5 8	43 2	I I	**CONTROLLER SELECT.** Selects the appropriate interface for the desired Ethernet controller. When CS0/1 = 0/0, supports Intel controllers. When CS0/1 = 0/1, supports Fujitsu controllers. When CS0/1 = 1/0, supports Western Digital and National controllers. When CS0/1 = 1/1, supports AMD controllers. (See Table 2.)
$\overline{LPBK}$	11	5	I	**LOOPBACK.** TTL input. An active low input signal that causes the 82503 to enter diagnostic loopback mode. The twisted pair or AUI medium will be removed from the circuit, thus isolating the node from the network. When not connected, this pin assumes the inactive (high) state. Diagnostic loopback does not disable the operation of the link integrity processor, link beat generator, or automatic port selection.
JABD	23	17	I	**JABBER DISABLE.** TTL input. When high, this pin disables the jabber function. When low, the jabber function is enabled and the device performs AUI or TP jabber protection for the active port. If this pin and TEST are asserted during a falling edge of RESET, the 82503 enters its low power mode; when either this pin or TEST deasserts, then the 82503 transitions to its normal operating mode.
TEST	19	13	I	**TEST MODE ENABLE.** TTL input. When TEST is high and RESET is deasserted, a customer test mode is directly accessed. When driven low, test mode is disabled. If this pin and JABD are asserted during a falling edge of RESET, the 82503 enters its low power mode; when either this pin or JABD deasserts, then the 82503 transitions to its normal operating mode.
RESET	22	16	I	**RESET.** TTL input. When high, resets internal circuitry. On the falling edge of RESET, either test mode or low power mode can be entered depending on the state of JABD and TEST.

2.7 LED Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TxLED	42	36	I/O	**TRANSMIT LED.** LED output. Indicates transmit status of the AUI or TPE port. Normally off (high) output. Turns on to indicate transmission. Flashes at a rate dependent on the level of transmit activity. Upon entering a customer test mode, this pin must be driven high either through an LED, or a resistor.
RxLED	43	37	I/O	**RECEIVE LED.** LED output. Indicates receive status of the AUI or TPE port. Normally off (high) output. Turns on to indicate reception. Flashes at a rate dependent on the level of receive activity. Upon entering a customer test mode, this pin must be driven high either through an LED, or a resistor.
COLED	44	38	I/O	**COLLISION LED.** LED output. Indicates collision status of the AUI or TPE port. Normally off (high) output. Turns on to indicate collision. Flashes at a rate dependent on the level of collision activity. This pin is also used to determine which customer test modes are entered.
LILED	41	35	O	**LINK INTEGRITY LED.** LED output. Normally on (low) output which indicates good link integrity on the TPE port during TPE mode. Remains on when link integrity function has been disabled. Turns off during AUI mode or when link integrity fails in TPE mode. Minimum off time is 100 ms, minimum on time is set by the link integrity function.
POLED	1	39	O	**POLARITY INDICATION.** LED output. If the 82503 detects that the receive TPE wires are reversed, POLED will turn on (low) to indicate the fault. POLED remains on even if APOL/XSQ is high and the 82503 has automatically corrected for the reversed wires.

NOTE:
1. The LED outputs have a weak pull-up capable of sourcing 500 μA. They can sink 10 mA while still meeting TTL levels. All LEDs can be used as indication pins if no LED is needed. Some of these outputs include pulse width conditioning, which should be accounted for in software.

3.0 82503 ARCHITECTURE

3.1 Clock Generation

A 20 MHz parallel resonant crystal is used to control the clock generation oscillator, which provides the basic 20 MHz clock source. An internal divide-by-two counter generates the 10 MHz ±0.01% clock required by the IEEE 802.3 specification.

We recommend a crystal that meets the following specifications be used.

- Quartz Crystal
- 20 MHz ± 0.002% at 25°C
- Accuracy ± 0.005% over full operating temperature, 0°C to +70°C
- Parallel resonant with 20 pF Load Fundamental Mode
- Maximum Series Resistance: $R_{SERIES} = 30\Omega$

Several vendors have such crystals; either-off-the shelf or custom made. Two possible vendors are:

1. M-Tron Industries, Inc.
   Yankton, SD 57078

   Specifications;
   Part No. HC49 with 20 MHz, 50 PPM over 0°C to +70°C, and 20 pF fundamental load.
2. Crystek Corporation
   100 Crystal Drive
   Ft. Myers, FL 33907

   Part No. 013212

The accuracy of the Crystal Oscillator frequency depends on the PC board characteristics, therefore it is advisable to keep the X1 and X2 traces as short as possible. The optimum value of C1 and C2 should be determined experimentally under nominal operating conditions. The typical value of C1 and C2 is between 22 pF and 35 pF.

An external 20 MHz MOS-level clock may be applied to pin X1, if pin X2 is left floating.

3.2 Transmit Blocks

3.2.1 MANCHESTER ENCODER

The 20 MHz clock is used to Manchester-encode data on the TxD input. This clock is also divided by two to produce the 10 MHz clock the LAN controller needs for synchronizing its $\overline{RTS}$ and TxD signals.

Data encoding and transmission begins with $\overline{RTS}$ asserting. Since the first bit of a transmission is a 1, the first transition is always negative on the transmit outputs (TRMT or TD pins). Transmission ends when $\overline{RTS}$ deasserts. The last transition is always positive at the transmit outputs (TRMT or TD pins) and may occur at the center of the bit cell if the last data bit to be transmitted is a 1, or at the boundary of the bit cell if the last data bit to be sent is a 0.

Immediately after the end of a transmission, all signals on the RCV pair (when AUI mode is selected) are inhibited for 4 to 5 μs. This dead time is necessary for proper operation of the SQE (heartbeat) test.

3.2.2 AUI CABLE DRIVER

The AUI cable driver (TRMT pair) is a differential circuit, which interfaces to the AUI cable through a pulse transformer.

High voltage protection is achieved by using a transformer to isolate the transmit pins (TRMT pair) from the transceiver cable. The total transmit circuit inductance, including the 802.3 transceiver transformers, should be a minimum of 27 μH for Ethernet applications.

3.2.3 TWISTED PAIR CABLE DRIVER

The twisted pair line drivers (TD pairs) begin transmitting the serial Manchester bit stream 3 bit times after $\overline{RTS}$ is asserted. The line drivers use a predistortion algorithm to improve jitter performance for up to 100 meters of twisted pair cable. The line drivers reduce their drive level during the second half of ''fat'' (100 ns) Manchester pulses and maintain a full drive level during all ''thin'' (50 ns) pulses and during the first half of the ''fat'' pulses. This reduces line overcharging during ''fat'' pulses, a major source of jitter.

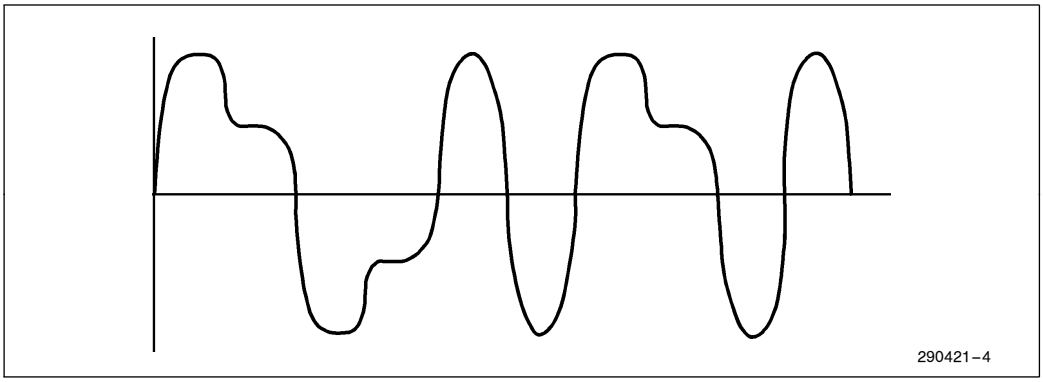

Figure 5. TPE Predistortion

3.3 Receive Blocks

3.3.1 MANCHESTER DECODER AND CLOCK RECOVERY

The 82503 performs Manchester decoding and timing recovery of the incoming data in AUI and TPE modes.

The Manchester-encoded data stream is decoded to separate the Receive Clock ($\overline{RxC}$) and the Receive Data (RxD) from the differential signal. The 82503 uses an advanced digital technique to perform the decoding function. The use of digital circuitry instead of analog circuitry (e.g., a phase-lock loop) to perform the decoding ensures that the decoding function is less sensitive to variations in operating conditions.

A high-resolution phase reference is used to digitize the phase of the incoming data bit-center transition. The digitizer has a phase resolution of 1/32 of a bit time.

The digitized phase is filtered by a digital low-pass filter to remove rapid phase variations, i.e., phase jitter. Slow phase variations, such as those caused by small differences between the data frequency and the clock frequency, are not filtered by the low-pass filter.

The $\overline{RxC}$ generator digitally sets the phases of the two $\overline{RxC}$ transitions to respectively lead and lag the bit-center transition by ¼ bit time. $\overline{RxC}$ is used to recover RxD by sampling the incoming data with an edge-triggered flip-flop.

Lock is achieved by reducing the time constant of the digital filter to zero at the start of a new frame. Any uncertainty in the bit-center phase of the first transition that is caused by jitter is subsequently removed by gradually increasing the filter time constant during the following preamble. By that time, the phase of the bit center is output by the filter, and lock is achieved. Lock is achieved within the first 14 bit times as seen by the AUI inputs. The maximum bit-cell timing distortion (jitter) tolerated by the Manchester decoder circuitry is ±12 ns (preamble), ±18 ns (data) for AUI, and ±13.5 ns for TPE (data and preamble).

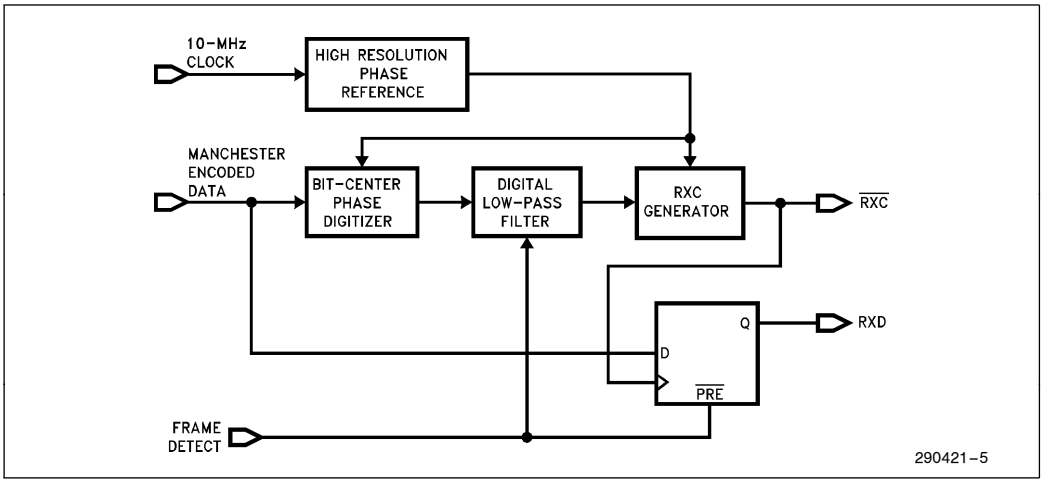

Figure 6. Manchester Decoder and Clock Recovery

3.3.2 AUI RECEIVE AND COLLISION BUFFERS

The AUI receive and collision inputs are driven through isolation transformers to provide high voltage protection and DC common mode voltage rejection. The incoming signals are converted to digital levels and passed to the Manchester decoder and collision detection circuitry.

3.3.3 AUI RECEIVE AND COLLISION SQUELCH CIRCUITS

Both the receive (RCV) and collision (CLSN) pairs have the following squelch characteristics.

- The squelch circuits are turned on at idle.
- A pulse is rejected if the peak differential voltage is more positive than −160 mV regardless of pulse width.
- A pulse is considered valid if its peak differential voltage is more negative than −300 mV and its width, measured at −285 mV, is greater than 25 ns.
- The squelch circuits are disabled by the first valid negative differential pulse on either the AUI receive (RCV) or the AUI collision (CLSN) pair.
- If a positive differential pulse occurs on either the AUI receive or collision pairs for greater than 160 ns, End of Frame (EOF) is assumed and the squelch circuitry is turned on.

3.3.4 TPE RECEIVE BUFFER

The TPE receive pins (RD and $\overline{RD}$) are connected to the twisted pair medium through an analog front end. The analog front end contains the line coupling devices and EMI filters necessary to conform to the 10BASE-T standards and local RF regulations. The input differential voltage range for the TPE receiver is greater than 500 mV and less than 3.1V differential.

3.3.5 TPE RECEIVE SQUELCH CIRCUITS

The TPE receive buffer distinguishes valid receive differential data, link test pulses, and the idle condition according to the requirements of the 10BASE-T standard. Signals at the output of the EMI filter (thus at the RD and $\overline{RD}$ pair) are rejected as follows:

- All differential pulses of peak magnitude less than 300 mV are rejected.
- All continuous sinusoids with a differential amplitude less than 6.2 V_{PP} and a frequency less than 2 MHz are rejected.
- All sine waves of single cycle duration starting with phase 0° or 180° that have an amplitude less than 6.2 V_{PP}, and a frequency of 2 MHz to 16 MHz are rejected, if the single cycle is preceeded and followed by 4 bit times of silence (i.e., a signal less than 300 mV).

3.3.6 TPE Extended Squelch Mode

By placing the 82503 into TPE extended squelch mode, the 82503 can support cable lengths greater than the 100m specified in the 10Base-T IEEE standard (802.3i-1990). The squelch thresholds for the signals at the RD/$\overline{RD}$ pair are typically reduced by 4.5 dB. This allows Grade 5 twisted-pair cable to be used to overcome attenuation and multipair crosstalk for cable lengths up to 200 meters.

TPE extended squelch mode is enabled by presenting a high-impedance (>100 KΩ) at the APOL/XSQ pin. This can be done by floating the APOL/XSQ pin, tying APOL/XSQ low through a 100 KΩ resistor, or driving APOL/XSQ with a three-state buffer. When driven high or low using a TTL driver or a low impedance pull-up or pull-down (<2 KΩ) extended squelch is disabled and the driven level at the APOL/XSQ pin determines the state of the polarity-correction function (APOL/XSQ = 1 enables polarity correction, APOL/XSQ = 0 disables polarity correction). The TPE extended squelch feature is transparent to previous steppings of the 82503. Polarity correction is always enabled when the TPE extended-squelch feature is enabled (APOL/XSQ = Z).

The APOL/XSQ pin senses a high-impedance state by an active-polling circuit implemented at the pin. Two small polling devices attempt to pull the APOL/XSQ pin up to V_{CC} and down to V_{SS}. If the pin is in a high-impedance state, the devices will be successful in pulling the APOL/XSQ pin high and low. If the pin is driven high or low, the polling devices will not be able to successfully pull the pin in the opposite direction. In this way, an internal state machine can correctly determine one of three states of the APOL/XSQ pin. The pin is polled every 25.6 μs.

3.4 Collision Detection

3.4.1 AUI COLLISION DETECTION

Collision detection in the AUI mode is performed by the attached transceiver, and signalled to the 82503 on the CLSN pair. A 10 MHz +25%, or −15%, square wave with transition times between 35 ns and 70 ns indicates the collision. The 82503 reports this to the LAN controller on the $\overline{CDT}$ pin.

3.4.2 TPE COLLISION DETECTION

Collision detection in the TPE mode is indicated by simultaneous transmission and reception on the twisted pair link segment. The $\overline{CDT}$ signal is asserted for the duration of both $\overline{RTS}$ and the presence of received data; $\overline{CRS}$ is asserted for the duration of either $\overline{RTS}$ or the presence of received data. During a collision, the source of RxD will be the received data. If the received data stream ends before the transmit data stream, the RxD source will be changed to transmit data stream until it ends.

3.5 Link Integrity

The 82503 supports the link integrity function as defined by 10BASE-T. During long periods of idle on the transmitter, link test pulses will be transmitted on to the twisted pair medium as an indication to the remote MAU that the link is good. These pulses will be transmitted 8 ms to 24 ms after the end of the last transmission or link test pulse.

The link integrity function continuously monitors activity on the receive circuit. If neither valid data nor link test pulses are received, the link integrity processor declares the link bad, and disables transmission and reception on the media, loopback, and the SQE test function. Transmission of link test pulses and monitoring receive activity are not affected. The idle time required for the link integrity processor to determine the link is bad is 50 ms to 150 ms.

Once a frame or a sequence of 2 to 10 valid consecutive link test pulses are detected, the Link Integrity Processor declares the link is good, and reconnects the transmitter and receiver.

The link integrity function can be disabled by driving the LID pin high or by disabling automatic port selection (APORT = 0) and selecting the AUI port. This option is intended primarily for use with pre-10BASE-T networks.

3.6 Jabber Function

The 82503 contains a jabber timer to implement the jabber function. If a transmission continues beyond the limits specified, the jabber function inhibits further transmission and asserts the collision indicator, $\overline{CDT}$. The limits for jabber transmission are 20 ms to 150 ms in TPE Mode, and 8 ms to 16 ms in AUI mode. For both AUI and TPE mode, the transmission inhibit period extends until the 82503 detects sufficient idle time (between 250 ms and 750 ns) on the $\overline{RTS}$ signal. The jabber function can be disabled by driving the JABD high.

In TPE mode the link integrity function continues to operate even if the jabber function is inhibiting transmission. Link test pulses continue to be sent and the receive circuit continues to be monitored. Additionally, the link integrity function reconnects to a restored link without waiting for the transmit input to go idle when the jabber function is inhibiting transmission.

3.7 TPE Loopback

In TPE mode the 82503 implements the transmit to receive loopback (DO to DI) mode specified in the 10BASE-T standard. This mode loops back transmitted data through the receive path.

This function is required to maintain full compatibility with coax MAUs where the data loopback is a natural result of the architecture.

The transmit to receive loopback function is disabled when the jabber function or link integrity function is inhibiting transmission.

3.8 SQE Test Function

The 82503 supports the SQE test function when in TPE mode or in Diagnostic Loopback mode. The 82503 will assert its $\overline{CDT}$ pin within 0.6 μs to 1.6 μs after the end of a transmission, and it will remain asserted for 5- to 15-bit times. If the 82503 is in the TPE mode and is not in diagnostic loopback mode, the link integrity function will disable the SQE test function when it detects a bad link.

3.9 Port Selection

The 82503 features both manual and automatic port selection. To enable automatic port selection, connect APORT to V_{CC}. The 82503 then starts in TPE mode and monitors link integrity. If the link is good, the 82503 stays in TPE mode and pulls TPE/$\overline{AUI}$ high to indicate that the TPE port was selected. If link integrity fails, the 82503 switches to AUI mode and pulls TPE/$\overline{AUI}$ low to indicate that the AUI port is now active. TPE/$\overline{AUI}$ can drive an LED to indicate port selection (on for AUI, off for TPE mode). Note that LILED will be on if TPE mode is selected and off if AUI mode is selected. If link integrity is disabled while automatic port selection is enabled, the 82503 defaults to TPE mode. If the 82503 changes ports while $\overline{RTS}$ is active, transmission is terminated with an End of Frame marker on the old port. Transmission of the remaining packet fragment is not allowed on the new port. Transmissions will begin with a complete data packet.

The port can be manually selected by driving APORT low. TPE/$\overline{AUI}$ = 0 selects AUI mode, and TPE/$\overline{AUI}$ = 1 TPE mode. When the port is manually selected, the circuitry for the unused port is powered down. Changing ports requires 100 μs to allow the circuitry for the new port to resume normal operation.

Table 1. Port Selection

Configuration			State
LID	APORT	TPE/$\overline{AUI}$	
X	0	0	AUI (TPE Port Powered Down)
X	0	1	TPE (AUI Port Powered Down)
0	1	X*	Automatic Port Selection
1	1	X*	TPE

NOTE:
*TPE/$\overline{AUI}$ is an output pin when APORT = 1.

3.10 LED Description

The 82503 supports six LED pins to indicate the status of important states; TPE/$\overline{AUI}$, TxLED, POLED, LILED, RxLED, COLED. Each pin is capable of directly driving an LED.

3.10.1 TPE/$\overline{AUI}$

When automatic port selection is enabled (APORT is high), TPE/$\overline{AUI}$ becomes an LED output and turns off if TPE mode is selected and on if AUI mode is selected.

3.10.2 TxLED

Transmit status. This LED is normally off and flashes at 2.5 Hz, 5 Hz, and 10 Hz to indicate respectively a low, medium, and high rate of transmit activity.

3.10.3 RxLED

Receive LED. This LED is normally off and flashes at 2.5 Hz, 5 Hz, and 10 Hz to indicate respectively a low, medium, and high rate of receive activity.

3.10.4 COLED

Collision LED. This LED is normally off and flashes at 2.5 Hz, 5 Hz, and 10 Hz to indicate respectively a low, medium, and high rate of collision activity.

3.10.5 POLED

Polarity Fault. This LED is normally off and turns on to indicate a polarity fault in the receive pair of the 10BASE-T link. Operation of this pin is not affected by the state of the polarity correction function (APOL/XSQ = X).

3.10.6 LILED

Link Integrity status. When Aport is enabled (APORT = 1), this LED is normally on (driven low) to indicate the presence of a valid 10BASE-T link when the TPE port is active. The LED will turn off (driven high) when the link fails. When link integrity is disabled (LID = 1) while APORT is enabled (APORT = 1) this LED is turned on (driven low). If APORT is disabled (APORT = 0) and the AUI port is manually selected (TPE/$\overline{AUI}$ = 0) the LED output is tristated.

3.11 Polarity Switching

In TPE mode, the 82503 monitors receive link beats and end-of-frame delimiters for a possible receiver

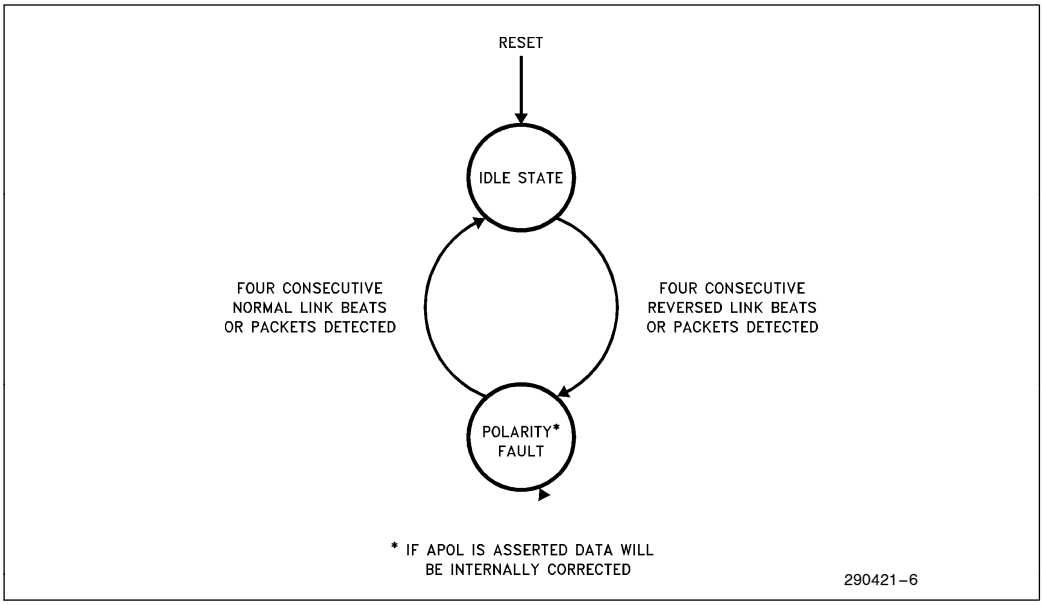

Figure 7. Polarity Fault State Diagram

polarity error due to crossed wires. If Pin 4 of the 82503 is high and the TPE receive pins are reversed, the 82503 will correct the error by reversing the signals internally, and turn POLED on (low) to indicate that the fault has been detected and corrected. The polarity correction function is defeatable by driving the APOL/XSQ input low. However, the polarity fault will continue to be indicated on the POLED.

3.12 Controller Interface

Connecting the 82503 to one of the Intel Ethernet controllers (82586, 82590, 82593, 82596) requires no additional components. Simply drive CS0 and CS1 both low, and connect $\overline{TxC}$, TxD, $\overline{RTS}$, $\overline{RxC}$, RxD, $\overline{CRS}$, $\overline{CDT}$, and $\overline{LPBK}$ to the corresponding controller pins.

The 82503 also works with other Ethernet controllers without additional components, including the National Semiconductor 8390 and 83932 (SONIC), Western Digital 83C690, Fujitsu 86950 (Etherstar), depending on the state of and CS0 and CS1 inputs.

The interface of the 82503 to the AMD 7990 (LANCE) requires external logic to control the $\overline{LPBK}$ pin of the 82503. Note that when an AMD LAN controller is used to interface to the 82503, the $\overline{LPBK}$ pin of the 82503 becomes active high. That is, the 82503 enters diagnostic loopback mode when $\overline{LPBK}$ pin is high and is in normal operation mode when $\overline{LPBK}$ pin is low.

The logic sense of the 82503 controller pins will change and should be connected to the controller pins according to the following table.

Table 2. Controller Interface Selection

82503 Pin	Intel Controller 825XX		National, WD Controllers 8390, 83C690, 83832 (SONIC)		AMD Controller 7990 (LANCE), 79C900 (ILACC)		Fujitsu Controllers 86950 (Etherstar)	
CS0[1]	0		1		1		0	
CS1	0		0		1		1	
Pin	**Pin**	**Sense**	**Pin**	**Sense**	**Pin**	**Sense**	**Pin**	**Sense**
$\overline{TxC}$	$\overline{TxC}$	Low	TXC	High	TCLK	High	TCKN	Low
TxD	TxD	High	TXD	High	TX	High	TXD	High
$\overline{RTS}$	$\overline{RTS}$	Low	TXE	High	TENA	High	TEN	High
$\overline{RxC}$	$\overline{RxC}$	Low	RXC	High	RCLK	High	RCKN	Low
RxD	RxD	High	RXD	High	RX	High	RXD	High
$\overline{CRS}$	$\overline{CRS}$	Low	CRS	High	RENA	High	XCD	High
$\overline{CDT}$	$\overline{CDT}$	Low	COL	High	CLSN	High	XCOL	Low
$\overline{LPBK}$	$\overline{LPBK}$	Low	LPBK	High	(Note 2)		LPBK	High

NOTES:
1. CS0 and CS1 are intended to be static pins only. Switching CS0 and CS1 during network reception or transmission will produce unpredictable results.
2. Refer to Section 3.12.

4.0 RESET, LOW-POWER AND TEST MODES

4.1 Reset

When RESET is asserted the device resets its internal circuits. RESET is required after power up, and before data can be transmitted or received. It is allowed any time thereafter, but any existing receive or transmit activity will be lost, and all state machines (Link integrity, Jabber, and Polarity Correction) return to their initial states. TEST must be held low for a device reset to prevent entering a test for low power mode. During RESET, $\overline{TxC}$ continues without interruption (in Fujitsu mode both $\overline{TxC}$ and $\overline{RxC}$ run continuously).

4.2 Low Power and High Impedance Modes

When RESET is deasserted while both TEST and JABD are held high, the 82503 enters its low power and high impedance modes. The majority of internal circuitry is powered down, and many inputs and outputs are three-stated. These pins are: APORT, APOL/XSQ, LID, TPE/$\overline{AUI}$, POLED, LILED, $\overline{RTS}$, $\overline{LPBK}$, RxD, TxD, $\overline{CRS}$ and $\overline{CDT}$. When either JABD or TEST is deasserted, the device begins a power on cycle which lasts less than 1 ms. During this cycle, all inputs are ignored and all transmissions are disabled. If $\overline{RTS}$ is active when the device returns to normal operation, the remainder of that packet fragment is not transmitted. Normal transmissions are resumed at the start of the first complete data packet.

4.3 Diagnostic Loopback

This is a diagnostic test mode to help in fault isolation and detection. Serial NRZ data input on TxD is Manchester encoded and then looped back through the Manchester decoder (TMD) appearing at the RxD output. Collision detect is asserted following each transmission to simulate the SQE test. Output cable drivers and input amplifiers are disconnected from the controller interface pins while in this mode. The link integrity and polarity fault detection functions are not inhibited by diagnostic loopback mode. If otherwise enabled, they continue to function.

4.4 Customer Test Mode (Continuous AUI/TPE Transmit)

In this mode, the 82503 continuously transmits data without the intervention of a LAN controller. Transmission is at 10 MHz (11-bit pattern), and can occur on either the TPE or AUI port. The jabber timer is disabled in this mode, allowing users to easily test the 10BASE-T harmonic content specification and the quality of their analog front end design without complex software exercisers.

Customer Test Mode—and Low Power Mode are selected at the deassertion of RESET as shown in the following table. (Note that the 82503 must be in non-loopback mode before it can enter the customer test mode.)

Table 3. Test and Low Power Mode Selection

RESET	TEST	JABD	TxLED(1)	RxLED(1)	COLED(1)	Mode Selected
↓	0	X	X	X	X	Normal Mode
↓	1	0	1	1	1	Cont Tx 10 MHz
↓	1	1	X	X	X	Low Power

NOTE:
1. A standard LED connection to these pins is sufficient to pull them to a logic 1.

The port on which the continuous transmit appears is determined by the APORT and TPE/$\overline{\text{AUI}}$ pins. If automatic port selection is enabled (APORT = 1) then the TPE port broadcasts the continuous transmit. If manual port selection is enabled (APORT = 0), then TPE/$\overline{\text{AUI}}$ selects the port (1 for TPE, 0 for AUI). Test mode is disabled when TEST is deasserted and the device is reset.

5.0 APPLICATION EXAMPLE

5.1 Introduction

The 82503 is designed to work directly with the Intel LAN controllers (82586, 82590, 82593, and 82596), as well as AMD's Am7990, National Semiconductor's 8390, Western Digital's 82C690, and Fujitsu's 86950. The serial interface signals connect directly between one of the aforementioned LAN controllers and the 82503 without the need for external logic.

This example is targeted toward interfacing the 82503 to the Intel 82596 in a two-port (TPE/AUI) application.

5.2 Design Guidelines

AUI Pulse Transformer

In order to meet the 16V fault tolerance specification of 802.3 a pulse transformer is recommended for the transmit, receive and collision pairs. The transformer should be placed between the TRMT, RCV, and CLSN pairs of the 503, and the DO, DI, and CI pairs respectively, of the AUI (DB-15 connector). The pulse transformer should have a parallel inductance of 75 μH minimum (100 μH recommended).

Several vendors stock such transformers. Two possible vendors are:

1. Pulse Engineering (P/N PE-64103)
2. Valor Electronics (P/N LT6003)

Terminating Resistors

The terminating resistors used across the receive and collision pairs are recommended to be 78.7 Ω $\pm$1%.

Analog Front-End

The 82503 provides six TPE pins (TDH, $\overline{\text{TDH}}$, TDL, $\overline{\text{TDL}}$, RD, and $\overline{\text{RD}}$) that connect to the Analog Front End through a resistor summing network (Figure 7). AFE solutions can be made discretely or purchased from several manufacturers. Two different solutions are described in Application Note 356. The example shown here uses a Pulse Engineering AFE package PE65434 which includes EMI filter, isolation transformer, and common mode choke. The output of the AFE connects directly to the 10BASE-T connector (RJ-45).

Decoupling

It is recommended that 0.01 μF X7R and 0.001 μF NPO decoupling capacitors be placed between the V_{CCA} and V_{CCD} of the 82503 to V_{SSA} and V_{SSD}.

Clock Generation

The clock input to the 82503 can be from a clock oscillator or a crystal. If a clock oscillator is used, X1 should be driven, and X2 left floating. If a crystal oscillator is used, refer to Section 3.1 for crystal specifications.

A complete 82596/82503 TPE/AUI Ethernet Solution is shown at the end of this section.

5.3 Layout Guidelines

General

The analog section, as well as, the entire board itself should conform to good high-frequency practices and standards to minimize switching transients and parasitic interaction between various circuits. To achieve this, the following guidelines are presented.

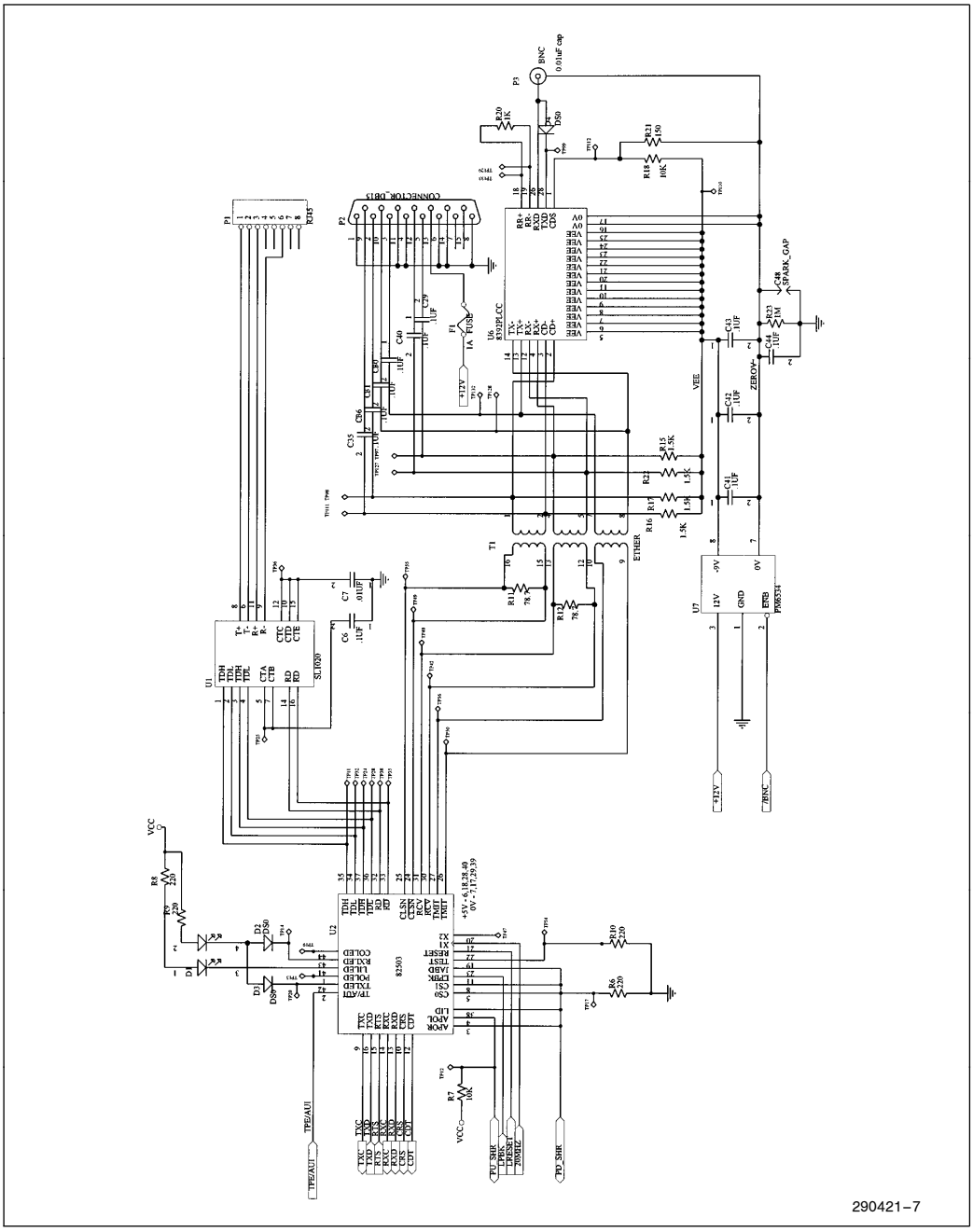

Figure 8. Application Example Schematic

Make power supply and ground traces as thick as possible. This will reduce high-frequency cross coupling caused by the inductance of thin traces.

Connect logic and chassis ground together.

Separate and decouple all of the analog and digital power supply lines.

Close signal paths to ground as close as possible to their sources to avoid ground loops and noise cross coupling.

Use high-loss magnetic beads on power supply distribution lines.

Crystal

The crystal should be adjacent to the 82503 and trace lengths should be as short as possible. The X1 and X2 traces should be symmetrical.

82503 Analog Differential Signals

The differential signals from the 82503 to the transformers, analog front end, and the connectors should be symmetrical for each pair and as short as possible. Differential signal layout should be performed to a characteristic impedance of 78Ω (for AUI) or 100Ω (for TPE).

As a general rule, the trace widths should be one to three times the distance between the PCB layers to eliminate excessive trace inductance.

The differential signals should also be isolated from the high speed logic signals on the same layer as well as on any sublayers of the PCB.

Group each of the circuits together, but keep them separate from each other. Separate their grounds.

In layout, the circuitry from the connectors to the filter network, should have the ground plane removed from beneath it. This will prevent ground noise from being induced into the analog front end.

All trace bends should not exceed 45 degrees.

6.0 PACKAGE THERMAL SPECIFICATIONS

The 82503 Dual Serial Transceiver is specified for operation when case temperature (T_C) is within the range of 0°C to +85°C. The case temperature can be measured in any environment, to determine if the 82503 is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The acceptable operating ambient temperature (T_A) is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from the θ_{ja} and θ_{jc} from the following equations:

$$T_J = T_C + P \times \theta_{jc}$$
$$T_J = T_A + P \times \theta_{ja}$$
$$T_A = T_C - P \times (\theta_{ja} - \theta_{jc})$$

Values for θ_{ja} and θ_{jc} are given in Table 4 for the 44-lead PLCC and 44-lead QFP packages. Various values for θ_{ja} at different airflows. Table 5 shows the maximum T_A allowable (without exceeding T_C) at various airflows.

Table 4. Thermal Resistance (°C/Watt) θ_{jc} and θ_{ja}

Package	θ_{jc}	θ_{ja} vs Airflow—ft/min (m/s)					
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
44-Lead PLCC	19	57	48	43	41	39	37
44-Lead QFP	26	98	94	78	70	66	64

Table 5. Maximum T_A at Various Airflows

Package	θ_{ja} vs Airflow—ft/min (m/s)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
44-Lead PLCC	66	71	73	74	75	76
44-Lead QFP	49	51	59	63	65	66

7.0 ELECTRICAL SPECIFICATIONS AND TIMINGS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

ABSOLUTE MAXIMUM RATINGS

Case Temperature Under Bias . . . . . 0°C to +85°C
Storage Temperature . . . . . −65°C to +140°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +6.0V(1)

DC CHARACTERISTICS (T_C = 0°C to +85°C, V_{CC} = 5V ±5%, V_{CCA} = 5V ±5%)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}(TTL)(2)	Input Low Voltage	−0.3	0.8	V	
V_{IH}(TTL)(2)	Input High Voltage	2.0	V_{CC}	V	
I_{LI}(2)	Input Leakage Current		±10	µA	0.0V ≤ V_I ≤ V_{CC}, RESET = 1
V_{OL}(MOS)(3)	Output Low Voltage		0.45	V	I_{OL} = 4 mA
V_{OH}(MOS)	Output High Voltage	3.9		V	I_{OH} = −500 µA
V_{OL}(LED)(4)	Output Low Voltage		0.45	V	I_{OL} = 10 mA
V_{OH}(LED)	Output High Voltage	3.9		V	I_{OH} = −500 µA
I_{LP}	Leakage Current, Low Power Mode(5)		±10	µA	0.0V ≤ V_I ≤ V_{CC}
R_{DIFF}	Input Differential Resistance(6)	10		kΩ	dc
V_{IDF}(TPE)(7)	Input Differential Accept Input Differential Reject Input Differential Accept (XSQ) Input Differential Reject (XSQ)	±0.500 (Note 8) 	±3.1 ±0.300 ±3.1 ±0.180	V_P V_P V_P V_P	5 MHz ≤ f ≤ 10 MHz
R_S(TPE)(8)	Output Source Resistance	6	13	Ω	$\|I_{LOAD}\|$ = 25 mA
V_{IDF}(AUI)(9)	Input Differential Accept Input Differential Reject	±0.300	±1.5 ±0.160	V_P V_P	
V_{ODF}(AUI)(10)	Output Differential Voltage	±0.450	±1.20	V	

NOTES:
1. The voltage levels for RCV, CLSN, and RD pairs are −0.75V to +8.5V.
2. TTL Input Pins: TxD, RTS, TPE/AUI, APORT, APOL/XSQ, LID, CS0, CS1, LPBK, JABD, TEST, RESET.
3. MOS Output Pins: TxC, RxD, RxC, CRS, CDT.
4. LED Pins: TPE/AUI, TxLED, RxLED, COLED, POLED, LILED. V_{OL} measured 10 ns after falling edge of TxC.
5. Pins: APORT, APOL/XSQ, LID, TPE/AUI, POLED, LILED, RTS, LPBK, RxD, TxD, CRS, CDT, CS0, CS1, JABD, TEST, and RESET.
6. Pins: RD to RD, RCV to RCV, and CLSN to CLSN.
7. TPE Input Pins: RD, and RD. See Section 3.3.4 and Section 3.3.5.
8. Typically it is −4.5 dB below normal squelch level.
9. TPE Output Pins: TDH, TDH, TDL, and TDL. R_S measures V_{CC} or V_{SS} to Pin.
10. AUI Input Pins: RCV, and CLSN pairs.
11. AUI Output Pins: TRMT pair.

DC CHARACTERISTICS (T_C = 0°C to +85°C, V_{CC} = 5V ±5%, V_{CCA} = 5V ±5%) (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{OSC}(AUI)	AUI Output Short Circuit Current		±150	mA	Short Circuit to V_{CC} or GND
V_U(AUI)	Output Differential Undershoot		−100	mV	
V_{ODI}(AUI)	Differential Idle Voltage(11)		±40	mV	
I_{CC}(HOT)	Power Supply Current(12)		65	mA	APORT = 1
I_{CC}	Power Supply Current		75	mA	APORT = 1
I_{CC}	Power Supply Current		60	mA	APORT = 0
I_{CCSB}	Standby Supply Current(13)		1	mA	Low Power Mode, 20 μA Typical
PD (HOT)	Power Dissipation(12)		0.38	W	APORT = 1, Continuous Transmission on AUI
PD	Power Dissipation		0.40	W	APORT = 1, Continuous Transmission on AUI
PD_{SB}	Standby Power Dissipation(13)		5.25	mW	Low Power Mode, 105 μW Typical
C_{IN}(14)	Input Capacitance		10	pF	at f = 1 MHz

NOTES:
11. Measured 8.0 μs after last positive transition of data packet.
12. I_{CC} HOT measurements made at T_C = +85°C. Additionally, TRMT, $\overline{\text{TRMT}}$, TDH, $\overline{\text{TDH}}$, TDL, $\overline{\text{TDL}}$ are loaded with 20 pF and load resistors removed.
13. Pins CS0 and CS1 connected to V_{CC} or V_{SS} through a 2.5 kΩ (or less) resistor. I_{CCSB} is typically at 20 μA after 30s from power down assertion—not tested.
14. Characterized, not tested. (Controller interface and mode pins only.)

AC TIMING CHARACTERISTICS

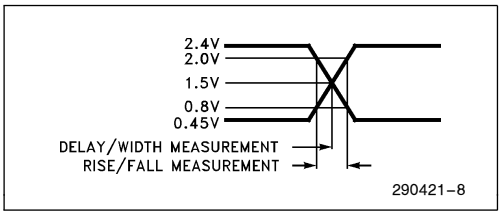

Figure 9. MOS Input Voltage Levels (TTL Compatible) for Timing Measurements (TxD, $\overline{\text{RTS}}$, TPE/$\overline{\text{AUI}}$, APORT, APOL/XSQ, LID, $\overline{\text{LPBK}}$, JABD, TEST, and RESET).

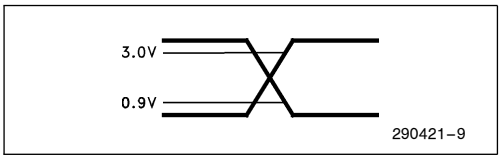

Figure 10. Voltage Levels for MOS Level Output Timing Measurements ($\overline{\text{TxC}}$, RxD, $\overline{\text{RxC}}$, $\overline{\text{CRS}}$, and $\overline{\text{CDT}}$).

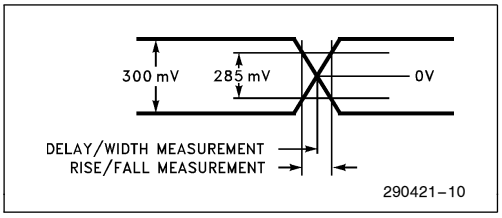

Figure 11. Voltage Levels for Differential Input Timing Measurements (RCV and CLSN Pairs).

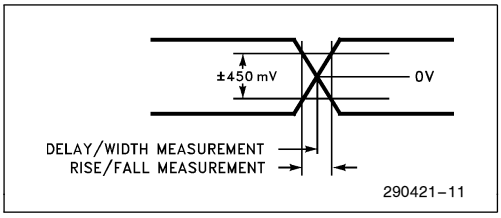

Figure 12. Voltage Levels for TRMT Pair Output Timing Measurements.

AC TIMING CHARACTERISTICS (Continued)

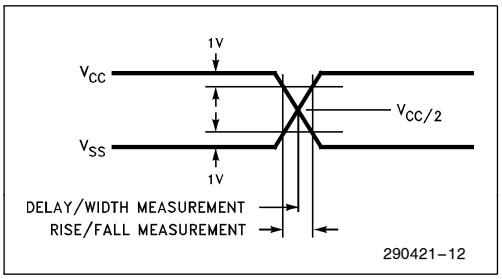

Figure 13. Voltage Levels for TDH, TDL, $\overline{TDH}$, and $\overline{TDL}$.

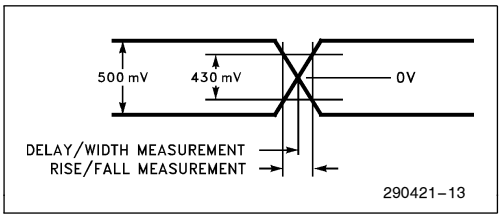

Figure 14. Voltage Levels for Differential Input Timing Measurements (RD Pair).

AC MEASUREMENT CONDITIONS

1. T_C = 0°C to +85°C, V_{CC} = 5V ±5%.
2. The AC MOS, TTL and differential signals are referred to in Figures, 8, 9, 10, 11, 12, and 13.
3. AC loads
   a. MOS: 20 pF total capacitance to ground.
   b. AUI Differential: a 10 pF total capacitance from each terminal to ground and a load resistor of 78Ω ±1% in parallel with a 27 μH ±1% inductor between terminals.
   c. TPE: 20 pF total capacitance to ground.
4. All parameters become valid 200 μs after the supply voltage and input clock has stabilized, or after RESET deasserts.

CLOCK TIMING (15)

Symbol	Parameter	Min	Typ	Max	Units
t_1	X1 Cycle Time	49.995		50.005	ns
t_2	X1 Fall Time			5	ns
t_3	X1 Rise Time			5	ns
t_4	X1 Low Time	15			ns
t_5	X1 High Time	15			ns

NOTE:
15. Refers to External Clock Input.

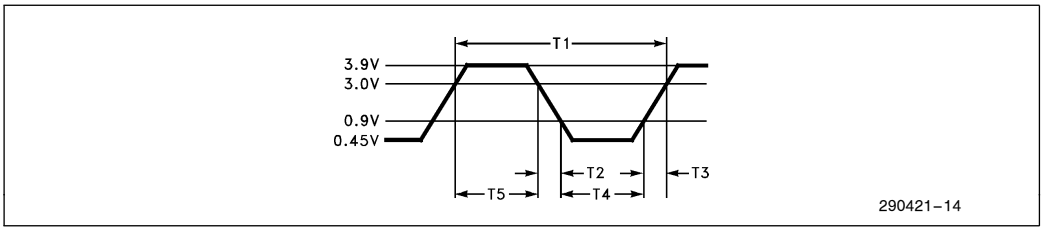

Figure 15. X1 Input Voltage Levels for Timing Measurements

Controller Interface Timings (Intel Mode)

TRANSMIT TIMINGS (Intel)

Symbol	Parameter	Min	Typ	Max	Units
t_{10}	$\overline{TxC}$ Cycle Time	99.99		100.01	ns
t_{11}	$\overline{TxC}$ High/Low Time	40			ns
t_{12}	$\overline{TxC}$ Rise/Fall Time			5	ns
t_{13}	TxD and $\overline{RTS}$ Rise/Fall Time			10	ns
t_{14}	TxD Setup Time to $\overline{TxC}$ ↓	45			ns
t_{15}	TxD Hold Time from $\overline{TxC}$ ↓	0			ns
t_{16}	$\overline{RTS}$ Setup Time to $\overline{TxC}$ ↓	45			ns
t_{17}	$\overline{RTS}$ Hold Time from $\overline{TxC}$ ↓	0			ns

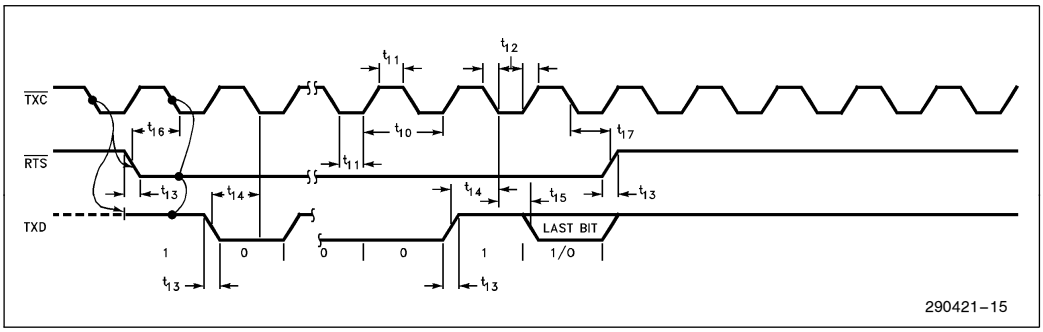

Figure 16. Transmit Timing (Intel)

RECEIVE TIMING (Intel)

Symbol	Parameter	Min	Typ	Max	Units
t_{20}	$\overline{RxC}$ Cycle Time	96	100		ns
t_{21}	$\overline{RxC}$ High Time	36			ns
t_{22}	$\overline{RxC}$ Low Time	40			ns
t_{23}	$\overline{RxC}$ Rise/Fall Time			5	ns
t_{24}	$\overline{RxC}$ Delay from $\overline{CRS}$ ↓		1100	1400	ns
t_{25}	RxD Rise/Fall Time			5	ns
t_{26}	RxD Setup from $\overline{RxC}$ ↓	30			ns
t_{27}	RxD Hold from $\overline{RxC}$ ↓	30			ns
t_{28}	$\overline{CRS}$ Deassertion Hold Time from $\overline{RxC}$ High	10		40	ns

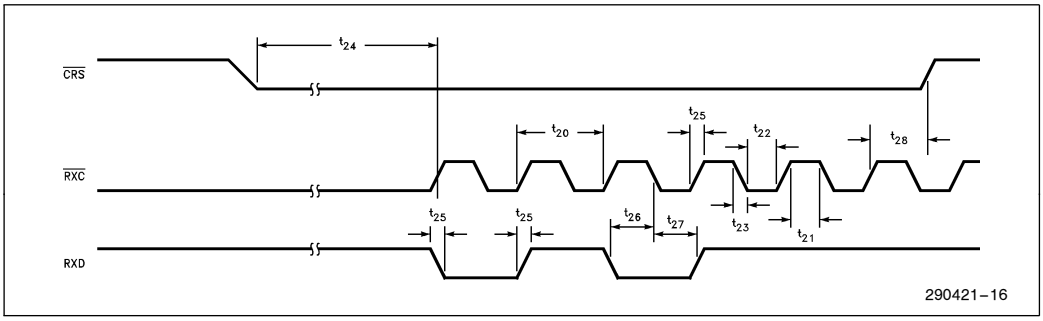

Figure 17. Receive Timing (Intel)

Controller Interface Timings (National Mode)

TRANSMIT TIMINGS (National)

Symbol	Parameter	Min	Typ	Max	Units
t_{30}	TXC Cycle Time(16)	99.99		100.01	ns
t_{31}	TXC High/Low Time	40	50		ns
t_{32}	TXC Rise/Fall Time at 20% to 80%			5	ns
t_{33}	TXD Setup Time to TXC ↑	20			ns
t_{34}	TXD Hold Time from TXC ↑	0			ns
t_{35}	TXE Setup Time to TXC ↑	20			ns
t_{36}	TXE Hold Time from TXC ↑	0			ns

NOTE:
16. All delay and width measurements on TxC are made at 1.5V.

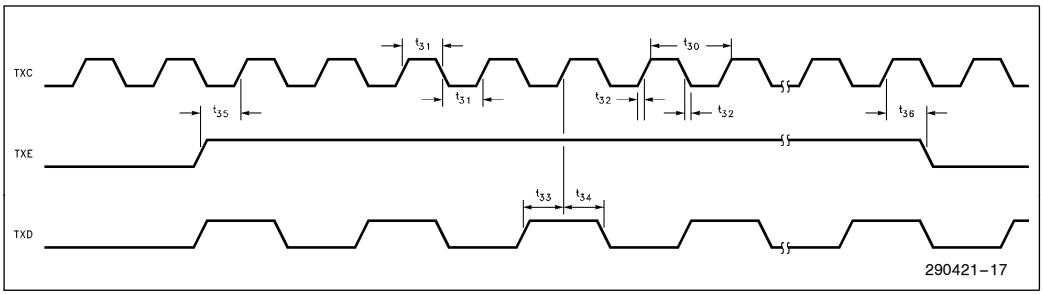

Figure 18. Transmit Timing (National)

RECEIVE TIMINGS (National)

Symbol	Parameter	Min	Typ	Max	Units
t_{40}	RxC Cycle Time	96	100		ns
t_{41}	RxC High/Low Time[17]	40	50	60	ns
t_{42}	RxC Rise/Fall Time at 20% to 80%			5	ns
t_{43}	RXD Rise/Fall Time at 20% to 80%			5	ns
t_{44}	RXD Setup Time to RxC ↑	30			ns
t_{45}	RXD Hold Time from RxC ↑	20			ns
t_{46}	RxC Delay from CRS ↑			1400	ns
t_{47}	RxC Continuing Beyond CRS ↓			5	cycles

NOTE:
17. All delay and width measurements on RXC are made at 1.5V.

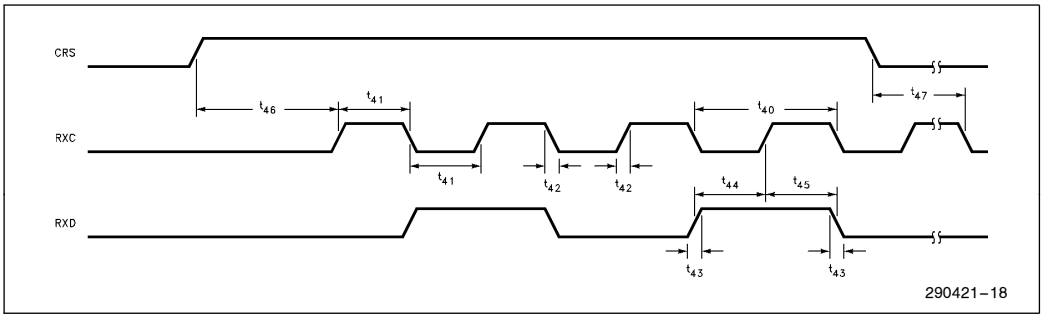

Figure 19. Receiving Timings (National)

Controller Interface Timing (AMD Mode)

TRANSMIT TIMINGS[18] (AMD)

Symbol	Parameter	Min	Typ	Max	Units
t_{50}	TCLK Cycle Time	99.99		100.01	ns
t_{51}	TCLK High Time (@ 0.8V to 2.0V)	45	50	58	ns
t_{52}	TCLK Low Time (@ 2.0V to 0.8V)	45	50	58	ns
t_{53}	TCLK Rise/Fall Time (@ 0.8V to 2.0V)		2.5	5	ns
t_{54}	TX Setup Time to TCLK ↑	20			ns
t_{55}	TX Hold Time from TCLK ↑	5			ns
t_{56}	TENA Setup Time to TCLK ↑	20			ns
t_{57}	TENA Hold Time from TCLK ↑	5			ns

NOTE:
18. Delay times for TX, TENA, and TCLK are measured from 0.8V for falling edges, and 2.0V for rising edges.

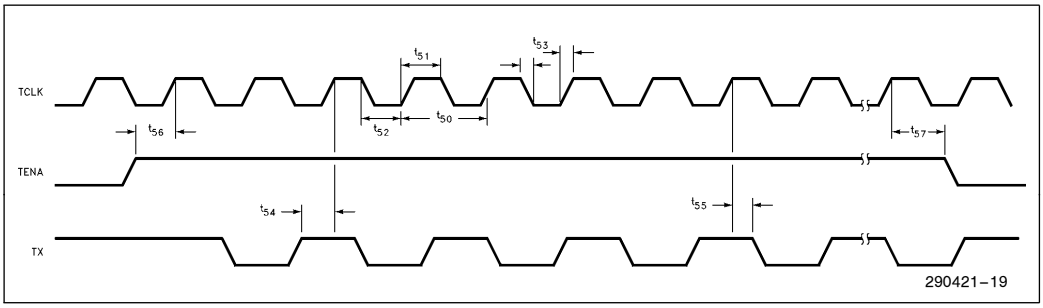

Figure 20. Transmit Timings (AMD)

RECEIVE TIMINGS[19] (AMD)

Symbol	Parameter	Min	Typ	Max	Units
t_{60}	RCLK Cycle Time	96	100		ns
t_{61}	RCLK High Time (@ 0.8V to 2.0V)	38	50		ns
t_{62}	RCLK Low Time (@ 2.0V to 0.8V)	38	50		ns
t_{63}	RCLK Rise/Fall Time (@ 0.8V to 2.0V)		2.5	5	ns
t_{64}	RX Rise/Fall Time (@ 0.8V to 2.0V)		2.5	5	ns
t_{65}	RX Hold time from RCLK ↑	10			ns
t_{66}	RX Setup Time to RCLK ↑	45			ns
t_{67}	RENA Deassertion Hold Time from RCLK ↑	40	50	80	ns
t_{68}	RCLK Delay from RENA ↑			450	ns

NOTE:
19. Delay times for RX, RENA, and RCLK are measured from 0.8V for falling edges and 2.0V for rising edges.

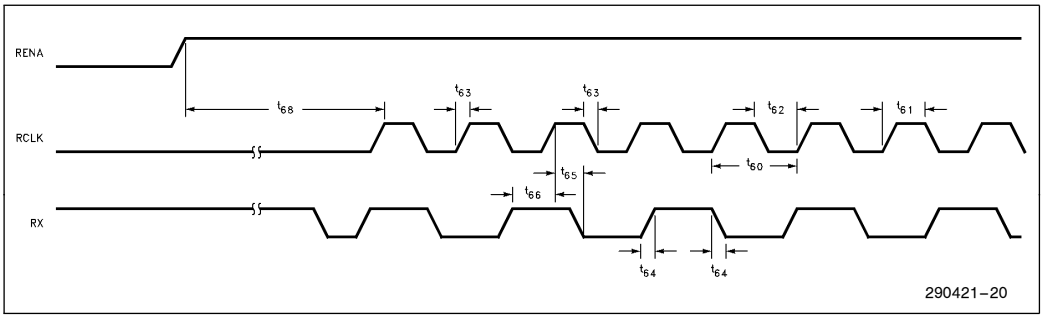

Figure 21. Receive Timings (AMD—Start of Frame)

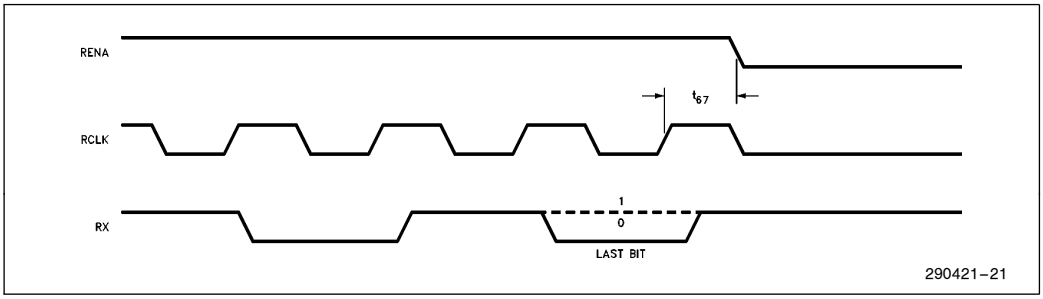

Figure 22. Receive Timings (AMD—End of Frame)

Controller Interface Timings (Fujitsu Mode)

TRANSMIT TIMINGS (Fujitsu)

Symbol	Parameter	Min	Typ	Max	Units
t_{70}	TCKN Cycle Time	99.99		100.01	ns
t_{71}	TCKN High/Low Time(20)	40	50		ns
t_{72}	TCKN Rise/Fall Time at 20% to 80%			5	ns
t_{73}	TXD Setup Time to TCKN ↓ (20)	20			ns
t_{74}	TXD Hold Time from TCKN ↓ (20)	0			ns
t_{75}	TEN Setup Time to TCKN ↓ (20)	20			ns
t_{76}	TEN Hold Time from TCKN ↓ (20)	0			ns

NOTE:
20. Timing measurements are referenced at 1.5V level.

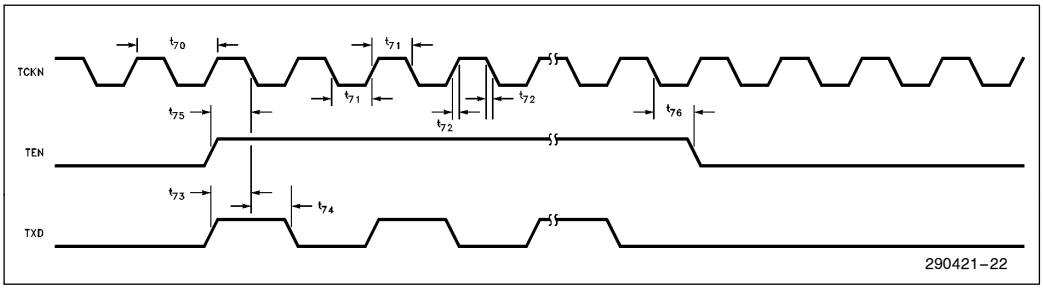

Figure 23. Transmit Timings (Fujitsu)

RECEIVE TIMINGS (Fujitsu)

Symbol	Parameter	Min	Typ	Max	Units
t_{80}	RCKN Cycle Time	96	100		ns
t_{81}	RCKN High/Low Time(21)	35	50	60	ns
t_{82}	RCKN Rise/Fall Time at 20% to 80%			5	ns
t_{83}	RXD Setup Time from RCKN ↓ (21)	20			ns
t_{84}	RXD Hold Time from RCKN ↓ (21)	10			ns
t_{85}	XCD Assertion Hold Time from RCKN ↓ (21)	0	10		ns
t_{86}	XCD Deassertion Hold Time from RCKN ↓ (21)		120		ns
t_{87}	XCD Deassertion Setup Time from RCKN ↓ (21)		80	130	ns
t_{88}	RCKN Delay from XCD ↑ (21)			1400	ns

NOTE:
21. Timing measurements are referenced at 1.5V.

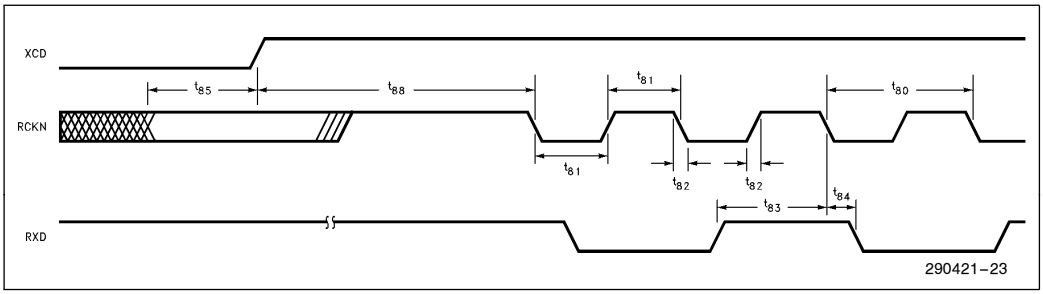

Figure 24. Receive Timings (Fujitsu—Start of Frame)

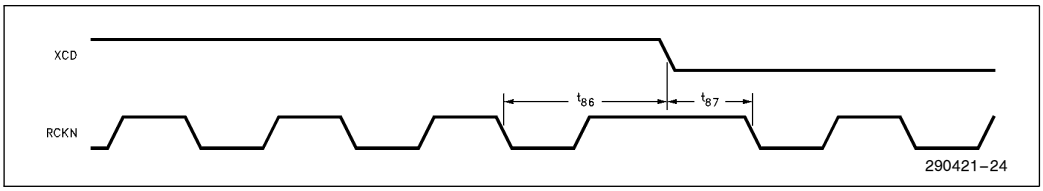

Figure 25. Receive Timings (Fujitsu—End of Frame)

TPE Timings

TPE TRANSMIT TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{90}	TxD to TD Bit Loss at Start of Packet			2	bits
t_{91}	TxD to TD Steady State Propagation Delay			400	ns
t_{92}	TxD to TD Startup Delay			600	ns
t_{93}	TDH and TDL Pairs Edge Skew (@ $V_{CC}/2$)		1.5	3	ns
t_{94}	TDH and TDL Pairs Rise/Fall Times (@ 0.5V to V_{CC} − 0.5V)		2	5	ns
t_{95}	TDH and TDL Pairs Bit Cell Center to Center	99	100	101	ns
t_{96}	TDH and TDL Pairs Bit Cell Center to Boundary	49	50	51	ns
t_{97}	TDH and TDL Pairs Return to Zero from Last TDH ↑	250		400	ns
t_{98}	Link Test Pulse Width	98	100	102	ns
t_{99}	Last TD Activity to Link Test Pulse	8	13	24	ms
t_{100}	Link Test Pulse to Data Separation	190	200		ns

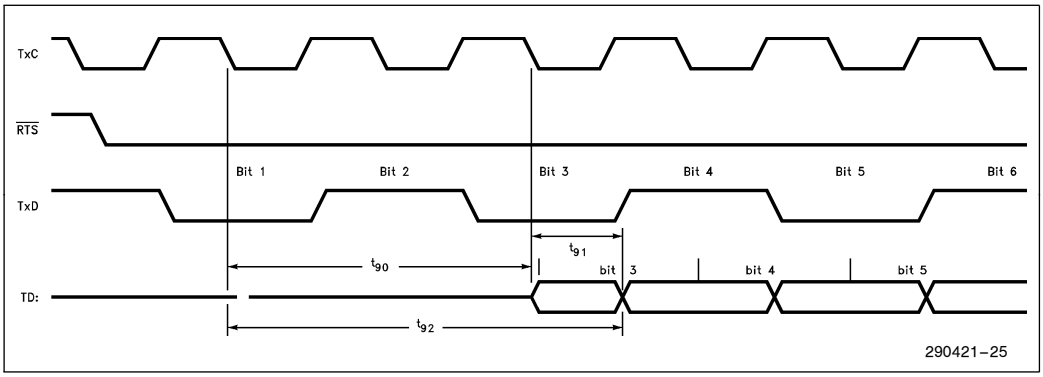

Figure 26. TPE Transmit Timings (Start of Frame)

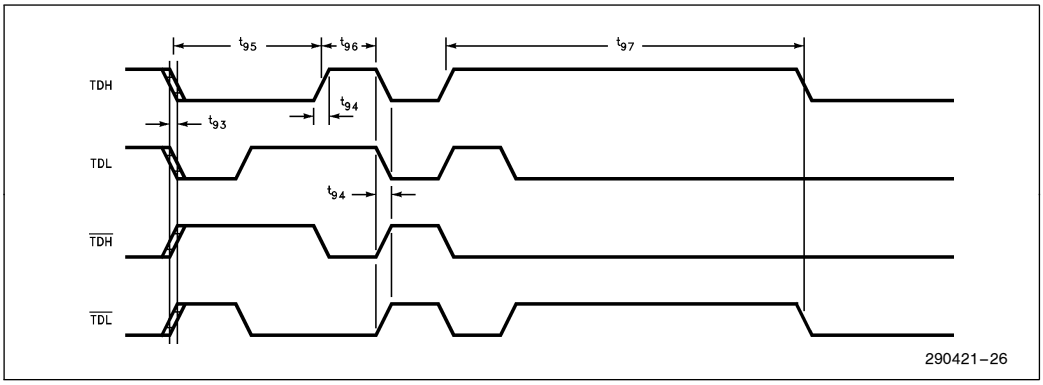

Figure 27. TPE Transmit Timings (End of Frame)

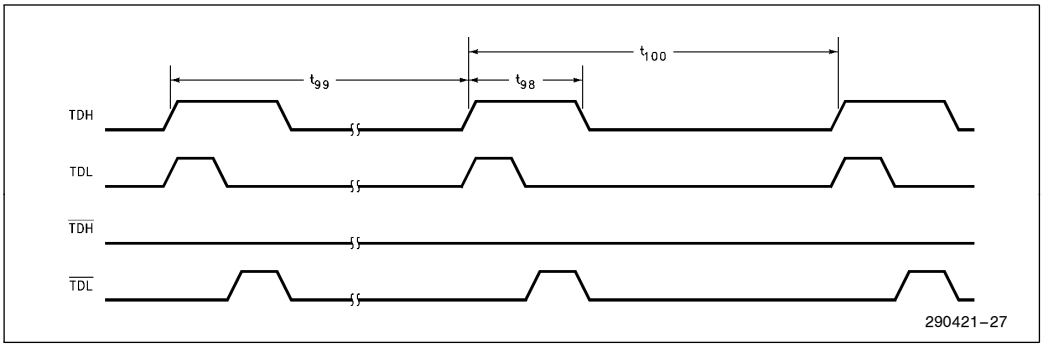

Figure 28. TPE Transmit Timings (Link Test Pulse)

TPE RECEIVE TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{105}	RD to RxD Bit Loss at Start of Packet	4		19	bits
t_{106}	RD to RxD Invalid Bits Allowed at Start of Packet			1	bits
t_{107}	RD to RxD Steady State Propagation Delay			400	ns
t_{108}	RD to RxD Start UP Delay			2.4	μs
t_{109}	RD Pair Bit Cell Center Jitter			$\pm$13.5	ns
t_{110}	RD Pair Bit Cell Boundary Jitter			$\pm$13.5	ns
t_{111}	RD Pair Held High from Last Valid Positive Transition	230		400	ns
t_{112}	$\overline{CRS}$ Assertion Delay (Intel, NS, and Fuji Mode) (AMD Mode)			700 1500	ns ns
t_{113}	$\overline{CRS}$ Deassertion Delay			450	ns

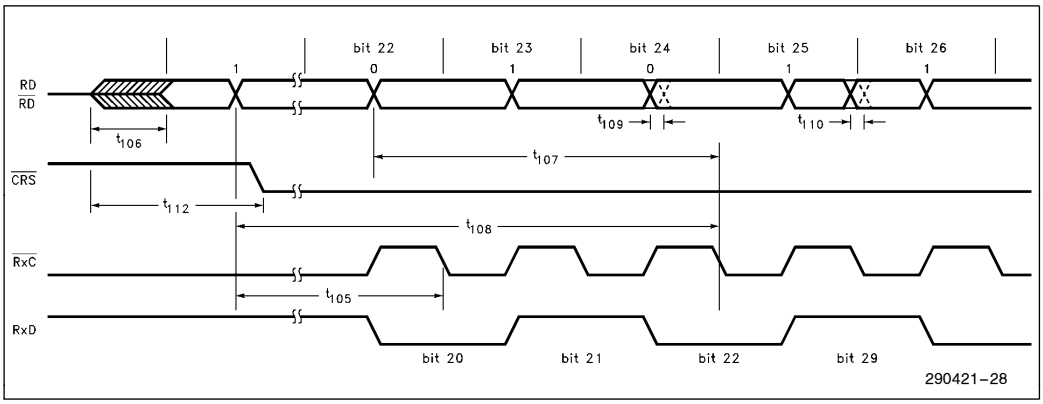

Figure 29. TPE Receive Timings (Start of Frame)

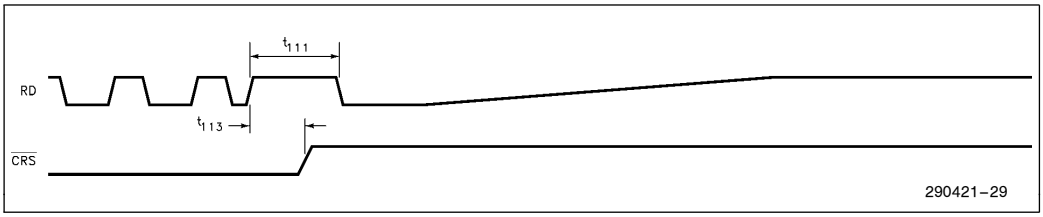

Figure 30. TPE Receive Timings (End of Frame)

TPE COLLISION TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{115}	Onset of Collision (RD Pair and $\overline{RTS}$ Active) to $\overline{CDT}$ Assert			900	ns
t_{116}	End of Collision (RD Pair or $\overline{RTS}$ Inactive) to $\overline{CDT}$ Deassert			900	ns
t_{117}	$\overline{CDT}$ Assert to RxD Sourced from RD Pair			900	ns
t_{118}	$\overline{CDT}$ Deassert (RD Pair Inactive) to RxD Sourced from TxD			900	ns

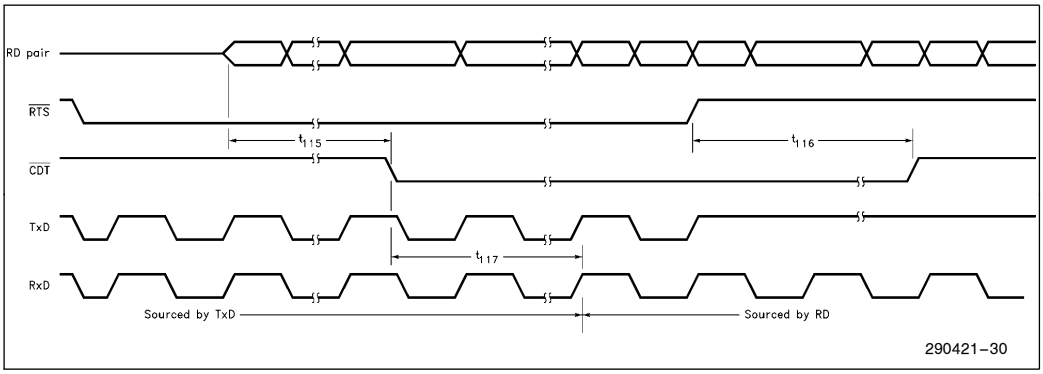

Figure 31. TPE Collision Timings (Start of Collision)

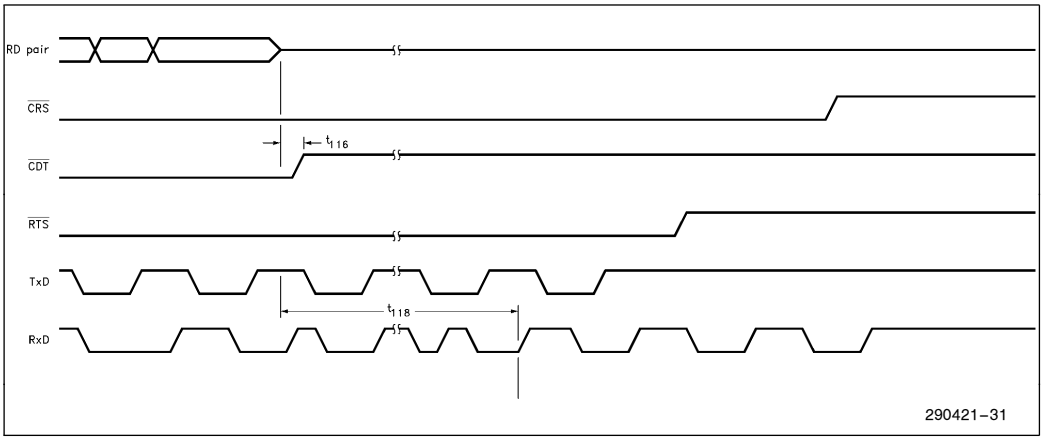

Figure 32. TPE Collision Timings (End of Collision)

TPE LINK INTEGRITY TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{120}	Last RD Activity to Link Fault (Link Loss Timer)	50	100	150	ms
t_{121}	Minimum Received Linkbeat Separation(20)	2	5	7	ms
t_{122}	Maximum Received Linkbeat Separation(21)	25	50	150	ms

NOTES:
20. Linkbeats closer in time to this value are considered noise, and are rejected.
21. Linkbeats further apart in time than this value are not considered consecutive, and are rejected.

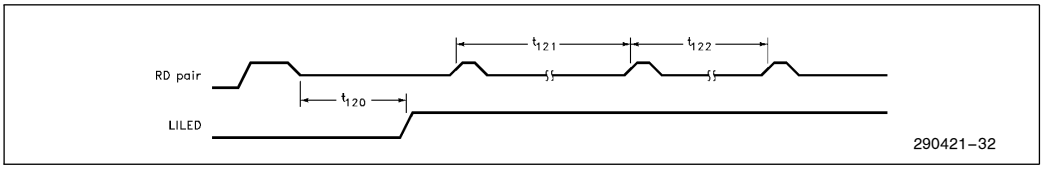

Figure 33. TPE Link Integrity Timings

AUI Timings

AUI TRANSMIT TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{125}	TxD to TRMT Pair Steady State Propagation Delay			200	ns
t_{126}	TRMT Pair Rise/Fall Times		3	5	ns
t_{127}	Bit Cell Center to Bit Cell Center of TRMT Pair	99.5	100	100.5	ns
t_{128}	Bit Cell Center to Bit Cell Boundary of TRMT Pair	49.5	50	50.5	ns
t_{129}	TRMT Pair Held at Positive Differential at Start of Idle	200			ns
t_{130}	TRMT Pair Return to $\leq$ 40 mV from Last Positive Transition			8.0	μs

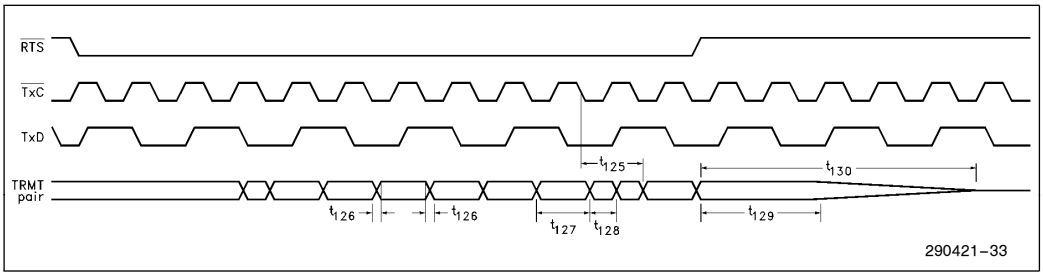

Figure 34. AUI Transmit Timings

AUI RECEIVE TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{135}	RCV Pair Rise/Fall Times			10	ns
t_{136}	RCV Pair Bit Cell Center Jitter in Preamble			$\pm$12	ns
t_{137}	RCV Pair Bit Cell Center/Boundary Jitter in Data			$\pm$18	ns
t_{138}	RCV Pair Idle Time after Transmission	8			μs
t_{139}	RCV Pair Return to Zero from Last Positive Transition	160			ns
t_{140}	$\overline{CRS}$ Assertion Delay (Intel, National, Fujitsu Modes) (AMD Mode)			100 1050	ns ns
t_{141}	$\overline{CRS}$ Deassertion Delay			350	ns
t_{142}	$\overline{CRS}$ Inhibited after Frame Transmission	4	4.3	5	μs

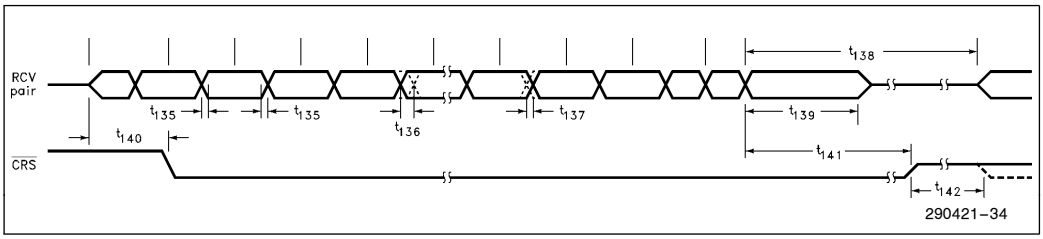

Figure 35. AUI Receive Timings

AUI COLLISION TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{145}	CLSN Pair Cycle Time	80		118	ns
t_{146}	CLSN Pair Rise/Fall Times			10	ns
t_{147}	CLSN Pair Return to Zero from Last Positive Transition	160			ns
t_{148}	CLSN Pair High/Low Times	35		70	ns
t_{149}	$\overline{CDT}$ Assertion Time			75	ns
t_{150}	$\overline{CDT}$ Deassertion Time			300	ns
t_{151}	$\overline{CRS}$ Deassertion Time (Intel Mode Only, RCV Pair Idle)			450	ns

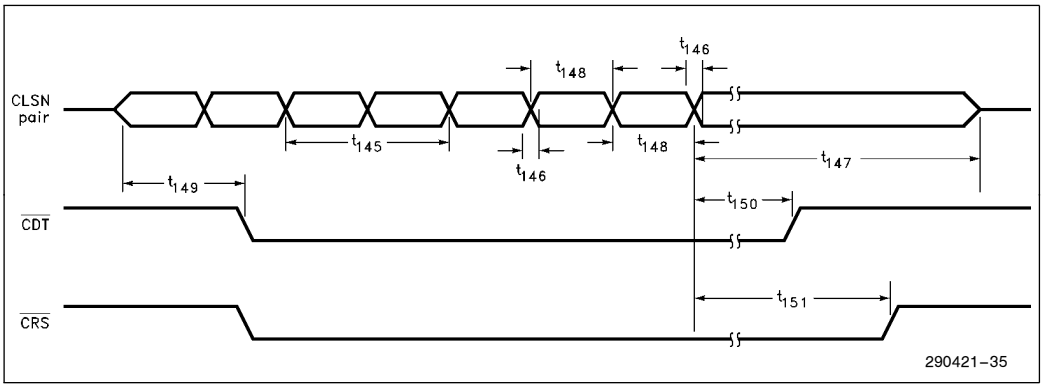

Figure 36. AUI Collision Timings

AUI NOISE FILTER TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{152}	RCV Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns
t_{153}	CLSN Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns

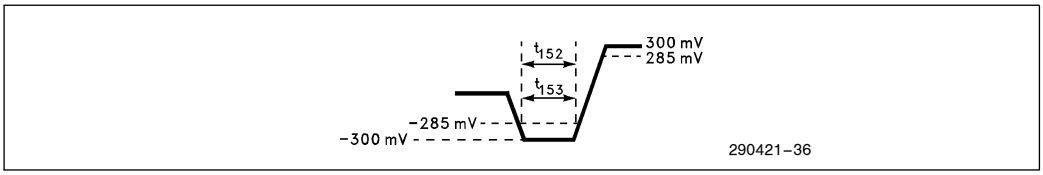

Figure 37. AUI Noise Filter Timings

LOOPBACK TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{155}	TxD to RxD Bit Loss at Start of Packet			16	bits
t_{156}	TxD to RxD Steady State Propagation Delay			600	ns
t_{157}	TxD to RxD Startup Delay			2.2	μs
t_{158}	SQE Test Wait Time	0.6	1.2	1.6	μs
t_{159}	SQE Test Duration	0.5	0.8	1.5	μs
t_{160}	$\overline{\text{LPBK}}$ Setup/Hold Times to $\overline{\text{RTS}}$(22)	1.0			μs

NOTE:
22. Guarantees proper processing of transmitted packets. Violation of this specification will not result in spurious data transmission. Incoming data packets occuring during transitions on $\overline{\text{LPBK}}$ will not be accepted.

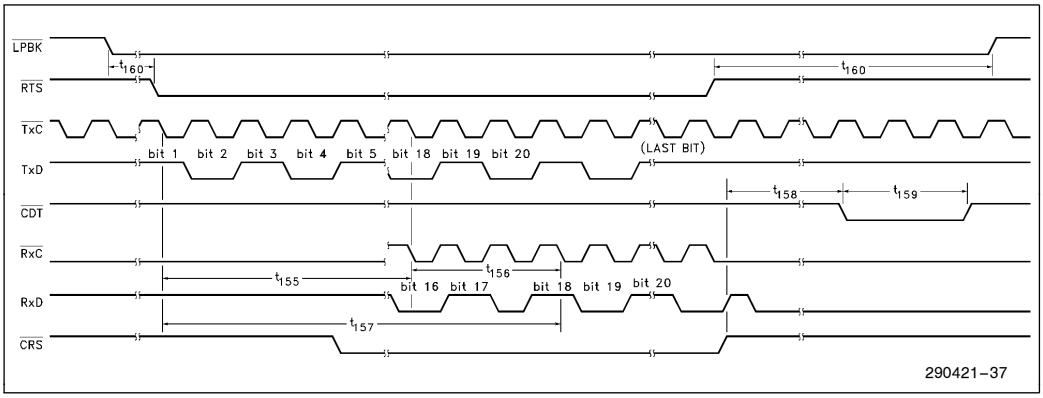

Figure 38. Loopback Timings

JABBER TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{165}	Maximum Length Transmission before Jabber Fault (TPE)	20	25	150	ms
t_{166}	Maximum Length Transmission before Jabber Fault (AUI)	10	13	18	ms
t_{167}	Minimum Idle Time to Clear Jabber Function	250	420	750	ms

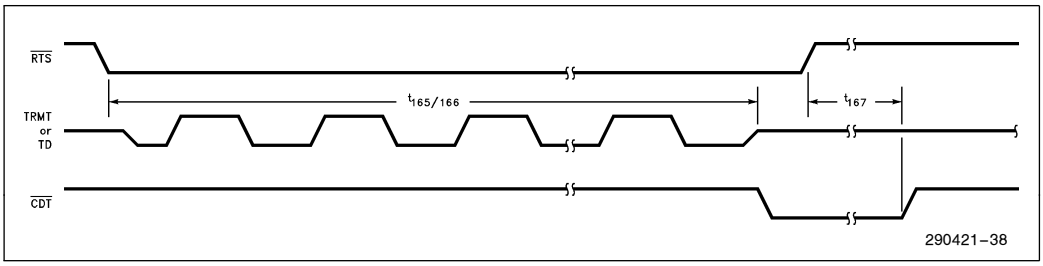

Figure 39. Jabber Timings

LED TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{170}	TxLED, RxLED, COLED On Time	50		450	ms
t_{171}	TxLED, RxLED, COLED Off Time	50			ms
t_{172}	LILED On Time	50			ms
t_{173}	LILED Off Time	100			ms

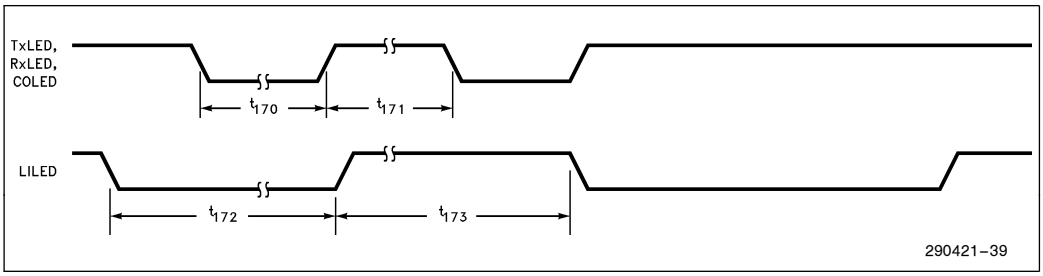

Figure 40. LED Timings

MODE TIMINGS(23, 24)

Symbol	Parameter	Min	Typ	Max	Units
t_{175}	Mode Pins Setup to $\overline{RTS}$ ↓	100			ms
t_{176}	Mode Pins Hold from $\overline{RTS}$ ↑	100			ms
t_{177}	Mode Pins Setup to RD Active(25)	100			ms
t_{178}	Mode Pins Hold from RD Active(25)	100			ms

NOTES:
23. Guarantees Proper processing of data packets. Violation of these specifications will not affect the integrity of the network.
24. Mode pins are: APORT, APOL/XSQ, LID, JABD, and TPE/$\overline{AUI}$.
25. Any data received within 100 ms of a mode transmission will be considered invalid.

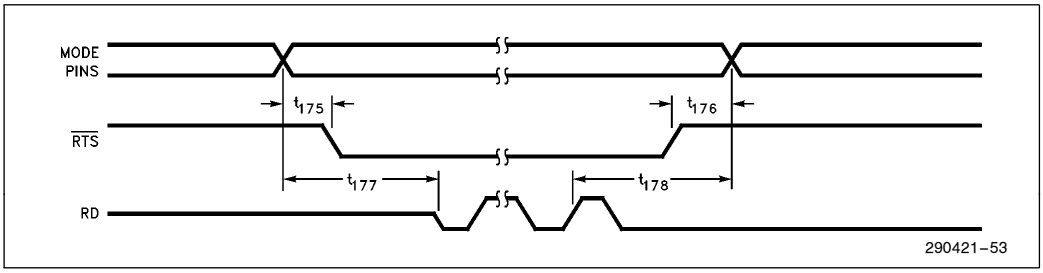

Figure 41. Mode Timings

RESET, TEST, AND LOW POWER MODE TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{180}	TEST and JABD Setup Time to RESET ↓	50			ns
t_{181}	RESET Pulse Width	300			ns
t_{182}	Low Power Mode Deactivation from TEST and JABD ↓			1	ms

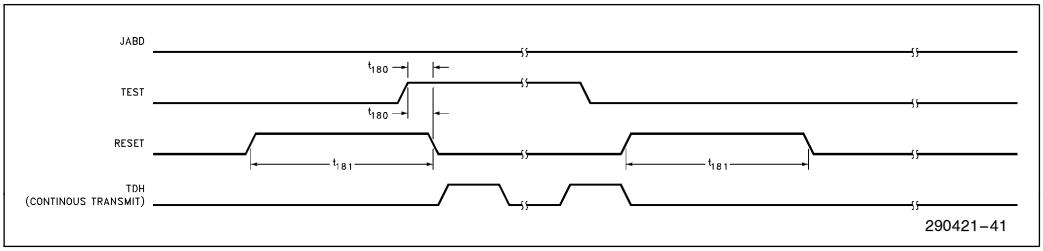

Figure 42. Reset Timings (Test Mode)

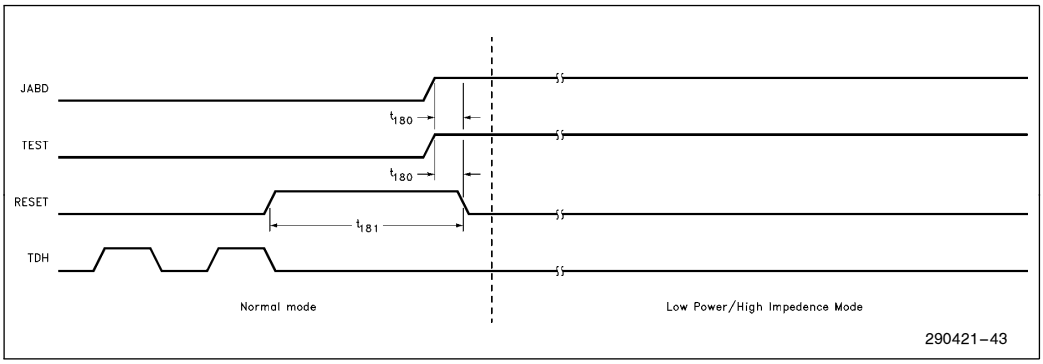

Figure 43. Reset Timings (Start of Low Power Mode)

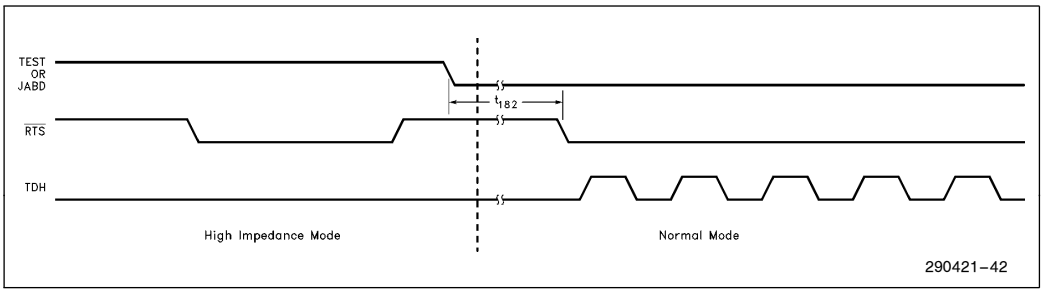

Figure 44. Reset Timings (End of Low Power Mode)

PACKAGE DIMENSIONS

PLASTIC LEADED CHIP CARRIER

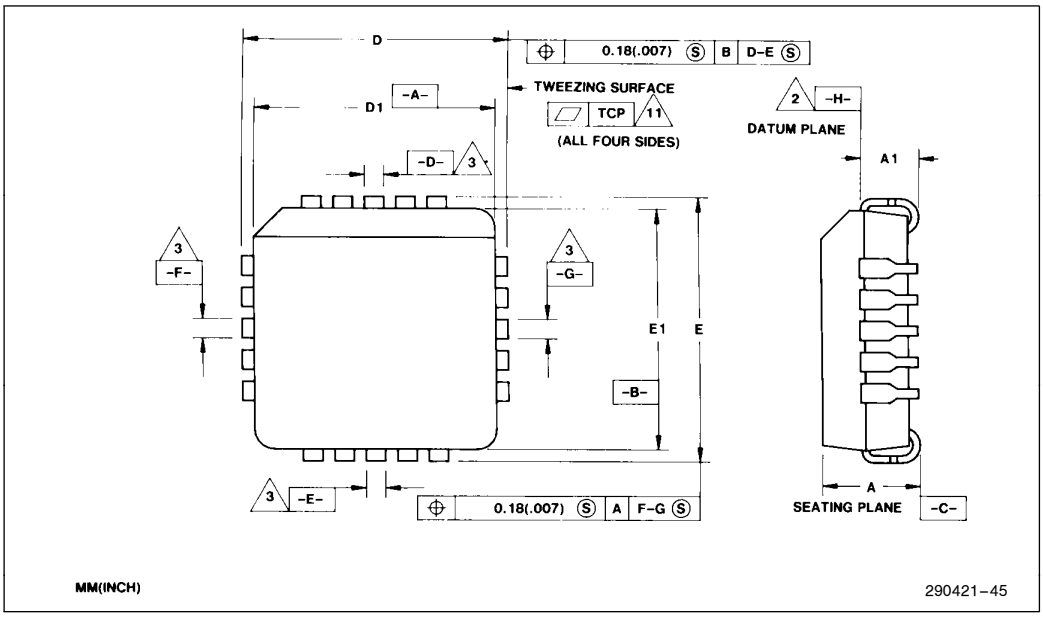

Figure 45. Principle Dimensions and Data

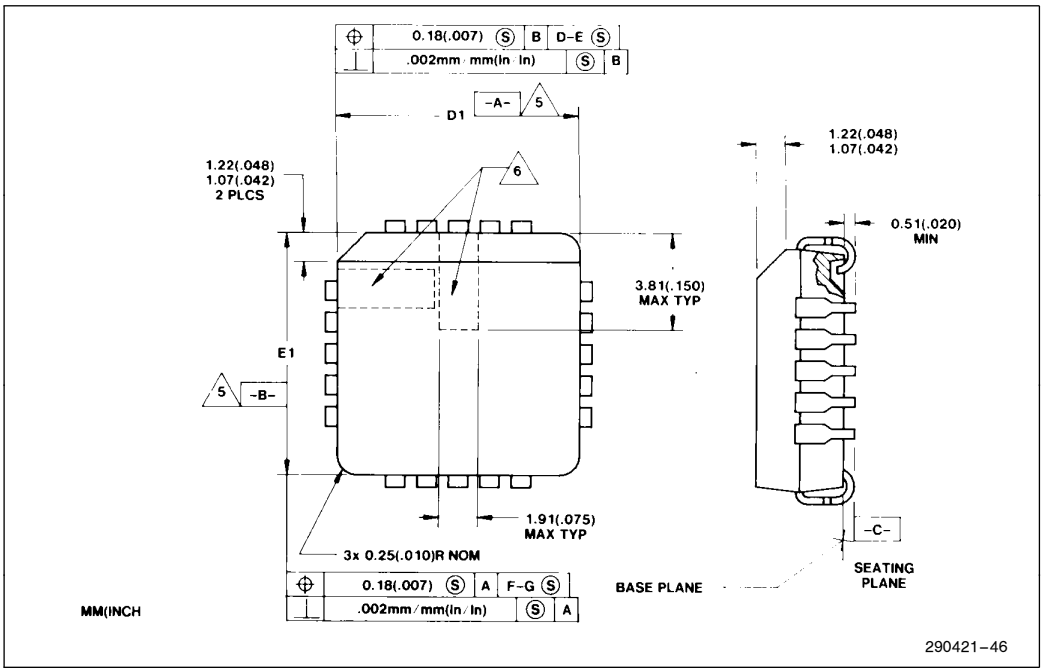

Figure 46. Molded Details

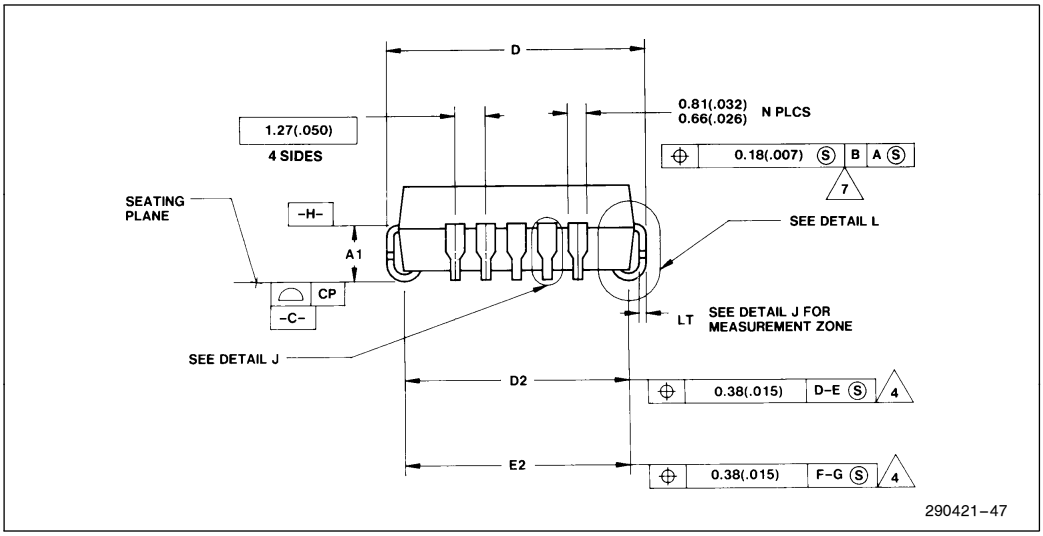

Figure 47. Terminal Details

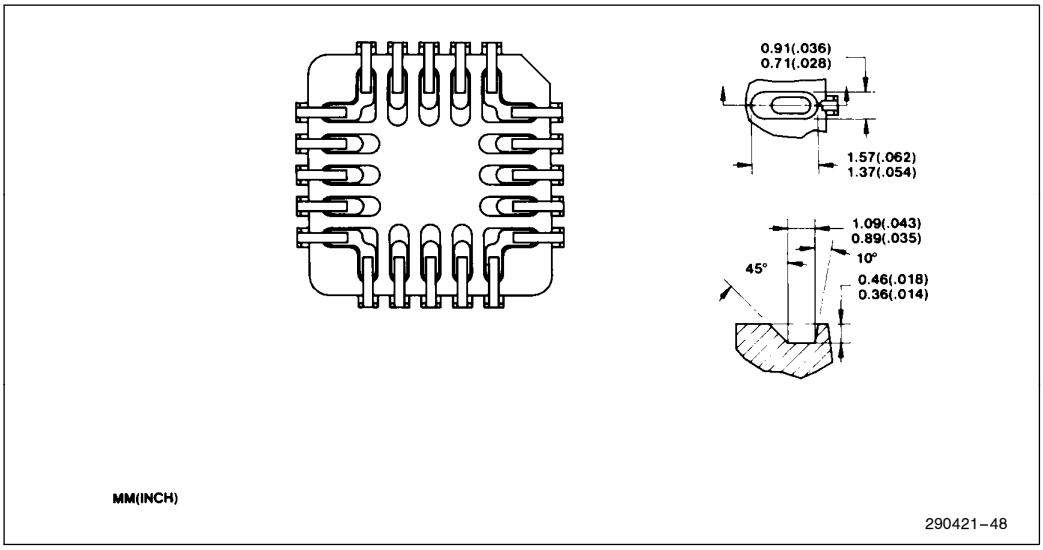

Figure 48. Standard Package Bottom View (Tooling Option 1)

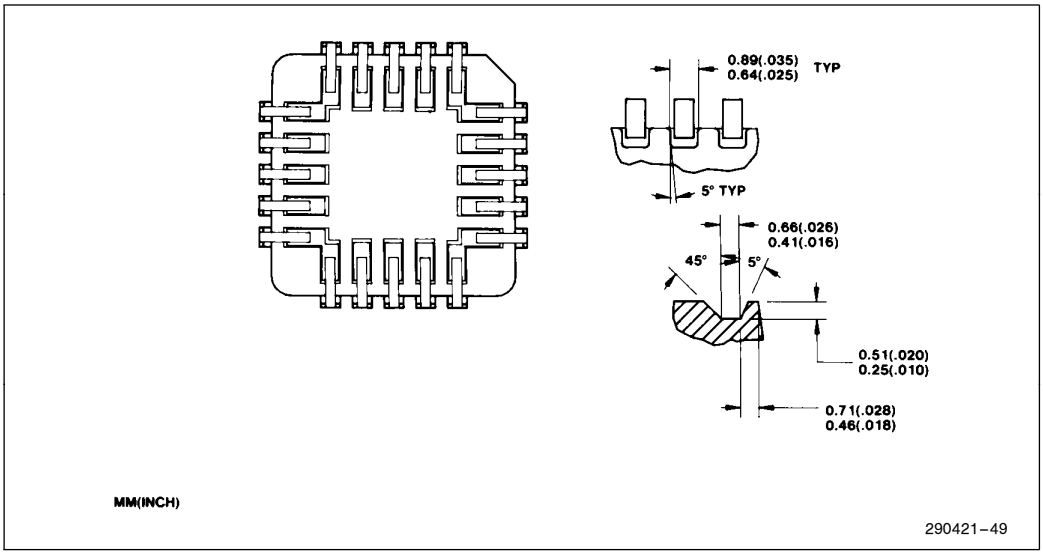

Figure 49. Standard Package Bottom View (Tooling Option II)

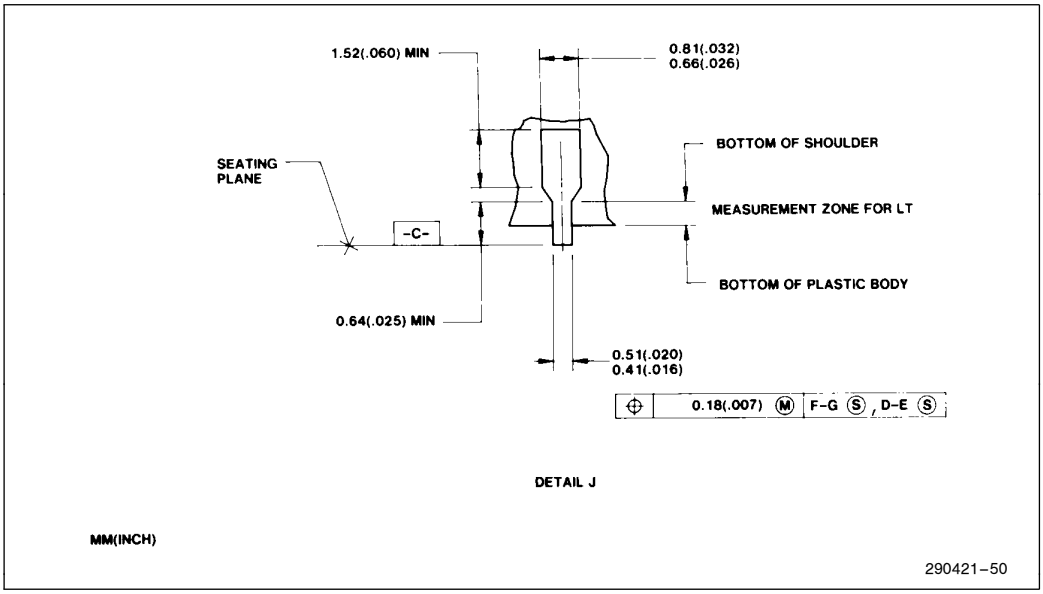

Figure 50. Detail J. Terminal Detail

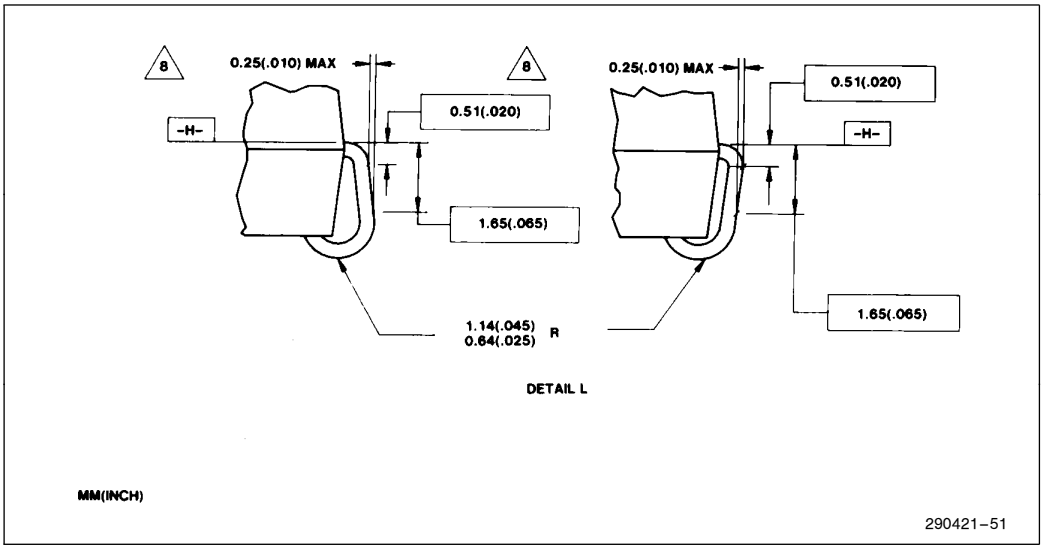

Figure 51. Detail L. Terminal Details

NOTES:
The above diagrams use a 20-lead PLCC package to show symbols for package dimensions. The table below indicates dimensions in mm that are specific to the 44-lead PLCC package.
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **—H—** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Datums **D–E** and **F–G** to be determined where center leads exit plastic body at datum plane **—H—**.
4. To be determined at seating plane **—C—**.
5. Dimensions D_1 and E_1 do not include mold protrusion.
6. Pin 1 identifier is located within one of the two defined zones.
7. Locations to datum **—A—** and **—B—** to be determined at plane **—H—**.
8. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
9. Controlling dimension, inch.
10. All dimensions and tolerances include lead trim offset and lead plating finish.
11. Tweezing surface planarity is defined as the furthest any lead on a side may be from the datum. The datum is established by touching the outermost lead on that side and parallel to **D–E** or **F–G**.

Symbol	Description	Min	Max
A	Overall Height	4.19	4.57
A_1	Distance from Lead Shoulder to Seating Plane	2.29	3.05
D	Overall Package Dimension	17.4	17.7
D_1	Plastic Body Dimension	16.5	16.7
D_2	Foot Print	15.0	16.0
E	Overall Package Dimension	17.4	17.7
E_1	Plastic Body Dimension	16.5	16.7
E_2	Foot Print	15.0	16.0
CP	Seating Plans Coplanarity	0.00	0.10
TCP	Tweezing Coplanarity	0.00	0.10
LT	Lead Thickness	0.23	0.38

44-LEAD QUAD FLATPACK PACKAGE

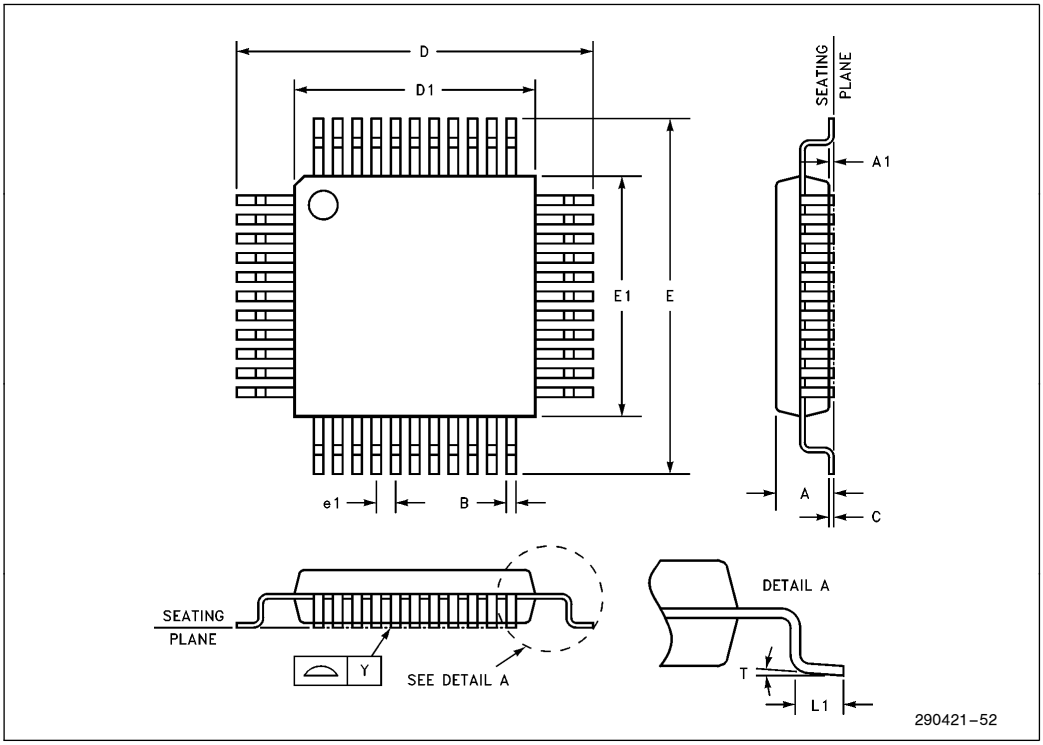

Figure 52. 44-Lead Quad Flatpack Package

Symbol	Description	Min	Nom	Max
A	Package Height			2.35
A1	Stand Off	0		0.60
B	Lead Width	0.2	0.3	0.4
C	Lead Thickness	0.1	0.15	0.2
D_1	Package Body		10	
E_1	Package Body		10	
e_1	Lead Pitch	0.65	0.8	0.95
D	Terminal Dimension	12.0	12.4	12.8
E	Terminal Dimension	12	12.4	12.8
L_1	Foot Length	0.38	0.58	0.78
Y	Coplanarity			0.1
T	Lead Angle	0		10°

NOTE:
Unless otherwise specified, all units are in millimeters.