
REALTEK FLAT PANEL DISPLAY CONTROLLER RTD2010

Product Brief

This document contains introductory information pertaining to the Realtek RTD2010 Flat Panel Display Controller. Because proprietary and confidential information is contained in the complete specifications, this brief is offered to those interested in the chip. For a more detailed description of the device, please contact your Realtek sales representative.

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1. Features

General

- Integrated Spread-Spectrum DCLK PLL
- Integrated 8-bit triple-channel 110MHz ADC/PLL
- Integrated programmable timing controller
- Integrated microcontroller compatible with the standard 8032
- 24 General-purpose input/outputs (GPIOs)
- Embedded fully functional multi-language OSD support
- Embedded DDC supports DDC1, DDC2B, and DDC/CI
- Supports ISP functionality on DDC channel
- 3 Embedded programmable PWM
- Zoom scaling up and down
- Embedded Pattern Generator
- No external memory required
- Requires only one crystal to generate all timing

Analog RGB Input Interface

- Supports up to 110MHz (XGA @ 75Hz)
- Supports Sync On Green (SOG) and de-composite sync modes
- On-chip high-performance PLLs

Digital Input Interface

- Supports 24-bit pixel digital input up to 160MHz
- Supports 12-bit DVO input
- Supports 16/24-bit YUV422/444 video format input
- Supports 8-bit video format input
- Built-in YUV to RGB color space converter & de-interlace
- Capture window auto position & auto phase tracking capability

Auto Detection /Auto Calibration

- Input format detection
- Compatibility with standard VESA mode and support for user-defined mode
- Smart engine for Phase and Image position calibration

Scaling

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement

Color Processor

- Digital brightness and contrast adjustments
- Gamma correction
- Dithering logic for 18-bit panel color depth enhancement

Output Interface

- Fully programmable, built-in display timing generator
- 1 and 2-pixel/clock panel support, up to 110MHz
- Pin swap, odd/even swap and red/blue group swap
- Programmable TCON function support
- Reduced EMI and Power saving features

Host Interface

- Supports 3/4 pins MCU serial bus interface
- Support parallel bus interface while using internal MCU

Embedded OSD

- 12*18 dot font per character
- Embedded 256 characters and symbols including 16 multi-color symbols
- User font RAM, which allows programming of 128 special symbols
- 7 background colors and 8 character colors
- Programmable width and height control
- 4 background windows
- Selectable shadow color for windows and characters
- Intensity, blinking effects
- Fade-in/out effect
- Frame shadowing and independent row shadowing
- Frame bordering and independent row bordering
- 4 channel 8-bits PWM output, and selectable PWM clock frequency
- Row-to-Row spacing to maintain constant display height
- Window alpha-blending effect

Power & Technology

- 2.5V/3.3V power supply
- 0.25µm CMOS process; 208-pin PQFP package

2. General Description

The Realtek RTD2010 is a highly-integrated single chip IC controller solution for producing real time, top quality digital video and computer graphic images on LCD monitor/flat panel displays, such as XGA LCD monitors. LCD monitors and flat panel displays provide a sharp, flicker free display while saving space and energy for desktop PC applications. The RTD2010 provides an ideal interface between industry standard digital graphics controllers and a wide variety of LCD panel devices. Flat panel devices using the RTD2010 can support all incoming VESA modes and interface to any TFT LCD device, up to XGA (1024x768) resolution.

For increased flexibility, the RTD2010 supports both analog and digital interface inputs. The embedded 8-bit triple-channel 110MHz high-quality Analog to Digital Converter (ADC) and PLL support up to a 1024x768 75Hz RGB analog input signal. The digital interface can support Transmission Minimized Differential Signaling (TMDS) receiver or Video-Decoder or DVO digital output signals up to 160MHz.

The RTD2010 features an embedded On-Screen Display (OSD) engine. This OSD enables either character based or bit map based menu display. Through this menu, display parameters, such as brightness and contrast, can be controlled, and information on resolution and frequency, can be displayed. The embedded display pattern generator is a function for panel testing.

Processing 24-bit RGB or 16-bit YUV input data streams, and conversion of input VGA signals to high resolution output, the RTD2010 implements a sophisticated scaling algorithm. This feature allows the RTD2010 to perform horizontal and vertical interpolation or replication and up & down image scaling, based on programmable parameters, to create images of the highest quality.

The built-in advanced filtering engine enables independent vertical and horizontal zoom/shrink, and, through enhancement of individual pixels, enhances image sharpness, and provides superb visual quality. This allows appropriate sized display of crisp, sharp text and smooth, clear graphics, taking full advantage of LCD flat panel technology.

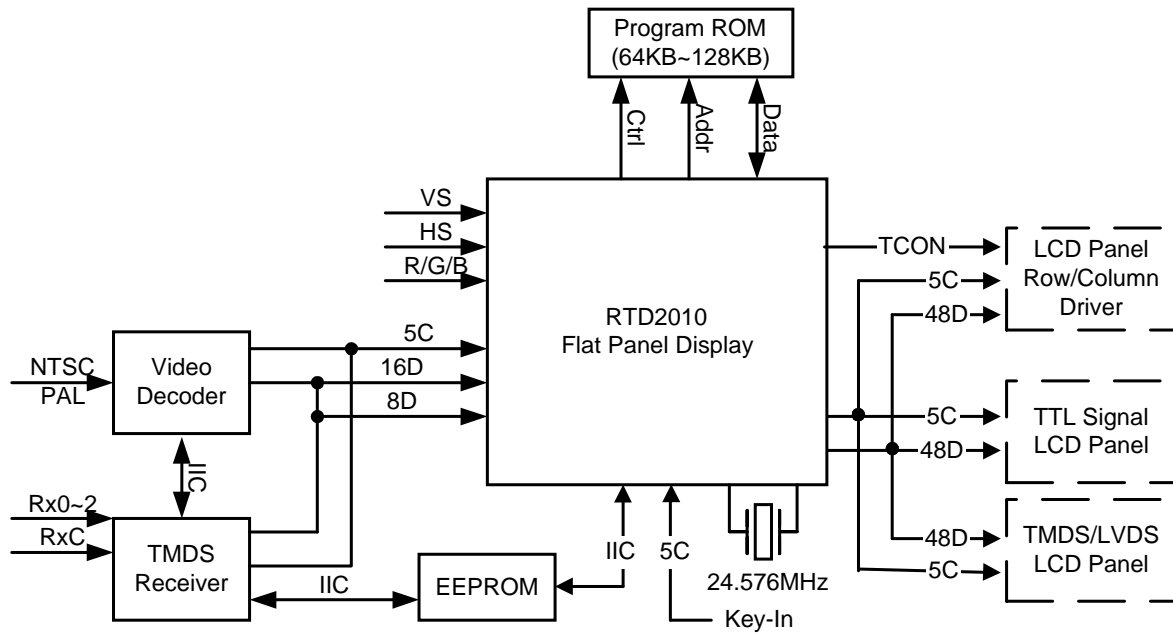
Also featured are enhanced color processing functions, including gamma correction and dithering logic. Brightness, contrast and gamma correction can be programmed through the internal gamma correction lookup tables. Full control of output panel data is obtained by color mapping input RGB data. The 8-bit/color pixel path offers up to 16.7 million color support for 24-bit TFT LCD panels. 18-bit LCD panels are also supported through spatial and temporal dither algorithms.

Increased integration in the RTD2010 includes components such as an 8032 compatible micro controller, and DDC RAM to provide monitor information the PC through the DDC1/DDC2B protocol. Internal System Programming (ISP) is accomplished through the DDC serial bus, supporting enhanced DDC-communication from PC to monitor, such as DDC/CI is also supported.

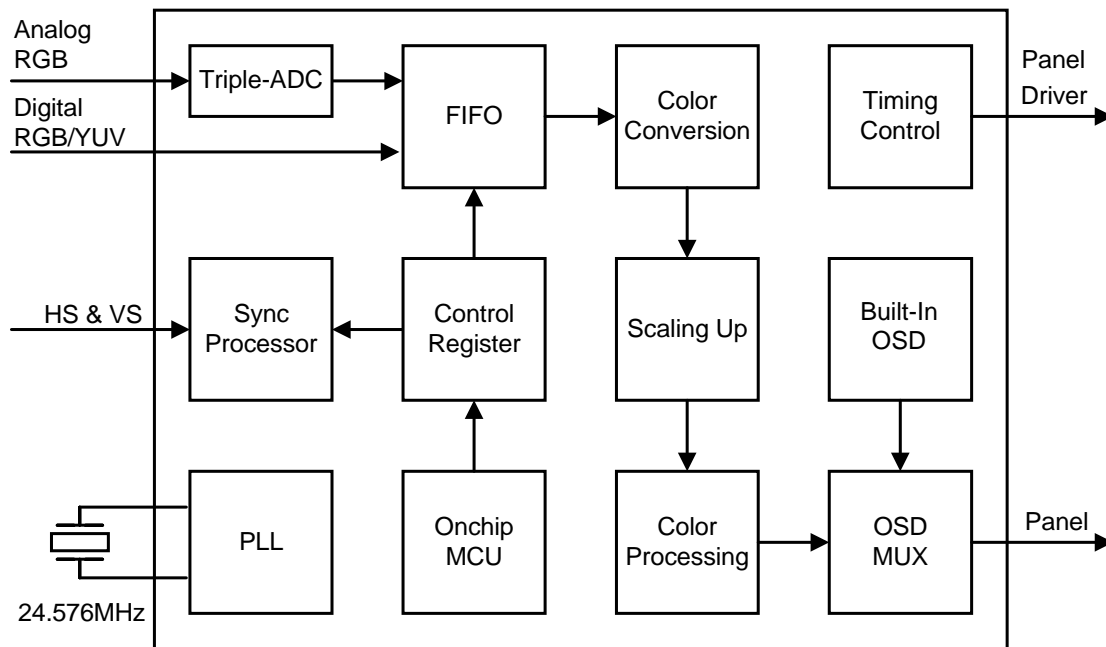
Finally, the Timing-Controller (TCON) generates the control signals for LCD-panel rather than LCD-monitor, and the embedded spread-spectrum technology reduces EMI effects.

All these features make the RTD2010 is the optimum solution for superior-quality image display.

3. Block Diagram



Application System Block Diagram

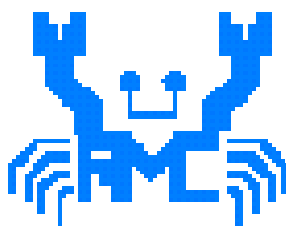


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Chip Functional Block Diagram

4. Pin Assignments

208	P.2.4/TCON15	156	VCC3IO
207	P.2.3/TCON14	155	EXT#
206	P.2.2/TCON13	154	ADC_VDD
205	P.2.1/TCON12	153	ADC_VDD
204	P.2.0/TCON11	152	R
203	P.1.7/TCON10	151	ADC_GND
202	P.1.6/TCON9	150	ADC_GND
201	GNDIK	149	ADC_GND
200	P.1.5/TCON8	148	G
199	P.1.4/TCON7	147	ADC_VDD
198	VCCK	146	ADC_VDD
197	BBLU0	145	B
196	BBLU1	144	ADC_GND
195	BBLU2	144	ADC_GND
194	BBLU3	143	ADC_TEST
193	BBLU4	142	ADC_VDD
192	BBLU5	141	ADC_VDD
191	BBLU6	140	ADC_REFIO
190	BBLU7	139	ADC_GND
189	BGRN0	138	ADC_GND
188	BGRN1	137	WE#/P0.4
187	BGRN2	136	ROM_ADDR_BANK
186	BGRN3	135	GNDIK
185	BGRN4	134	ROM_ADDR15
184	BGRN5	133	VCCK
183	GNDIK	132	ROM_ADDR14
182	BGRN6	131	ROM_ADDR13
181	BGRN7	130	ROM_ADDR12
180	VCCK	129	GNDIK
179	BRED0	128	ROM_ADDR11
178	BRED1	127	VCCK
177	BRED2	126	ROM_ADDR10
176	BRED3	125	GNDIO
175	BRED4	124	ROM_ADDR9
174	BRED5	123	ROM_ADDR8
173	BRED6	122	VCC3IO
172	BRED7	121	ROM_ADDR7
171	BCLK	120	ROM_ADDR6
170	BLE_N	119	ROM_ADDR5
169	BLE_S	118	ROM_ADDR4
168	BMS	117	ROM_ADDR3
167	VDD	116	ROM_ADDR2
166	PWM0	115	ROM_ADDR1
165	P.2.7/PWM2	114	ROM_ADDR0
164	P.2.6/PWM1	113	ROM_DATA0
163	P.3.3	112	ROM_DATA1
162	INT0#P3.2	111	ROM_DATA2
161	DDCSCL	110	ROM_DATA3
160	AUS	109	GNDIO
159	GNDIO	108	ROM_DATA4
158	GNDIO	107	ROM_DATA5
157	AHS	106	VCC3IO
		105	ROM_DATA6
209	P.2.5/TCON16	53	DAGR4
208	DBBLU0	54	DAGR6
207	DBBLU1	55	DAGR0
206	VCC3IO	56	DAGN0
205	DBBLU2	57	DARE0
204	GNDIO	58	DARE1
203	DBBLU3	59	DARE2
202	DBBLU4	60	DARE3
201	DBBLU5	61	DARE4
200	DBBLU6	62	DARE5
199	DBBLU7	63	DARE6
198	GNDIK	64	DARE7
197	VCCK	65	DEN/TCON4
196	DBGRN3	66	DVS/TCON5
195	VCC3IO	67	DHS/TCON6
194	DBGRN4	68	VCC3IO
193	GNDIO	69	DCLK/ECLK
192	DBGRN5	70	GNDIO
191	DBGRN6	71	P1.0/TCON1
190	DBGRN7	72	P1.1/TCON1
189	DBRED0	73	P1.2/TCON2
188	DBRED1	74	VCCK
187	DBRED2	75	P1.3/TCON3
186	DBRED3	76	GNDIK
185	DBRED4	77	T0#P3.4/ISCB
184	DBRED5	78	T1#P3.5/SCLK
183	DBRED6	79	P3.7/SIO1
182	DBRED7	80	P3.7/SIO0
181	BCLK	81	INT1#P3.1/IRQ#
180	BLE_N	82	P3.0/PWDN#
179	BLE_S	83	RESET#
178	BMS	84	PLL_VDD
177	VDD	85	PLL_GND
176	PWM0	86	PLL_GND
175	P.2.7/PWM2	87	PLL_GND
174	P.2.6/PWM1	88	PLL_GND
173	P.3.3	89	PLL_GND
172	INT0#P3.2	90	PLL_GND
171	DDCSCL	91	PLL_GND
170	AUS	92	PLL_GND
169	GNDIO	93	PLL_GND
168	GNDIO	94	PLL_GND
167	AHS	95	PLL_GND
166		96	PLL_GND
165		97	PLL_GND
164		98	PLL_GND
163		99	PLL_GND
162		100	PLL_GND
161		101	PLL_GND
160		102	PLL_GND
159		103	PLL_GND
158		104	PLL_GND
157		105	PLL_GND



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RTD2010

RTD2010 Pin-Out Diagram

5. Pin Descriptions

In order to reduce pin count, and therefore size and cost, some pins have multiple functions. In those cases, the functions are separated with a “/” symbol. Refer to the Pin Assignment diagram for a graphical representation.

A = Analog **P = Power**
I = Input **G = Ground**
O = Output

5.1 ADC

Name	Type	Pin No	Description
ADC_REFIO	AI	140	ADC Reference Pad
ADC_TEST	AIO	143	ADC Test Pin / SOG input
B	AI	146	Analog Input from BLUE Channel
G	AI	149	Analog Input from GREEN Channel
R	AI	152	Analog Input from RED Channel
ADC_VDD	AP	141,142 147,148 153,154	ADC Analog Power
ADC_GND	AG	138,139 144,145 150,151	ADC Analog Ground
			Total: 17 Pins

5.2 PLL

Name	Type	Pin No	Description
XI	AI	92	Reference Clock Input
XO	AO	93	Reference Clock Output
PLL_TEST1	AIO	96	Test Pin 1
PLL_TEST2	AIO	97	Test Pin 2
PLL_VDD	AP	88,94 95,100 101	PLL Analog Power
PLL_GND	AG	89,90 91,98 99,102	PLL Analog Ground
			Total: 15 Pins

5.3 Control Interface

Name	Type	Pin No	Description
(EXT#=0): SCSB (EXT#=1): GPIO_P3.4	I I/O	81	Serial Control I/F Chip Select GPIO_P3.4 / T0#
(EXT#=0): SCLK (EXT#=1): GPIO_P3.5	I I/O	82	Serial Control I/F Clock GPIO_P3.5 / T1#
(EXT#=0): SDI (EXT#=1): GPIO_P3.6	I I/O	83	Serial Control I/F Data in GPIO_P3.6
(EXT#=0): SDO (EXT#=1): GPIO_P3.7	O I/O	84	Serial Control I/F Data out GPIO_P3.7
(EXT#=0): IRQ# (EXT#=1): GPIO_P3.1	O I/O	85	Controller's IRQ# Output; GPIO_P3.1 / INT#1
(EXT#=0): PWDN# (EXT#=1): GPIO_P3.0	I I/O	86	PowerDown# for Controller GPIO_P3.0
RESET#	I	87	(EXT#=0): RESET# for Controller; (EXT#=1): RESET# for MCU
			Total: 7 Pins

5.4 Digital Input

Name	Type	Pin No	Description
AHS	I	158	VGA-port Horizontal Sync
AVS	I	160	VGA-port Vertical Sync
VODD	I	167	Video ODD Signal
BHS	I	168	VGB-port Horizontal Sync
BVS	I	169	VGB-port Vertical Sync
BENA	I	170	VGB-port Input Data Enable
BCLK	I	171	VGB-port Input Clock
BRED/YIN [7:0] / DVODATA [11:4] / VIDEO8	I	172,173 174,175 176,177 178,179	VGB-port Input Data (Red/Y)
BGRN [7:0] / DVODATA [3:0]	I	181,182 184,185 186,187 188,189	VGB-port Input Data (Green)
BBLU/UVIN [7:0]	I	190,191 192,193 194,195 196,197	VGB-port Input Data (Blue/UV)
			Total: 31 Pins

5.5 Display Port

Name	Type	Pin No	Description
DCLK	O	73	Display clock; / TCON_ECLK
DHS	O	71	Display Horizontal Sync; / TCON_6
DVS	O	70	Display Vertical Sync; / TCON_5
DEN	O	69	Display Data Enable; / TCON_4
DARED [7:0]	O	68, 67, 66 65, 63, 61 59, 58	Display A-port RED Data
DAGR [7:0]	O	57, 55, 54 53, 52, 51 50, 49	Display A-port GREEN Data
DABLU [7:0]	O	47, 45, 43 42, 40, 39 38, 37	Display A-port BLUE Data
DBRED [7:0]	O	35, 33, 31 30, 28, 26 25, 24	Display B-port RED Data
DBG [7:0]	O	23, 22, 21 19, 17, 15 14, 13	Display B-port GREEN Data
DBBLU [7:0]	O	11, 10, 9, 8 7, 5, 3, 2	Display B-port BLUE Data
			Total: 52 Pins

5.6 Miscellaneous Interface

Name	Type	Pin No	Description
REFCLK	IO	36	In/out Test Pin for DCLK; / TCON_OCLK
PWM_0	O	166	PWM_0 Output
			Total: 2 Pins

5.7 DDC Channel

Name	Type	Pin No	Description
DDCSDA	I	156	DDC Serial Control I/F Data Input
	O		DDC Serial Control I/F Data Output
DDCSCL	I	161	DDC Serial Control I/F Clock
			Total: 2 Pins

5.8 Power & Ground

Name	Type	Pin No	Description
3.3V Power	P	4, 18 32, 46 60, 72 106,122 157	VCC3IO: 9
3.3V Ground	G	6, 20 34, 48 56, 74 109,125 159	GND0: 9
2.5V Power	P	16, 29 41, 64 78,127 133,180 198	VCCK: 9
2.5V Ground	G	12, 27 44, 62 80,129 135,183 201	GNDIK: 9
			Total: 36 Pins

5.9 MCU Interface

Name	I/O	Pin No	Description
PSEN#	O	103	Program Load Enable
ROM_DATA [7:0]	IO	104,105,107 108,110,111 112,113	ROM Data Input
ROM_ADDR [15:9]	O I	134,132,131 130,128,126 124	ROM Address Output DDC_CA latch
ROM_ADDR [8:0]	O	123,121,120 119,118,117 116,115,114	ROM Address Output
ROM_ADDR_BA NK	O	136	XDATA/PROG# Bank Select
GPIO_P0.4	I/O	137	GPIO_P0.4 / WR#
EXT#	I	155	External MCU, Internal MCU Disable
GPIO_P1.0	I/O	75	GPIO_P1.0 / TCON_0
GPIO_P1.1	I/O	76	GPIO_P1.1 / TCON_1
GPIO_P1.2	I/O	77	GPIO_P1.3 / TCON_2
GPIO_P1.3	I/O	79	GPIO_P1.3 / TCON_3
GPIO_P1.4	I/O	199	GPIO_P1.4 / TCON_7
GPIO_P1.5	I/O	200	GPIO_P1.5 / TCON_8
GPIO_P1.6	I/O	202	GPIO_P1.6 / TCON_9
GPIO_P1.7	I/O	203	GPIO_P1.7 / TCON_10
GPIO_P2.0	I/O	204	GPIO_P2.0 / TCON_11
GPIO_P2.1	I/O	205	GPIO_P2.1 / TCON_12
GPIO_P2.2	I/O	206	GPIO_P2.2 / TCON_13
GPIO_P2.3	I/O	207	GPIO_P2.3 / TCON_14
GPIO_P2.4	I/O	208	GPIO_P2.4 / TCON_15
GPIO_P2.5	I/O	1	GPIO_P2.5 / TCON_16
GPIO_P2.6	I/O	164	GPIO_P2.6 / PWM1
GPIO_P2.7	I/O	165	GPIO_P2.7 / PWM2
(EXT#=0): PWDN# (EXT#=1): GPIO_P3.0	I I/O	Share	PowerDown# for Controller GPIO_P3.0
(EXT#=0): IRQ# (EXT#=1): GPIO_P3.1	O I/O	Share	Controller's IRQ# output; GPIO_P3.1 / INT1#
GPIO_P3.2	I/O	162	GPIO_P3.2 / INT0#
GPIO_P3.3	I/O	163	GPIO_P3.3
(EXT#=0): SCSB (EXT#=1): GPIO_P3.4	I I/O	Share	Serial control I/F chip select GPIO_P3.4 / T0#
(EXT#=0): SCLK (EXT#=1): GPIO_P3.5	I I/O	Share	Serial control I/F clock GPIO_P3.5 / T1#
(EXT#=0): SDI (EXT#=1): GPIO_P3.6	I I/O	Share	Serial control I/F data in GPIO_P3.6
(EXT#=0): SDO (EXT#=1): GPIO_P3.7	O I/O	Share	Serial control I/F data out GPIO_P3.7
			Total: 46 pins (6 share)

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