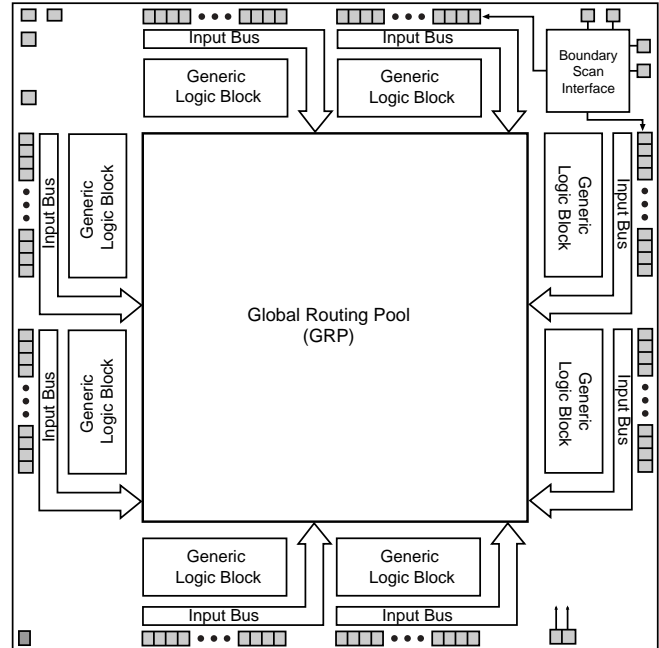


Features

- **SuperWIDE HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
 - 3.3V Power Supply
 - User Selectable 3.3V/2.5V I/O
 - 12000 PLD Gates / 256 Macrocells
 - Up to 192 I/O Pins
 - 256 Registers
 - High-Speed Global Interconnect
 - SuperWIDE 32 Generic Logic Block (GLB) Size for Optimum Performance
 - SuperWIDE Input Gating (68 Inputs) for Fast Counters, State Machines, Address Decoders, etc.
 - PCB Efficient Ball Grid Array (BGA) Package Options
 - Interfaces with Standard 5V TTL Devices
- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - $f_{max} = 125$ MHz Maximum Operating Frequency
 - $t_{pd} = 7.5$ ns Propagation Delay
 - Enhanced $t_{su2} = 7$ ns, $t_{su3} (CLK0/1) = 4.5$ ns, $t_{su3} (CLK2/3) = 3.5$ ns
 - TTL/3.3V/2.5V Compatible Input Thresholds and Output Levels
 - Electrically Erasable and Reprogrammable
 - Non-Volatile
 - Programmable Speed/Power Logic Path Optimization
- **IN-SYSTEM PROGRAMMABLE**
 - Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality
 - Reprogram Soldered Devices for Faster Debugging
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE AND 3.3V IN-SYSTEM PROGRAMMABLE**
- **ARCHITECTURE FEATURES**
 - Enhanced Pin-Locking Architecture with Single-Level Global Routing Pool and SuperWIDE GLBs
 - Wrap Around Product Term Sharing Array Supports up to 35 Product Terms Per Macrocell
 - Macrocells Support Concurrent Combinatorial and Registered Functions
 - Macrocell Registers Feature Multiple Control Options Including Set, Reset and Clock Enable
 - Four Dedicated Clock Input Pins Plus Macrocell Product Term Clocks
 - Slew and Skew Programmable I/O (SASPI/O) Supports Programmable Bus Hold, Pull-up, Open Drain and Slew and Skew Rate Options
 - Six Global Output Enable Terms, Two Global OE Pins and One Product Term OE per Macrocell
 - PC and UNIX Platforms

Functional Block Diagram



ispLSI 5000V Description

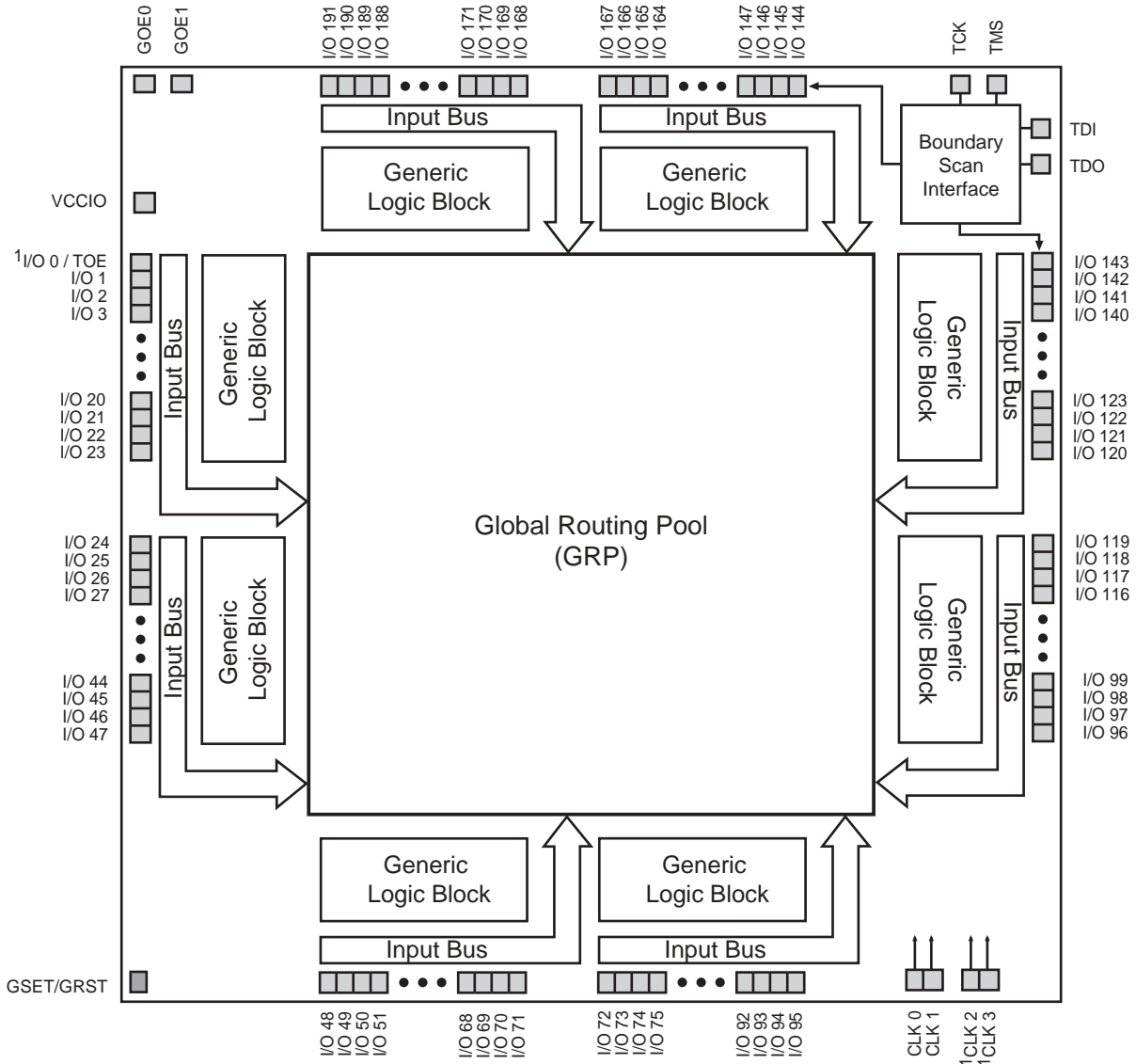
The ispLSI 5000V Family of In-System Programmable High Density Logic Devices is based on Generic Logic Blocks (GLBs) of 32 registered macrocells and a single Global Routing Pool (GRP) structure interconnecting the GLBs.

Outputs from the GLBs drive the Global Routing Pool (GRP) between the GLBs. Switching resources are provided to allow signals in the Global Routing Pool to drive any or all the GLBs in the device. This mechanism allows fast, efficient connections across the entire device.

Each GLB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and five extra control product terms. The GLB has 68 inputs from the Global Routing Pool which are available in both true and complement form for every product term. The 160 product terms are grouped in 32 sets of five and sent into a Product Term Sharing Array (PTSA) which allows sharing up to a maximum of 35 product terms for a single function. Alternatively, the PTSA can be bypassed for functions of five product terms or less. The

Functional Block Diagram

Figure 1. ispLSI 5256VA Functional Block Diagram (272 BGA Option)



1. CLK2, CLK3 and TOE signals are multiplexed with I/O signals. Which I/O is multiplexed is determined by the package type used (see table below).

| Package Type | Multiplexed Signals | | |
|--------------|---------------------|----------------|-------------|
| 208 PQFP | I/O 89 / CLK2 | I/O 98 / CLK3 | I/O 0 / TOE |
| 208 fpBGA | I/O 89 / CLK2 | I/O 98 / CLK3 | I/O 0 / TOE |
| 272 BGA | I/O 119 / CLK2 | I/O 131 / CLK3 | I/O 0 / TOE |

ispLSI 5000V Description (Continued)

five extra product terms are used for shared GLB controls, set, reset, clock, clock enable and output enable.

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch/toggle flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. The macrocells each have two outputs, which can be fed back through the Global Routing Pool. This dual output capability from the macrocell allows efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O pad facilitates efficient use of this feature to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register, a D-type latch or a T-type flip flop.

The 32 outputs from the GLB can drive both the Global Routing Pool and the device I/O cells. The Global Routing Pool contains one line from each macrocell output and one line from each I/O pin.

The input buffer threshold has programmable TTL/3.3V/2.5V compatible levels. The output driver can source 4mA and sink 8mA in 3.3V mode. The output drivers have a separate VCCIO reference input which is independent of the main VCC supply for the device. This feature allows the output drivers to drive either 3.3V or 2.5V output levels while the device logic and the output current drive is always powered from 3.3V. The output drivers also provide individually programmable edge

rates and open drain capability. A programmable pullup resistor is provided to tie off unused inputs and a programmable bus-hold latch is available to hold tristate outputs in their last valid state until the bus is driven again by some device.

The ispLSI 5000V Family features 3.3V, non-volatile in-system programmability for both the logic and the interconnect structures, providing the means to develop truly reconfigurable systems. Programming is achieved through the industry standard IEEE 1149.1-compliant Boundary Scan interface. Boundary Scan test is also supported through the same interface.

An enhanced, multiple cell security scheme is provided that prevents reading of the JEDEC programming file when secured. After the device has been secured using this mechanism, the only way to clear the security is to execute a bulk-erase instruction.

ispLSI 5000V Family Members

The ispLSI 5000V Family ranges from 256 macrocells to 512 macrocells and operates from a 3.3V power supply. All family members will be available with multiple package options. The ispLSI 5000V Family device matrix showing the various bondout options is shown in the table below.

The interconnect structure (GRP) is very similar to Lattice's existing ispLSI 1000, 2000 and 3000 families, but with an enhanced interconnect structure for optimal pin locking and logic routing. This eliminates the need for registered I/O cells or an Output Routing Pool.

Table 1. ispLSI 5000V Family

| Device | GLBs | Macrocells | Package Type | | | |
|---------------|------|------------|--------------|----------|---------|---------|
| | | | 208 fpBGA | 208 PQFP | 272 BGA | 388 BGA |
| ispLSI 5256VA | 8 | 256 | 144 I/O | 144 I/O | 192 I/O | — |
| ispLSI 5384VA | 12 | 384 | 144 I/O | 144 I/O | 192 I/O | 288 I/O |
| ispLSI 5512VA | 16 | 512 | — | 144 I/O | 192 I/O | 288 I/O |

Figure 2. ispLSI 5256VA Block Diagram (192 I/O Version)

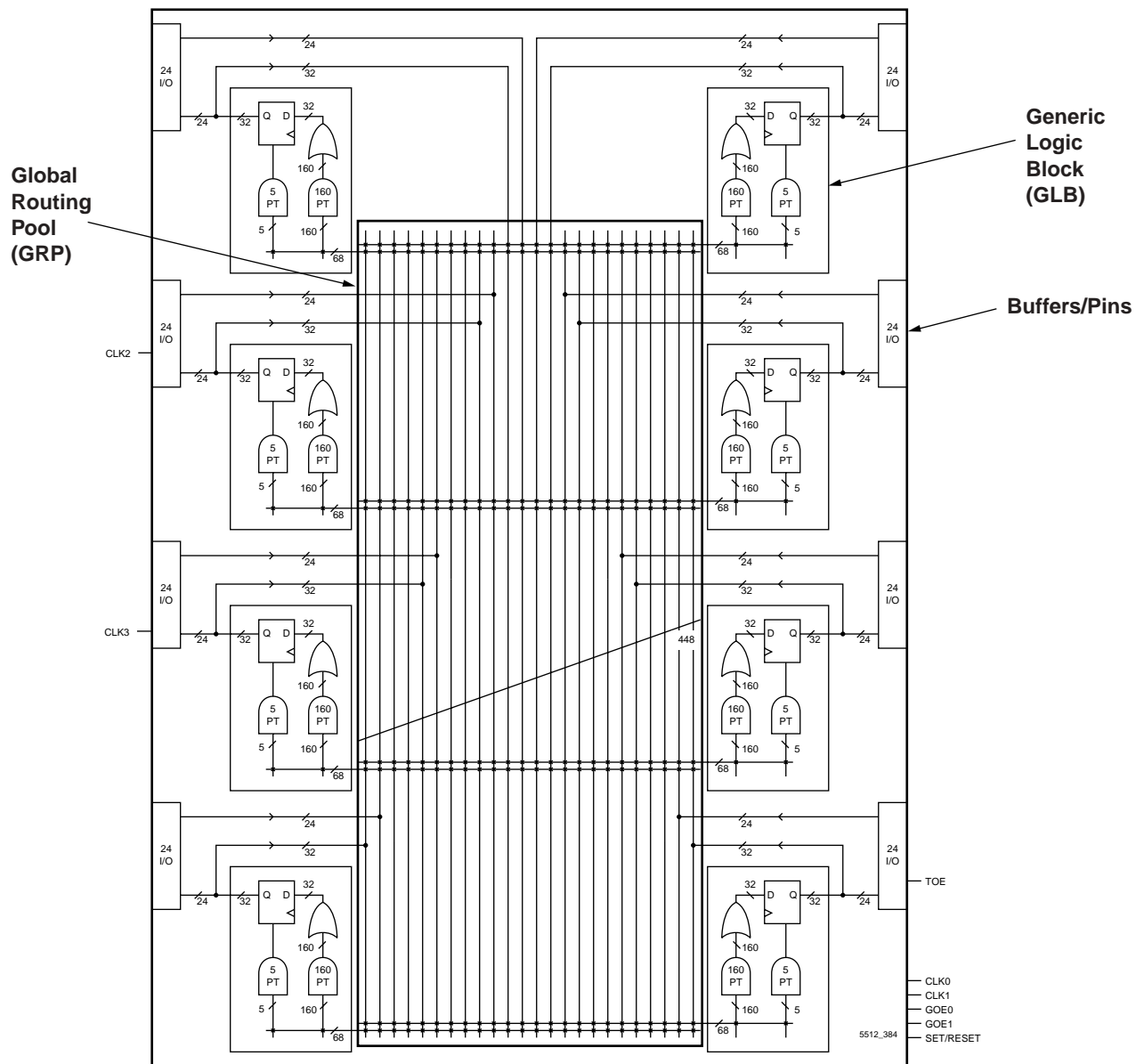


Figure 3. ispLSI 5000V Generic Logic Block (GLB)

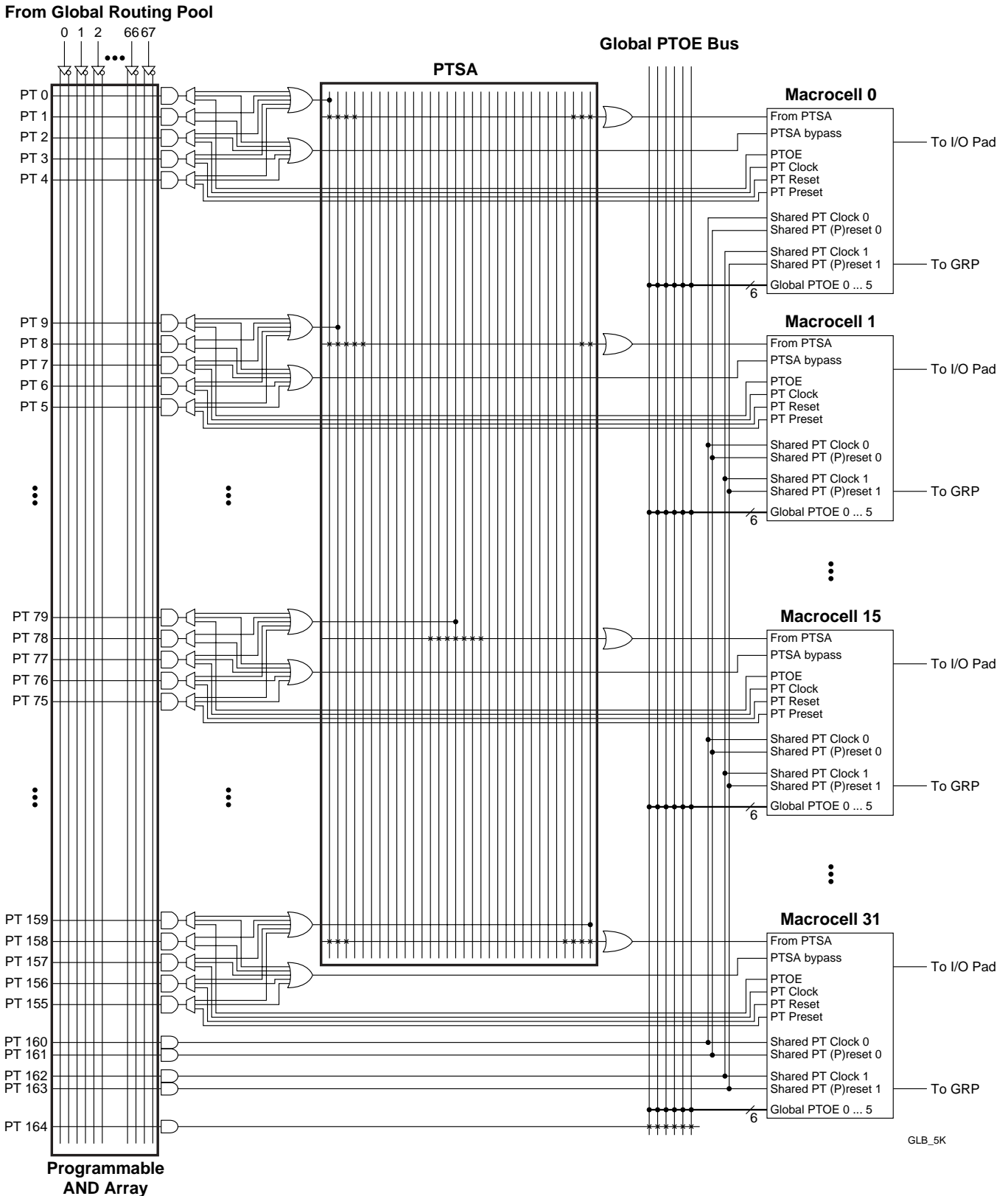
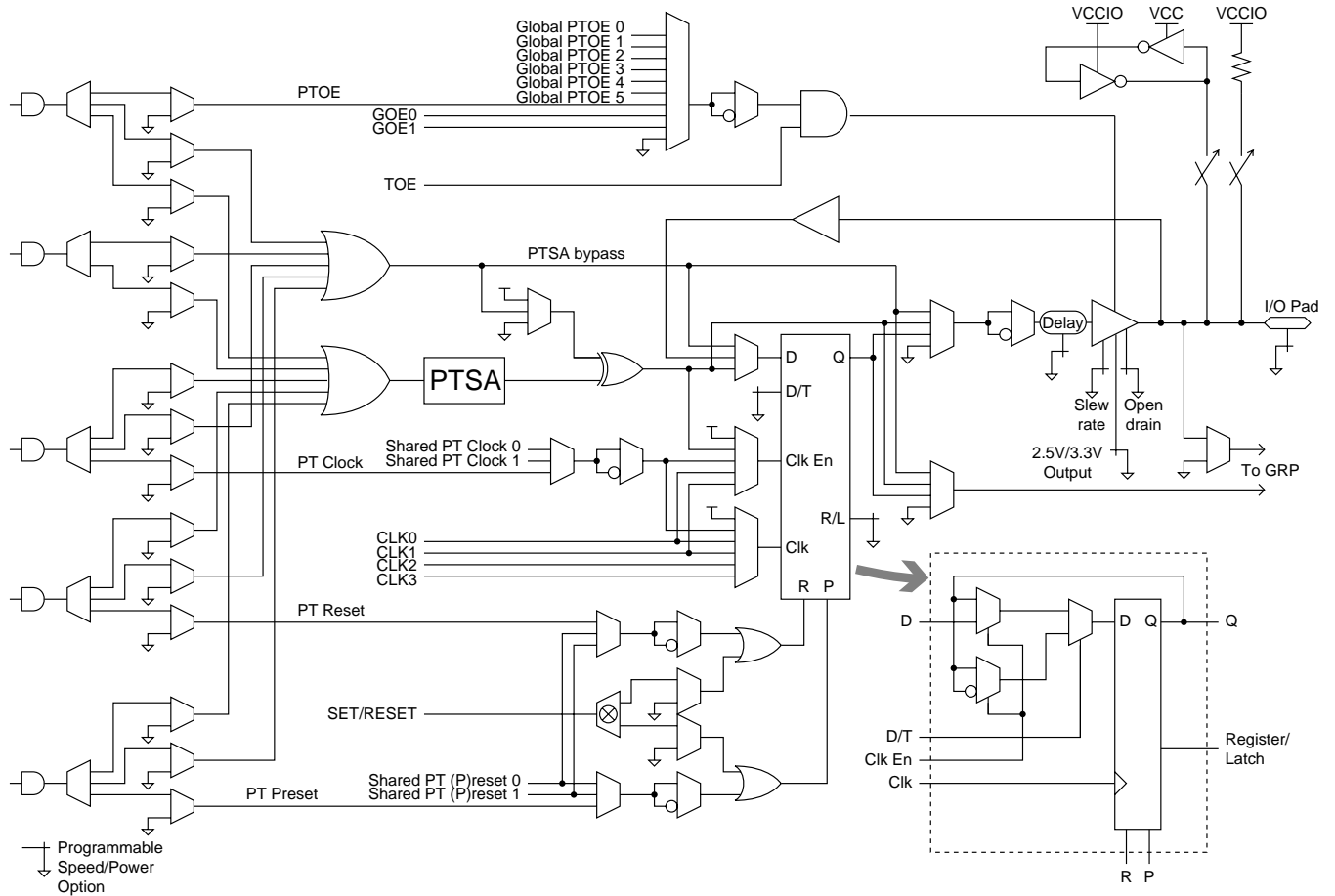


Figure 4. ispLSI 5000V Macrocell



Global Clock Distribution

The ispLSI 5000V Family has four dedicated clock input pins: CLK0 - CLK3. CLK0 input is used as the dedicated master clock that has the lowest internal clock skew with no clock inversion to maintain the fastest internal clock

speed. The clock inversion is available on the remaining CLK1 - CLK3 signals. By sharing the pins with the I/O pins, CLK2 and CLK3 can not only be inverted but also is available for logic implementation through GRP signal routing. Figure 5 shows these different clock distribution options.

Figure 5. ispLSI 5000V Global Clock Structure

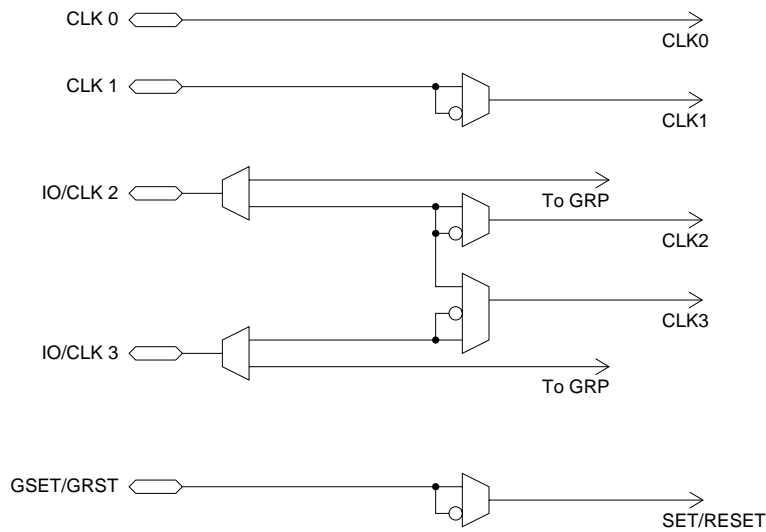
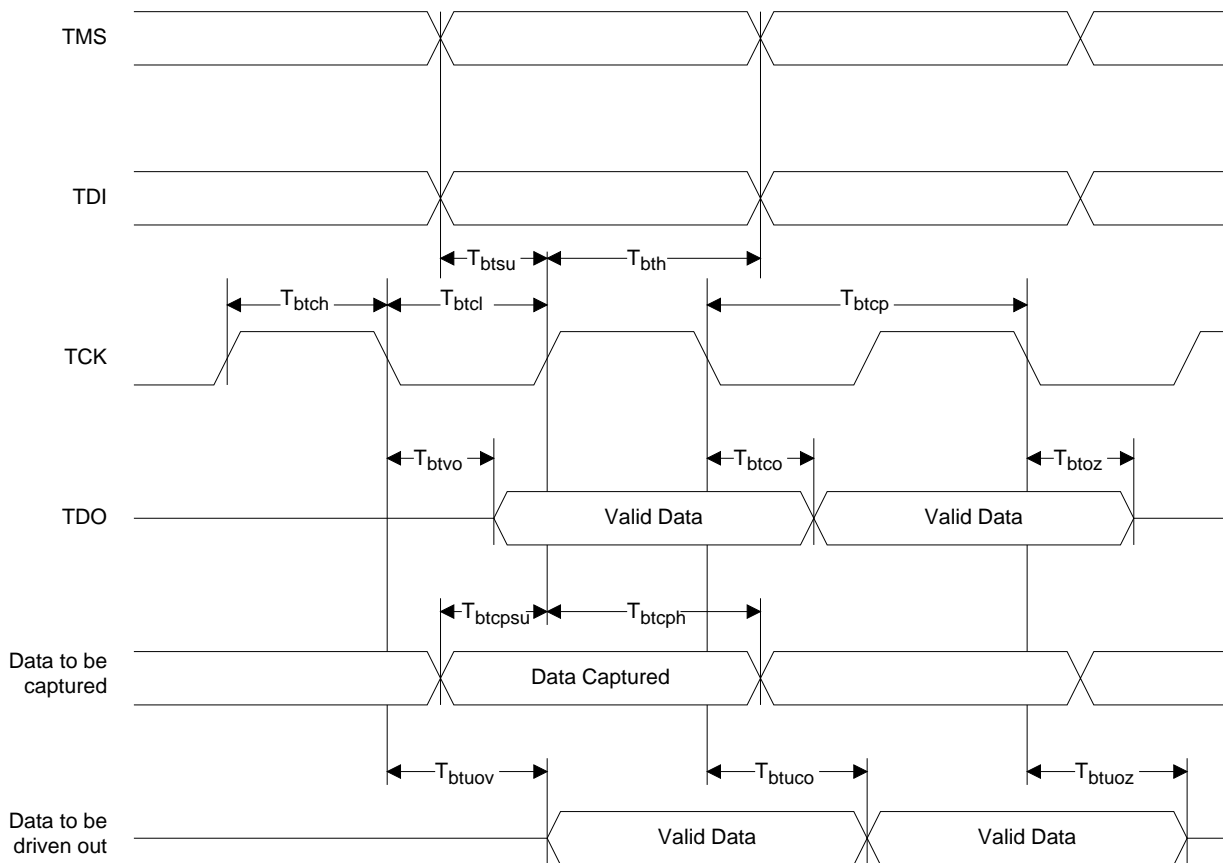


Figure 8. Boundary Scan Waveforms and Timing Specifications



| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|-------------|--|------|-----|-------|
| t_{btcp} | TCK [BSCAN test] clock pulse width | 125 | – | ns |
| t_{btch} | TCK [BSCAN test] pulse width high | 62.5 | – | ns |
| t_{btcl} | TCK [BSCAN test] pulse width low | 62.5 | – | ns |
| t_{btsu} | TCK [BSCAN test] setup time | 25 | – | ns |
| t_{bth} | TCK [BSCAN test] hold time | 25 | – | ns |
| t_{rf} | TCK [BSCAN test] rise and fall time | 50 | – | mV/ns |
| t_{btco} | TAP controller falling edge of clock to valid output | – | 25 | ns |
| t_{btouz} | TAP controller falling edge of clock to data output disable | – | 25 | ns |
| t_{btvo} | TAP controller falling edge of clock to data output enable | – | 25 | ns |
| t_{btcpu} | BSCAN test Capture register setup time | 25 | – | ns |
| t_{btcpu} | BSCAN test Capture register hold time | 25 | – | ns |
| t_{btuco} | BSCAN test Update reg, falling edge of clock to valid output | – | 50 | ns |
| t_{btuo} | BSCAN test Update reg, falling edge of clock to output disable | – | 50 | ns |
| t_{btuo} | BSCAN test Update reg, falling edge of clock to output enable | – | 50 | ns |

Absolute Maximum Ratings ^{1, 2}

Supply Voltage V_{CC} -0.5 to +5.4V
 Input Voltage Applied -0.5 to +5.6V
 Tri-Stated Output Voltage Applied -0.5 to +5.6V
 Storage Temperature -65 to 150°C
 Case Temp. with Power Applied -55 to 125°C
 Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

DC Recommended Operating Condition

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS | |
|------------|-----------------------|---|------|-------|---|
| V_{CC} | Supply Voltage | Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ | 3.00 | 3.60 | V |
| | | Industrial $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | 3.00 | 3.60 | V |
| V_{CCIO} | I/O Reference Voltage | 2.3 | 3.60 | V | |

Table 2 - 0005/5256

Capacitance ($T_A=25^\circ\text{C}, f=1.0\text{ MHz}$)

| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|--------|--------------------------|---------|-------|---|
| C_1 | I/O Capacitance | 10 | pf | $V_{CC} = 3.3\text{V}, V_{I/O} = 2.0\text{V}$ |
| C_2 | Clock Capacitance | 10 | pf | $V_{CC} = 3.3\text{V}, V_{CK} = 2.0\text{V}$ |
| C_3 | Global Input Capacitance | 10 | pf | $V_{CC} = 3.3\text{V}, V_G = 2.0\text{V}$ |

Table 2 - 0006/5384

Erase Reprogram Specification

| PARAMETER | MINIMUM | MAXIMUM | UNITS |
|-------------------------------|---------|---------|--------|
| ispLSI Erase/Reprogram Cycles | 10000 | – | Cycles |

Table 2-0008/3320

Switching Test Conditions

| | |
|--------------------------------|-------------------------|
| Input Pulse Levels | GND to $V_{CCIO_{min}}$ |
| Input Rise and Fall Time | $\leq 1.5ns$ 10% to 90% |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| Output Load | See figure |

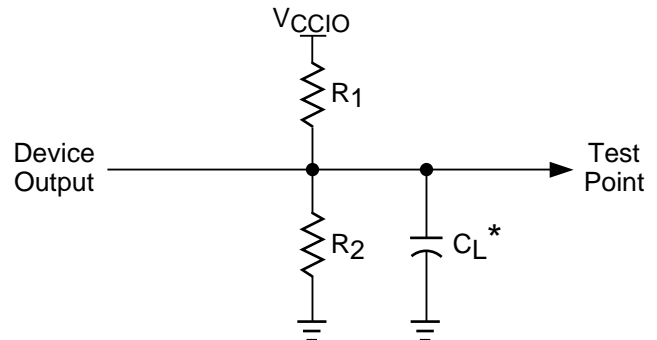
3-state levels are measured 0.5V from steady-state active level. Table 2 - 0003/5384

Output Load Conditions (See Figure 8)

| TEST CONDITION | 3.3V | | 2.5V | | CL | |
|----------------|-----------------------------------|------|------|------|------|------|
| | R1 | R2 | R1 | R2 | | |
| A | 316Ω | 348Ω | 511Ω | 475Ω | 35pF | |
| B | Active High | ∞ | 348Ω | ∞ | 475Ω | 35pF |
| | Active Low | 316Ω | ∞ | 511Ω | ∞ | 35pF |
| C | Active High to Z at $V_{OH}-0.5V$ | ∞ | 348Ω | ∞ | 475Ω | 5pF |
| | Active Low to Z at $V_{OL}+0.5V$ | 316Ω | ∞ | 511Ω | ∞ | 5pF |
| D | Slow Slew | ∞ | ∞ | ∞ | ∞ | 35pF |

Table 2 - 0004A/5384

Figure 9. Test Load



* C_L includes Test Fixture and Probe Capacitance.

0213D

DC Electrical Characteristics for 3.3V Range¹

Over Recommended Operating Conditions

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNITS |
|------------|-----------------------|---|------|------|------|-------|
| V_{CCIO} | I/O Reference Voltage | | 3.0 | – | 3.6 | V |
| V_{IL} | Input Low Voltage | $V_{OH} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$ | -0.3 | – | 0.8 | V |
| V_{IH} | Input High Voltage | $V_{OH} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$ | 2.0 | – | 5.25 | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 8\text{ mA}$ | – | – | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -4\text{ mA}$ | 2.4 | – | – | V |

Table 2-0007/5256VA

1. I/O voltage configuration must be set to VCC.

DC Electrical Characteristics for 2.5V Range¹

Over Recommended Operating Conditions

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNITS |
|-------------------|-----------------------|---|------|------|------|-------|
| V _{CCIO} | I/O Reference Voltage | | 2.3 | – | 2.7 | V |
| V _{IL} | Input Low Voltage | $V_{OH(min)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$ | -0.3 | – | 0.7 | V |
| V _{IH} | Input High Voltage | $V_{OH(min)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$ | 1.7 | – | 5.25 | V |
| V _{OL} | Output Low Voltage | $V_{CCIO=min}, V_{IN}=V_{IH}$ or $V_{IL}, I_{OL}=100\mu A$ | – | – | 0.2 | V |
| | | $V_{CCIO=min}, V_{IN}=V_{IH}$ or $V_{IL}, I_{OL}=2mA$ | – | – | 0.7 | V |
| V _{OH} | Output High Voltage | $V_{CCIO=min}, V_{IN}=V_{IH}$ or $V_{IL}, I_{OH}=-100\mu A$ | 2.1 | – | – | V |
| | | $V_{CCIO=min}, V_{IN}=V_{IH}$ or $V_{IL}, I_{OH}=-2mA$ | 1.7 | – | – | V |

1. I/O voltage configuration must be set to V_{CCIO}.

2.5V/5256VA

DC Electrical Characteristics

Over Recommended Operating Conditions

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNITS |
|------------------------------|--|--|-----------------|------|-----------------|-------|
| I _{IL} | Input or I/O Low Leakage Current | $0V \leq V_{IN} \leq V_{IL(Max.)}$ | – | – | -10 | μA |
| I _{IH} | Input or I/O High Leakage Current | $(V_{CCIO}-0.2)V \leq V_{IN} \leq V_{CCIO}$ | – | – | 10 | μA |
| | | $V_{CCIO} \leq V_{IN} \leq 5.25V$ | – | – | 50 | μA |
| I _{PU} ¹ | I/O Active Pullup Current | $0V \leq V_{IN} \leq V_{IL}$ | – | – | -150 | μA |
| I _{BHL} | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL(max)}$ | 40 | – | – | μA |
| I _{BHH} | Bus Hold High Sustaining Current | $V_{IN} = V_{IH(min)}$ | -40 | – | – | μA |
| I _{BHLO} | Bus Hold Low Overdrive Current | $0V \leq V_{IN} \leq V_{CCIO}$ | – | – | 550 | μA |
| I _{BHLH} | Bus Hold High Overdrive Current | $0V \leq V_{IN} \leq V_{CCIO}$ | – | – | -550 | μA |
| I _{BHT} | Bus Hold Trip Points | | V _{IL} | – | V _{IH} | V |
| I _{VCCIO} | Current Needed for V _{CCIO} Pin | All I/Os Pulled-up, (Total I/Os * I _{PUmax}) | – | – | 30 | mA |

1. Pullup is capable of pulling to a minimum voltage of V_{OH} under no-load conditions.

DC Char_5256VA

External Switching Characteristics

Over Recommended Operating Conditions

| PARAM. | TEST ³ COND. | # | DESCRIPTION ^{4,5} | -125 | | -100 | | -70 | | UNITS |
|-------------------------------|-------------------------|----|--|------|------|------|------|------|------|-------|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{pd1} ⁶ | A | 1 | Data Prop. Delay, 5PT Bypass | — | 7.5 | — | 10 | — | 15 | ns |
| t _{pd2} ⁶ | A | 2 | Data Propagation Delay | — | 9.5 | — | 13 | — | 19 | ns |
| f _{max} | A | 3 | Clock Frequency with Internal Feedback ¹ | 125 | — | 100 | — | 70 | — | MHz |
| f _{max} (Ext.) | — | 4 | Clock Freq. with Ext. Feedback, 1/(tsu2 + tco1) | 91 | — | 69 | — | 45 | — | MHz |
| f _{max} (Tog.) | — | 5 | Clock Frequency, Max Toggle ² | 167 | — | 125 | — | 83 | — | MHz |
| t _{su1} | — | 6 | GLB Reg. Setup Time before Clk, 5PT bypass | 6 | — | 8 | — | 12 | — | ns |
| t _{co1} ⁶ | A | 7 | GLB Reg. Clock to Output Delay | — | 4 | — | 5.5 | — | 8 | ns |
| t _{h1} | — | 8 | GLB Reg. Hold Time after Clock, 5PT bypass | 0 | — | 0 | — | 0 | — | ns |
| t _{su2} | — | 9 | GLB Reg. Setup Time before Clock | 7 | — | 9 | — | 14 | — | ns |
| t _{h2} | — | 10 | GLB Reg. Hold Time after Clock | 0 | — | 0 | — | 0 | — | ns |
| t _{su3} (CLK0/1) | — | 11 | GLB Reg. Setup Time before Clock, Input Reg. Path (CLK0/1) | 4.5 | — | 6 | — | 9 | — | ns |
| t _{su3} (CLK2/3) | — | 12 | GLB Reg. Setup Time before Clock, Input Reg. Path (CLK2/3) | 3.5 | — | 5 | — | 7 | — | ns |
| t _{h3} (CLK0/1) | — | 13 | GLB Reg. Hold Time after Clock, Input Reg. Path (CLK0/1) | 0 | — | 0 | — | 0 | — | ns |
| t _{h3} (CLK2/3) | — | 14 | GLB Reg. Hold Time after Clock, Input Reg. Path (CLK2/3) | 0 | — | 0 | — | 0 | — | ns |
| t _{r1} | A | 15 | Ext. Reset Pin to Output Delay | — | 15 | — | 20 | — | 30 | ns |
| t _{rw1} | — | 16 | Ext. Reset Pulse Duration | 7 | — | 9 | — | 14 | — | ns |
| t _{ptoe/dis} | B/C | 17 | Local Product Term Output Enable/Disable | — | 9 | — | 12 | — | 18 | ns |
| t _{gptoe/dis} | B/C | 18 | Global Product Term Output Enable/Disable | — | 18 | — | 24 | — | 30 | ns |
| t _{goe/dis} | B/C | 19 | Global OE Input to Output Enable/Disable | — | 6 | — | 8 | — | 12 | ns |
| t _{wh} | — | 20 | Ext. Sync. Clock Pulse Duration, High | 3 | — | 4 | — | 6 | — | ns |
| t _{wl} | — | 21 | Ext. Sync. Clock Pulse Duration, Low | 3 | — | 4 | — | 6 | — | ns |

1. Standard 32-bit counter using GRP feedback.

2. f_{max} (Toggle) may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.

3. Reference Switching Test Conditions section.

4. Unless noted otherwise, all timing numbers are taken with worst case PTSA fanout, a GRP load of 1 GLB, and CLK0.

5. Timing parameters measured using normal active output driver.

6. The delay parameters are measured with V_{cc} as I/O voltage reference. An additional 0.5ns delay is incurred when V_{ccio} is used as I/O voltage reference.

Timing Ext.5256va/4.0.eps

Internal Timing Parameters¹

Over Recommended Operating Conditions

| PARAM | # ² | DESCRIPTION | -125 | | -100 | | -70 | | UNIT |
|-------------------------------------|----------------|---|------|------|------|------|-----|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| I/O Buffer | | | | | | | | | |
| tidcom | 22 | Input Pad and Buffer, Combinatorial Input | – | 0.7 | – | 0.9 | – | 1.4 | ns |
| tidreg | 23 | Input Pad and Buffer, Registered Input | – | 4.7 | – | 6.6 | – | 9.7 | ns |
| todcom | 24 | Output Pad and Buffer, Combinatorial Output | – | 1.3 | – | 1.7 | – | 2.6 | ns |
| todreg | 25 | Output Pad and Buffer, Registered Output | – | 1.8 | – | 2.8 | – | 4.6 | ns |
| todz | 26 | Output Buffer Enable/Disable | – | 1.3 | – | 1.7 | – | 2.6 | ns |
| tslf | 27 | Slew Rate Adder, Fast Slew | – | 0 | – | 0 | – | 0 | ns |
| tsls | 28 | Slew Rate Adder, Slow Slew | – | 7.5 | – | 10 | – | 15 | ns |
| tslfd | 29 | Programmable Delay Adder, Fast Slew | – | 0.5 | – | 0.7 | – | 1 | ns |
| tslsd | 30 | Programmable Delay Adder, Slow Slew | – | 8 | – | 10.7 | – | 16 | ns |
| GLB/Macrocell Delay Register | | | | | | | | | |
| tmbp | 31 | Macrocell Register/Latch Bypass | – | 0 | – | 0 | – | 0 | ns |
| tmlat | 32 | Macrocell Latch Delay | – | 1 | – | 1.4 | – | 2 | ns |
| tmco | 33 | Macrocell Register/Latch Clock to Output | – | 1 | – | 1 | – | 1 | ns |
| tmsu | 34 | Macrocell Register/Latch Setup Time | 1 | – | 1.1 | – | 1.7 | – | ns |
| tmh | 35 | Macrocell Register/Latch Hold Time | 2.5 | – | 3.9 | – | 5.3 | – | ns |
| tmsuce | 36 | Macrocell Register/Latch CLKEN Setup Time | 1 | – | 1.4 | – | 2 | – | ns |
| tmhce | 37 | Macrocell Register/Latch CLKEN Hold Time | 1 | – | 1.4 | – | 2 | – | ns |
| tmrst | 38 | Macrocell Register/Latch Set/Reset Time | – | 1 | – | 1.4 | – | 2 | ns |
| tftog | 39 | Toggle Flip-Flop Feedback | – | 1 | – | 1.3 | – | 2 | ns |
| AND Array | | | | | | | | | |
| tandhs | 40 | AND Array, High Speed Mode | – | 3 | – | 4 | – | 6 | ns |
| tandlp | 41 | AND Array, Low Power Mode | – | 5 | – | 6.6 | – | 10 | ns |
| PTSA | | | | | | | | | |
| t5ptcom | 42 | 5 Product Term Bypass, Combinatorial | – | 1 | – | 1.4 | – | 2 | ns |
| t5ptreg | 43 | 5 Product Term Bypass, Registered | – | 1 | – | 1.7 | – | 2.3 | ns |
| t5ptxcom | 44 | 5 Product Term XOR, Combinatorial | – | 2.5 | – | 3.6 | – | 5 | ns |
| t5ptxreg | 45 | 5 Product Term XOR, Registered | – | 1.5 | – | 2.2 | – | 3.3 | ns |
| tptsacom | 46 | Product Term Sharing Array, Combinatorial | – | 3 | – | 4.1 | – | 6 | ns |
| tptsareg | 47 | Product Term Sharing Array, Registered | – | 2.0 | – | 2.7 | – | 4.3 | ns |
| PTSA Controls | | | | | | | | | |
| tpck | 48 | Product Term Clock Delay | – | 0.5 | – | 0.7 | – | 1 | ns |
| tpcken | 49 | Product Term CLKEN Delay | – | 1 | – | 1.4 | – | 2 | ns |
| tscken | 50 | Shared Product Term CLKEN Delay | – | 1 | – | 1.4 | – | 2 | ns |
| tsck | 51 | Shared Product Term Clock Delay | – | 0.5 | – | 0.7 | – | 1 | ns |
| tptsacken | 52 | Product Term Sharing Array CLKEN Delay | – | 2.0 | – | 2.4 | – | 4 | ns |
| tsrst | 53 | Shared Product Term Set/Reset Delay | – | 2.5 | – | 3.4 | – | 5 | ns |
| tprst | 54 | Product Term Set/Reset Delay | – | 1.5 | – | 2 | – | 3 | ns |
| tpoe | 55 | Product Term Output Enable/Disable | – | 2.5 | – | 3.4 | – | 5 | ns |
| tgpo | 56 | Global PT Output Enable/Disable | – | 11.5 | – | 15.4 | – | 17 | ns |

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Timing Rev. 4.0

Internal Timing Parameters¹

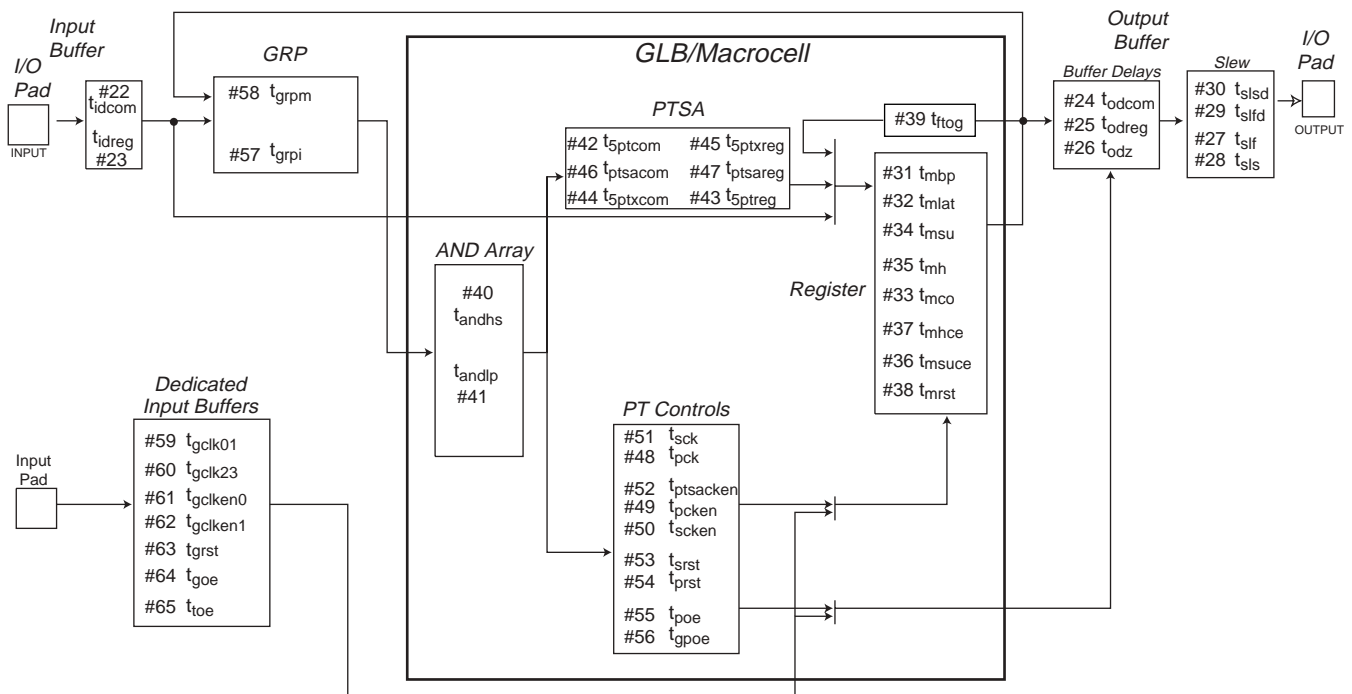
Over Recommended Operating Conditions

| PARAM | # ² | DESCRIPTION | -125 | | -100 | | -70 | | UNIT |
|-----------------------|----------------|---------------------------|------|------|------|------|-----|------|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| GRP | | | | | | | | | |
| tgrpi | 57 | GRP Delay from I/O Pad | – | 1.5 | – | 2 | – | 3 | ns |
| tgrpm | 58 | GRP Delay from Macrocell | – | 1.0 | – | 1.2 | – | 1.2 | ns |
| Global Control Delays | | | | | | | | | |
| tgclk01 | 59 | Global Clock 0 or 1 Delay | – | 1.2 | – | 1.7 | – | 2.4 | ns |
| tgclk23 | 60 | Global Clock 2 or 3 Delay | – | 2.2 | – | 2.7 | – | 4.4 | ns |
| tgclken0 | 61 | Global CLKEN 0 Delay | – | 1.7 | – | 2.4 | – | 3.4 | ns |
| tgclken1 | 62 | Global CLKEN 1 Delay | – | 2.7 | – | 3.4 | – | 5.4 | ns |
| tgrst | 63 | Global Set/Reset Delay | – | 12.2 | – | 15.8 | – | 23.4 | ns |
| tgoe | 64 | Global OE Delay | – | 4.7 | – | 6.3 | – | 9.4 | ns |
| ttoe | 65 | Test OE Delay | – | 4.7 | – | 6.2 | – | 9.4 | ns |

- Internal Timing Parameters are not tested and are for reference only.
- Refer to Timing Model in this data sheet for further details.

Timing Rev. 4.0

ispLSI 5256VA Timing Model

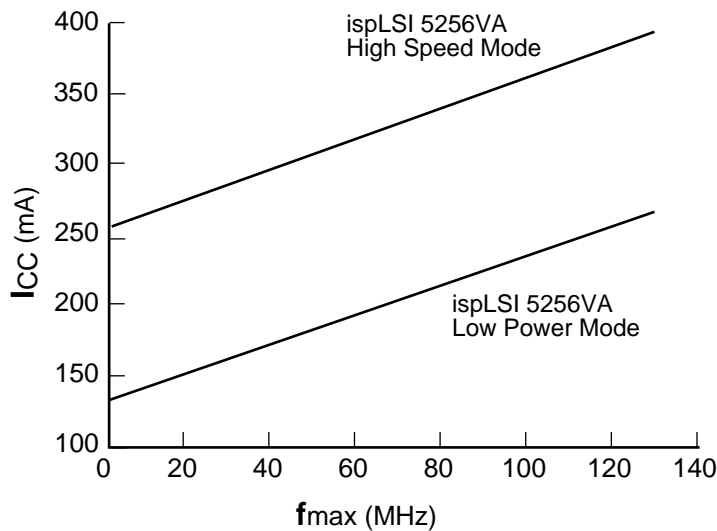


Power Consumption

Power consumption in the ispLSI 5256VA device depends on two primary factors: the speed at which the device is operating and the number of product terms used. The product terms have a fuse-selectable speed/power tradeoff setting. Each group of four product terms has a single speed/power tradeoff control fuse that acts

on the complete group of four. The fast “high-speed” setting operates product terms at their normal full power consumption. For portions of the logic that can tolerate longer propagation delays, selecting the slower “low-power” setting will significantly reduce the power dissipation for these product terms. Figure 10 shows the relationship between power and operating speed.

Figure 10. Typical Device Power Consumption vs fmax



Notes: Configuration of 16 16-bit Counters
Typical Current at 3.3V, 25° C

ICC can be estimated for the ispLSI 5256VA using the following equation:

High Speed Mode: $ICC = 30 + (\# \text{ of PTs} * 0.456) + (\# \text{ of nets} * \text{Max. freq} * 0.0039)$

Low Power Mode: $ICC = 30 + (\# \text{ of PTs} * 0.22) + (\# \text{ of nets} * \text{Max. freq} * 0.0039)$

of PTs = Number of Product Terms used in design

of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions (VCC = 3.3V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127/5256va

Signal Descriptions

| Signal Name | Description |
|---------------------------|--|
| TMS | Input - This pin is the Test Mode Select input, which is used to control the JTAG state machine. |
| TCK | Input - This pin is the Test Clock input pin used to clock through the JTAG state machine. |
| TDI | Input - This pin is the JTAG Test Data In pin used to load data. |
| TDO | Output - This pin is the JTAG Test Data Out pin used to shift data out. |
| TOE / I/O0 | Input/Output - This pin functions as either the Test Output Enable pin or an I/O pin based upon customer's design. TOE tristates all I/O pins when a logic low is driven. |
| GOE0, GOE1 | Input - These two pins are the Global Output Enable input pins. |
| GSET/GRST | Dedicated Set/Reset Input - This pin is available to all registers in the device and can independently be configured as preset, reset or no effect on each register. The global polarity (active high or low input) for this pin is also selectable. |
| I/O | Input/Output – These are the general purpose I/O used by the logic array. |
| GND | Ground |
| NC ¹ | No connect. |
| VCC | Vcc |
| CLK0, CLK1 | Dedicated clock inputs for all registers. Both clocks are muxed before being used as the clock input to all registers in the device. |
| CLK2 / I/O, CLK3 / I/O | Input/Output - These pins function as either dedicated clock inputs for all registers or an I/O pin based upon customer's design. Both clocks are muxed before being used as the clock input to all registers in the device. |
| VCCIO | Input - This pin is used if an optional 2.5V output is to be used. Every I/O can independently select either 3.3V or the optional voltage as its output level. If the optional output voltage is not required, this pin must be connected to the Vcc supply. Programmable pull-up resistors and bus-hold latches only draw current from this supply. |

1. NC pins are not to be connected to any active signals, VCC or GND.

272-Ball BGA Signal Locations

| Signal | Ball |
|-----------------|--|
| GOE0, GOE1 | V11, U11 |
| TOE / I/O 0 | M2 |
| SET/RST | J18 |
| TCK | L4 |
| TDI | M1 |
| TDO | J20 |
| TMS | L3 |
| CLK0, CLK1 | C10, D10 |
| CLK2 / I/O 119 | A18 |
| CLK3 / I/O 131 | B13 |
| VCCIO | J19 |
| GND | A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17 |
| VCC | D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15 |
| NC ¹ | A17, B3, B18, B19, B20, C3, C5, C18, C19, D3, D19, E2, P19, R3, T4, T17, T20, U1, U2, U3, W1, W2, W4, W17, W19, W20, Y2, Y12, Y20, |

1. NCs are not to be connected to any active signals, VCC or GND.

272-Ball BGA I/O Locations (Sorted by I/O)

| I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball |
|-------|------|-------|------|-------|------|-------|------|-------|------|-------|------|
| 0* | M2 | 32 | W7 | 64 | U16 | 96 | J17 | 128 | B14 | 160 | A3 |
| 1 | M3 | 33 | Y7 | 65 | V17 | 97 | H20 | 129 | A14 | 161 | D5 |
| 2 | M4 | 34 | V8 | 66 | W18 | 98 | H19 | 130 | C13 | 162 | C4 |
| 3 | N1 | 35 | W8 | 67 | Y19 | 99 | H18 | 131* | B13 | 163 | B2 |
| 4 | N2 | 36 | Y8 | 68 | V18 | 100 | G20 | 132 | A13 | 164 | A2 |
| 5 | N3 | 37 | U9 | 69 | V19 | 101 | G19 | 133 | D12 | 165 | B1 |
| 6 | P1 | 38 | V9 | 70 | U19 | 102 | F20 | 134 | C12 | 166 | C2 |
| 7 | P2 | 39 | W9 | 71 | U18 | 103 | G18 | 135 | B12 | 167 | D2 |
| 8 | R1 | 40 | Y9 | 72 | V20 | 104 | F19 | 136 | A12 | 168 | E4 |
| 9 | P3 | 41 | W10 | 73 | U20 | 105 | E20 | 137 | B11 | 169 | C1 |
| 10 | R2 | 42 | V10 | 74 | T18 | 106 | G17 | 138 | C11 | 170 | D1 |
| 11 | T1 | 43 | Y10 | 75 | T19 | 107 | F18 | 139 | A11 | 171 | E3 |
| 12 | P4 | 44 | Y11 | 76 | R18 | 108 | E19 | 140 | A10 | 172 | E1 |
| 13 | T2 | 45 | W11 | 77 | P17 | 109 | D20 | 141 | B10 | 173 | F3 |
| 14 | T3 | 46 | W12 | 78 | R19 | 110 | E18 | 142 | A9 | 174 | G4 |
| 15 | V1 | 47 | V12 | 79 | R20 | 111 | C20 | 143 | B9 | 175 | F2 |
| 16 | V2 | 48 | U12 | 80 | P18 | 112 | E17 | 144 | C9 | 176 | F1 |
| 17 | V3 | 49 | Y13 | 81 | P20 | 113 | D18 | 145 | D9 | 177 | G3 |
| 18 | Y1 | 50 | W13 | 82 | N18 | 114 | A20 | 146 | A8 | 178 | G2 |
| 19 | W3 | 51 | V13 | 83 | N19 | 115 | A19 | 147 | B8 | 179 | G1 |
| 20 | V4 | 52 | Y14 | 84 | N20 | 116 | B17 | 148 | C8 | 180 | H3 |
| 21 | U5 | 53 | W14 | 85 | M17 | 117 | C17 | 149 | A7 | 181 | H2 |
| 22 | Y3 | 54 | Y15 | 86 | M18 | 118 | D16 | 150 | B7 | 182 | H1 |
| 23 | Y4 | 55 | V14 | 87 | M19 | 119* | A18 | 151 | A6 | 183 | J4 |
| 24 | V5 | 56 | W15 | 88 | M20 | 120 | C16 | 152 | C7 | 184 | J3 |
| 25 | W5 | 57 | Y16 | 89 | L19 | 121 | B16 | 153 | B6 | 185 | J2 |
| 26 | Y5 | 58 | U14 | 90 | L18 | 122 | A16 | 154 | A5 | 186 | J1 |
| 27 | V6 | 59 | V15 | 91 | L20 | 123 | C15 | 155 | D7 | 187 | K2 |
| 28 | U7 | 60 | W16 | 92 | K20 | 124 | D14 | 156 | C6 | 188 | K3 |
| 29 | W6 | 61 | Y17 | 93 | K19 | 125 | B15 | 157 | B5 | 189 | K1 |
| 30 | Y6 | 62 | V16 | 94 | K18 | 126 | A15 | 158 | A4 | 190 | L1 |
| 31 | V7 | 63 | Y18 | 95 | K17 | 127 | C14 | 159 | B4 | 191 | L2 |

* I/O 119 is multiplexed with CLK2, I/O 131 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

272-Ball BGA I/O Locations (Sorted by Ball)

| I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball |
|-------|------|-------|------|-------|------|-------|------|-------|------|-------|------|
| 164 | A02 | 121 | B16 | 108 | E19 | 93 | K19 | 11 | T01 | 72 | V20 |
| 160 | A03 | 116 | B17 | 105 | E20 | 92 | K20 | 13 | T02 | 19 | W03 |
| 158 | A04 | 169 | C01 | 176 | F01 | 190 | L01 | 14 | T03 | 25 | W05 |
| 154 | A05 | 166 | C02 | 175 | F02 | 191 | L02 | 74 | T18 | 29 | W06 |
| 151 | A06 | 162 | C04 | 173 | F03 | 90 | L18 | 75 | T19 | 32 | W07 |
| 149 | A07 | 156 | C06 | 107 | F18 | 89 | L19 | 21 | U05 | 35 | W08 |
| 146 | A08 | 152 | C07 | 104 | F19 | 91 | L20 | 28 | U07 | 39 | W09 |
| 142 | A09 | 148 | C08 | 102 | F20 | 0* | M02 | 37 | U09 | 41 | W10 |
| 140 | A10 | 144 | C09 | 179 | G01 | 1 | M03 | 48 | U12 | 45 | W11 |
| 139 | A11 | 138 | C11 | 178 | G02 | 2 | M04 | 58 | U14 | 46 | W12 |
| 136 | A12 | 134 | C12 | 177 | G03 | 85 | M17 | 64 | U16 | 50 | W13 |
| 132 | A13 | 130 | C13 | 174 | G04 | 86 | M18 | 71 | U18 | 53 | W14 |
| 129 | A14 | 127 | C14 | 106 | G17 | 87 | M19 | 70 | U19 | 56 | W15 |
| 126 | A15 | 123 | C15 | 103 | G18 | 88 | M20 | 73 | U20 | 60 | W16 |
| 122 | A16 | 120 | C16 | 101 | G19 | 3 | N01 | 15 | V01 | 66 | W18 |
| 119* | A18 | 117 | C17 | 100 | G20 | 4 | N02 | 16 | V02 | 18 | Y01 |
| 115 | A19 | 111 | C20 | 182 | H01 | 5 | N03 | 17 | V03 | 22 | Y03 |
| 114 | A20 | 170 | D01 | 181 | H02 | 82 | N18 | 20 | V04 | 23 | Y04 |
| 165 | B01 | 167 | D02 | 180 | H03 | 83 | N19 | 24 | V05 | 26 | Y05 |
| 163 | B02 | 161 | D05 | 99 | H18 | 84 | N20 | 27 | V06 | 30 | Y06 |
| 159 | B04 | 155 | D07 | 98 | H19 | 6 | P01 | 31 | V07 | 33 | Y07 |
| 157 | B05 | 145 | D09 | 97 | H20 | 7 | P02 | 34 | V08 | 36 | Y08 |
| 153 | B06 | 133 | D12 | 186 | J01 | 9 | P03 | 38 | V09 | 40 | Y09 |
| 150 | B07 | 124 | D14 | 185 | J02 | 12 | P04 | 42 | V10 | 43 | Y10 |
| 147 | B08 | 118 | D16 | 184 | J03 | 77 | P17 | 47 | V12 | 44 | Y11 |
| 143 | B09 | 113 | D18 | 183 | J04 | 80 | P18 | 51 | V13 | 49 | Y13 |
| 141 | B10 | 109 | D20 | 96 | J17 | 81 | P20 | 55 | V14 | 52 | Y14 |
| 137 | B11 | 172 | E01 | 189 | K01 | 8 | R01 | 59 | V15 | 54 | Y15 |
| 135 | B12 | 171 | E03 | 187 | K02 | 10 | R02 | 62 | V16 | 57 | Y16 |
| 131* | B13 | 168 | E04 | 188 | K03 | 76 | R18 | 65 | V17 | 61 | Y17 |
| 128 | B14 | 112 | E17 | 95 | K17 | 78 | R19 | 68 | V18 | 63 | Y18 |
| 125 | B15 | 110 | E18 | 94 | K18 | 79 | R20 | 69 | V19 | 67 | Y19 |

* I/O 119 is multiplexed with CLK2, I/O 131 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

208-Pin PQFP Signal Locations

| Signal | Pin |
|--------------|---|
| GOE0, GOE1 | 78, 79 |
| TOE / I/O0 | 32 |
| GSET/GRST | 138 |
| TCK | 29 |
| TDI | 30 |
| TDO | 136 |
| TMS | 28 |
| CLK0, CLK1 | 184,185 |
| CLK2 / I/O89 | 162 |
| CLK3 / I/O98 | 173 |
| VCCIO | 137 |
| GND | 3, 12, 19, 27, 39, 48, 58, 69, 77, 88, 99, 113, 121, 128, 135, 150, 164, 170, 179, 191, 199 |
| VCC | 7, 14, 22, 31, 41, 61, 80, 90, 110, 123, 139, 152, 156, 177, 186, 201 |
| NC | 49, 50, 51, 52, 101, 102, 103, 104, 105, 106, 107, 108, 109, 157, 158, 207, 208 |

1. NCs are not to be connected to any active signals, VCC or GND.

208-Pin PQFP I/O Locations

| I/O # | Pin | I/O # | Pin | I/O # | Pin | I/O # | Pin | I/O # | Pin | I/O # | Pin |
|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|
| 0* | 32 | 24 | 65 | 48 | 96 | 72 | 140 | 96 | 171 | 120 | 203 |
| 1 | 33 | 25 | 66 | 49 | 97 | 73 | 141 | 97 | 172 | 121 | 204 |
| 2 | 34 | 26 | 67 | 50 | 98 | 74 | 142 | 98* | 173 | 122 | 205 |
| 3 | 35 | 27 | 68 | 51 | 100 | 75 | 143 | 99 | 174 | 123 | 206 |
| 4 | 36 | 28 | 70 | 52 | 111 | 76 | 144 | 100 | 175 | 124 | 1 |
| 5 | 37 | 29 | 71 | 53 | 112 | 77 | 145 | 101 | 176 | 125 | 2 |
| 6 | 38 | 30 | 72 | 54 | 114 | 78 | 146 | 102 | 178 | 126 | 4 |
| 7 | 40 | 31 | 73 | 55 | 115 | 79 | 147 | 103 | 180 | 127 | 5 |
| 8 | 42 | 32 | 74 | 56 | 116 | 80 | 148 | 104 | 181 | 128 | 6 |
| 9 | 43 | 33 | 75 | 57 | 117 | 81 | 149 | 105 | 182 | 129 | 8 |
| 10 | 44 | 34 | 76 | 58 | 118 | 82 | 151 | 106 | 183 | 130 | 9 |
| 11 | 45 | 35 | 81 | 59 | 119 | 83 | 153 | 107 | 187 | 131 | 10 |
| 12 | 46 | 36 | 82 | 60 | 120 | 84 | 154 | 108 | 188 | 132 | 11 |
| 13 | 47 | 37 | 83 | 61 | 122 | 85 | 155 | 109 | 189 | 133 | 13 |
| 14 | 53 | 38 | 84 | 62 | 124 | 86 | 159 | 110 | 190 | 134 | 15 |
| 15 | 54 | 39 | 85 | 63 | 125 | 87 | 160 | 111 | 192 | 135 | 16 |
| 16 | 55 | 40 | 86 | 64 | 126 | 88 | 161 | 112 | 193 | 136 | 17 |
| 17 | 56 | 41 | 87 | 65 | 127 | 89* | 162 | 113 | 194 | 137 | 18 |
| 18 | 57 | 42 | 89 | 66 | 129 | 90 | 163 | 114 | 195 | 138 | 20 |
| 19 | 59 | 43 | 91 | 67 | 130 | 91 | 165 | 115 | 196 | 139 | 21 |
| 20 | 60 | 44 | 92 | 68 | 131 | 92 | 166 | 116 | 197 | 140 | 23 |
| 21 | 62 | 45 | 93 | 69 | 132 | 93 | 167 | 117 | 198 | 141 | 24 |
| 22 | 63 | 46 | 94 | 70 | 133 | 94 | 168 | 118 | 200 | 142 | 25 |
| 23 | 64 | 47 | 95 | 71 | 134 | 95 | 169 | 119 | 202 | 143 | 26 |

* I/O 89 is multiplexed with CLK2, I/O 98 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

208-Ball fpBGA Signal Locations

| Signal | Ball |
|-----------------|--|
| GOE0, GOE1 | P9, P10 |
| TOE / I/O0 | K1 |
| GSET/GRST | H14 |
| TCK | K2 |
| TDI | K3 |
| TDO | G14 |
| TMS | J1 |
| CLK0, CLK1 | A7, B8 |
| CLK2 / I/O89 | B13 |
| CLK3 / I/O98 | A11 |
| VCCIO | H15 |
| GND | D5, D7, D8, D10, D12, D13, E4, F13, G4, G8, G9, H7, H10, H13, J4, J7, J10, J13, K8, K9, L4, L13, M13, N4, N5, N7, N8, N10, N12 |
| VCC | D4, D6, D9, D11, E13, F4, G7, G10, G13, H4, H8, H9, J8, J9, K4, K7, K10, K13, M4, N6, N9, N11, N13 |
| NC ¹ | C14, E15 |

1. NCs are not to be connected to any active signals, VCC or GND.

208-Ball fpBGA I/O Locations (Sorted by I/O)

| I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball |
|-------|------|-------|------|-------|------|-------|------|-------|------|-------|------|
| 0* | K1 | 24 | T4 | 48 | R12 | 72 | G16 | 96 | C11 | 120 | C3 |
| 1 | L2 | 25 | T5 | 49 | P14 | 73 | F14 | 97 | B11 | 121 | C2 |
| 2 | L1 | 26 | R7 | 50 | P13 | 74 | G15 | 98* | A11 | 122 | B3 |
| 3 | L3 | 27 | P6 | 51 | R13 | 75 | F16 | 99 | B10 | 123 | B2 |
| 4 | M1 | 28 | T6 | 52 | R15 | 76 | E14 | 100 | A10 | 124 | A1 |
| 5 | M2 | 29 | T7 | 53 | P15 | 77 | F15 | 101 | C10 | 125 | D2 |
| 6 | M3 | 30 | R8 | 54 | R16 | 78 | E16 | 102 | B9 | 126 | B1 |
| 7 | N1 | 31 | P8 | 55 | P16 | 79 | D16 | 103 | C9 | 127 | D3 |
| 8 | N3 | 32 | P7 | 56 | N15 | 80 | C16 | 104 | A9 | 128 | E2 |
| 9 | N2 | 33 | T8 | 57 | N14 | 81 | B16 | 105 | A8 | 129 | C1 |
| 10 | P2 | 34 | T9 | 58 | M14 | 82 | D15 | 106 | C8 | 130 | E3 |
| 11 | P1 | 35 | R9 | 59 | N16 | 83 | D14 | 107 | C7 | 131 | D1 |
| 12 | R1 | 36 | R10 | 60 | M15 | 84 | A16 | 108 | B7 | 132 | F2 |
| 13 | R2 | 37 | T10 | 61 | M16 | 85 | C15 | 109 | A6 | 133 | E1 |
| 14 | R3 | 38 | T11 | 62 | L14 | 86 | B15 | 110 | A5 | 134 | F1 |
| 15 | P3 | 39 | T12 | 63 | L15 | 87 | A15 | 111 | C6 | 135 | G2 |
| 16 | T1 | 40 | T13 | 64 | L16 | 88 | B14 | 112 | B6 | 136 | F3 |
| 17 | P4 | 41 | T14 | 65 | K14 | 89* | B13 | 113 | A4 | 137 | H2 |
| 18 | R4 | 42 | P11 | 66 | K15 | 90 | C13 | 114 | A3 | 138 | H3 |
| 19 | R5 | 43 | P12 | 67 | K16 | 91 | A14 | 115 | A2 | 139 | G3 |
| 20 | P5 | 44 | R11 | 68 | J14 | 92 | C12 | 116 | C5 | 140 | G1 |
| 21 | T2 | 45 | T15 | 69 | J15 | 93 | B12 | 117 | B5 | 141 | H1 |
| 22 | R6 | 46 | T16 | 70 | J16 | 94 | A13 | 118 | B4 | 142 | J2 |
| 23 | T3 | 47 | R14 | 71 | H16 | 95 | A12 | 119 | C4 | 143 | J3 |

* I/O 89 is multiplexed with CLK2, I/O 98 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

208-Ball fpBGA I/O Locations (Sorted by Ball)

| I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball | I/O # | Ball |
|-------|------|-------|------|-------|------|-------|------|-------|------|-------|------|
| 124 | A01 | 97 | B11 | 83 | D14 | 143 | J03 | 56 | N15 | 35 | R09 |
| 115 | A02 | 93 | B12 | 82 | D15 | 68 | J14 | 59 | N16 | 36 | R10 |
| 114 | A03 | 89* | B13 | 79 | D16 | 69 | J15 | 11 | P01 | 44 | R11 |
| 113 | A04 | 88 | B14 | 133 | E01 | 70 | J16 | 10 | P02 | 48 | R12 |
| 110 | A05 | 86 | B15 | 128 | E02 | 0* | K01 | 15 | P03 | 51 | R13 |
| 109 | A06 | 81 | B16 | 130 | E03 | 65 | K14 | 17 | P04 | 47 | R14 |
| 105 | A08 | 129 | C01 | 76 | E14 | 66 | K15 | 20 | P05 | 52 | R15 |
| 104 | A09 | 121 | C02 | 78 | E16 | 67 | K16 | 27 | P06 | 54 | R16 |
| 100 | A10 | 120 | C03 | 134 | F01 | 2 | L01 | 32 | P07 | 16 | T01 |
| 98* | A11 | 119 | C04 | 132 | F02 | 1 | L02 | 31 | P08 | 21 | T02 |
| 95 | A12 | 116 | C05 | 136 | F03 | 3 | L03 | 42 | P11 | 23 | T03 |
| 94 | A13 | 111 | C06 | 73 | F14 | 62 | L14 | 43 | P12 | 24 | T04 |
| 91 | A14 | 107 | C07 | 77 | F15 | 63 | L15 | 50 | P13 | 25 | T05 |
| 87 | A15 | 106 | C08 | 75 | F16 | 64 | L16 | 49 | P14 | 28 | T06 |
| 84 | A16 | 103 | C09 | 140 | G01 | 4 | M01 | 53 | P15 | 29 | T07 |
| 126 | B01 | 101 | C10 | 135 | G02 | 5 | M02 | 55 | P16 | 33 | T08 |
| 123 | B02 | 96 | C11 | 139 | G03 | 6 | M03 | 12 | R01 | 34 | T09 |
| 122 | B03 | 92 | C12 | 74 | G15 | 58 | M14 | 13 | R02 | 37 | T10 |
| 118 | B04 | 90 | C13 | 72 | G16 | 60 | M15 | 14 | R03 | 38 | T11 |
| 117 | B05 | 85 | C15 | 141 | H01 | 61 | M16 | 18 | R04 | 39 | T12 |
| 112 | B06 | 80 | C16 | 137 | H02 | 7 | N01 | 19 | R05 | 40 | T13 |
| 108 | B07 | 131 | D01 | 138 | H03 | 9 | N02 | 22 | R06 | 41 | T14 |
| 102 | B09 | 125 | D02 | 71 | H16 | 8 | N03 | 26 | R07 | 45 | T15 |
| 99 | B10 | 127 | D03 | 142 | J02 | 57 | N14 | 30 | R08 | 46 | T16 |

* I/O 89 is multiplexed with CLK2, I/O 98 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

Signal Configuration

ispLSI 5256VA 272-ball BGA

| | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | | | | | | | | | | | | | | | |
|-----|-----------------|-----------------|------------------|-----------------|--|-----------------|---------|------------------|-----------------|---------|---------|---------|---------|---------|---------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|---------|---------|-----------------|---------|
| A | I/O 114 | I/O 115 | CLK2/ I/O 119 | NC ¹ | I/O 122 | I/O 126 | I/O 129 | I/O 132 | I/O 136 | I/O 139 | I/O 140 | I/O 142 | I/O 146 | I/O 149 | I/O 151 | I/O 154 | I/O 158 | I/O 160 | I/O 164 | GND | | | | | | | | | | | | | | | | |
| B | NC ¹ | NC ¹ | NC ¹ | I/O 116 | I/O 121 | I/O 125 | I/O 128 | CLK3/ I/O 131 | I/O 135 | I/O 137 | I/O 141 | I/O 143 | I/O 147 | I/O 150 | I/O 153 | I/O 157 | I/O 159 | NC ¹ | I/O 163 | I/O 165 | | | | | | | | | | | | | | | | |
| C | I/O 111 | NC ¹ | NC ¹ | I/O 117 | I/O 120 | I/O 123 | I/O 127 | I/O 130 | I/O 134 | I/O 138 | CLK0 | I/O 144 | I/O 148 | I/O 152 | I/O 156 | NC ¹ | I/O 162 | NC ¹ | I/O 166 | I/O 169 | | | | | | | | | | | | | | | | |
| D | I/O 109 | NC ¹ | I/O 113 | GND | I/O 118 | VCC | I/O 124 | GND | I/O 133 | VCC | CLK1 | I/O 145 | GND | I/O 155 | VCC | I/O 161 | GND | NC ¹ | I/O 167 | I/O 170 | | | | | | | | | | | | | | | | |
| E | I/O 105 | I/O 108 | I/O 110 | I/O 112 | <p>ispLSI 5256VA</p> <p>Bottom View</p> <table border="1" style="margin: auto;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> | | | | | | | | | | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | I/O 168 | I/O 171 | NC ¹ | I/O 172 |
| GND | GND | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | GND | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | GND | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | GND | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | I/O 102 | I/O 104 | I/O 107 | VCC | | | | | | | | | | | | | I/O 183 | I/O 184 | I/O 185 | I/O 186 | | | | | | | | | | | | | | | | |
| G | I/O 100 | I/O 101 | I/O 103 | I/O 106 | | | | | | | | | | | | | VCC | I/O 188 | I/O 187 | I/O 189 | | | | | | | | | | | | | | | | |
| H | I/O 97 | I/O 98 | I/O 99 | GND | | | | | | | | | | | | | TCK | TMS | I/O 191 | I/O 190 | | | | | | | | | | | | | | | | |
| J | TDO | vccio | SET/ RST | I/O 96 | | | | | | | | | | | | | I/O 2 | I/O 1 | TOE I/O 0 | TDI | | | | | | | | | | | | | | | | |
| K | I/O 92 | I/O 93 | I/O 94 | I/O 95 | | | | | | | | | | | | | GND | I/O 5 | I/O 4 | I/O 3 | | | | | | | | | | | | | | | | |
| L | I/O 91 | I/O 89 | I/O 90 | VCC | I/O 12 | I/O 9 | I/O 7 | I/O 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | I/O 88 | I/O 87 | I/O 86 | I/O 85 | VCC | NC ¹ | I/O 10 | I/O 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | I/O 84 | I/O 83 | I/O 82 | GND | NC ¹ | I/O 14 | I/O 13 | I/O 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | I/O 81 | NC ¹ | I/O 80 | I/O 77 | I/O 73 | I/O 70 | I/O 71 | GND | I/O 64 | VCC | I/O 58 | GND | I/O 48 | GOE1 | VCC | I/O 37 | GND | I/O 28 | VCC | I/O 21 | GND | NC ¹ | NC ¹ | NC ¹ | | | | | | | | | | | | |
| R | I/O 79 | I/O 78 | I/O 76 | VCC | I/O 72 | I/O 69 | I/O 68 | I/O 65 | I/O 62 | I/O 59 | I/O 55 | I/O 51 | I/O 47 | GOE0 | I/O 42 | I/O 38 | I/O 34 | I/O 31 | I/O 27 | I/O 24 | I/O 20 | I/O 17 | I/O 16 | I/O 15 | | | | | | | | | | | | |
| T | NC ¹ | I/O 75 | I/O 74 | NC ¹ | NC ¹ | NC ¹ | I/O 66 | NC ¹ | I/O 60 | I/O 56 | I/O 53 | I/O 50 | I/O 46 | I/O 45 | I/O 41 | I/O 39 | I/O 35 | I/O 32 | I/O 29 | I/O 25 | NC ¹ | I/O 19 | NC ¹ | NC ¹ | | | | | | | | | | | | |
| U | I/O 73 | I/O 70 | I/O 71 | GND | I/O 64 | VCC | I/O 58 | GND | I/O 48 | GOE1 | VCC | I/O 37 | GND | I/O 28 | VCC | I/O 21 | GND | NC ¹ | NC ¹ | NC ¹ | | | | | | | | | | | | | | | | |
| V | I/O 72 | I/O 69 | I/O 68 | I/O 65 | I/O 62 | I/O 59 | I/O 55 | I/O 51 | I/O 47 | GOE0 | I/O 42 | I/O 38 | I/O 34 | I/O 31 | I/O 27 | I/O 24 | I/O 20 | I/O 17 | I/O 16 | I/O 15 | | | | | | | | | | | | | | | | |
| W | NC ¹ | NC ¹ | I/O 66 | NC ¹ | I/O 60 | I/O 56 | I/O 53 | I/O 50 | I/O 46 | I/O 45 | I/O 41 | I/O 39 | I/O 35 | I/O 32 | I/O 29 | I/O 25 | NC ¹ | I/O 19 | NC ¹ | NC ¹ | | | | | | | | | | | | | | | | |
| Y | NC ¹ | I/O 67 | I/O 63 | I/O 61 | I/O 57 | I/O 54 | I/O 52 | I/O 49 | NC ¹ | I/O 44 | I/O 43 | I/O 40 | I/O 36 | I/O 33 | I/O 30 | I/O 26 | I/O 23 | I/O 22 | NC ¹ | I/O 18 | | | | | | | | | | | | | | | | |

1. NCs are not to be connected to any active signals, Vcc or GND.

272 BGA/5256VA

Note: Ball A1 indicator dot on top side of package.

Signal Configuration

ispLSI 5256VA 208-ball fpBGA

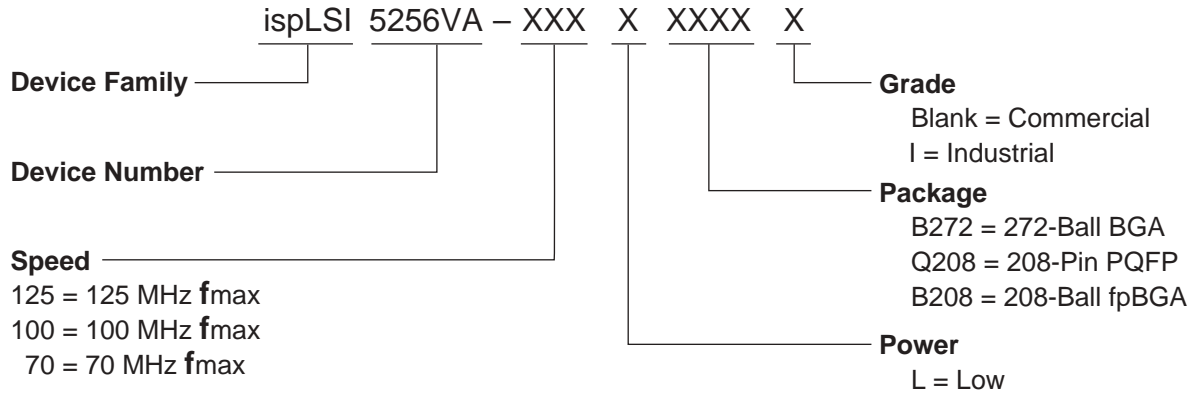
| | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | | | | | | | | | | | | | | | | |
|----------|--------|-----------------|-----------------|----------------|---|----------------|---------|---------|----------|---------|---------|---------|--------------|----------|---------|---------|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|---------|---------|----------|
| A | I/O 84 | I/O 87 | I/O 91 | I/O 94 | I/O 95 | CLK3/ I/O98 | I/O 100 | I/O 104 | I/O 105 | CLK 0 | I/O 109 | I/O 110 | I/O 113 | I/O 114 | I/O 115 | I/O 124 | A | | | | | | | | | | | | | | | | |
| B | I/O 81 | I/O 86 | I/O 88 | CLK2/ I/O89 | I/O 93 | I/O 97 | I/O 99 | I/O 102 | CLK 1 | I/O 108 | I/O 112 | I/O 117 | I/O 118 | I/O 122 | I/O 123 | I/O 126 | B | | | | | | | | | | | | | | | | |
| C | I/O 80 | I/O 85 | NC ¹ | I/O 90 | I/O 92 | I/O 96 | I/O 101 | I/O 103 | I/O 106 | I/O 107 | I/O 111 | I/O 116 | I/O 119 | I/O 120 | I/O 121 | I/O 129 | C | | | | | | | | | | | | | | | | |
| D | I/O 79 | I/O 82 | I/O 83 | GND | GND | VCC | GND | VCC | GND | GND | VCC | GND | VCC | I/O 127 | I/O 125 | I/O 131 | D | | | | | | | | | | | | | | | | |
| E | I/O 78 | NC ¹ | I/O 76 | VCC | <div style="border: 1px solid black; padding: 5px; display: inline-block;"> <table border="1" style="border-collapse: collapse;"> <tr> <td>VCC</td> <td>GND</td> <td>GND</td> <td>VCC</td> </tr> <tr> <td>GND</td> <td>VCC</td> <td>VCC</td> <td>GND</td> </tr> <tr> <td>GND</td> <td>VCC</td> <td>VCC</td> <td>GND</td> </tr> <tr> <td>VCC</td> <td>GND</td> <td>GND</td> <td>VCC</td> </tr> </table> </div> <p>ispLSI 5256VA Bottom View</p> | | | | | | | | VCC | GND | GND | VCC | GND | VCC | VCC | GND | GND | VCC | VCC | GND | VCC | GND | GND | VCC | GND | I/O 130 | I/O 128 | I/O 133 | E |
| VCC | GND | GND | VCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | VCC | VCC | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | VCC | VCC | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VCC | GND | GND | VCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | I/O 75 | I/O 77 | I/O 73 | GND | VCC | I/O 136 | I/O 132 | I/O 134 | F | | | | | | | | | | | | | | | | | | | | | | | | |
| G | I/O 72 | I/O 74 | TDO | VCC | GND | I/O 139 | I/O 135 | I/O 140 | G | | | | | | | | | | | | | | | | | | | | | | | | |
| H | I/O 71 | VCCIO | GSET/ GRST | GND | VCC | I/O 138 | I/O 137 | I/O 141 | H | | | | | | | | | | | | | | | | | | | | | | | | |
| J | I/O 70 | I/O 69 | I/O 68 | GND | GND | VCC | VCC | GND | GND | I/O 143 | I/O 142 | TMS | J | | | | | | | | | | | | | | | | | | | | |
| K | I/O 67 | I/O 66 | I/O 65 | VCC | VCC | GND | GND | VCC | VCC | VCC | TDI | TCK | TOE/ I/O0 | K | | | | | | | | | | | | | | | | | | | |
| L | I/O 64 | I/O 63 | I/O 62 | GND | GND | I/O 3 | I/O 1 | I/O 2 | L | | | | | | | | | | | | | | | | | | | | | | | | |
| M | I/O 61 | I/O 60 | I/O 58 | GND | VCC | I/O 6 | I/O 5 | I/O 4 | M | | | | | | | | | | | | | | | | | | | | | | | | |
| N | I/O 59 | I/O 56 | I/O 57 | VCC | GND | VCC | GND | VCC | GND | GND | VCC | GND | GND | I/O 8 | I/O 9 | I/O 7 | N | | | | | | | | | | | | | | | | |
| P | I/O 55 | I/O 53 | I/O 49 | I/O 50 | I/O 43 | I/O 42 | GOE1 | GOE0 | I/O 31 | I/O 32 | I/O 27 | I/O 20 | I/O 17 | I/O 15 | I/O 10 | I/O 11 | P | | | | | | | | | | | | | | | | |
| R | I/O 54 | I/O 52 | I/O 47 | I/O 51 | I/O 48 | I/O 44 | I/O 36 | I/O 35 | I/O 30 | I/O 26 | I/O 22 | I/O 19 | I/O 18 | I/O 14 | I/O 13 | I/O 12 | R | | | | | | | | | | | | | | | | |
| T | I/O 46 | I/O 45 | I/O 41 | I/O 40 | I/O 39 | I/O 38 | I/O 37 | I/O 34 | I/O 33 | I/O 29 | I/O 28 | I/O 25 | I/O 24 | I/O 23 | I/O 21 | I/O 16 | T | | | | | | | | | | | | | | | | |

208 fpBGA/5256VA

1. NCs are not to be connected to any active signals, Vcc or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212/5256VA

Ordering Information

COMMERCIAL

| FAMILY | f _{max} (MHz) | t _{pd} (ns) | ORDERING NUMBER | PACKAGE |
|--------|------------------------|----------------------|------------------------|----------------|
| ispLSI | 125 | 7.5 | ispLSI 5256VA-125LB272 | 272-Ball BGA |
| | 125 | 7.5 | ispLSI 5256VA-125LQ208 | 208-Pin PQFP |
| | 125 | 7.5 | ispLSI 5256VA-125LB208 | 208-Ball fpBGA |
| | 100 | 10 | ispLSI 5256VA-100LB272 | 272-Ball BGA |
| | 100 | 10 | ispLSI 5256VA-100LQ208 | 208-Pin PQFP |
| | 100 | 10 | ispLSI 5256VA-100LB208 | 208-Ball fpBGA |
| | 70 | 15 | ispLSI 5256VA-70LB272 | 272-Ball BGA |
| | 70 | 15 | ispLSI 5256VA-70LQ208 | 208-Pin PQFP |
| | 70 | 15 | ispLSI 5256VA-70LB208 | 208-Ball fpBGA |

Table 2-0041A/5256VA

INDUSTRIAL

| FAMILY | f _{max} (MHz) | t _{pd} (ns) | ORDERING NUMBER | PACKAGE |
|--------|------------------------|----------------------|------------------------|--------------|
| ispLSI | 70 | 15 | ispLSI 5256VA-70LB272I | 272-Ball BGA |

Table 2-0041B/5256VA