To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Renesas Technology Corp.

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Description

The M16C/62M group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 100-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, low voltage (2.2V to 3.6V), they are capable of executing instructions at high speed. They also feature a built-in multiplier and DMAC, making them ideal for controlling office, communications, industrial equipment, and other high-speed processing applications.
The M16C/62M group includes a wide range of products with different internal memory types and sizes and various package types.

Features

- Memory capacity .... ROM (See Figure 1.1.4. ROM Expansion)
  RAM 10K to 20K bytes
- Shortest instruction execution time ...... 100ns (f(X_{IN})=10MHz, V_{CC}=2.7V to 3.6V)
  142.9ns (f(X_{IN})=7MHz, V_{CC}=2.2V to 3.6V with software one-wait)
- Supply voltage .... 2.7V to 3.6V (f(X_{IN})=10MHz, without software wait)
  2.4V to 2.7V (f(X_{IN})=7MHz, without software wait)
  2.2V to 2.4V (f(X_{IN})=7MHz with software one-wait)
- Low power consumption .... 28.5mW (V_{CC} = 3V, f(X_{IN})=10MHz, without software wait)
- Interrupts .... 25 internal and 8 external interrupt sources, 4 software interrupt sources; 7 levels (including key input interrupt)
- Multifunction 16-bit timer .... 5 output timers + 6 input timers
- Serial I/O .... 5 channels
  (3 for UART or clock synchronous, 2 for clock synchronous)
- DMAC .... 2 channels (trigger: 24 sources)
- A-D converter .... 10 bits X 8 channels (Expandable up to 10 channels)
- D-A converter .... 8 bits X 2 channels
- CRC calculation circuit .... 1 circuit
- Watchdog timer .... 1 line
- Programmable I/O .... 87 lines
- Input port .... 1 line ($P8_5$ shared with $\overline{NMI}$ pin)
- Memory expansion .... Available (to a maximum of 1M bytes)
- Chip select output .... 4 lines
- Clock generating circuit .... 2 built-in clock generation circuits
  (built-in feedback resistor, and external ceramic or quartz oscillator)

Applications

Audio, cameras, office equipment, communications equipment, portable equipment

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Pin Configuration

Figures 1.1.1 and 1.1.2 show the pin configurations (top view).

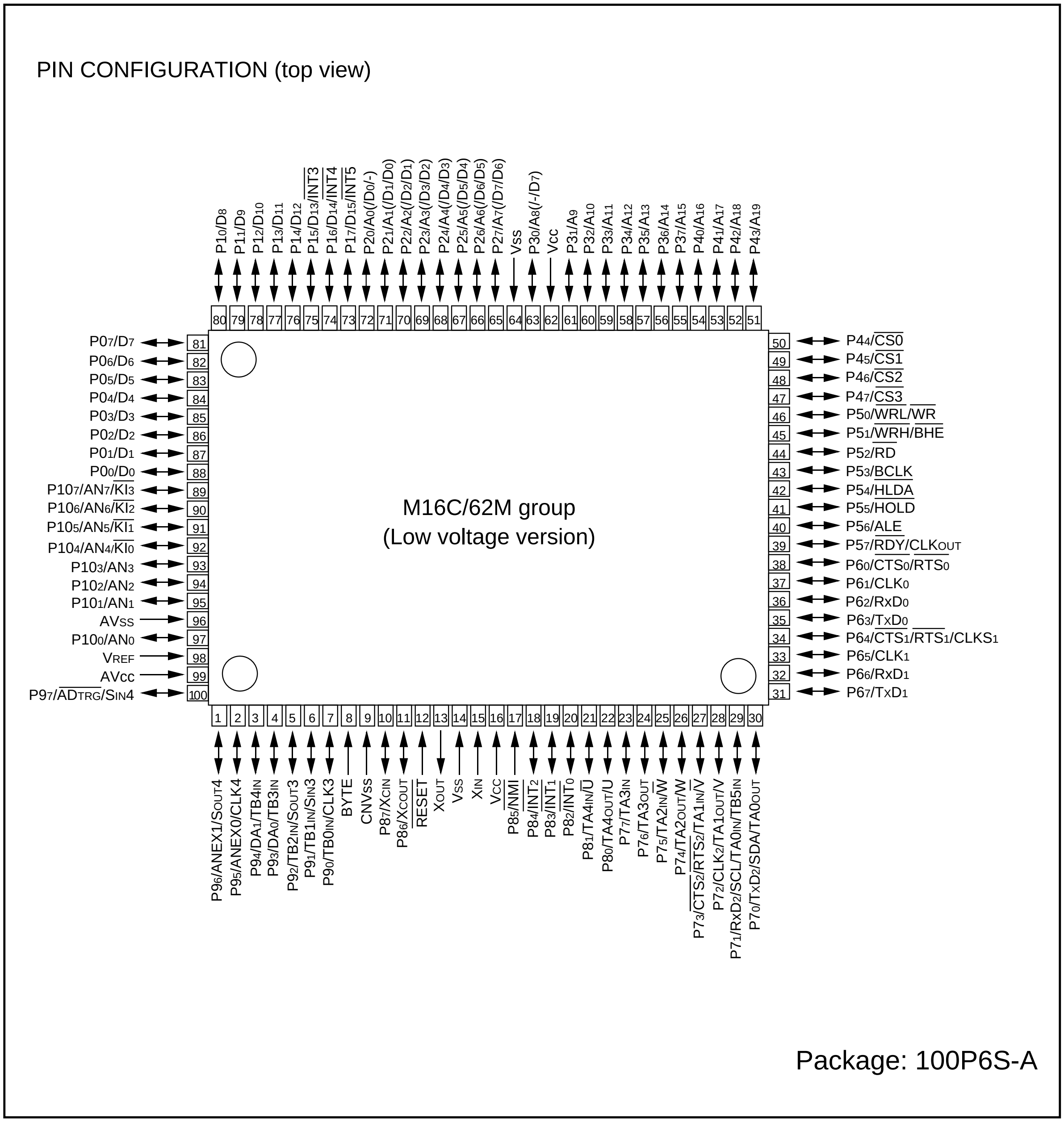

Figure 1.1.1. Pin configuration (top view)

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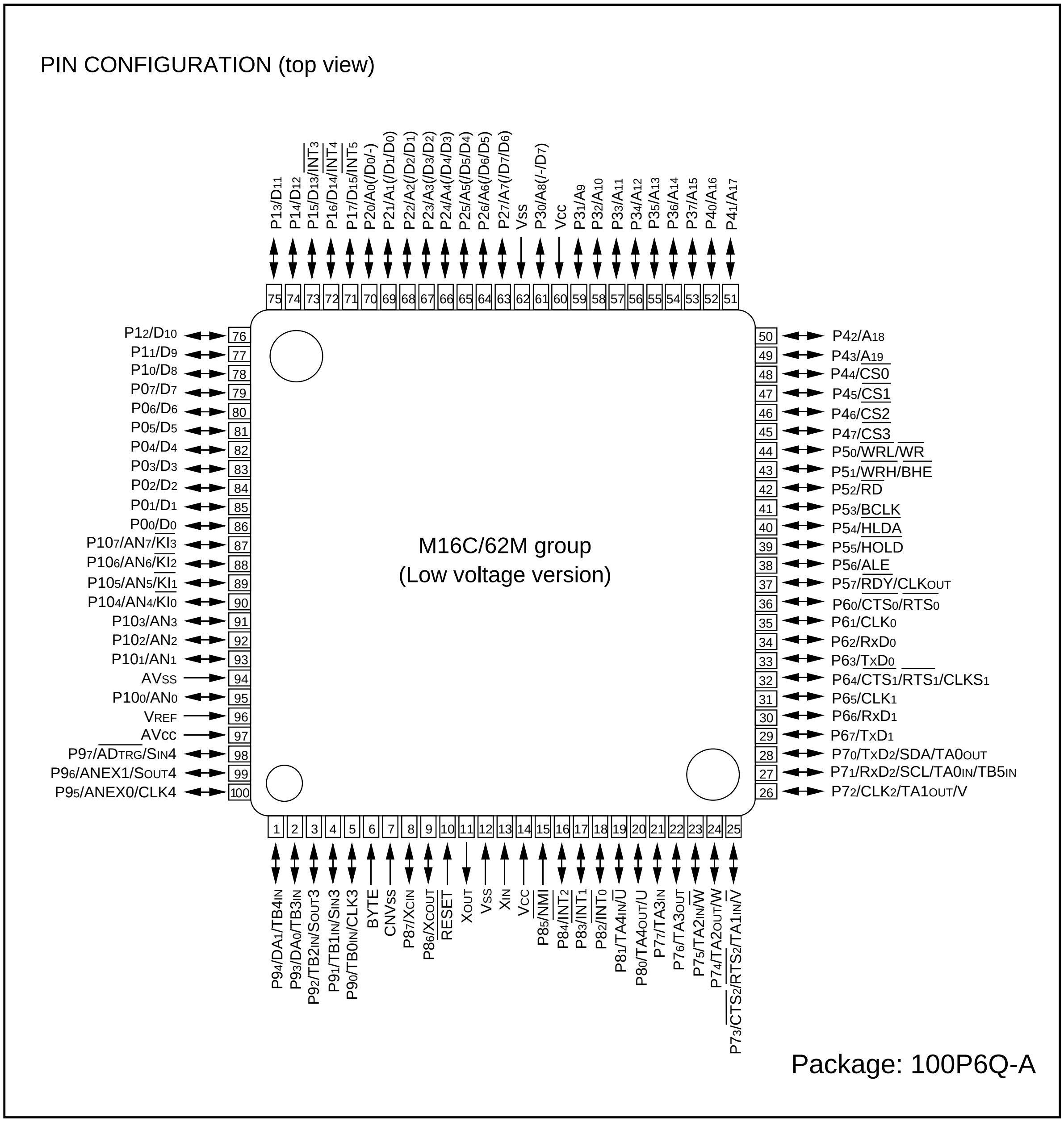

Figure 1.1.2. Pin configuration (top view)

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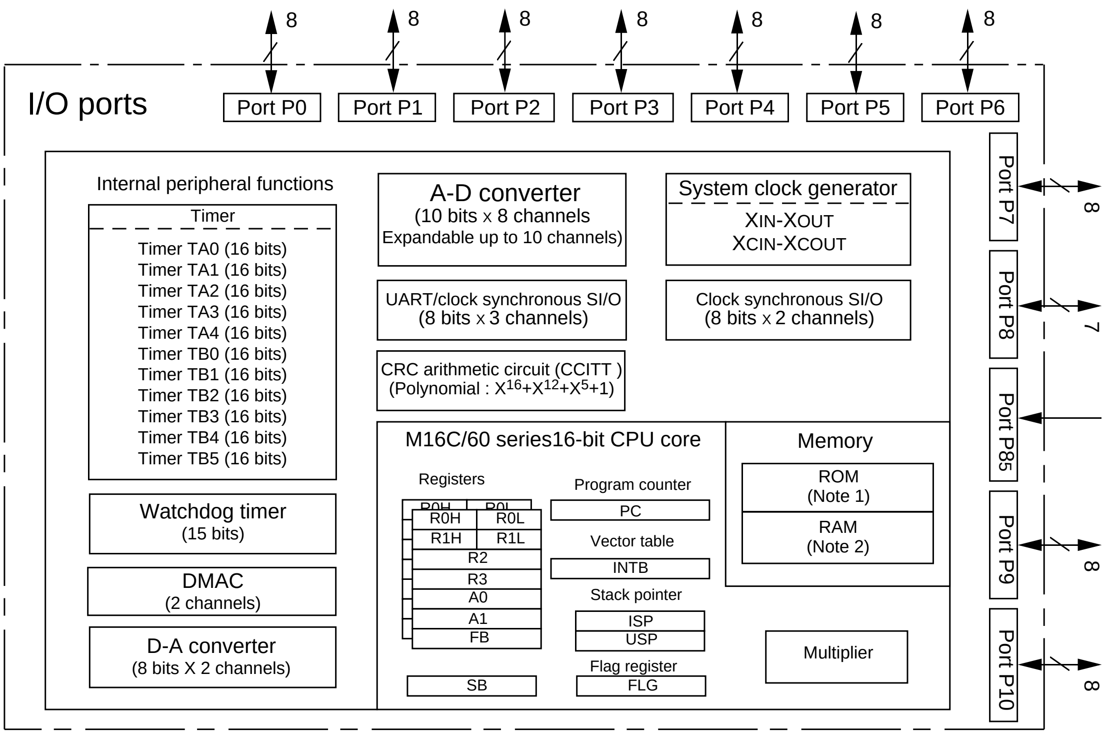
Block Diagram

Figure 1.1.3 is a block diagram of the M16C/62M group.



Note 1: ROM size depends on MCU type.
Note 2: RAM size depends on MCU type.

Figure 1.1.3. Block diagram of M16C/62M group

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Performance Outline

Table 1.1.1 is a performance outline of M16C/62M group.

Table 1.1.1. Performance outline of M16C/62M group

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		100ns(f(X_{IN})=10MHz, V_{CC}=2.7V to 3.6V) 142.9ns (f(X_{IN})=7MHz, V_{CC}=2.2V to 3.6V with software one-wait)
Memory capacity	ROM	(See the figure 1.1.4. ROM Expansion)
	RAM	10K to 20K bytes
I/O port	P0 to P10 (except $P8_5$)	8 bits x 10, 7 bits x 1
Input port	$P8_5$	1 bit x 1
Multifunction timer	TA0, TA1, TA2, TA3, TA4	16 bits x 5
	TB0, TB1, TB2, TB3, TB4, TB5	16 bits x 6
Serial I/O	UART0, UART1, UART2	(UART or clock synchronous) x 3
	SI/O3, SI/O4	(Clock synchronous) x 2
A-D converter		10 bits x (8 + 2) channels
D-A converter		8 bits x 2
DMAC		2 channels (trigger: 24 sources)
CRC calculation circuit		CRC-CCITT
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		25 internal and 8 external sources, 4 software sources, 7 levels
Clock generating circuit		2 built-in clock generation circuits (built-in feedback resistor, and external ceramic or quartz oscillator)
Supply voltage		2.7V to 3.6V (f(X_{IN})=10MHz, without software wait) 2.4V to 2.7V (f(X_{IN})=7MHz, without software wait) 2.2V to 2.4V (f(X_{IN})=7MHz with software one-wait)
Power consumption		28.5mW (f(X_{IN}) =10MHz, V_{CC}=3V without software wait)
I/O characteristics	I/O withstand voltage	3V
	Output current	1mA
Memory expansion		Available (to a maximum of 1M bytes)
Device configuration		CMOS high performance silicon gate
Package		100-pin plastic mold QFP

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Mitsubishi plans to release the following products in the M16C/62M group:
(1) Support for mask ROM version and Flash memory version
(2) ROM capacity
(3) Package
100P6S-A : Plastic molded QFP (mask ROM and flash memory versions)
100P6Q-A : Plastic molded QFP (mask ROM and flash memory versions)

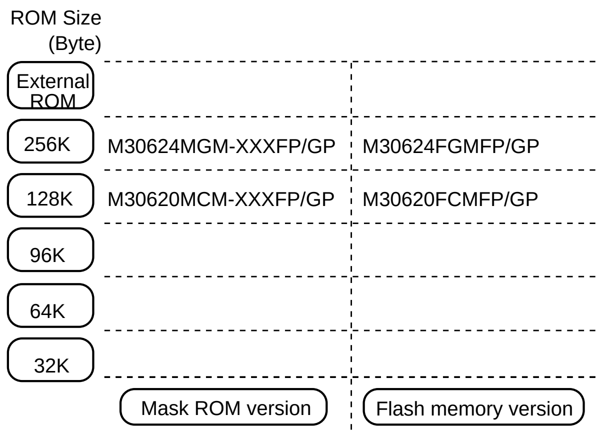

Figure 1.1.4. ROM expansion

The M16C/62M group products currently supported are listed in Table 1.1.2.

Table 1.1.2. M16C/62M group

June, 2001

Type No	ROM capacity	RAM capacity	Package type	Remarks
M30620MCM-XXXFP	128K byte	10K byte	100P6S-A	mask ROM version
M30620MCM-XXXGP			100P6Q-A	
M30624MGM-XXXFP	256K byte	20K byte	100P6S-A	
M30624MGM-XXXGP			100P6Q-A	
M30620FCMFP	128K byte	10K byte	100P6S-A	Flash memory 3V version
M30620FCMGP			100P6Q-A	
M30624FGMFP	256K byte	20K byte	100P6S-A	
M30624FGMGP			100P6Q-A	

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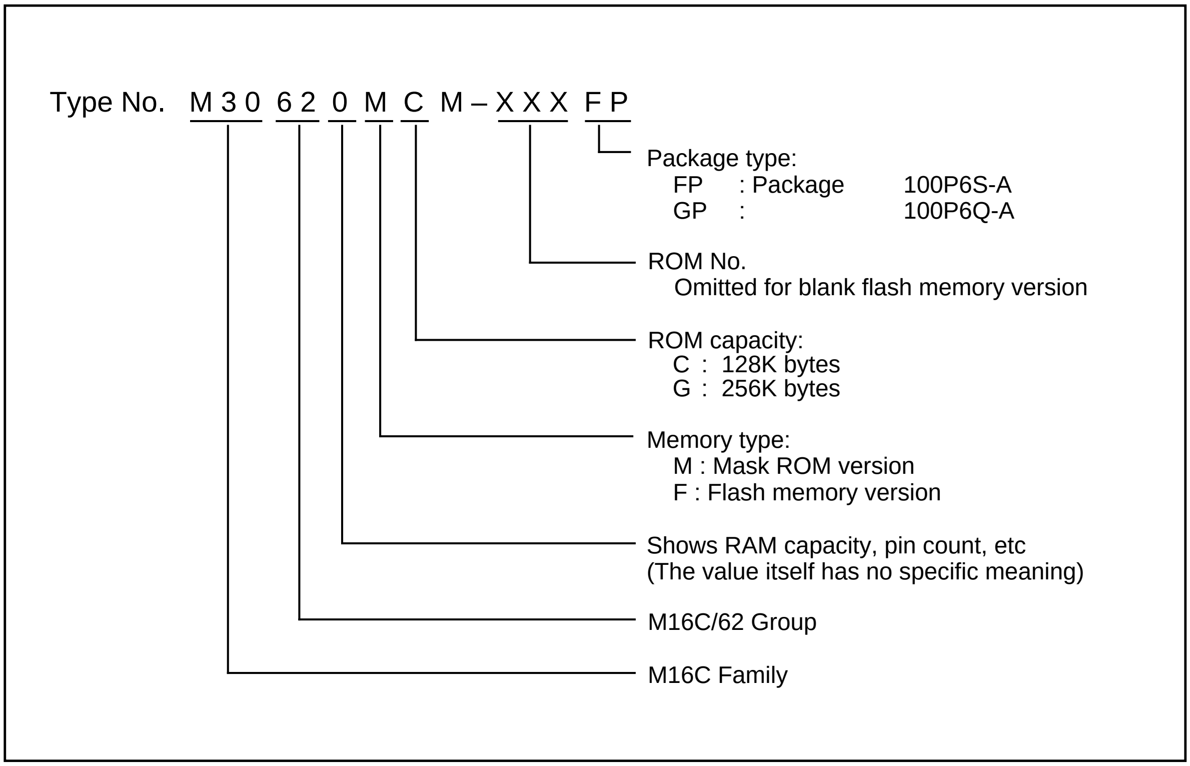

Figure 1.1.5. Type No., memory size, and package

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Table 1.26.1. Absolute maximum ratings

Symbol	Parameter		Condition	Rated value	Unit
V_{CC}	Supply voltage		$V_{CC}=AV_{CC}$	- 0.3 to 4.6	V
AV_{CC}	Analog supply voltage		$V_{CC}=AV_{CC}$	- 0.3 to 4.6	V
V_I	Input voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_2$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_7$, $P10_0$ to $P10_7$, V_{REF}, X_{IN}		- 0.3 to Vcc + 0.3	V
		$P7_0$, $P7_1$		- 0.3 to 4.6	V
V_O	Output voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_2$ to $P7_7$, $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$ to $P9_7$, $P10_0$ to $P10_7$, X_{OUT}		- 0.3 to Vcc + 0.3	V
		$P7_0$, $P7_1$		- 0.3 to 4.6	V
P_d	Power dissipation		Topr=25 °C	300	mW
T_{opr}	Operating ambient temperature			- 20 to 85 / -40 to 85 (Note)	°C
T_{stg}	Storage temperature			- 65 to 150	°C

Note : Specify a product of -40°C to 85°C to use it.

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Table 1.26.2. Recommended operating conditions (referenced to V_{CC} = 2.2V to 3.6V at Topr = –20°C to 85°C / – 40°C to 85°C (Note 3) unless otherwise specified)

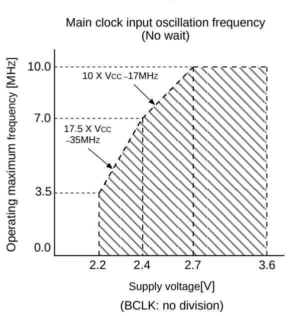
Symbol	Parameter			Standard Min.	Standard Typ.	Standard Max.	Unit
V_{CC}	Supply voltage			2.2	3.0	3.6	V
AV_{CC}	Analog supply voltage				Vcc		V
V_{SS}	Supply voltage				0		V
AV_{SS}	Analog supply voltage				0		V
V_{IH}	HIGH input voltage	$P3_1$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_2$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_7$, $P10_0$ to $P10_7$, X_{IN}, RESET, CNV_{SS}, BYTE		0.8Vcc		Vcc	V
		$P7_0$, $P7_1$		0.8Vcc		4.6	V
		$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ (during single-chip mode)		0.8Vcc		Vcc	V
		$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ (data input function during memory expansion and microprocessor modes)		0.5Vcc		Vcc	V
V_{IL}	LOW input voltage	$P3_1$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_7$, $P10_0$ to $P10_7$, X_{IN}, RESET, CNV_{SS}, BYTE		0		0.2Vcc	V
		$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ (during single-chip mode)		0		0.2Vcc	V
		$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ (data input function during memory expansion and microprocessor modes)		0		0.16Vcc	V
$I_{OH (peak)}$	HIGH peak output current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_2$ to $P7_7$, $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$ to $P9_7$, $P10_0$ to $P10_7$				- 10.0	mA
$I_{OH (avg)}$	HIGH average output current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_2$ to $P7_7$, $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$ to $P9_7$, $P10_0$ to $P10_7$				- 5.0	mA
$I_{OL (peak)}$	LOW peak output current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$ to $P9_7$, $P10_0$ to $P10_7$				10.0	mA
$I_{OL (avg)}$	LOW average output current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_4$, $P8_6$, $P8_7$, $P9_0$ to $P9_7$, $P10_0$ to $P10_7$				5.0	mA
$f (X_{IN})$	Main clock input oscillation frequency	No wait	Vcc=2.7V to 3.6V	0		10	MHz
			Vcc=2.4V to 2.7V	0		10 X Vcc - 17	MHz
			Vcc=2.2V to 2.4V	0		17.5 X Vcc - 35	MHz
		with wait	Vcc=2.7V to 3.6V	0		10	MHz
			Vcc=2.2V to 2.7V	0		6 X Vcc - 6.2	MHz
$f (X_{CIN})$	Subclock oscillation frequency				32.768	50	kHz

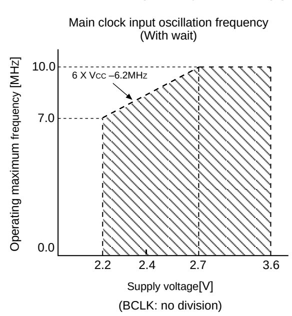
Note 1: The mean output current is the mean value within 100ms.

Note 2: The total I_{OL} (peak) for ports P0, P1, P2, $P8_6$, $P8_7$, P9, and P10 must be 80mA max. The total I_{OH} (peak) for ports P0, P1, P2, $P8_6$, $P8_7$, P9, and P10 must be 80mA max. The total I_{OL} (peak) for ports P3, P4, P5, P6, P7, and $P8_0$ to $P8_4$ must be 80mA max. The total I_{OH} (peak) for ports P3, P4, P5, P6, $P7_2$ to $P7_7$, and $P8_0$ to $P8_4$ must be 80mA max.

Note 3: Specify a product of -40°C to 85°C to use it.

Note 4: Relationship between main clock oscillation frequency and supply voltage.





Flash memory version program voltage and read operation voltage characteristics

Flash program voltage	Flash read operation voltage
Vcc=2.7V to 3.6V	Vcc=2.4V to 3.6V
Vcc=2.7V to 3.4V	Vcc=2.2V to 2.4V

Note 5: Execute case without wait, program / erase of flash memory by V_{CC}=2.7V to 3.6V and f(BCLK) ≤ 6.25 MHz. Execute case with wait, program / erase of flash memory by V_{CC}=2.7V to 3.6V and f(BCLK) ≤ 10.0 MHz.

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Table 1.26.3. Electrical characteristics (referenced to V_{CC} = 2.7V to 3.6V, V_{SS} = 0V at Topr = – 20°C to 85°C / – 40°C to 85°C (Note 1), f(X_{IN}) = 10MHz without wait unless otherwise specified)

Symbol	Parameter			Measuring condition		Standard Min	Standard Typ.	Standard Max.	Unit
V_{OH}	HIGH output voltage	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P77, P80 to P84, P86,P87, P90 to P97, P100 to P107		I_{OH}=–1mA		2.5			V
V_{OH}	HIGH output voltage	X_{OUT}	HIGHPOWER	I_{OH}=–0.1mA		2.5			V
			LOWPOWER	I_{OH}=–50μA		2.5			
	HIGH output voltage	X_{COUT}	HIGHPOWER	With no load applied			3.0		V
			LOWPOWER	With no load applied			1.6		
V_{OL}	LOW output voltage	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P84, P86,P87, P90 to P97, P100 to P107		I_{OL}=1mA				0.5	V
V_{OL}	LOW output voltage	X_{OUT}	HIGHPOWER	I_{OL}=0.1mA				0.5	V
			LOWPOWER	I_{OL}=50μA				0.5	
	LOW output voltage	X_{COUT}	HIGHPOWER	With no load applied			0		V
			LOWPOWER	With no load applied			0		
$V_{T+}-V_{T-}$	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT_0}$ to $\overline{INT_5}$, $\overline{NMI}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$ to $\overline{CTS_2}$, SCL, SDA, CLK0 to CLK4, TA2OUT to TA4OUT, $\overline{KI_0}$ to $\overline{KI_3}$, RxD0 to RxD2, SIN3, SIN4				0.2		0.8	V
$V_{T+}-V_{T-}$	Hysteresis	$\overline{RESET}$				0.2		1.8	V
I_{IH}	HIGH input current	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P107, XIN, $\overline{RESET}$, CNVss, BYTE		V_I=3V				4.0	μA
I_{IL}	LOW input current	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P107, XIN, $\overline{RESET}$, CNVss, BYTE		V_I=0V				–4.0	μA
R_{PULLUP}	Pull-up resistance	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P77, P80 to P84, P86,P87, P90 to P97, P100 to P107		V_I=0V		20	75	330	kΩ
R_{fXIN}	Feedback resistance	X_{IN}					3.0		MΩ
R_{fXCIN}	Feedback resistance	X_{CIN}					10.0		MΩ
V_{RAM}	RAM retention voltage			When clock is stopped		2.0			V
I_{CC}	Power supply current	In single-chip mode, the output pins are open and other pins are V_{SS}		Mask ROM version	f(X_{IN})=10MHz Square wave, no division		9.5	21.25	mA
				Flash memory 3V version	f(X_{IN})=10MHz Square wave, no division		12.0	21.25	mA
				Mask ROM version, flash memory 3V version	f(X_{CIN})=32kHz Square wave		45.0		μA
				Flash memory 3V version program	f(X_{IN})=10MHz Square wave, division by 2		14.0		mA
				Flash memory 3V version erase	f(X_{IN})=10MHz Square wave, division by 2		17.0		mA
				Mask ROM version, flash memory 3V version	f(X_{CIN})=32kHz When a WAIT instruction is executed. Oscillation capacity High (Note 2)		2.8		μA
					f(X_{CIN})=32kHz When a WAIT instruction is executed. Oscillation capacity Low (Note 2)		0.9		μA
					When clock is stopped Topr=25°C			1.0	μA
					When clock is stopped Topr=85°C			20.0	

Note 1: Specify a product of -40°C to 85°C to use it.

Note 2: With one timer operated using f_{C32}.

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Table 1.26.4. A-D conversion characteristics (referenced to VCC = AVCC = VREF = 2.4V to 3.6V, VSS = AVSS = 0V, at Topr = – 20°C to 85°C / – 40°C to 85°C (Note 2), f(XIN)=10MHz unless otherwise specified)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max	
–	Resolution		VREF =VCC			10	Bits
–	Absolute accuracy	Sample & hold function not available (8 bit)	VREF =VCC=3V, fAD=fAD/2			±2	LSB
RLADDER	Ladder resistance		VREF =VCC	10		40	kΩ
tCONV	Conversion time(8bit)			9.8			µs
VREF	Reference voltage			2.4		VCC	V
VIA	Analog input voltage			0		VREF	V

Note 1: Connect AVCC pin to VCC pin and apply the same electric potential.

Note 2: Specify a product of –40°C to 85°C to use it.

Table 1.26.5. D-A conversion characteristics (referenced to VCC = 2.4V to 3.6V, VSS = AVSS = 0V, VREF=3V, at Topr = – 20°C to 85°C / – 40°C to 85°C (Note 2), f(XIN)=10MHz unless otherwise specified)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setup time				3	µs
RO	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(Note1)			1.0	mA

Note 1: This applies when using one D-A converter, with the D-A register for the unused D-A converter set to "00_{16}". The A-D converter's ladder resistance is not included.

Also, when D-A register contents are not "00_{16}", the current IVREF always flows even though Vref may have been set to be "unconnected" by the A-D control register.

Note 2: Specify a product of –40°C to 85°C to use it.

Table 1.26.6. Flash memory version electrical characteristics (referenced to VCC = 2.7V to 3.6V, at Topr = 0°C to 60°C unless otherwise specified)

Parameter	Standard			Unit
	Min.	Typ.	Max	
Page program time		6	120	ms
Block erase time		50	600	ms
Erase all unlocked blocks time		50 X n (Note)	600 X n (Note)	ms
Lock bit program time		6	120	ms

Note : n denotes the number of block erases.

Table 1.26.7. Flash memory version program voltage and read operation voltage characteristics (Topr = 0°C to 60°C)

Flash program voltage	Flash read operation voltage
VCC=2.7V to 3.6V	VCC=2.4V to 3.6V
VCC=2.7V to 3.4V	VCC=2.2V to 2.4V

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Timing requirements
(referenced to VCC = 3V, VSS = 0V, at Topr = – 20°C to 85°C / – 40°C to 85°C (*) unless otherwise specified)
* : Specify a product of -40°C to 85°C to use it.

Table 1.26.8. External clock input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	100		ns
$t_{w(H)}$	External clock input HIGH pulse width	40		ns
$t_{w(L)}$	External clock input LOW pulse width	40		ns
t_r	External clock rise time		18	ns
t_f	External clock fall time		18	ns

Table 1.26.9. Memory expansion and microprocessor modes

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (no wait)		(Note)	ns
$t_{ac2(RD-DB)}$	Data input access time (with wait)		(Note)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note)	ns
$t_{su(DB-RD)}$	Data input setup time	80		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	60		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ input setup time	80		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time		100	ns

Note: Calculated according to the BCLK frequency as follows:

$$t_{ac1(RD-DB)} = \frac{10^9}{f(BCLK) \times 2} - 90 \quad [ns]$$

$$t_{ac2(RD-DB)} = \frac{3 \times 10^9}{f(BCLK) \times 2} - 90 \quad [ns]$$

$$t_{ac3(RD-DB)} = \frac{3 \times 10^9}{f(BCLK) \times 2} - 90 \quad [ns]$$

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Timing requirements
(referenced to VCC = 3V, VSS = 0V, at Topr = – 20°C to 85°C / – 40°C to 85°C (*) unless otherwise specified)
* : Specify a product of –40°C to 85°C to use it.

Table 1.26.10. Timer A input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	60		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	60		ns

Table 1.26.11. Timer A input (gating input in timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	300		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	300		ns

Table 1.26.12. Timer A input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 1.26.13. Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 1.26.14. Timer A input (up/down input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	3000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1500		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1500		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	600		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	600		ns

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Timing requirements

(referenced to VCC = 3V, VSS = 0V, at Topr = – 20°C to 85°C / – 40°C to 85°C (*) unless otherwise specified)

* : Specify a product of –40°C to 85°C to use it.

Table 1.26.15. Timer B input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	160		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	160		ns

Table 1.26.16. Timer B input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 1.26.17. Timer B input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 1.26.18. A-D trigger input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1500		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	200		ns

Table 1.26.19. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_{d(C-Q)}$	TxDi output delay time		160	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	50		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 1.26.20. External interrupt $\overline{INTi}$ inputs

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	380		ns

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Switching characteristics (referenced to VCC = 3V, VSS = 0V at Topr = – 20°C to 85°C / – 40°C to 85°C (Note 3), CM15 = “1” unless otherwise specified)

Table 1.26.21. Memory expansion and microprocessor modes (with no wait)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.26.1		60	ns
$t_{h(BCLK-AD)}$	Address output hold time (BCLK standard)		4		ns
$t_{h(RD-AD)}$	Address output hold time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address output hold time (WR standard)		0		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			60	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (BCLK standard)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			60	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		– 4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			60	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			60	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (BCLK standard)			80	ns
$t_{h(BCLK-DB)}$	Data output hold time (BCLK standard)		4		ns
$t_{d(DB-WR)}$	Data output delay time (WR standard)		(Note1)		ns
$t_{h(WR-DB)}$	Data output hold time (WR standard)(Note2)		0		ns

Note 1: Calculated according to the BCLK frequency as follows:

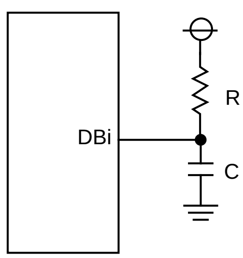
$$td(DB – WR) = \frac{10^{9}}{f(BCLK) \times 2} – 80 \quad [ns]$$

Note 2: This is standard value shows the timing when the output is off, and doesn't show hold time of data bus.
Hold time of data bus is different by capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in

$t = –CR \times \ln (1 – V_{OL} / V_{CC})$

by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC}$, C = 30pF, R = 1kΩ, hold time of output “L” level is

$t = – 30pF \times 1kΩ \times \ln (1 – 0.2V_{CC} / V_{CC})$
$= 6.7ns.$



Note 3: Specify a product of –40°C to 85°C to use it.

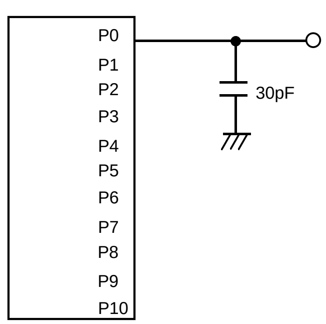


Figure 1.26.1. Port P0 to P10 measurement circuit

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Switching characteristics (referenced to V_{CC} = 3V, V_{SS} = 0V at Topr = – 20°C to 85°C / – 40°C to 85°C (Note 3), CM15 = “1” unless otherwise specified)

Table 1.26.22. Memory expansion and microprocessor modes (when accessing external memory area with wait)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.31.1		60	ns
$t_{h(BCLK-AD)}$	Address output hold time (BCLK standard)		4		ns
$t_{h(RD-AD)}$	Address output hold time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address output hold time (WR standard)		0		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			60	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (BCLK standard)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			60	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		– 4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			60	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			60	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (BCLK standard)			80	ns
$t_{h(BCLK-DB)}$	Data output hold time (BCLK standard)		4		ns
$t_{d(DB-WR)}$	Data output delay time (WR standard)		(Note1)		ns
$t_{h(WR-DB)}$	Data output hold time (WR standard)(Note2)		0		ns

Note 1: Calculated according to the BCLK frequency as follows:

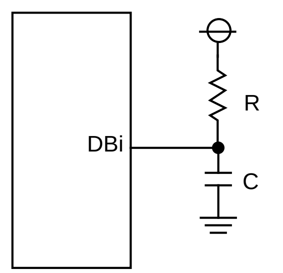
$$td(DB – WR) = \frac{10^{9}}{f(BCLK)} – 80 \quad [ns]$$

Note 2: This is standard value shows the timing when the output is off, and doesn't show hold time of data bus.
Hold time of data bus is different by capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in

$$t = –CR \times \ln (1 – V_{OL} / V_{CC})$$

by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC}$, C = 30pF, R = 1kΩ, hold time of output “L” level is

$$t = – 30pF \times 1kΩ \times \ln (1 – 0.2V_{CC} / V_{CC}) = 6.7ns.$$



Note 3: Specify a product of –40°C to 85°C to use it.

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Switching characteristics (referenced to VCC = 3V, VSS = 0V at Topr = – 20°C to 85°C / – 40°C to 85°C (Note 2), CM15 = “1” unless otherwise specified)

Table 1.26.23. Memory expansion and microprocessor modes (when accessing external memory area with wait, and select multiplexed bus)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.26.1		60	ns
$t_{h(BCLK-AD)}$	Address output hold time (BCLK standard)		4		ns
$t_{h(RD-AD)}$	Address output hold time (RD standard)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			60	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (BCLK standard)		4		ns
$t_{h(RD-CS)}$	Chip select output hold time (RD standard)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			60	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			60	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (BCLK standard)			80	ns
$t_{h(BCLK-DB)}$	Data output hold time (BCLK standard)		4		ns
$t_{d(DB-WR)}$	Data output delay time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (BCLK standard)			60	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (BCLK standard)		– 4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (Address standard)		(Note 1)		ns
$t_{h(ALE-AD)}$	ALE signal output hold time(Address standard)		40		ns
$t_{d(AD-RD)}$	Post-address RD signal output delay time		0		ns
$t_{d(AD-WR)}$	Post-address WR signal output delay time		0		ns
$t_{dZ(RD-AD)}$	Address output floating start time			8	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$th(RD – AD) = \frac{10^{9}}{f(BCLK) \times 2} \quad [ns]$$

$$th(WR – AD) = \frac{10^{9}}{f(BCLK) \times 2} \quad [ns]$$

$$th(RD – CS) = \frac{10^{9}}{f(BCLK) \times 2} \quad [ns]$$

$$th(WR – CS) = \frac{10^{9}}{f(BCLK) \times 2} \quad [ns]$$

$$td(DB – WR) = \frac{10^{9} \times 3}{f(BCLK) \times 2} – 80 \quad [ns]$$

$$th(WR – DB) = \frac{10^{9}}{f(BCLK) \times 2} \quad [ns]$$

$$td(AD – ALE) = \frac{10^{9}}{f(BCLK) \times 2} – 45 \quad [ns]$$

Note 2: Specify a product of –40°C to 85°C to use it.

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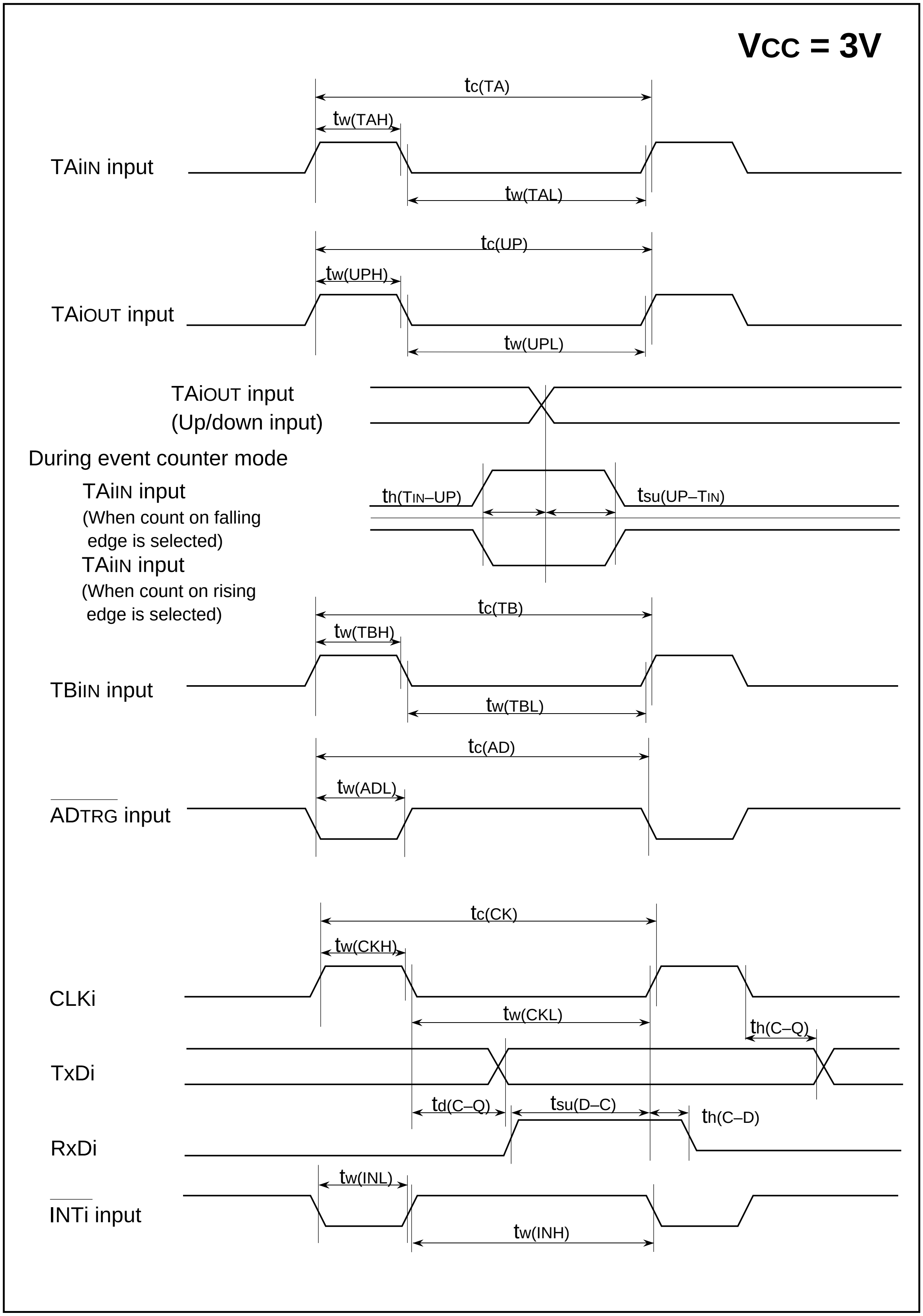

Figure 1.26.2. Vcc=3V timing diagram (1)

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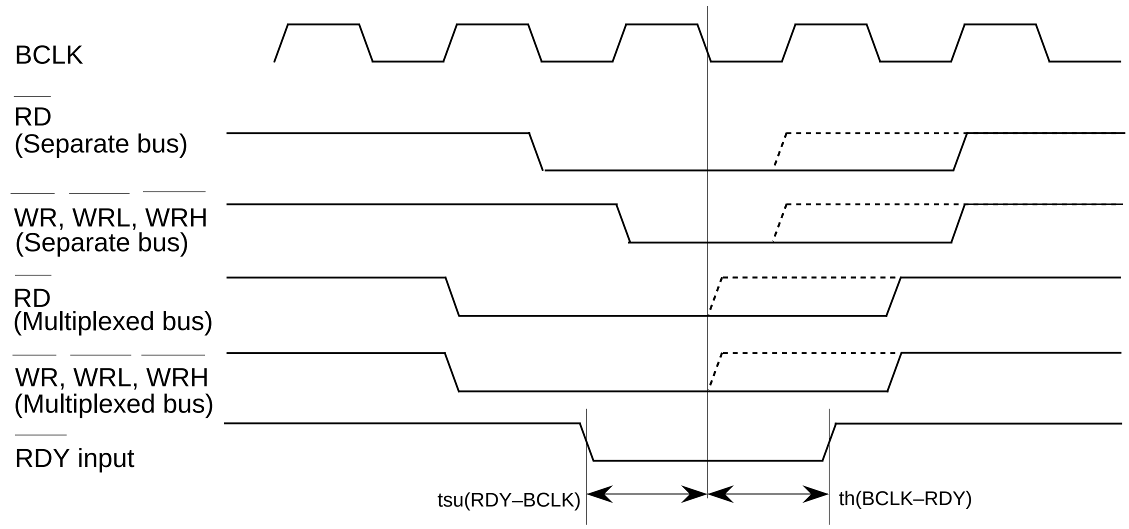
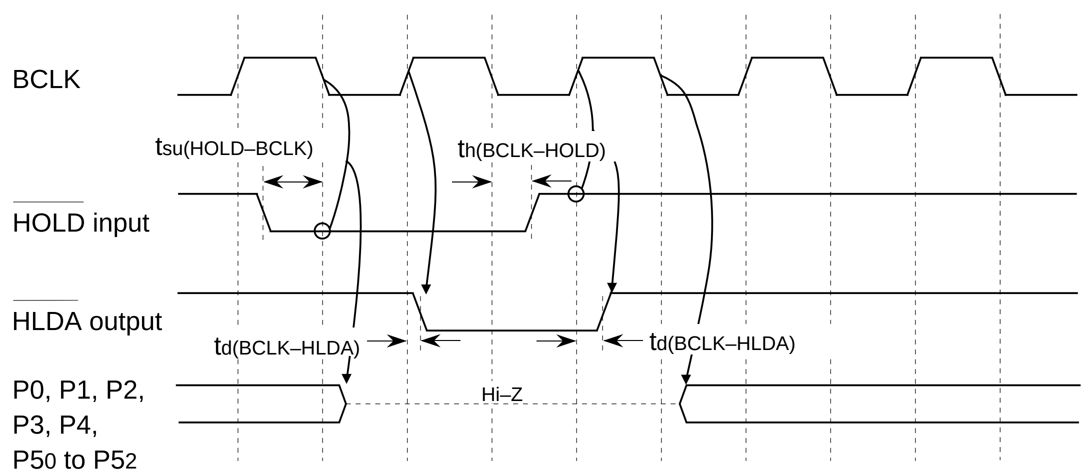
Vcc = 3V

Memory Expansion Mode and Microprocessor Mode

(Valid only with wait)



(Valid with or without wait)



Note: The above pins are set to high-impedance regardless of the input level of the BYTE pin and bit (PM06) of processor mode register 0 selects the function of ports P40 to P43.

Measuring conditions :
- V_{CC}=3V
- Input timing voltage : Determined with V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : Determined with V_{OL}=1.5V, V_{OH}=1.5V

Figure 1.26.3. V_{CC}=3V timing diagram (2)

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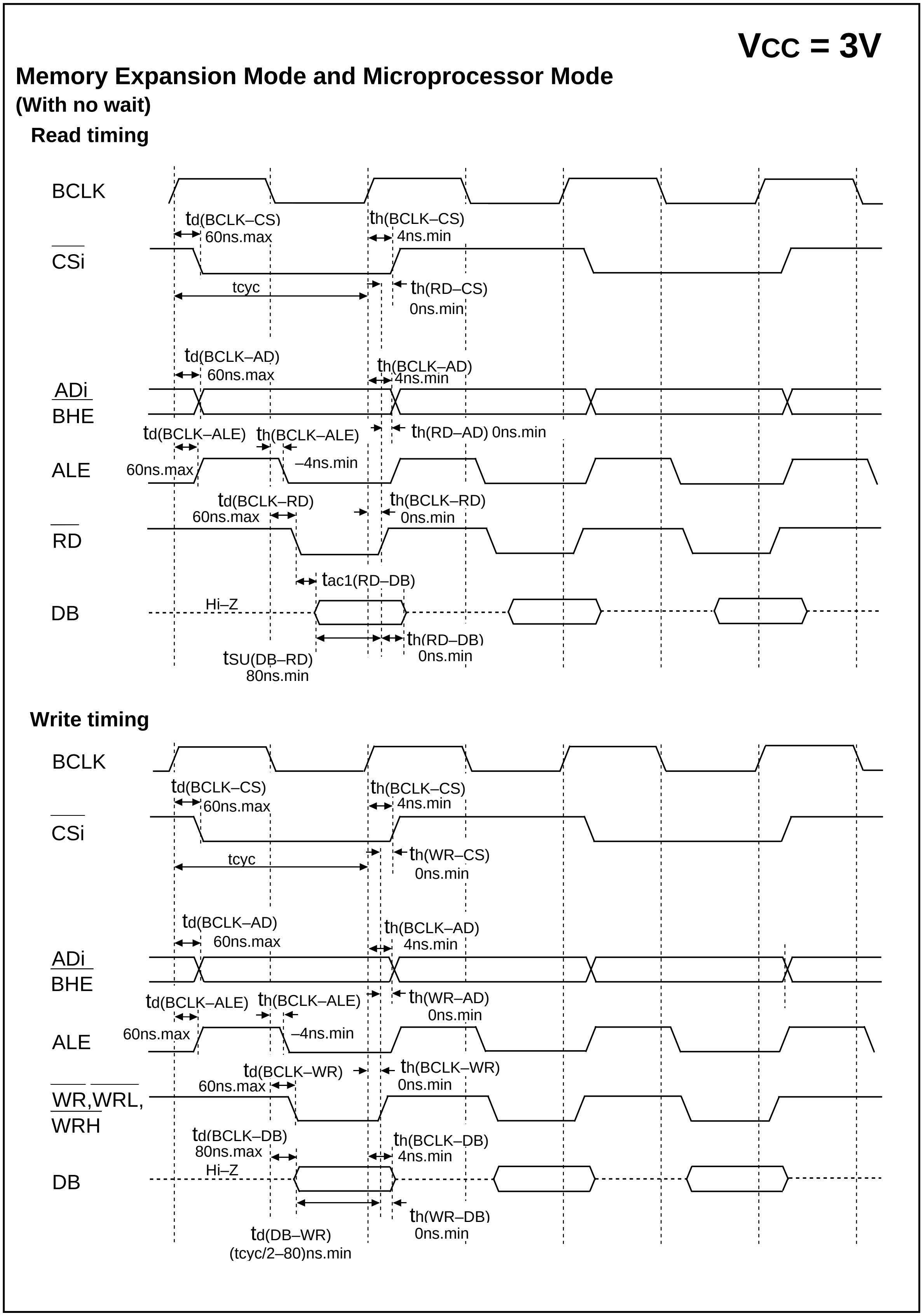

Figure 1.26.4. Vcc=3V timing diagram (3)

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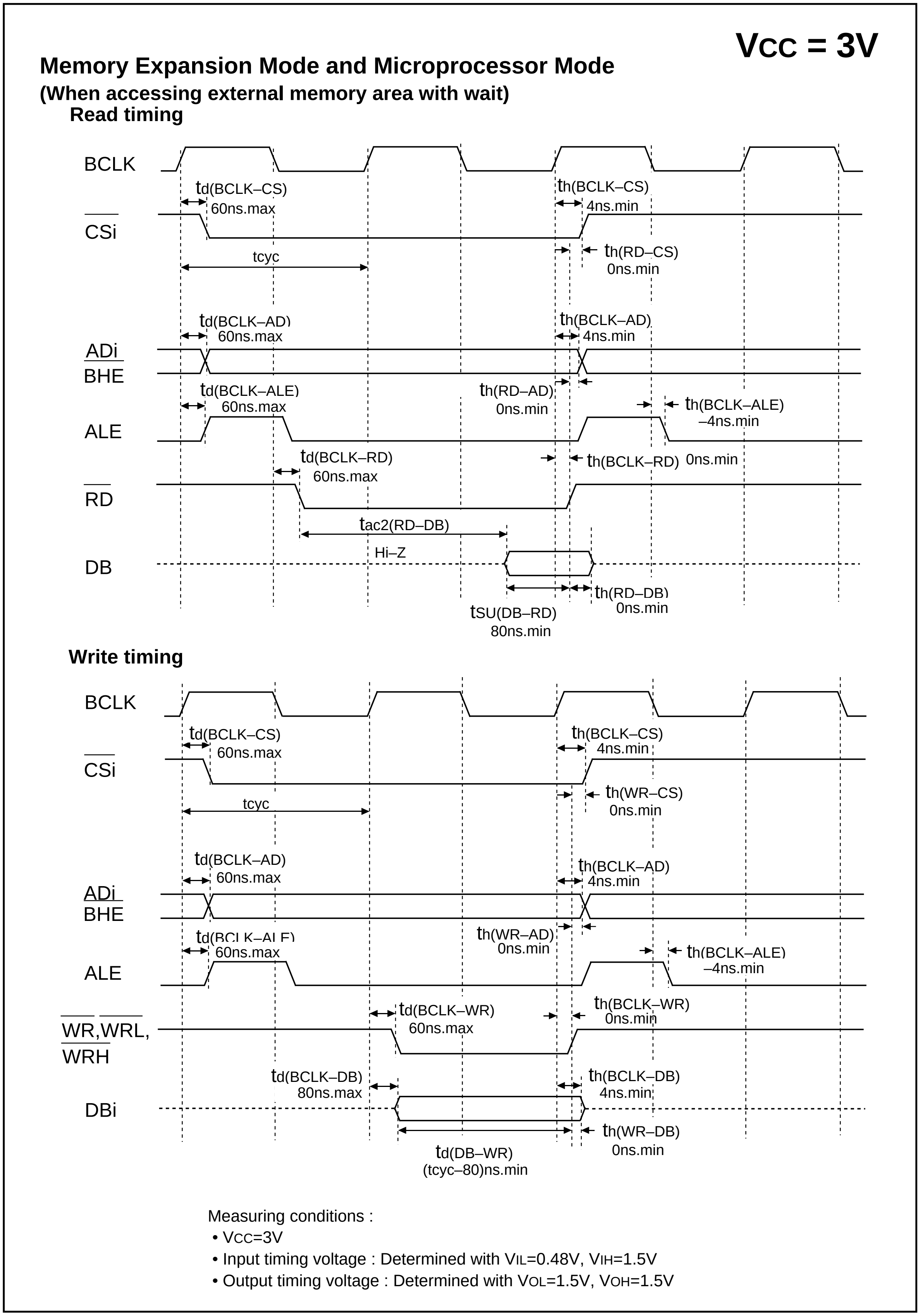

Figure 1.26.5. V_{CC}=3V timing diagram (4)

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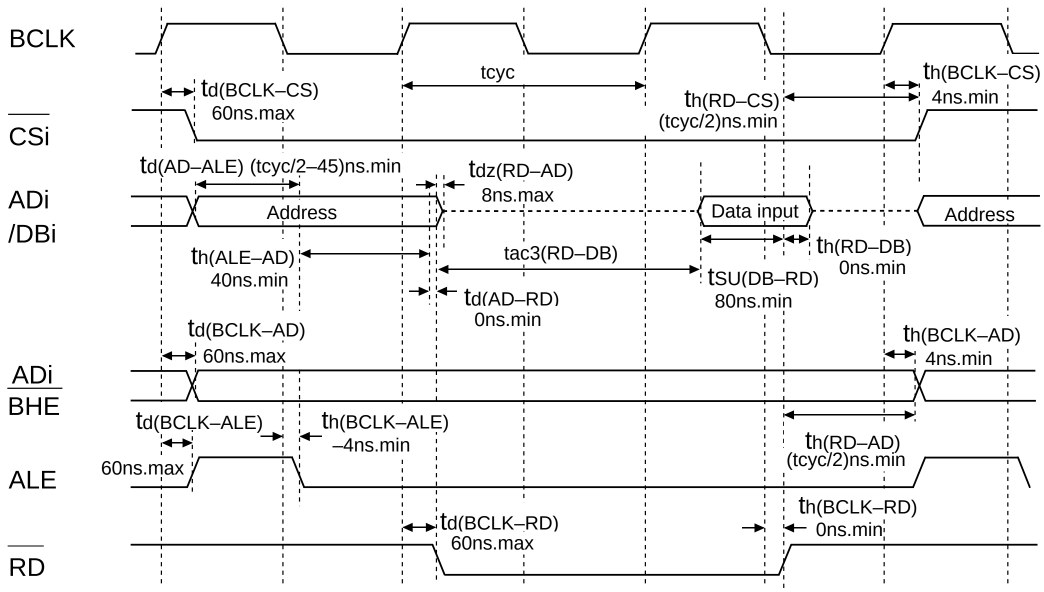
Vcc = 3V

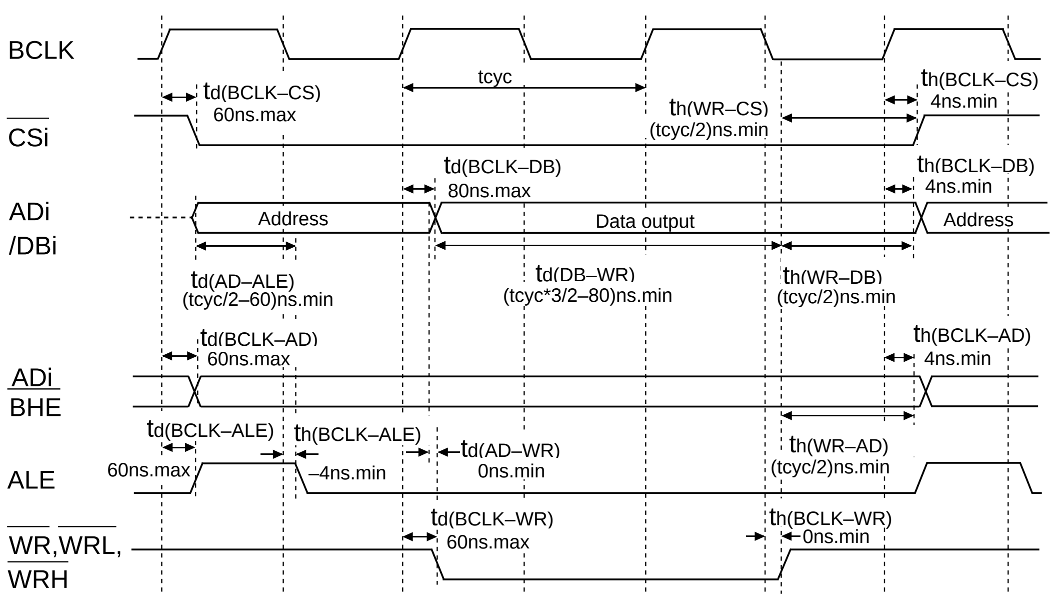
Memory Expansion Mode and Microprocessor Mode

(When accessing external memory area with wait, and select multiplexed bus)

Read timing



Write timing



Measuring conditions :
- V_{CC}=3V
- Input timing voltage : Determined with V_{IL}=0.48V,V_{IH}=1.5V
- Output timing voltage : Determined with V_{OL}=1.5V,V_{OH}=1.5V

Figure 1.26.6. V_{CC}=3V timing diagram (5)

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GZZ-SH13-95B<02A0>

Mask ROM number	

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30620MCM-XXXFP/GP MASK ROM CONFIRMATION FORM

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please complete all items marked ❋ .

❋ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

❋1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. : ☐ M30620MCM-XXXFP ☐ M30620MCM-XXXGP

File code : | | | | | | | | | (hex)

Mask file name : | | | | | | | | | .MSK (alpha-numeric 8-digit)

❋2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30620MCM-XXXFP, submit the 100P6S mark specification sheet. For the M30620MCM-XXXGP, submit the 100P6Q mark specification sheet.

❋3. Usage Conditions

For our reference when of testing our products, please reply to the following questions about the usage of the products you ordered.

(1) Which kind of XIN-XOUT oscillation circuit is used?

☐ Ceramic resonator ☐ Quartz-crystal oscillator

☐ External clock input ☐ Other ( )

What frequency do not use?

f(XIN) = [ ] MHz

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GZZ-SH13-95B<02A0>

Mask ROM number	

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30620MCM-XXXFP/GP MASK ROM CONFIRMATION FORM

(2) Which kind of XCIN-XCOUT oscillation circuit is used?

☐ Ceramic resonator ☐ Quartz-crystal oscillator

☐ External clock input ☐ Other ( )

What frequency do not use?

f(XCIN) = ☐ kHz

(3) Which operation mode do you use?

☐ Single-chip mode ☐ Memory expansion mode

☐ Microprocessor mode

(4) Which operating supply voltage do you use?

(Circle the operating voltage range of use)

2.2 2.4 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 (V)

(5) Which operating ambient temperature do you use?

(Circle the operating temperature range of use)

-50 -40 -30 -20 -10 0 10 20 30 40 50 60 70 80 90 (°C)

(6) Do you use I^2C (Inter IC) bus function?

☐ Not use ☐ Use

(7) Do you use IE (Inter Equipment) bus function?

☐ Not use ☐ Use

Thank you cooperation.

❋4. Special item (Indicate none if there is not specified item)

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GZZ-SH13-48B<98A1>

Mask ROM number	

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30624MGM-XXXFP/GP MASK ROM CONFIRMATION FORM

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please complete all items marked ❋ .

❋ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

❋1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. : ☐ M30624MGM-XXXFP ☐ M30624MGM-XXXGP

File code : ☐☐☐☐☐☐☐☐ (hex)

Mask file name : ☐☐☐☐☐☐☐☐ .MSK (alpha-numeric 8-digit)

❋2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30624MGM-XXXFP, submit the 100P6S mark specification sheet. For the M30624MGM-XXXGP, submit the 100P6Q mark specification sheet.

❋3. Usage Conditions

For our reference when of testing our products, please reply to the following questions about the usage of the products you ordered.

(1) Which kind of XIN-XOUT oscillation circuit is used?

☐ Ceramic resonator ☐ Quartz-crystal oscillator

☐ External clock input ☐ Other ( )

What frequency do not use?

f(XIN) = ☐ MHz

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Mask ROM number	

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30624MGM-XXXFP/GP MASK ROM CONFIRMATION FORM

(2) Which kind of XCIN-XCOUT oscillation circuit is used?

☐ Ceramic resonator ☐ Quartz-crystal oscillator

☐ External clock input ☐ Other ( )

What frequency do not use?

f(XCIN) = ☐ kHz

(3) Which operation mode do you use?

☐ Single-chip mode ☐ Memory expansion mode

☐ Microprocessor mode

(4) Which operating supply voltage do you use?

(Circle the operating voltage range of use)

2.2 2.4 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 (V)

(5) Which operating ambient temperature do you use?

(Circle the operating temperature range of use)

-50 -40 -30 -20 -10 0 10 20 30 40 50 60 70 80 90 (°C)

(6) Do you use I^2C (Inter IC) bus function?

☐ Not use ☐ Use

(7) Do you use IE (Inter Equipment) bus function?

☐ Not use ☐ Use

Thank you cooperation.

❋4. Special item (Indicate none if there is not specified item)

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Differences between M16C/62M (Low voltage version) and M30624FGLFP/GP

Item	M16C/62M (Low voltage version)	M30624FGLFP/GP
Memory area	1 Mbyte fixed	Memory expansion 1.2 Mbytes mode 4 Mbytes mode
Serial I/O	No CTS/RTS separate function	CTS/RTS separate function
IIC bus mode	Analog or digital delay is selected as SDA delay	Only analog delay is selected as SDA delay
Memory version	Mask ROM version Flash memory version	Flash memory version only
Standard serial I/O mode (Flash memory version)	Clock synchronized Clock asynchronized	Clock synchronized only

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Version	Contents for change	Revision date
REV. B1	Page 8-17 All symbols of Ta are revised to Topr.	01.6.22

Revision history	M16C/62M Group data sheet	

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- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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MITSUBISHI SEMICONDUCTORS
M16C/62M Group (Low voltage version) Data Sheet REV.B1

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