

P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
- 12	0.016 at $V_{GS} = -4.5$ V	- 13
	0.022 at $V_{GS} = -2.5$ V	- 11
	0.028 at $V_{GS} = -1.8$ V	- 9.8

FEATURES

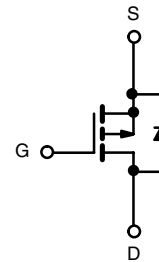
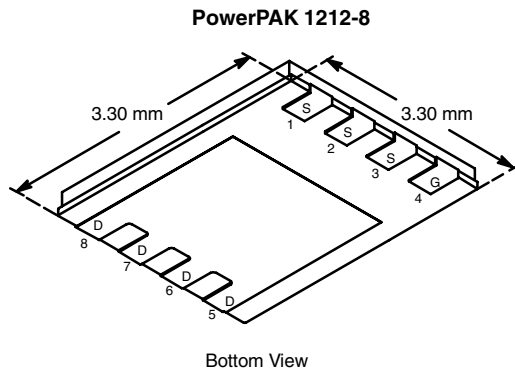
- TrenchFET[®] Power MOSFETS: 1.8-V Rated
- New PowerPAK[®] Package
 - Low Thermal Resistance, R_{thJC}
 - Low 1.07-mm Profile



RoHS*
COMPLIANT

APPLICATIONS

- Load Switch
- Power Switch
- PA Switch



P-Channel MOSFET

Ordering Information: Si7405DN-T1
Si7405DN-T1-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	10 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	- 12		V
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	- 13	A
		$T_A = 85$ °C	- 9.4	
Pulsed Drain Current	I_{DM}	- 30		
Continuous Source Current (Diode Conduction) ^a	I_S	- 3.2	- 1.3	
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	3.8	W
		$T_A = 85$ °C	2.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations ^{b,c}		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	26	°C/W
		Steady State	65	
Maximum Junction-to-Case	R_{thJC}	1.9	2.4	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
 b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
 c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

* Pb containing terminations are not RoHS compliant, exemptions may apply

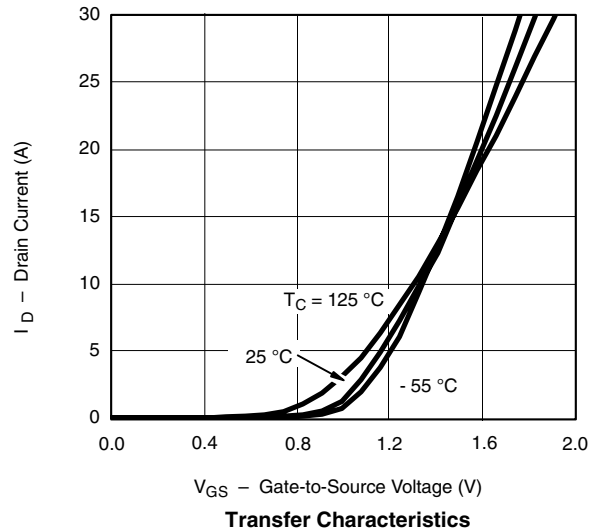
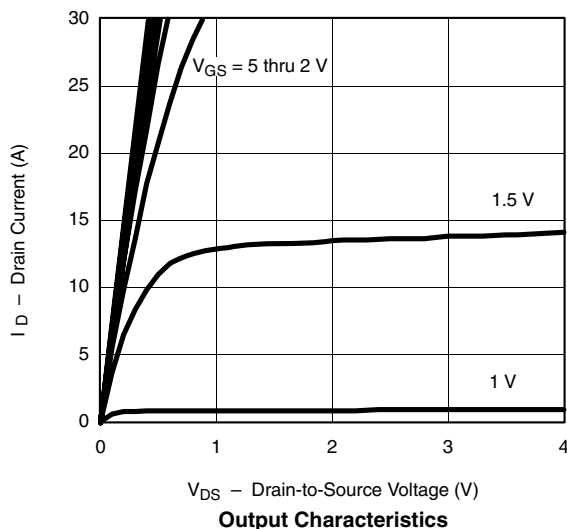
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -2\text{ mA}$	-0.45		-1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -13\text{ A}$		0.013	0.016	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -11\text{ A}$		0.018	0.022	
		$V_{GS} = -1.8\text{ V}, I_D = -3\text{ A}$		0.022	0.028	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -6\text{ V}, I_D = -13\text{ A}$		35		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -3.2\text{ A}, V_{GS} = 0\text{ V}$		-0.7	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -13\text{ A}$		35	50	nC
Gate-Source Charge	Q_{gs}		6.6			
Gate-Drain Charge	Q_{gd}		7.7			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 6\text{ }\Omega$ $I_D = -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 6\text{ }\Omega$		25	40	ns
Rise Time	t_r		50	75		
Turn-Off Delay Time	$t_{d(off)}$		175	260		
Fall Time	t_f		150	225		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -3.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		30	60	

Notes

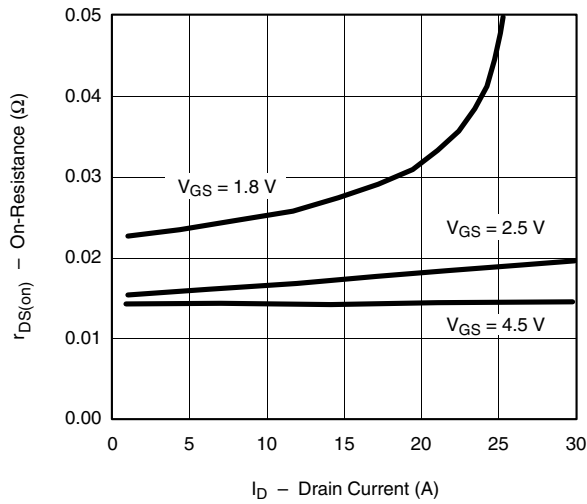
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

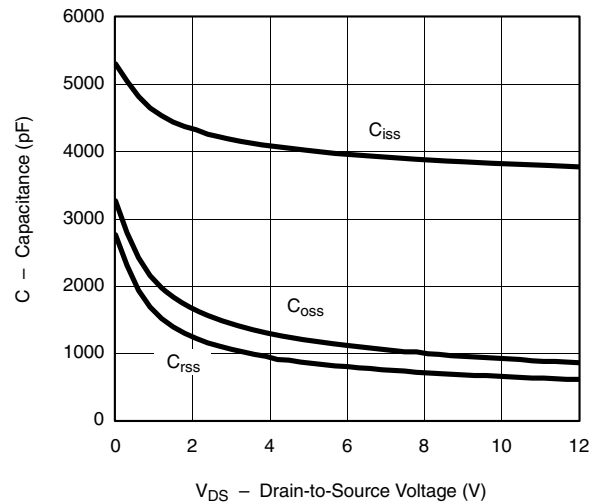
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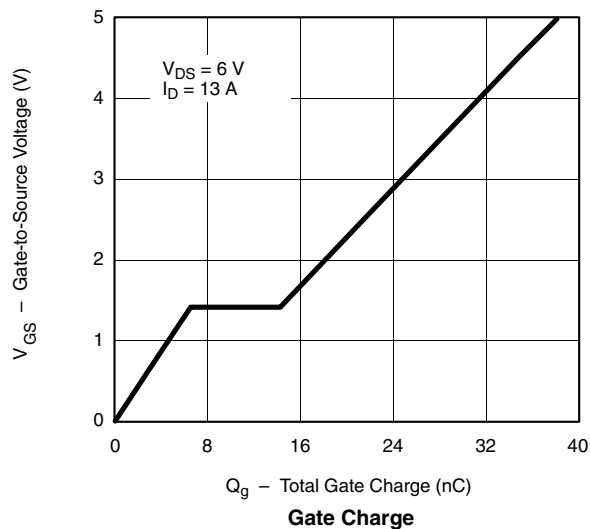
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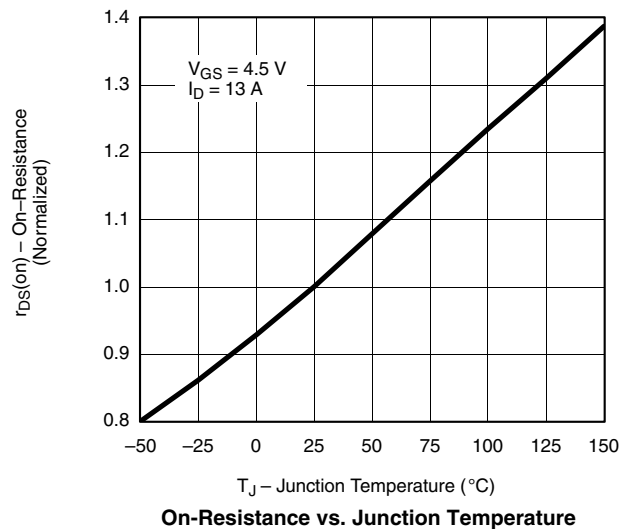
On-Resistance vs. Drain Current



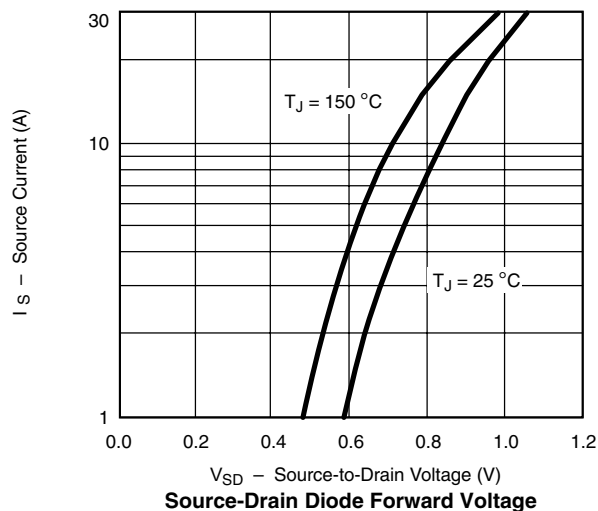
Capacitance



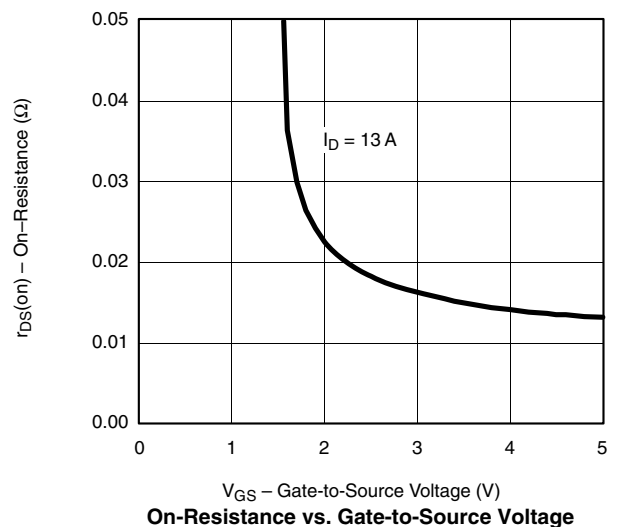
Gate Charge



On-Resistance vs. Junction Temperature

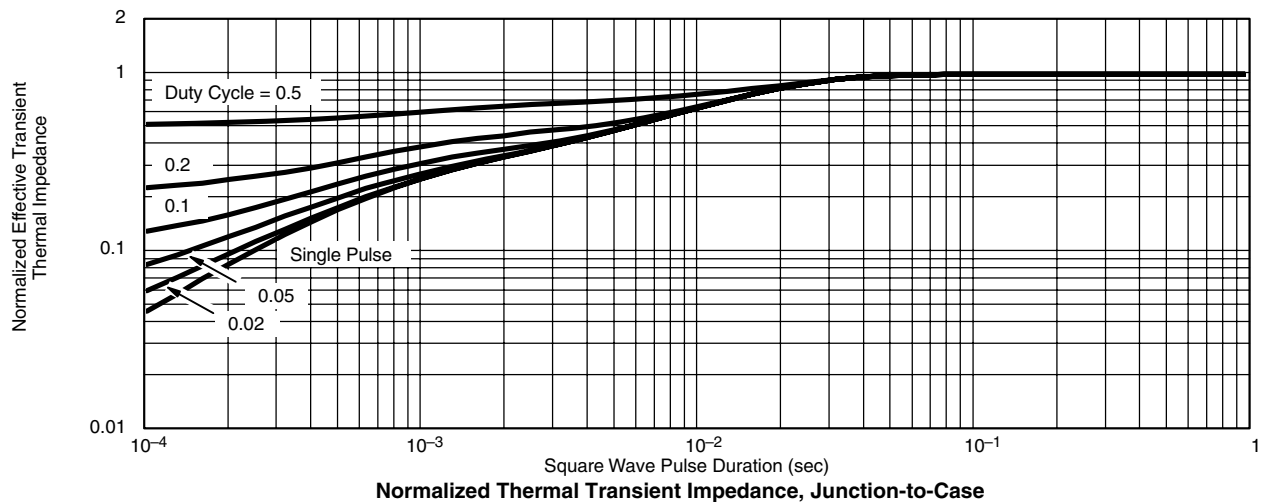
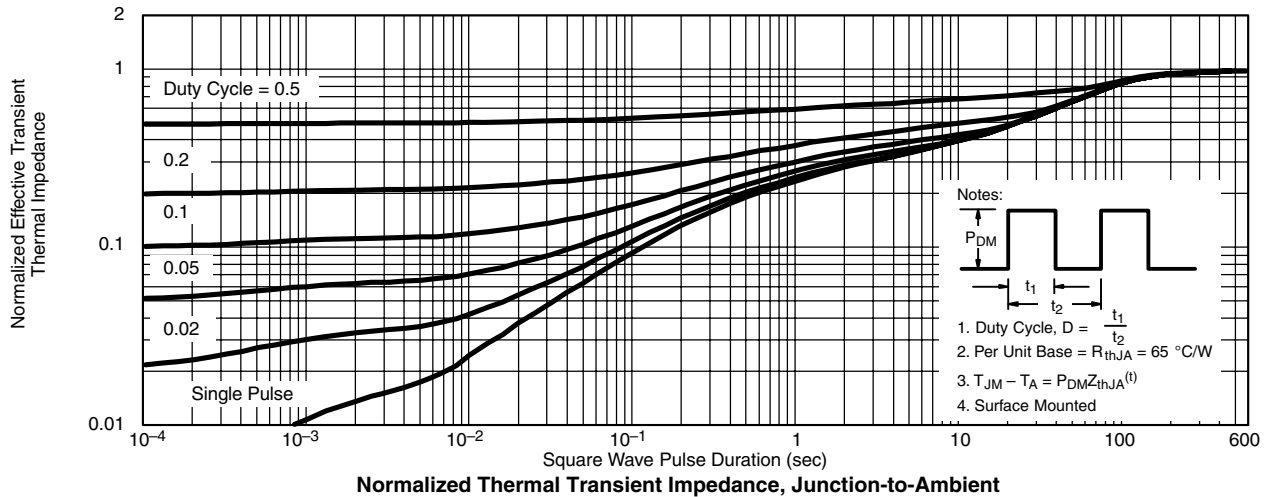
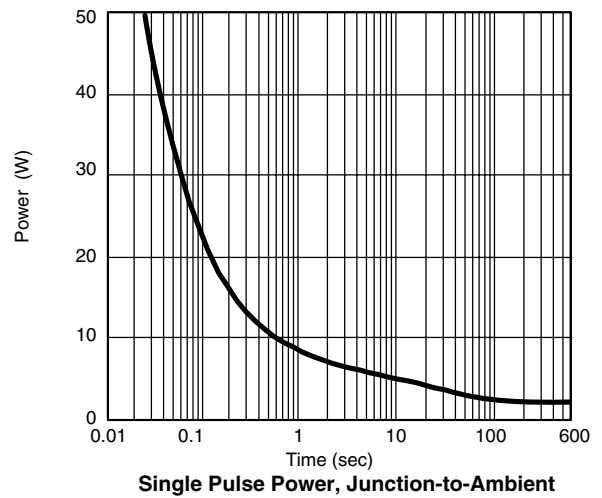
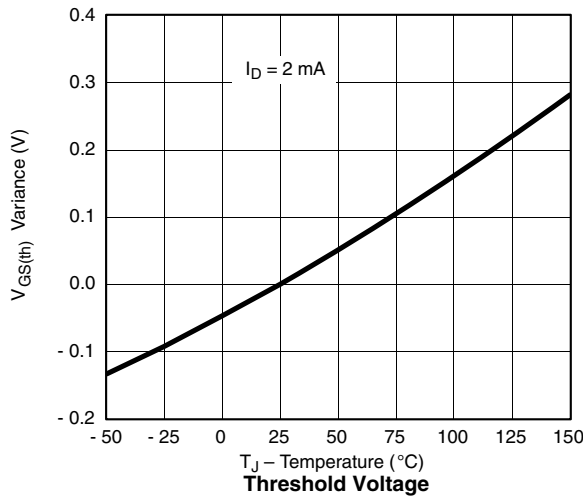


Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

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