PM8313

D3MX

M13 MULTIPLEXER

ISSUE 5: JULY 1998

CONTENTS

LIST OF REGISTERS

LIST OF FIGURES

LIST OF TABLES

1 FEATURES

- Integrates a full featured M13 multiplexer and DS-3 framer in a single monolithic device.
- Supports the M23 or C-bit parity DS3 formats.
- Supports the M12 or G.747 formats allowing DS1 or E1 signals to be multiplexed into a DS3 signal.
- • Allows the M12 stages to be bypassed allowing direct input of DS2 signals into the M23 multiplexer stage.
- Provides a generic microprocessor interface for configuration, control, and status monitoring.
- Low power CMOS technology.
- Packaged in a 208 pin Plastic Quad Flat Pack (PQFP) package.

Each DS3 framer/performance monitor section:

- Frames to a DS3 signal with a maximum average reframe time of less than 1.5 ms (as required by TR-TSY-000009 Section 4.1.2 and TR-TSY-000191 Section 5.2).
- Decodes a B3ZS-encoded signal and indicates line code violations. The definition of line code violation is software selectable.
- Detects and accumulates occurrences of excessive zeros and loss of signal.
- Provides indication of M-frame and M-subframe boundaries, and overhead bit positions in the DS3 stream.
- Detects the DS3 alarm indication signal (AIS) and idle signal. Detection algorithms operate correctly in the presence of a 10^{-3} bit error rate.
- Extracts valid X-bits and indicates far end receive failure. Accumulates up to 65,535 line code violation (LCV) events per second, 16,383 P-bit parity error events per second, 1023 F-bit or M-bit (framing bit) events per second, 65,535 excessive zero (EXZ) events per second, and when enabled for C-bit

parity mode operation, up to 16,383 C-bit parity error events per second, and 16,383 far end block error (FEBE) events per second.

- Detects and validates bit-oriented codes in the C-bit parity far end alarm and control channel.
- Terminates the C-bit parity path maintenance data link with an integral HDLC receiver having a 4-byte deep FIFO buffer. Supports polled, interrupt-driven or DMA access.
- Optionally extracts the C-bit parity mode path maintenance data link signal and serializes it at 28.2 kbit/s.
- Extracts the X, P, M, F, C and stuff opportunity bits and serializes them at 526 kbit/s on a time division multiplex signal.

Each DS3 transmit framer section:

- Provides the overhead bit insertion for a DS3 stream.
- Provides a bit serial clock and data interface, and allows the M-frame boundary and/or the overhead bit positions to be located via an external interface
- Provides optional insertion of the X, P, M, F, C, and stuff opportunity bits via a 526 kbit/s serial interface.
- Provides B3ZS encoding.
- Inserts far end receive failure (FERF), the DS3 alarm indication signal (AIS) and the idle signal when enabled by external inputs, or internal register bits.
- Provides diagnostic features to allow the generation of line code violation error events, parity error events, framing bit error events, and when enabled for the C-bit parity application, C-bit parity error events, and far end block error events.
- Inserts bit-oriented codes in the C-bit parity far end alarm and control channel.
- Optionally inserts the C-bit parity path maintenance data link with an integral HDLC transmitter. Supports polled, interrupt-driven, or DMA access.

- Optionally inserts the C-bit parity mode path maintenance data link signal from a 28.2 kbit/s serial input.

Each M23 multiplexer section:

- Multiplexes 7 DS2 bit streams into a single M23 format DS3 bit stream.
- Performs required bit stuffing including generation of C-bits.
- Includes required FIFO buffers for rate adaptation in the multiplex path.
- Allows insertion of per DS2 payload loopback requests encoded in the transmitted C-bits to be activated or cleared under microprocessor control.
- Provides generated DS2 clock for use in integrated M13 or C-bit parity multiplex applications.
- Demultiplexes a single M23 format DS3 bit stream into 7 DS2 bit streams.
- Performs required bit destuffing including interpretation of C-bits.
- Detects per DS2 payload loopback requests encoded in the received C-bits.
- Allows per DS2 payload loopback to be activated or cleared under microprocessor control.
- Allows per DS2 alarm indication signal (AIS) to be activated or cleared for either direction under microprocessor control.
- Allows DS2 alarm indication signal (AIS) to be activated or cleared in the demultiplex direction automatically upon loss of DS3 frame alignment or signal.
- Supports C-bit parity DS3 format.

Each DS2 framer and M12 multiplexer section:

- Supports two asynchronous multiplexing standards: the combination of four DS1 bit streams into a single M12 format DS2 bit stream and the combination of three 2048 kbit/s tributaries into a 6312 kbit/s high speed signal according to CCITT Recommendation G.747.
- Frames to either a DS2 or G.747 signal.

- Maximum average reframe time of less than 7 ms (as required by TR-TSY-000009 Section 4.1.2 and TR-TSY-000191 Section 5.2) for DS2 format and 1 ms for G.747 format.
- Allows forcing of reframe via an internal register.
- Detects the alarm indication signal in 9.9 ms in the presence of a 10^{-3} bit error rate.
- Extracts the DS2 X-bit or G.747 remote alarm bit and indicates far end receive failure.
- Accumulates error events over consecutive accumulation intervals as defined by writes to internal registers.
- Accumulates up to 255 DS2 M-bit or F-bit error events per second. Accumulates up to 255 G.747 framing bit or word (selectable) error events per second.
- Accumulates up to 8191 G.747 parity error events per second.
- Optionally generates interrupts when various events or status changes occur.
- Performs required bit stuffing including generation of C-bits.
- Performs required bit destuffing including interpretation of C-bits.
- Includes required FIFO buffers for rate adaptation in the multiplex path.
- Allows per tributary alarm indication signal (AIS) to be activated or cleared for either direction under microprocessor control.

DS2 Functionality

- Multiplexes four DS1 bit streams into a single M12 format DS2 bit stream.
- Performs required inversion of second and fourth multiplexed DS1 streams as required by ANSI T1.107 Section 7.2.
- Allows insertion of per DS1 payload loopback requests encoded in the transmitted C-bits to be activated or cleared under microprocessor control.
- Inserts X, F, and M bits into transmitted DS2 bit stream.

- Allows transmission of far end receive failure (FERF) and alarm indication signal (AIS) under microprocessor control.
- Allows inversion of inserted F or M bits for diagnostic purposes.
- Demultiplexes a single M12 format DS2 bit stream into four DS1 bit streams.
- Detects per DS1 payload loopback requests encoded in the received C-bits.
- Allows per DS1 payload loopback to be activated or cleared under microprocessor control.
- Performs required inversion of second and fourth demultiplexed DS1 streams.

E1 Functionality

- Multiplexes three 2048 kbit/s bit streams into a single G.747 format 6312 kbit/s bit stream.
- Inserts frame alignment signal and parity bit into transmitted 6312 kbit/s bit stream.
- Allows transmission of remote alarm indication (RAI) and reserved bit (Set II, bit 3) under microprocessor control.
- Allows inversion of inserted frame alignment signal for diagnostic purposes.
- Allows inversion of the C-bits in anticipation of remote loopback recommendations.
- Demultiplexes a single G.747 format 6312 kbit/s bit stream into three 2048 kbit/s bit streams.

2 APPLICATIONS

- M23 Based M13 Multiplexer
- C-Bit Parity Based M13 Multiplexer
- M23 Multiplexer
- M13 Multiplexer Supporting G.747 Tributary Format

3 STANDARD REFERENCES

1. American National Standard for Telecommunications, ANSI T1.103-1987 - "Digital Hierarchy - Synchronous DS3 Format Specifications".

2. American National Standard for Telecommunications, ANSI T1.107-1988 - "Digital Hierarchy - Formats Specifications".

3. American National Standard for Telecommunications, ANSI T1.404-1989 - "Customer Installation-to-Network - DS3 Metallic Interface Specification".

4. American National Standard for Telecommunications, ANSI T1.107a-1990 - "Digital Hierarchy - Supplement to Formats Specifications (DS3 Format Applications)".

5. American National Standard for Telecommunications, T1M1.3/91-003R3 - "In-Service Digital Transmission Performance Monitoring Draft Standard".

6. Bell Communications Research, TR-TSY-000009 - "Asynchronous Digital Multiplexes Requirements and Objectives," Issue 1, May 1986.

7. Bell Communications Research, TR-TSY-000191 - "Alarm Indication Signal Requirements and Objectives," Issue 1, May 1986.

8. Bell Communications Research, TR-TSY-000233 - "Wideband and Broadband Digital Cross-Connect Systems Generic Requirements and Objectives," Issue 2, September 1990.

9. Bell Communications Research, TR-TSY-000820 - "OTGR: Network Maintenance Transport Surveillance - Generic Digital Transmission Surveillance, Section 5.1," Issue 1, June 1990.

10. Bell Communications Research, TR-NWT-000499 - "Transport Systems Generic Requirements (TSGR) - Common Requirements," Issue 4, November 1991.

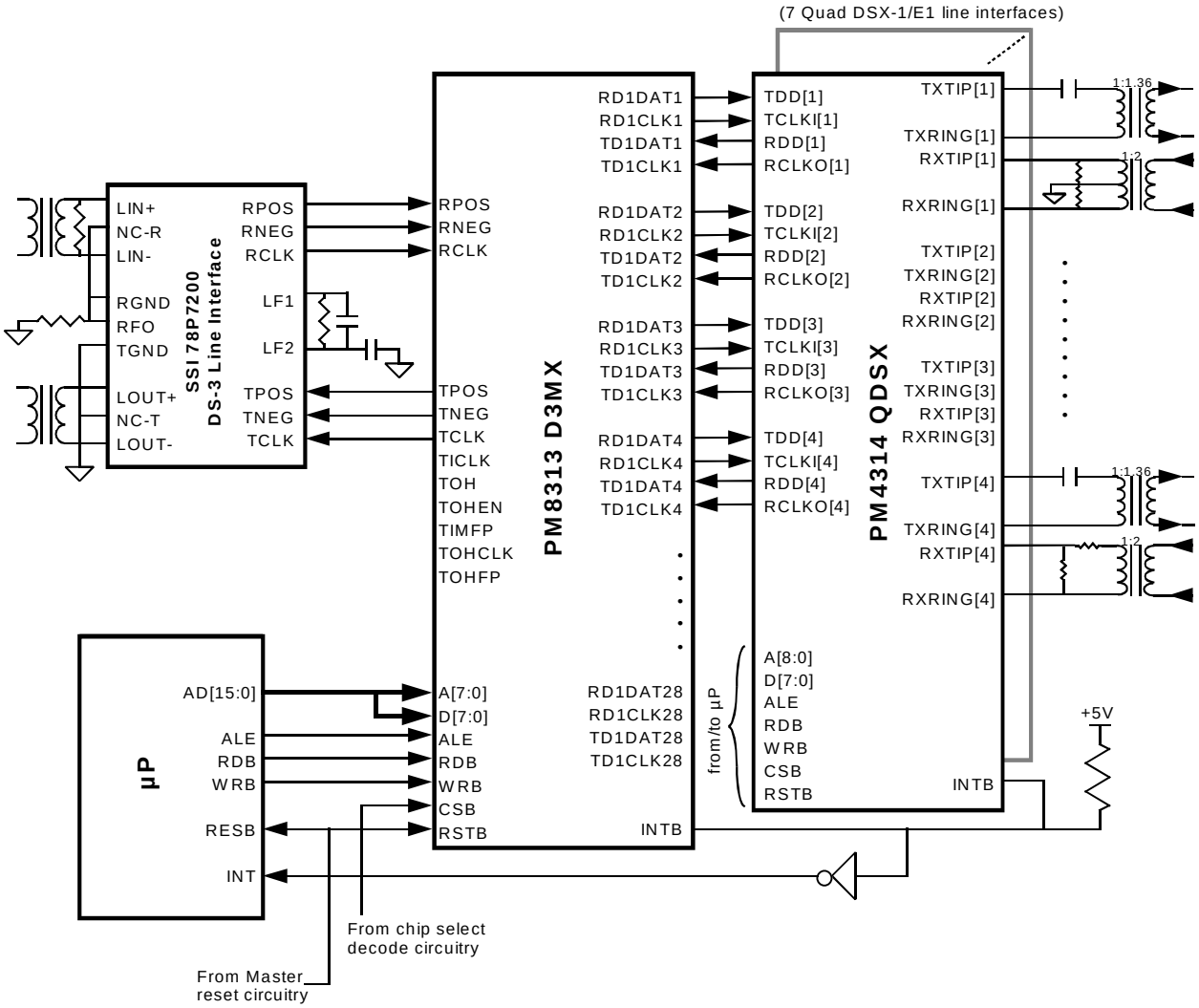
11. CCITT Blue Book, Recommendation Q.921 - "ISDN User-Network Interface Data Link Layer Specification", Volume VI, Fascicle VI.10, 1988.

12. CCITT Blue Book, Recommendation G.747 - "Second Order Digital Multiplex Equipment Operating at 6312 kbit/s and Multiplexing Three Tributaries at 2048 kbit/s", Volume III, Fascicle III.4, 1988.

13. International Organization for Standardization, ISO 3309:1984 - "High-Level Data Link Control Procedures -- Frame Structure".

4 APPLICATION EXAMPLE

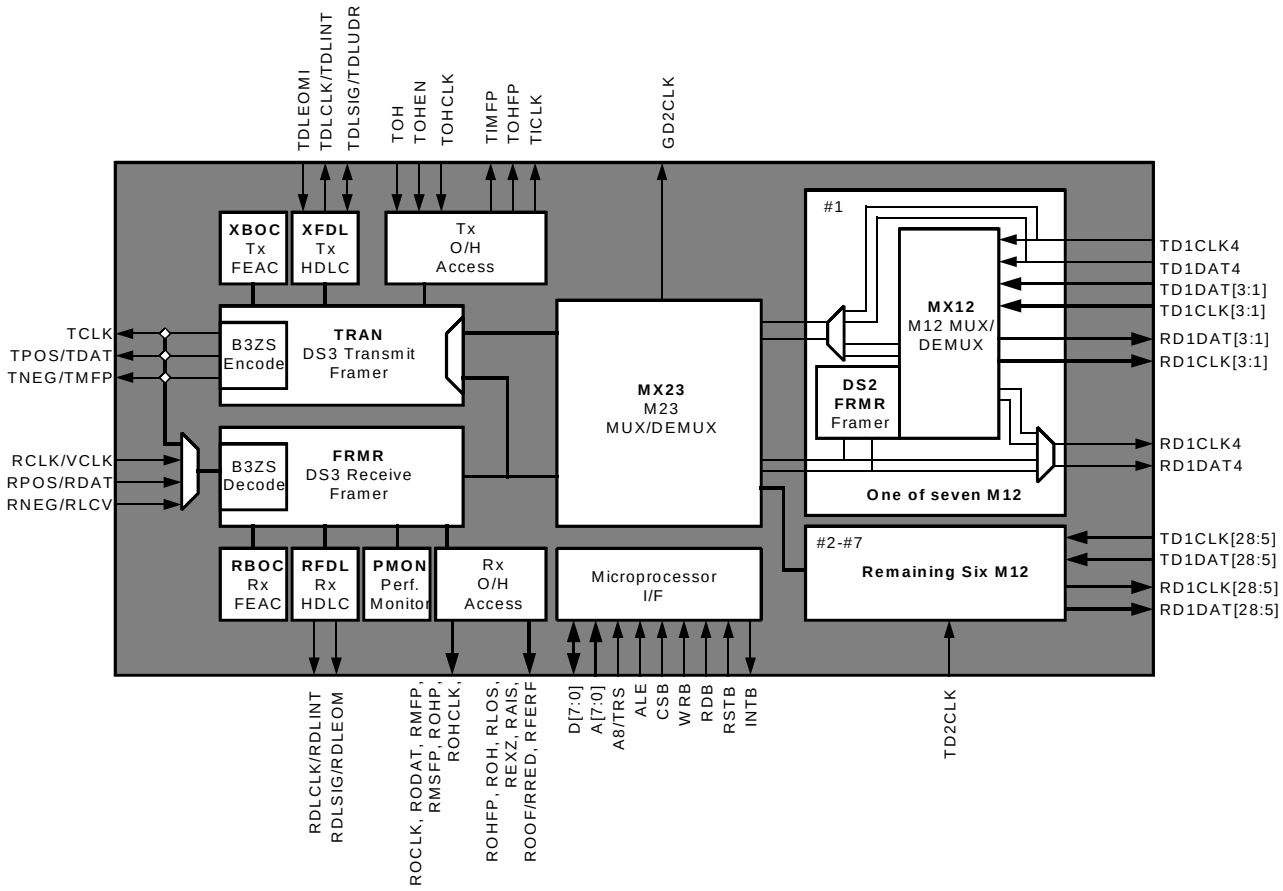
Figure 1 - M1-3 Multiplexer/Demultiplexer



Note:

Use of the SSI LIU as illustrated requires that TICLK has a duty cycle of 45% min 55% max or better (e.g. using a Connor Winfield S65T3 reference oscillator).

5 BLOCK DIAGRAM



DESCRIPTION

The PM8313 D3MX M13 Multiplexer supports asynchronous multiplexing and demultiplexing of 28 DS1s, 21 E1s or 7 DS2s into a DS3 signal. The device supports ANSI T1.107, Bell Communications Research TR-TSY-000009 and CCITT Recommendation G.747 standards.

Receive DS3 framing is provided by the DS3 FRMR Framer Block. The FRMR accepts either a B3ZS encoded bipolar, or a unipolar signal compatible with M23 and C-bit parity applications. The FRMR frames to a DS3 signal with a maximum average reframe time of 1.5 ms in the presence of a 10^{-3} bit error rate. The FRMR indicates line code violations, loss of signal, framing bit errors, parity errors, C-bit parity errors, and far end block errors (FEBE). The FRMR detects far end receive failure (X-bits set to 0), the alarm indication signal (AIS), and the idle signal. The FRMR is an off-line framer, indicating both out of frame (OOF) and change of frame alignment (COFA) events. The error events (FER, CBIT PARITY ERROR, FEBE, etc.) are still indicated while the framer is OOF, based on the previous frame alignment.

The C-bit parity far end alarm channel (FEAC) and path maintenance data link are supported. Bit oriented codes in the FEAC channel are detected by the RBOC Bit-Oriented Code Receiver Block. If enabled, the RBOC generates an interrupt when a valid code has been received. The path maintenance data link is terminated using either the RFDL Data Link Receiver Block or an external HDLC receiver. The RFDL supports polled, interrupt driven, and DMA servicing.

DS3 error event accumulation is provided by the DS3 PMON Performance Monitor Block. The PMON accumulates framing bit errors, line code violations, excessive zeros occurrences, parity errors, C-bit parity errors, and far end block errors. Error accumulation continues even while the off-line framer is indicating OOF. The counters are intended to be polled once per second, and are sized so as not to saturate at a 10^{-3} bit error rate. Transfer of count values to holding registers is initiated through the microprocessor interface.

DS3 transmit framing insertion is provided by the DS3 TRAN Transmitter Block. It outputs either a B3ZS encoded bipolar signal, or a unipolar signal. The DS3 TRAN inserts the X, P, M, C, and F bits into the outgoing DS3 stream. The DS3 TRAN block inserts far end receive failure, AIS, and the idle signal under the control of external inputs, or internal register bits. Diagnostic features are provided to allow the generation of line code violation error events, parity error events, framing bit error events, and when enabled for the C-bit parity application, C-bit parity error events, and far end block error events. External

inputs allow substitution of the overhead bits or the sourcing of AIS, idle signal or far end receive failure indication.

When configured for the C-bit parity application, bit oriented codes in the FEAC channel are inserted by the XBOC Bit-Oriented Code Transmitter Block. The FEAC code is controlled by an internal register. The path maintenance data link is inserted using the XFDL Data Link Transmitter Block or an external HDLC transmitter. The XFDL supports polled, interrupt driven, and DMA servicing.

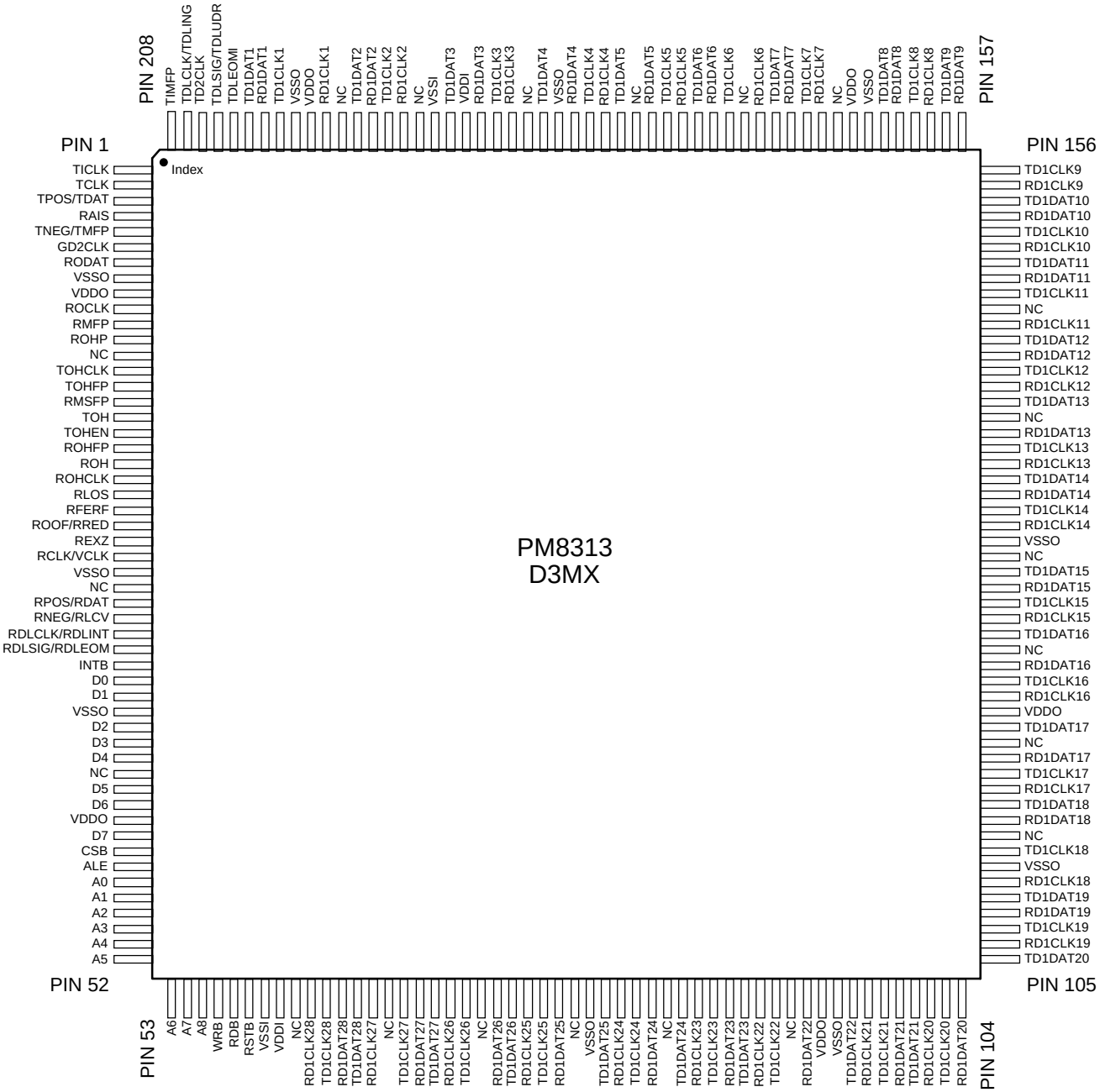
The demultiplexing and multiplexing of seven 6312 kbit/s data streams into and out of the DS3 is performed by the MX23 M23 Multiplexer Block. The MX23 contains FIFOs and performs bit stuffing for the rate adaptation of the DS2s. The C-bits are set appropriately, with the option of inserting DS2 loopback requests. The MX23 may be configured to generate an interrupt upon the detection of loopback requests in the received DS3. AIS may be inserted in the any of the 6312 kbit/s tributaries in both directions. C-bit parity is supported by sourcing a 6.3062723 MHz clock, which corresponds to a stuffing ratio of 100%.

Framing to the demultiplexed 6312 kbit/s data streams is provided by the DS2 FRMR Framer. It supports both DS2 (ANSI TI.107) and CCITT Recommendation G.747 frame formats. The maximum average reframe time is 7 ms for DS2 and 1ms for G.747. In DS2 mode, it detects far end receive failure and accumulates M-bit and F-bit errors. In G.747 mode, it detects remote alarm and accumulates framing word errors and parity errors. The DS2 FRMR is an off-line framer, indication both OOF and COFA events. Error events (FERF, MERR, FERR, PERR, RAI, framing word errors) are still indicated while the DS2 framer is indicating OOF, based on the previous alignment.

The multiplexing and demultiplexing of the low speed tributaries into and out of a 6312 kbit/s data stream is performed by seven MX12 M12 Multiplexers. Each of the MX12 blocks may be independently configured to multiplex and demultiplex four 1544 kbit/s DS1s into and out of a DS2 formatted signal or to multiplex and demultiplex three 2048 kbit/s signals into and out of a G.747 formatted signal. Each MX12 may be independently bypassed so an external DS2 may by multiplexed and demultiplexed directly into and out of the DS3. The MX12 contains FIFOs and performs bit stuffing to accommodate the tributary frequency deviations. The C-bits are set appropriately, with the option of inserting DS1 loopback requests. The MX12 block may be configured to generate an interrupt upon the detection of loopback requests in the received DS2. AIS may be inserted in any of the low speed tributaries in both directions.

6 PIN DIAGRAM

The D3MX is packaged in a 208 pin PQFP package having a body size of 28 mm by 28 mm and a pin pitch of 0.5 mm.



7 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
RCLK/ VCLK	Input	26	The receive input clock (RCLK) provides timing for the receive side of the D3MX. RCLK is nominally a 44.736 MHz, 50% duty cycle clock. The test vector clock (VCLK) signal is used during D3MX production testing to verify internal functionality.
RPOS/ RDAT	Input	29	The positive input pulse (RPOS) signal represents the positive pulses received on the B3ZS-encoded line when configured for dual rail reception. The receive data input (RDAT) signal represents the unipolar DS3 input stream when configured for single rail operation. Both RPOS and RDAT are sampled on the rising edge of RCLK by default and may be enabled to be sampled on the falling edge of RCLK.
RNEG/ RLCV	Input	30	The negative input pulse (RNEG) signal represents the negative pulses received on the B3ZS-encoded line when configured for dual rail reception. Line code violations (LCVs) may be input on the receive line code violation (RLCV) signal when configured for single rail operation. Both RNEG and RLCV are sampled on the rising edge of RCLK by default and may be enabled to be sampled on the falling edge of RCLK.
ROCLK	Output	10	The receive output clock (ROCLK) signal provides timing for downstream processing. ROCLK is nominally a 44.736 MHz, 50% duty cycle clock. RODAT, RMFP, RMSFP, RLOS, REXZ and ROHP are updated on the falling edge of ROCLK. ROCLK is a buffered version of RCLK.

Pin Name	Type	Pin No.	Function
RODAT	Output	7	The receive data output (RODAT) signal carries the 44.736 Mbit/s NRZ stream decoded from the B3ZS line signal. The frame alignment signals (RMFP, RMSFP, and ROHP) are aligned to the RODAT stream. RODAT is updated on the falling edge of ROCLK.
RMFP	Output	11	The receive M-frame pulse (RMFP) signal marks the first bit (X1) in the M-frame of the DS3 signal on RODAT. When the framer is out-of-frame, RMFP continues to operate with timing aligned to the old M-frame position. When the framer regains frame alignment the RMFP timing is updated, which may result in a change of frame alignment. RMFP is updated on the falling edge of ROCLK.
RMSFP	Output	16	The receive M-subframe pulse (RSMFP) signal marks the first bit (X, P, and M) in each M-subframe of the received DS3 stream (RODAT) when the framer is in-frame. When the framer is out-of-frame, RSMFP continues to operate with timing aligned to the old M-frame position. When the framer regains frame alignment the RMSFP timing is updated, which may result in a change of frame alignment. RSMFP is updated on the falling edge of ROCLK.
ROHP	Output	12	The receive overhead pulse (ROHP) signal marks the overhead bit positions (X, P, M, C, and F) in the received DS3 stream (RODAT) when the framer is in-frame. When the framer is out-of-frame, ROHP continues to operate with timing aligned to the old M-frame position. When the framer regains frame alignment the ROHP timing is updated, which may result in a change of frame alignment. ROHP is updated on the falling edge of ROCLK.

Pin Name	Type	Pin No.	Function
ROHCLK	Output	21	The receive overhead clock (ROHCLK) cycles once per overhead bit. ROHCLK is nominally a 526 kHz clock. ROOF, RFERF, RAIS, RIDL, RFERR, ROH, and ROHFP are updated on the falling edge of ROHCLK.
ROH	Output	20	The receive overhead data (ROH) signal contains the overhead bits (C, F, X, P, and M) extracted from the received DS3 stream. ROH is updated on the falling edge of ROHCLK.
ROHFP	Output	19	The receive overhead frame position (ROHFP) signal may be used to locate the individual overhead bits in the received overhead data stream, ROH. ROHFP is high during the X1 overhead bit position in the ROH stream. ROHFP is updated on the falling edge of ROHCLK.
RLOS	Output	22	The receive loss of signal (RLOS) status is set high when the dual rail NRZ format stream is selected, and 175 successive zeros are detected on the RPOS and RNEG inputs. RLOS is set low when the ones' density is greater than 33% for 175 ± 1 bit periods on the RPOS and RNEG inputs. RLOS is updated on the falling edge of ROCLK.
REXZ	Output	25	The receive excessive zero (REXZ) signal indicates the presence of 3 or more consecutive zeros in the received DS3 bipolar stream. REXZ pulses high for one ROCLK cycle whenever 3 or more consecutive zeros are detected. When the Receive DS3 interface is configured to for uni-polar data, the REXZ output is forced low. REXZ is updated on the falling edge of ROCLK.

Pin Name	Type	Pin No.	Function
RAIS	Output	4	The receive alarm indication signal (RAIS) indicates the presence of AIS in the received DS3 stream. RAIS is set high when the AIS pattern has been received for 2.23 ms or 13.5 ms (software selectable). RAIS is set low when the AIS pattern has not been received for 2.23 ms or 13.5 ms. RAIS is updated on the falling edge of ROHCLK.
ROOF/	Output	24	The receive out-of-frame (ROOF) signal is set high when an out-of-frame condition is declared. An out-of-frame is declared when 3 out of 16 (default) or 3 out of 8 consecutive F-bit errors are detected, or when one or more M-bit errors is detected in 3 out of 4 consecutive M-frames. ROOF is set low when an in-frame condition is declared. ROOF is updated on the falling edge of ROHCLK. This ROOF signal is available when the REDO bit in the Master Alarm Enable register is logic 0.
RRED			The receive RED Alarm (RRED) signal is available when the REDO bit in the Master Alarm Enable register is logic 1. The RRED output is set high when a DS3 out-of-frame condition or DS3 loss of signal condition has been present for either 2.23ms or 13.5 ms. The RRED output is set low when a DS3 out-of-frame condition or DS3 loss of signal condition has been absent for either 2.23ms or 13.5 ms. RRED is updated on the falling edge of ROHCLK.

Pin Name	Type	Pin No.	Function
RFERF	Output	23	The receive far end receive failure (RFERF) signal reflects the value of the internal FERF state buffered by two M-frames. Internally, FERF is set high when both X-bits (X1 and X2) are received as logic 0 in the current M-frame; FERF is set low when both X-bits are received as logic 1. FERF remains in its previous state when X1 • X2 in the current M-frame. The RFERF output latency provides a better than 99.99% chance of freezing (i.e. holding RFERF in its previous state) upon a valid state value during the occurrence of an out of frame. RFERF is updated once per M-frame on the falling edge of ROHCLK.

Pin Name	Type	Pin No.	Function
RDLCLK/ RDLINT	Output	31	The receive data link clock (RDLCLK) signal is active when an external HDLC receiver is selected (the REXHDLC bit in the Master HDLC Configuration Register is a logic 1). The RDLCLK signal provides timing for the external processing of the path maintenance data link signal extracted by the DS3 FRMR. RDLCLK is updated on the falling edge of the ROHCLK signal and cycles 3 times per M-frame. RDLCLK is nominally a 28.2 kHz clock, which is low for at least 1.9 µs per cycle. The data link interrupt (RDLINT) signals is active when the internal HDLC receiver is selected (the REXHDLC in the Master HDLC Configuration Register bit is a logic 0). The RDLINT signal is asserted when an event occurs which changes the status of the HDLC receiver. RDLINT is updated on the falling edge of the ROHCLK signal. RDLINT is deasserted when the Interrupt Enable/Status Register is read in the HDLC receiver. By default RDLINT is an active low open-drain output, but can be configured as active high. Typically, RDLINT would be connected to an external DMA device. If the supervising microprocessor is desired to service the RFDL, this output can be wired-ORed with the INTB output when RDLINT is configured as an active-low open drain output.

Pin Name	Type	Pin No.	Function
RDLSIG/ RDLEOM	Output	32	The receive data link (RDLSIG) signal is active when an external HDLC receiver is selected (the REXHDLC bit in the corresponding Master HDLC Configuration Register is a logic 1). The RDLSIG signal carries bits extracted from the three C-bits in M-subframe #5 by the DS3 framer. RDLSIG is held high when C-bit parity mode is not enabled. RDLSIG is updated on the falling edge of the corresponding RDLCLK signal. The receive end of message (RDLEOM) signal is active if the internal HDLC receiver is selected (the REXHDLC bit in the Master HDLC Configuration Register is a logic 0). The RDLEOM signal is asserted when the last byte of a sequence is read from the HDLC receiver, or if the receiver's buffer overruns. RDLEOM is updated on the falling edge of the ROHCLK signal. RDLEOM is deasserted when the Interrupt Enable/Status Register is read in the HDLC Receiver. By default, RDLEOM is an active low open-drain output, but can be configured as active high. Typically, RDLEOM would be connected to the supervising microprocessor when an external DMA is used, signaling the microprocessor that a complete message is ready. In this case the RDLEOM is configured as an active-low open drain output and wired-ORed with the INTB output.

Pin Name	Type	Pin No.	Function
RD1CLK1	Output	198	The receive DS1 clock (RD1CLK[28:1]) signals provide timing for each of the 28 demultiplexed DS1 streams. The RD1CLK[28:1] signals are nominally 1.544 MHz clocks, but have substantial jitter due to the demultiplexing and destuffing processes. The RD1DAT[28:1] outputs are updated on the falling edges of the corresponding RD1CLK[28:1] signals. When the internal M12 multiplexers are configured for G.747 multiplexing, every fourth RD1CLK signal (RD1CLK4, 8, 12, 16, 20, 24, 28) is unused and held low. The remaining RD1CLK signals are then nominally 2.048 MHz clocks. When the internal M12 multiplexers are bypassed, every fourth RD1CLK signal (RD1CLK4, 8, 12, 16, 20, 24, 28) may become a DS2 rate clock operating at nominally 6.312 MHz. The remaining RD1CLK signals for the particular M12 multiplexer bypassed are then unused and held low. The internal M12 multiplexers may be bypassed or configured for G.747 multiplexing on an individual basis. Thus the configuration of each of the seven blocks of four RD1CLK signals is independently programmable.
RD1CLK2		193	
RD1CLK3		186	
RD1CLK4		180	
RD1CLK5		175	
RD1CLK6		170	
RD1CLK7		166	
RD1CLK8		159	
RD1CLK9		155	
RD1CLK10		151	
RD1CLK11		146	
RD1CLK12		142	
RD1CLK13		137	
RD1CLK14		133	
RD1CLK15		127	
RD1CLK16		122	
RD1CLK17		116	
RD1CLK18		110	
RD1CLK19		106	
RD1CLK20		102	
RD1CLK21		98	
RD1CLK22		91	
RD1CLK23		87	
RD1CLK24		82	
RD1CLK25		76	
RD1CLK26		71	
RD1CLK27		66	
RD1CLK28		62	

Pin Name	Type	Pin No.	Function
RD1DAT1	Output	202	The receive DS1 data (RD1DAT[28:1]) signals carry the 28 demultiplexed DS1 streams. The RD1DAT[28:1] outputs are updated on the falling edges of the corresponding RD1CLK[28:1] signals. When the internal M12 multiplexers are configured for G.747 multiplexing, every fourth RD1DAT signal (RD1DAT4, 8, 12, 16, 20, 24, 28) is unused and held low. The remaining RD1DAT signals are then nominally 2.048 Mbit/s data streams. When the internal M12 multiplexers are bypassed, every fourth RD1DAT signal (RD1DAT4, 8, 12, 16, 20, 24, 28) may become a DS2 rate data stream operating at nominally 6.312 Mbit/s. The remaining RD1DAT signals for the particular M12 multiplexer bypassed are then unused and held low. The internal M12 multiplexers may be bypassed or configured for G.747 multiplexing on an individual basis. Thus the configuration of each of the seven blocks of four RD1DAT signals is independently programmable.
RD1DAT2		195	
RD1DAT3		188	
RD1DAT4		182	
RD1DAT5		177	
RD1DAT6		173	
RD1DAT7		168	
RD1DAT8		161	
RD1DAT9		157	
RD1DAT10		153	
RD1DAT11		149	
RD1DAT12		144	
RD1DAT13		139	
RD1DAT14		135	
RD1DAT15		129	
RD1DAT16		124	
RD1DAT17		118	
RD1DAT18		114	
RD1DAT19		108	
RD1DAT20		104	
RD1DAT21		100	
RD1DAT22		94	
RD1DAT23		89	
RD1DAT24		84	
RD1DAT25		78	
RD1DAT26		74	
RD1DAT27		69	
RD1DAT28		64	

Pin Name	Type	Pin No.	Function
TD1CLK1	Input	201	The transmit DS1 clock (TD1CLK[28:1]) signals provide timing for each of the 28 DS1 streams to be multiplexed. The TD1CLK[28:1] signals should nominally be 1.544 MHz clocks, and should have the minimal jitter and wander of a standard DS1 line signal. The TD1DAT[28:1] inputs are sampled on the rising edges of the corresponding TD1CLK[28:1] signals. When the internal M12 multiplexers are configured for G.747 multiplexing, every fourth TD1CLK signal (TD1CLK4, 8, 12, 16, 20, 24, 28) is unused and ignored. The remaining TD1CLK signals should then nominally be 2.048 MHz clocks. When the internal M12 multiplexers are bypassed, every fourth TD1CLK signal (TD1CLK4, 8, 12, 16, 20, 24, 28) should then become a DS2 rate clock operating at nominally 6.312 MHz. The remaining TD1CLK signals for the particular M12 multiplexer bypassed are then unused and ignored. The internal M12 multiplexers may be bypassed or configured for G.747 multiplexing on an individual basis. Thus the configuration of each of the seven blocks of four TD1CLK signals is independently programmable.
TD1CLK2		194	
TD1CLK3		187	
TD1CLK4		181	
TD1CLK5		176	
TD1CLK6		172	
TD1CLK7		167	
TD1CLK8		160	
TD1CLK9		156	
TD1CLK10		152	
TD1CLK11		148	
TD1CLK12		143	
TD1CLK13		138	
TD1CLK14		134	
TD1CLK15		128	
TD1CLK16		123	
TD1CLK17		117	
TD1CLK18		112	
TD1CLK19		107	
TD1CLK20		103	
TD1CLK21		99	
TD1CLK22		92	
TD1CLK23		88	
TD1CLK24		83	
TD1CLK25		77	
TD1CLK26		72	
TD1CLK27		68	
TD1CLK28		63	

Pin Name	Type	Pin No.	Function
TD1DAT1	Input	203	The transmit DS1 data (TD1DAT[28:1]) signals carry the 28 DS1 streams to be multiplexed. The TD1DAT[28:1] inputs are sampled on the rising edges of the corresponding TD1CLK[28:1] signals. When the internal M12 multiplexers are configured for G.747 multiplexing, every fourth TD1DAT signal (TD1DAT4, 8, 12, 16, 20, 24, 28) is unused and ignored. The remaining TD1DAT signals should then nominally be 2.048 Mbit/s data streams. When the internal M12 multiplexers are bypassed, every fourth TD1DAT signal (TD1DAT4, 8, 12, 16, 20, 24, 28) may become a DS2 rate data stream operating at nominally 6.312 Mbit/s. The remaining TD1DAT signals for the particular M12 multiplexer bypassed are then unused and ignored. The internal M12 multiplexers may be bypassed or configured for G.747 multiplexing on an individual basis. Thus the configuration of each of the seven blocks of four TD1DAT signals is independently programmable.
TD1DAT2		196	
TD1DAT3		190	
TD1DAT4		184	
TD1DAT5		179	
TD1DAT6		174	
TD1DAT7		169	
TD1DAT8		162	
TD1DAT9		158	
TD1DAT10		154	
TD1DAT11		150	
TD1DAT12		145	
TD1DAT13		141	
TD1DAT14		136	
TD1DAT15		130	
TD1DAT16		126	
TD1DAT17		120	
TD1DAT18		115	
TD1DAT19		109	
TD1DAT20		105	
TD1DAT21		101	
TD1DAT22		97	
TD1DAT23		90	
TD1DAT24		86	
TD1DAT25		81	
TD1DAT26		75	
TD1DAT27		70	
TD1DAT28		65	

Pin Name	Type	Pin No.	Function
GD2CLK	Output	6	The transmit generated DS2 clock (GD2CLK) signal is provided for use in integrated M13 or C-bit parity multiplex applications. When configured for M13 operation, GD2CLK is nominally a 6.311993 MHz clock, which corresponds to a stuffing ratio of 39.1%. When configured for C-bit parity operation, GD2CLK is nominally a 6.3062723 MHz clock, which corresponds to a stuffing ratio of 100%. The GD2CLK may be connected to the TD2CLK input clock. GD2CLK is updated on the falling edge of TCLK.
TD2CLK	Input	206	The transmit DS2 clock (TD2CLK) signal provides timing for the multiplex side of all of the MX12 TSBs. TD2CLK is nominally a 6.312 MHz, 50% duty cycle clock.

Pin Name	Type	Pin No.	Function
TDLSIG/ TDLUDR	I/O	205	The transmit data link (TDLSIG) signal is active when an external HDLC receiver is selected (the TEXHDLC bit in the corresponding Master HDLC Configuration Register is a logic 1). The TDLSIG signal carries bits to be inserted in the three C-bits in M-subframe #5 by the DS3 transmitter. TDLSIG is ignored when C-bit parity mode is not enabled. TDLSIG is sampled on the rising edge of the TDLCLK signal. The transmit data link underrun (TDLUDR) signal is active when the internal HDLC receiver is selected (the TEXHDLC bit in the corresponding Master HDLC Configuration Register is a logic 0). TDLUDR is asserted when the internal HDLC transmitter underruns. TDLUDR is deasserted by writing to the XFDL Interrupt Status Register. By default TDLUDR is an active low open-drain output, but can be configured as active high. Upon a reset, the TEXHDLC bit a logic 1, thus, the pin is configured as an input, TDLSIG. Typically, TDLUDR would be connected to the supervising microprocessor when an external DMA is used, signaling the microprocessor that a severe error has occurred causing the transmit buffer to underrun. In this case the TDLUDR is configured as an active-low open drain output and wired-ORed with the INTB output.

Pin Name	Type	Pin No.	Function
TDLCLK/ TDLINT	Output	207	The transmit data link clock (TDLCLK) signal is active when an external HDLC receiver is selected (the TEXHDLC bit in the Master HDLC Configuration Register is a logic 1). The TDLCLK signal provides timing for the external sourcing of the path maintenance data link signal inserted by the DS3 TRAN. TDLCLK is updated on the falling edge of the TOHCLK signal and cycles 3 times per M-frame. TDLCLK is nominally a 28.2 kHz clock, which is low for at least 1.9 µs per cycle. The transmit data link interrupt (TDLINT) signal is active when the internal HDLC transmitter is selected (the TEXHDLC bit in the corresponding Master HDLC Configuration Register is a logic 0).TDLINT is asserted when the last data byte written to the internal HDLC transmitter has been setup for transmission, and a write is required to the XFDL Configuration Register, or the XFDL Transmit Data Register to either end the current message transmission, or to provide more data. By default TDLINT is an active low open-drain output, but can be configured as active high. Typically, TDLINT would be connected to an external DMA device. If the supervising microprocessor is desired to service the XFDL, this output can be wired-ORed with the INTB output when TDLINT is configured as an active-low open drain output.

Pin Name	Type	Pin No.	Function
TDLEOMI	Input	204	The transmit data link end of message input (TDLEOMI) provides a method for an external DMA controller to signal the end of the transmitted message to the HDLC transmitter without needing to write to the XFDL Configuration Register. The TDLEOMI input is active high and must be glitch-free. It internally sets the corresponding EOM register bit in the XFDL Configuration register. The TDLEOMI input may be asserted during or after the write of the last byte of a packet but before the next byte would be expected (within 210 µs of the last assertion of TDLINT or the INT bit in the XFDL Status Register). TDLEOMI must be deasserted before the write of the first byte of the next packet. TDLEOMI is ignored if no data transmission is pending.
TICLK	Input	1	The transmit input clock (TICLK) provides the transmit direction timing. TICLK is nominally a 44.736 MHz, 50% duty cycle clock. TIMFP is sampled on the rising edge of TICLK.
TIMFP	Input	208	The transmit M-frame pulse input (TIMFP) signal allows one to control the alignment of the M-frame of the transmitted DS3 stream (TDAT). The first bit (X1) of the M-frame on TDAT will occur within several TICLK cycles and be identified by the TMFP output signal. TIMFP may be tied low if such control is not required. TIMFP is sampled on the rising edge of TICLK.
TOH	Input	17	The transmit overhead data (TOH) signal contains the overhead bits (C, F, X, P, and M) that may be inserted in the transmitted DS3 stream. TOH is sampled on the rising edge of TOHCLK.

Pin Name	Type	Pin No.	Function
TOHEN	Input	18	The transmit overhead insertion (TOHEN) signal controls the insertion of DS3 overhead bits from the TOH input. When TOHEN is high, the associated overhead bit in the TOH stream is inserted in the transmitted DS3 frame. When TOHEN is low, the DS3 overhead bit is generated and inserted internally. TOHEN is sampled on the rising edge of TOHCLK.
TOHFP	Output	15	The transmit overhead frame position (TOHFP) signal may be used to align the individual overhead bits in the transmitted overhead data stream, TOH, to the DS3 M-frame. TOHFP is high during the X1 overhead bit position in the TOH stream. TOHFP is updated on the falling edge of TOHCLK.
TOHCLK	Output	14	The transmit overhead clock (TOHCLK) cycles once per overhead bit. TOHCLK is nominally a 526 kHz clock. TOHFP is updated on the falling edge of TOHCLK. TOH, and TOHEN are sampled on the rising edge of TOHCLK.
TCLK	Output	2	The transmit clock (TCLK) provides timing for circuitry downstream of the DS3 transmitter of the D3MX. TCLK is nominally a 44.736 MHz, 50% duty cycle clock.
TPOS/ TDAT	Output	3	The transmit positive pulse (TPOS) signal represents the positive pulses transmitted on the B3ZS-encoded line when configured for dual-rail operation. TPOS is updated on the falling edge of TCLK by default but may be enabled to be updated on the rising edge of TCLK. The transmit data output (TDAT) signal represents a unipolar DS3 output stream when configured for single rail operation. TDAT is updated on the falling edge of TCLK by default but may be enabled to be updated on the rising edge of TCLK.

Pin Name	Type	Pin No.	Function
TNEG/ TMFP	Output	5	The transmit negative pulse (TNEG) signal represents the negative pulses transmitted on the B3ZS-encoded line when configured for dual rail operation. TNEG is updated on the falling edge of TCLK by default but may be enabled to be updated on the rising edge of TCLK. The transmit multiframe pulse (TMFP) signal marks the transmit M-frame alignment when configured for single rail operation. The TMFP output is high during the first bit (X1) of the DS3 multiframe presented on TDAT. TMFP is updated on the falling edge of TCLK by default but may be enabled to be updated on the rising edge of TCLK.
INTB	Output	33	The active low interrupt (INTB) signal goes low when one of the DS3 FRMR, RBOC, DS2 FRMR, MX12, MX23 or PMON TSBs generates an interrupt, provided that the interrupt source in question is not masked. INTB goes high when the Interrupt Enable/Status Register is read in the corresponding TSB. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged. The INTB signal is an open drain output.
CSB	Input	45	The active low chip select (CSB) signal is low during D3MX register accesses. CSB must go high at least once after a powerup to clear internal test modes. If CSB is not used, then it should be tied to an inverted version of RSTB, in which case RDB and WRB determine register accesses
RDB	Input	57	The active low read enable (RDB) signal is low during D3MX register read accesses. The D3MX drives the D7-D0 bus with the contents of the addressed register while RDB and CSB are low.

Pin Name	Type	Pin No.	Function
WRB	Input	56	The active low write strobe (WRB) signal is low during a D3MX register write access. The D7-D0 bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D0 D1 D2 D3 D4 D5 D6 D7	I/O	34 35 37 38 39 41 42 44	The bidirectional data bus (D7-D0) is used during D3MX register read and write accesses.
A0 A1 A2 A3 A4 A5 A6 A7 A8/TRS	Input	47 48 49 50 51 52 53 54 55	The address bus (A8-A0) selects specific registers during D3MX register accesses. The test register select (TRS) signal discriminates between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. The TRS input has an integral pull down resistor. TRS should be connected to ground for normal mode register access.
RSTB	Input	58	The active low reset (RSTB) signal provides an asynchronous D3MX reset. RSTB is a Schmitt triggered input with an integral pull up resistor.

Pin Name	Type	Pin No.	Function
ALE	Input	46	The address latch enable (ALE) is active high and latches the address bus (A7-A0) and TRS when low. When ALE is high, the internal address latches are transparent. It allows the D3MX to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor.
VDDI1 VDDI2	Power	60 189	The core power (VDDI) pins should be connected to a well decoupled +5 V DC in common with VDDO.
VSSI1 VSSI2	Ground	59 191	The core ground (VSSI) pins should be connected to GND in common with VSSO.
VDDO1 VDDO2 VDDO3 VDDO4 VDDO5 VDDO6	Power	199 9 43 95 121 164	The pad ring power (VDDO) pins should be connected to a well decoupled +5 V DC in common with VDDI.
VSSO1 VSSO2 VSSO3 VSSO4 VSSO5 VSSO6 VSSO7 VSSO8 VSSO9 VSSO10	Ground	200 8 36 96 111 163 183 27 80 132	The pad ring ground (VSSO) pins should be connected to GND in common with VSSI.

Notes on Pin Description:

All D3MX inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.

All D3MX digital outputs and bidirectionals have 2 mA drive capability, except the INTB, TPOS/TDAT, TNEG/TMFP, TCLK, ROCLK, RODAT, RMFP, RMSFP, ROHP outputs and the D7-D0 bidirectionals, which have 4 mA drive capability.

The VSSO and VSSI ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the D3MX.

The VDDO and VDDI power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the D3MX.

208-pin QFP pins # 13, 28, 40, 61, 67, 73, 79, 85, 93, 113, 119, 125, 131, 140, 147, 165, 171, 178, 185, 192, 197 are all "no-connect".

8 FUNCTIONAL DESCRIPTION

8.1 DS3 Framer

The DS3 Framer (FRMR) Block integrates circuitry required for decoding a B3ZS-encoded signal and framing to the resulting DS3 bit stream. The FRMR is directly compatible with the M23 and C-bit parity DS3 applications.

The FRMR decodes a B3ZS-encoded signal and provides indications of line code violations. The B3ZS decoding algorithm and the LCV definition can independently be chosen via software. Loss of signal is also detected.

The framing algorithm examines five F-bit candidates simultaneously. When at least one discrepancy has occurred in all the candidates, the algorithm examines the next set of candidates. When a single F-bit candidate remains in a set, the first bit in the supposed M-subframe is examined for the M-frame alignment signal (i.e. the M-bits, M1,M2,M3, are following the 010 pattern). Framing is declared if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. During the examination of the M-bits the X-bits and P-bits are ignored. The algorithm gives a maximum average reframe time of less than 1.5 ms.

Once in-frame, the FRMR provides indications of the M-frame and M-subframe boundaries, and identifies the overhead bit positions in the incoming DS3 signal.

While the FRMR is in-frame, the F-bit and M-bit positions in the DS3 stream are examined. Out-of-frame is declared when 3 F-bit errors out of 16 consecutive F-bits or 8 consecutive F-bits are observed (selectable by the M3O8 bit), or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. The M-bit error criteria for OOF can be disabled via the MBDIS bit in the DS3 Framer configuration register. The 3 out of 8 consecutive F-bits out-of-frame ratio provides more robust operation in the presence of a 10^{-3} bit error rate than the 3 out of 16 consecutive F-bits ratio (less than one false OOF every minute verses one false OOF every 6 seconds, respectively); either choice of out-of-frame ratios allows an out-of-frame to be declared quickly when the M-subframe alignment patterns or, optionally, when the M-frame alignment is lost.

Also while in-frame, M-bit or F-bit framing bit errors and P-bit parity errors are indicated. When C-bit parity mode is enabled, both C-bit parity errors and far end block errors are indicated. These error indications, as well as the line code violation and excessive zeros indication, may be accumulated over 1 second intervals with the T3 Performance Monitor (PMON). Note that the framer is an

off-line framer, indicating both OOF and COFA events. Even if an OOF is indicated, the framer will continue indicating performance monitoring information based on the previous frame alignment.

Status signals such as the RED alarm, alarm indication signal, and the idle signal are detected. The framer employs a simple integration algorithm (with a 1:1 slope) that is based on the occurrence of "valid" M-frame intervals. For the RED alarm, an M-frame is said to be a "valid" interval if it contains a RED defect, defined as an occurrence of an OOF or LOS event during that M-frame. For AIS and IDLE, an M-frame is said to be a "valid" interval if it contains AIS or idle, defined as the occurrence of less than 15 discrepancies in the expected signal pattern ("1010" or "1111" for AIS; "1100" for idle) while valid frame alignment is maintained. The discrepancy threshold ensures the detection algorithms operate in the presence of bit error rates of up to 10^{-3}. For AIS, the expected pattern may be selected to be: the framed "1010" signal; the framed arbitrary DS3 signal and the C-bits all zero; the framed "1010" signal and the C-bits all zero; the framed all-ones signal (with overhead bits ignored); or the unframed all-ones signal (with overhead bits equal to ones). Each "valid" M-frame interval causes an associated integration counter to increment; "non-valid" M-frames cause a decrement. With the slow detection option, RED, AIS, or idle is declared if the associated count saturates at 127 which results in a detection time of 13.5 ms. With the fast detection option, RED, AIS, or idle is declared if the associated count saturates at 21 which results in a detection time of 2.23 ms. RED, AIS, or idle declaration is deasserted when the associated interval count decrements to 0.

Valid X-bits are extracted by the FRMR to provide indication of far end receive failure. The FERF status is set to logic 1 if the extracted X-bits are equal and are logic 0 (i.e. X1=X2=0); the status is set to logic 0 if the extracted X-bits are equal and are logic 1(i.e. X1=X2=1). If the X-bits are not equal, the FERF status remains in its previous state. The extracted FERF status is buffered for 2 M-frames before being reported within the DS3 FRMR Status register or being output on the RFERF pin. This buffer ensures a better than 99.99% chance of freezing the FERF status on a correct value during the occurrence of an out of frame. When an OOF occurs, the FERF value is held at the state contained in the buffer location corresponding to the second to last M-frame. This location is not updated until the OOF condition is deasserted. Meanwhile, the buffer location corresponding to the last M-frame is continually updated every M-frame based on the above FERF definition. Once correct frame alignment has been found and OOF is deasserted, the buffer location corresponding to the last M-frame will contain valid FERF status and the buffer location corresponding to the second to last M-frame is enabled to be updated every M-frame.

When enabled for C-bit parity operation, both the far end alarm and control channel and the path maintenance data link are extracted and serialized at 9.4 kbit/s and 28.2 kbit/s, respectively. Codes in the extracted far end alarm and control (FEAC) channel may be detected with the Bit-Oriented Code Detector (RBOC). HDLC messages in the extracted path maintenance data link may be received with the Data Link Receiver (RFDL).

The FRMR may be configured for C-bit parity mode or left in M23 mode. When C-bit parity mode is not enabled, outputs relating to C-bit parity features are forced to an inactive state. The FRMR, however, provides an indication of whether the C-bit parity application is present or absent, independent of how it is configured.

The FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the FRMR. Access to these registers is via a generic microprocessor bus.

Under DS3 AIS, LOF or LOS conditions, the M23 and M12 Multiplexers can receive data which corresponds to a continuous C-bit stuff ratio of between 0 and 100%. At the extremes of the stuff ratio (i.e. 0% and 100%) the recovered DS1/E1 tributary clocks will exceed their nominal value by up to +/-1750 ppm. This tributary frequency excursion could pose a problem for downstream circuitry in some applications.

8.2 DS3 Performance Monitor

The DS3 Performance Monitor (PMON) Block interfaces directly with the T3 Framer (FRMR) to accumulate line code violation (LCV) events, excessive zeros occurrences (EXZS), P-bit parity error (PERR) events, C-bit parity error (CPERR) events, far end block error (FEBE) events, and framing bit error (FERR) events in counters over intervals which are defined by successive microprocessor writes to a PMON counter register location. Each counter saturates at a specific value.

Due to the off-line nature of the T3 Framer, PMON continues to accumulate error events even while the FRMR is indicating OOF.

When a microprocessor write to a PMON count register is performed, a transfer clock signal is generated. This transfer clock causes the PMON block to transfer the current counter values into holding registers and reset the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

Whenever counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled. If the holding registers have not been read since the last interrupt, an overrun status bit is set.

8.3 Path Maintenance Data Link Receiver

The RFDL Data Link Receiver is a microprocessor peripheral used to receive LAPD/HDLC frames from the DS3 C-bit parity path maintenance data link

The RFDL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives frame data, and calculates the CRC-CCITT frame check sequence (FCS).

Received data is placed into a 4-level FIFO buffer. The Status Register contains bits which indicate overrun, end of message, flag detected, and buffered data available.

On end of message, the Status Register also indicates the FCS status and the number of valid bits in the final data byte. Interrupts are generated when one, two or three (programmable count) bytes are stored in the FIFO buffer. Interrupts are also generated when the terminating flag sequence, abort sequence, or FIFO buffer overrun are detected.

8.4 Alarm And Control Channel Bit Oriented Code Detector

The Bit-Oriented Code Detector (RBOC) Block detects the presence of 63 of the 64 possible bit-oriented codes (BOCs) transmitted in the DS3 C-bit parity far-end alarm and control (FEAC) channel. The 64th code ("111111") is similar to the HDLC flag sequence and is ignored.

Bit-oriented codes are received on the FEAC channel as 16-bit sequences each consisting of 8 ones, a zero, 6 code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are validated when repeated at least 10 times . The RBOC can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable Register.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all ones ("111111") if no valid code has been detected. The RBOC can be programmed to generate an interrupt when a detected code has been validated and when the code disappears.

8.5 DS3 Transmitter

The TRAN T3 transmitter integrates circuitry required to insert the overhead bits into a DS3 bit stream and produce a B3ZS encoded signal. The TRAN is directly compatible with the M23 and C-bit parity DS3 formats specified in ANSI T1.107a.

When configured for the C-bit parity application, all overhead bits are inserted. When configured for the M23 application, all overhead bits except the stuff control bits (the C-bits) are inserted; the C-bits must be inserted by upstream circuitry (such as the MX23 TSB). The TRAN provides indication of the M-frame boundary in the outgoing DS3 signal. The DS3 signal may optionally be encoded in B3ZS format.

Status signals such as far end receive failure, the alarm indication signal, and the idle signal can be inserted when their transmission is enabled by internal register bits.

A valid pair of P-bits is automatically calculated and inserted by the TRAN. When C-bit parity mode is selected, the C-bit parity bits, and far end block error (FEBE) indications are automatically inserted.

When enabled for C-bit parity operation, the alarm and control channel and the path maintenance data link are input serially at 9.4 kbit/s and 28.2 kbit/s, respectively, and inserted into the appropriate overhead bits. Codes to be inserted into the alarm and control channel are sourced by the XBOC bit-oriented code transmitter TSB. LAPD messages to be inserted in the path maintenance data link are sourced by the XFDL data link transmitter.

The TRAN supports diagnostic modes in which it inserts P or C-bit parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, or all-zeros.

8.6 Path Maintenance Data Link Transmitter

The XFDL Data Link Transmitter is designed to provide a serial path maintenance HDLC data link for the DS3 C-bit parity application. The XFDL is used under microprocessor to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, idle, and abort sequence insertion. Data to be transmitted is provided on an interrupt-driven basis by writing to a double-buffered transmit data register. Upon completion of the frames, a CRC-CCITT frame check sequence is transmitted, followed by idle flag sequences. If the transmit data register underflows, an abort sequence is automatically transmitted.

When enabled, the XFDL continuously transmits the flag character (01111110). Data bytes to be transmitted are written into the Transmit Data Register. After the parallel-to-serial conversion of each data byte, an interrupt is generated to signal the controller to write the next byte into the Transmit Data Register. After the last data frame byte, the CRC word (if CRC insertion has been enabled), or a flag (if CRC insertion has not been enabled) is transmitted. The XFDL then returns to the transmission of flag characters. The last data frame byte can be indicated by either writing to the EOM bit in the XFDL configuration register or by setting the TDLEOMI input high.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort characters.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the Transmit Data Register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDR status bit.

8.7 Alarm And Control Channel Bit Oriented Code Transmitter

The XBOC Bit-Oriented Code Transmitter TSB transmits 63 of the possible 64 bit-oriented codes (BOCs) over the DS3 C-bit parity far end alarm and control (FEAC) channel. The 64th possible code (111111) is similar to the HDLC idle sequence and is used in the XBOC to disable transmission of any bit-oriented codes.

BOCs are transmitted on the FEAC as a 16 bit sequence consisting of 8 ones, 1 zero, 6 code bits, and 1 trailing zero (111111110xxxxxx0). An internal register is loaded with the 6 code bits to be transmitted. The 16 bit sequence is continuously transmitted until disabled by forcing the six code bits to 111111.

8.8 M23 Multiplexer

The MX23 M23 Multiplexer integrates circuitry required to asynchronously multiplex and demultiplex seven DS2 streams into, and out of, an M23 or C-bit Parity formatted DS3 serial stream.

When multiplexing seven DS2 streams into an M23 formatted DS3 stream, the MX23 TSB performs rate adaptation to the DS3 by integral FIFO buffers, controlled by timing circuitry. The FIFO buffers accommodate in excess of 5.0 UIpp of sinusoidal jitter on TD2CLK for all jitter frequencies. The C-bits are also

generated and inserted by the timing circuitry. Software control is provided to transmit DS2 AIS and DS2 payload loopback requests. The loopback request is coded by inverting one of the three C-bits (the default option is compatible with ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7). The TSB also supports generation of a C-bit Parity formatted DS3 stream by providing a generated DS2 rate clock (GD2CLK) corresponding to a 100% stuffing ratio. Integrated M13 applications are supported by providing a generated DS2 rate clock corresponding to a 39.1% stuffing ratio.

When demultiplexing seven DS2 streams from an M23 formatted DS3, the MX23 performs bit destuffing via interpretation of the C-bits. The MX23 also detects and indicates DS2 payload loopback requests encoded in the C-bits. As per ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7, the loopback command is identified as C3 being the inverse of C1 and C2. Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames.

DS2 payload loopback can be activated or deactivated under software control. During payload loopback the DS2 stream being looped back still continues unaffected in the demultiplex direction to the DS2 Framer. All seven demultiplexed DS2 streams can also be replaced with AIS on an individual basis.

8.9 DS2 Framer

The FRMR DS2 Framer integrates circuitry required for framing to a DS2 bit stream and is directly compatible with the M12 DS2 application. The FRMR can also be configured to frame to a G.747 bit stream.

The DS2 FRMR frames to a DS2 signal with a maximum average reframe time of less than 7 ms and frames to a G.747 signal with a maximum average reframe time of 1 ms. In DS2 mode, both the F-bits and M-bits must be correct for a significant period of time before frame alignment is declared. In G.747 mode, frame alignment is declared if the candidate frame alignment signal has been correct for 3 consecutive frames (in accordance with CCITT Rec. G.747 Section 4). Once in frame, the DS2 FRMR provides indications of the M-frame and M-subframe boundaries, and identifies the overhead bit positions in the incoming DS2 signal or provides indications of the frame boundaries and overhead bit positions in the incoming G.747 signal.

Depending on configuration, declaration of DS2 out-of-frame occurs when 2 out of 4 or 2 out of 5 consecutive F-bits are in error (These two ratios are

recommended in TR-TSY-000009 Section 4.1.2) or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. The M-bit error criteria for OOF can be disabled via the MBDIS bit in the DS2 Framer configuration register. In G.747 mode, out-of-frame is declared when four consecutive frame alignment signals are incorrectly received (in accordance with CCITT Rec. G.747 Section 4). Note that the DS2 framer is an off-line framer, indicating both OFF and COFA. Error events continue to be indicated even when the FRMR is indicating OOF, based on the previous frame alignment.

The RED alarm and alarm indication signal are detected by the DS2 FRMR in 9.9 ms for DS2 format and in 6.9 ms for G.747 format. The framer employs a simple integration algorithm (with a 1:1 slope) that is based on the occurrence of "valid" DS2 M-frame or G.747 frame intervals. For the RED alarm, a DS2 M-frame (or G.747 frame, depending upon the framing format selected) is said to be a "valid" interval if it contains a RED defect, defined as the occurrence of an OOF event during that M-frame (or G.747 frame). For AIS, a DS2 M-frame (or G.747 frame) is said to be a "valid" interval if it contains AIS, defined as the occurrence of less than 9 zeros while the framer is out of frame during that M-frame (or G.747 frame). The discrepancy threshold ensures the detection algorithm operates in the presence of bit error rates of up to 10^{-3}. Each "valid" DS2 M-frame (or G.747 frame) causes an integration counter to increment; "non-valid" DS2 M-frame (or G.747 frame) intervals cause a decrement. RED or AIS is declared if the associated integrator count saturates at 53, resulting in a detection time of 9.9 ms for DS2 and 6.9 ms for G.747. RED or AIS declaration is deasserted when the associated count decrements to 0.

The DS2 X-bit or G.747 remote alarm indication (RAI) bit is extracted by the DS2 FRMR to provide an indication of far end receive failure. The FERF status is set to the current X/RAI state only if the two successive X/RAI bits were in the same state. The extracted FERF status is buffered for 6 DS2 M-frames or 6 G.747 frames before being reported within the DS2 FRMR Status register. This buffer ensures a virtually 100% probability of freezing the FERF status in a valid state during an out of frame occurrence in DS2 mode, and ensures a better than 99.9% probability of freezing the valid status during an OOF occurrence in G.747 mode. When an OOF occurs, the FERF value is held at the state contained in the last buffer location corresponding to the previous sixth M-frame or G.747 frame. This location is not updated until the OOF condition is deasserted. Meanwhile, the last four of the remaining five buffer locations are loaded with the frozen FERF state while the first buffer location corresponding to the current M-frame/ G.747 frame is continually updated every M-frame/G.747 frame based on the above FERF definition. Once correct frame alignment has been found and OOF is deasserted, the first buffer location will contain a valid FERF status and the

remaining five buffer locations are enabled to be updated every M-frame or G.747 frame.

DS2 M-bit and F-bit framing errors are indicated as are G.747 framing word errors (or bit errors) and G.747 parity errors. These error indications are accumulated for performance monitoring purposes in internal, microprocessor readable counters. The performance monitoring accumulators continue to count error indication even while the framer is indicating OOF.

The DS2 FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the DS2 FRMR.

8.10 M12 Multiplexer

The MX12 M12 Multiplexer integrates circuitry required to asynchronously multiplex and demultiplex four DS1 streams into, and out of, an M12 formatted DS2 serial stream (as defined in ANSI T1.107 Section 7) and to support asynchronous multiplexing and demultiplexing of three 2048 kbit/s into and out of a G.747 formatted 6312 kbit/s high speed signal (as defined in CCITT Rec. G.747).

When multiplexing four DS1 streams into an M12 formatted DS2 stream, the MX12 TSB performs logical inversion on the second and fourth tributary streams. Rate adaptation to the DS2 is performed by integral FIFO buffers, controlled by timing circuitry. The FIFO buffers accommodate in excess of 5.0 UIpp of sinusoidal jitter on the DS1 clocks for all jitter frequencies. X, F, M, and C bits are also generated and inserted by the timing circuitry. Software control is provided to transmit Far End Receive Failure (FERF) indications, DS2 AIS, and DS1 payload loopback requests. The loopback request is coded by inverting one of the three C-bits (the default option is compatible with ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7).Two diagnostic options are provided to invert the transmitted F or M bits.

When demultiplexing four DS1 streams from an M12 formatted DS2, the MX12 performs bit destuffing via interpretation of the C-bits. The MX12 also detects and indicates DS1 payload loopback requests encoded in the C-bits. As per ANSI T1.107 Section 7.2.1.1 and TR-TSY-000009 Section 3.7, the loopback command is identified as C3 being the inverse of C1 and C2. Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames.

DS1 payload loopback can be activated or deactivated under software control. During payload loopback the DS1 stream being looped back still continues unaffected in the demultiplex direction. The second and fourth demultiplexed DS1 streams are logically inverted, and all four demultiplexed DS1 streams can be replaced with AIS on an individual basis.

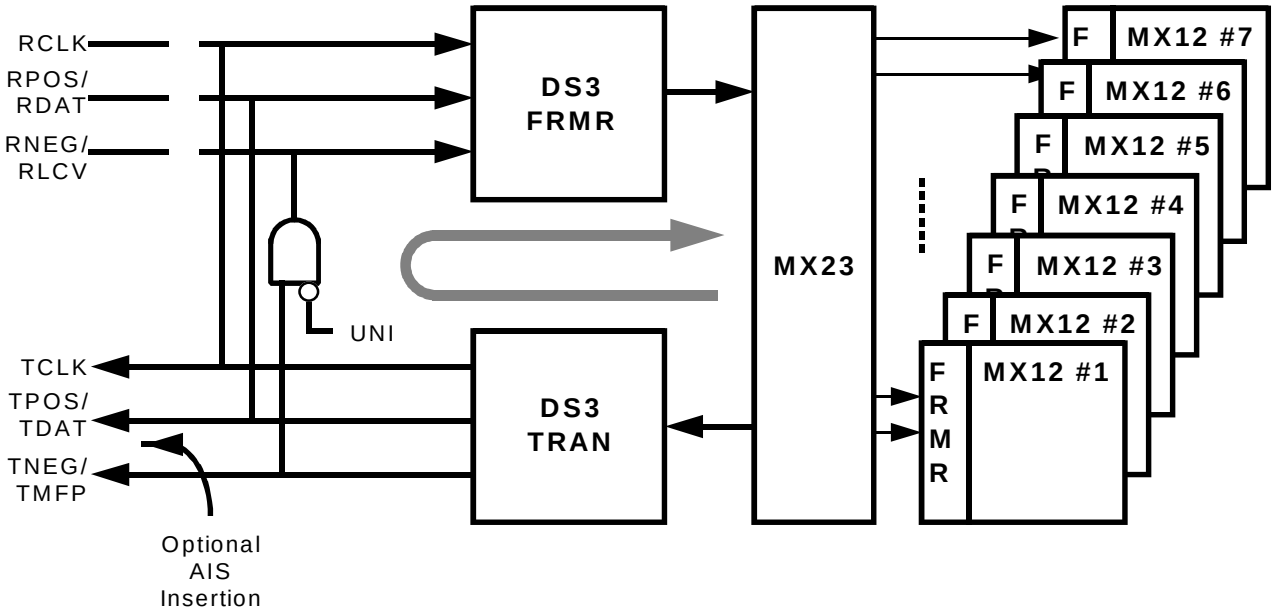
Similar functionality supports CCITT Recommendation G.747. The FIFO is still required for rate adaptation. The frame alignment signal and parity bit are generated and inserted by the timing circuitry. Software control is provided to transmit Remote Alarm Indication (RAI), high speed signal AIS, and the reserved bit. A diagnostic option is provided to invert the transmitted frame alignment signal and parity bit.

When demultiplexing three 2048 kbit/s streams from a G.747 formatted 6312 kbit/s stream, the MX12 performs bit destuffing via interpretation of the C-bits. Tributary payload loopback can be activated or deactivated under software control. Although no remote loopback request has been defined for G.747, inversion of the third C-bit triggers a loopback request detection indication in anticipation of Recommendation G.747 refinement. All three demultiplexed 2048 kbit/s streams can be replaced with AIS on an individual basis.

8.11 Loopback Modes

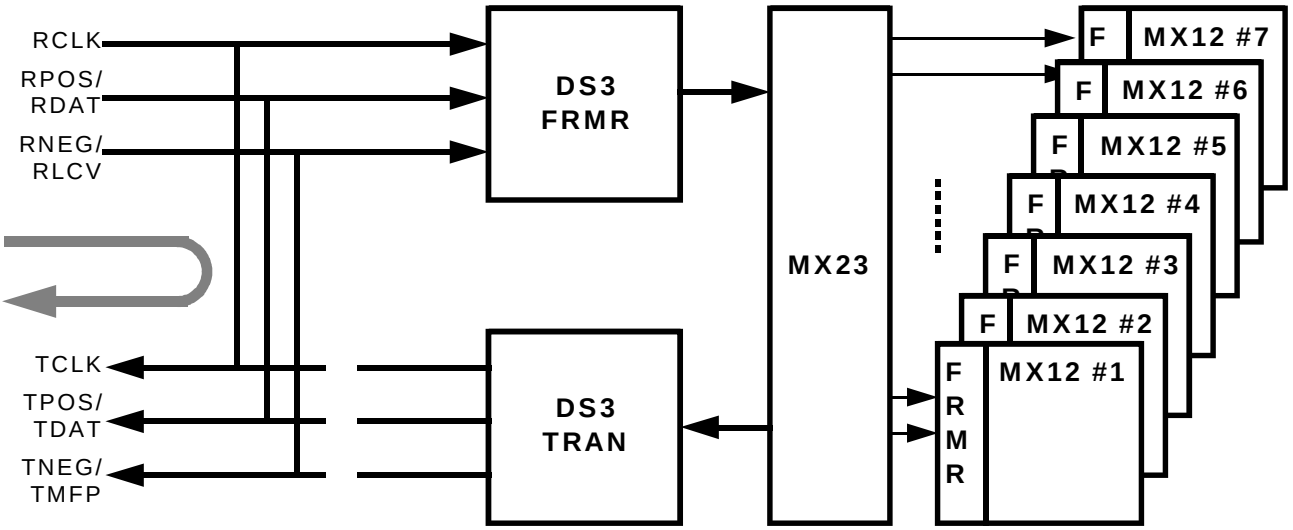
DS3 Diagnostic Loopback allows the transmitted DS3 stream to be looped back into the receive DS3 path, overriding the DS3 stream received on the RDAT/RPOS and RNEG/RLCV inputs. The RCLK signal is also substituted with the transmit DS3 clock, TCLK. While this mode is active, AIS may be substituted for the DS3 payload being transmitted on the TPOS/TDAT and TNEG/TMFP outputs. The configuration of the receive interface determines how the TNEG/TMFP signal is handled during loopback: if the UNI bit in the DS-3 FRMR is set, then the receive interface is configured for RDAT and RLCV, therefore the TNEG/TMFP signal is suppressed during loopback so that transmit MFP indications will not be seen nor accumulated as input LCVs; if the UNI bit is clear, then the interface is configured for bipolar signals RPOS and RNEG, therefore the TNEG is fed directly to the RNEG input. This loopback mode is shown diagrammatically, below:

Figure 2 - DS3 Diagnostic Loopback



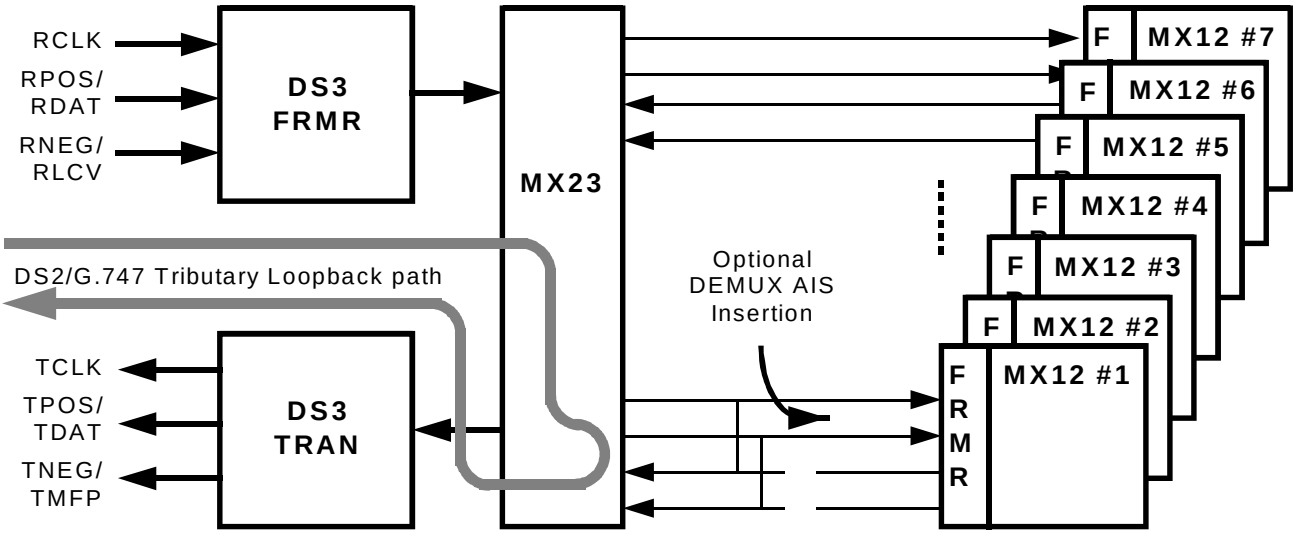
DS3 Line Loopback allows the received DS3 stream to be looped back into the transmit DS3 path, overriding the DS3 stream created internally by the multiplexing of the lower speed tributaries. The transmit signals on TPOS/TDAT and TNEG/TMFP are substituted with the receive signals on RPOS/RDAT and RNEG/RLCV. The TCLK signal is also substituted with the receive DS3 clock, RCLK. While this mode is active, AIS may be substituted for the DS3 payload being transmitted on the TPOS/TDAT and TNEG/TMFP outputs. Note that the transmit interface must be configured to be the same as the DS3-FRMR receive interface for this mode to work properly. This loopback mode is shown diagrammatically, below:

Figure 3 - DS3 Line Loopback



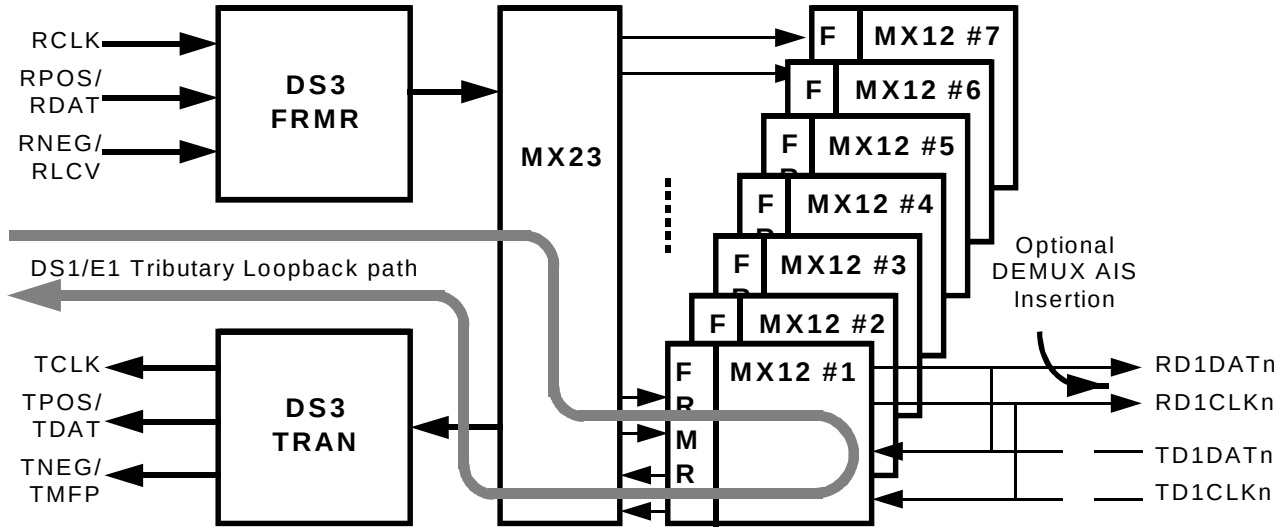
DS2/G.747 Demultiplex Loopback allows each of the seven demultiplexed DS2 or G.747 streams to be looped back into the MX23 and multiplexed up into the transmit DS3 stream, overriding the tributary DS2 stream coming from the MX12. This loopback mode is shown diagrammatically, below:

Figure 4 - DS2/G.747 Demultiplex Loopback



DS1/E1 Demultiplex Loopback allows each of the four demultiplexed DS1 or E1 streams to be looped back into the MX12 and ultimately multiplexed into the transmit DS3 stream, overriding the tributary DS1 or E1 stream coming from the T1DAT and T1CLK inputs. This loopback mode is shown diagrammatically, below:

Figure 5 - DS1/E1 Demultiplex Loopback



8.12 Microprocessor Interface

The Microprocessor Interface Block provides normal and test mode registers, the interrupt logic, and the logic required to connect to the Microprocessor Interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the D3MX. The register set is accessed as follows:

9 REGISTER MEMORY MAP

Address	Register
00H	Master Reset/Clock Status
01H	Revision/Global PMON Update
02H	Master Bypass Configuration
03H	Master HDLC Configuration
04H	Master Loopback Configuration
05H	Master Interface Configuration
06H	Master Alarm Enable/Network Requirement Bit
07H	Master Test
08H	Master Interrupt Source #1
09H	Master Interrupt Source #2
0AH	Master Interrupt Source #3
0BH	Reserved
0CH	DS3 TRAN Configuration
0DH	DS3 TRAN Diagnostic
0EH	DS3 TRAN Reserved
0FH	DS3 TRAN Reserved
10H	Reserved for DS3 PMON test
11H	DS3 PMON Interrupt Enable/Status
12H - 13H	Reserved
14H	DS3 PMON LCV Count (LSB)
15H	DS3 PMON LCV Count (MSB)
16H	DS3 PMON FERR Count (LSB)
17H	DS3 PMON FERR Count (MSB)
18H	DS3 PMON EXZS Count (LSB)
19H	DS3 PMON EXZS Count (MSB)
1AH	DS3 PMON PERR Count (LSB)

Address	Register
1BH	DS3 PMON PERR Count (MSB)
1CH	DS3 PMON CPERR Count (LSB)
1DH	DS3 PMON CPERR Count (MSB)
1EH	DS3 PMON FEBE Count (LSB)
1FH	DS3 PMON FEBE Count (MSB)
20H	XFDL TSB Configuration
21H	XFDL TSB Interrupt Status
22H	XFDL TSB Transmit Data
23H	XFDL Reserved
24H	RFDL TSB Configuration
25H	RFDL TSB Interrupt Control/Status
26H	RFDL TSB Status
27H	RFDL TSB Receive Data
28H	MX23 Configuration
29H	MX23 Demux AIS Insert
2AH	MX23 Mux AIS Insert
2BH	MX23 Loopback Activate
2CH	MX23 Loopback Request Insert
2DH	MX23 Loopback Request Detect
2EH	MX23 Loopback Request Interrupt
2FH	MX23 Reserved
30H	FEAC XBOC Reserved
31H	FEAC XBOC Code
32H	FEAC RBOC Configuration/Interrupt Enable
33H	FEAC RBOC Interrupt Status
34H	DS3 FRMR Configuration
35H	DS3 FRMR Interrupt Enable/Additional Configuration

Address	Register
36H	DS3 FRMR Interrupt Status
37H	DS3 FRMR Status
38H - 3FH	Reserved
40H	DS2 #1 FRMR Configuration
41H	DS2 #1 FRMR Interrupt Enable
42H	DS2 #1 FRMR Interrupt Status
43H	DS2 #1 FRMR Status
44H	DS2 #1 FRMR Monitor Interrupt Enable/Status
45H	DS2 #1 FRMR FERR Count
46H	DS2 #1 FRMR PERR Count (LSB)
47H	DS2 #1 FRMR PERR Count (MSB)
48H	DS2 #1 MX12 Configuration and Control
49H	DS2 #1 MX12 Loopback Code Select
4AH	DS2 #1 MX12 AIS Insert
4BH	DS2 #1 MX12 Loopback Activate
4CH	DS2 #1 MX12 Loopback Interrupt
50H - 57H	DS2 #2 FRMR Registers
58H - 5CH	DS2 #2 MX12 Registers
60H - 67H	DS2 #3 FRMR Registers
68H - 6CH	DS2 #3 MX12 Registers
70H - 77H	DS2 #4 FRMR Registers
78H - 7CH	DS2 #4 MX12 Registers
80H - 87H	DS2 #5 FRMR Registers
88H - 8CH	DS2 #5 MX12 Registers
90H - 97H	DS2 #6 FRMR Registers
98H - 9CH	DS2 #6 MX12 Registers
A0H - A7H	DS2 #7 FRMR Registers
A8H - ACH	DS2 #7 MX12 Registers

Address	Register
ACH - FFH	Reserved
100H-1FFH	Reserved for Test

For all register accesses, CSB must be low.

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the D3MX. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[8]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits typically has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bit must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the D3MX to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect D3MX operation unless otherwise noted.

Register 00H: Master Reset / Clock Status

Bit	Type	Function	Default
Bit7	R	DS3RCACT	X
Bit6	R	DS3TCACT	X
Bit5	R	DS2TCACT	X
Bit4		Unused	X
Bit3		Unused	X
Bit2		Unused	X
Bit1		Unused	X
Bit0	R/W	RESET	0

The Master Reset Register is provided at D3MX read/write address 00H.

RESET:

The RESET bit implements a software reset. If the RESET bit is a logic 1, the entire D3MX is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the D3MX out of reset. Holding the D3MX in a reset state effectively puts it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

DS3RCACT:

The DS3 Receive Clock Activity (DS3RCACT) bit indicates at least one low to high transition has occurred on the RCLK input since the last read of this register. The DS3RCACT bit is set to a logic 1 by a rising edge on the RCLK input and is cleared to a logic 0 by a read of this register.

DS3TCACT:

The DS3 Transmit Clock Activity (DS3TCACT) bit indicates at least one low to high transition has occurred on the TICLK input since the last read of this register. The DS3TCACT bit is set to a logic 1 by a rising edge on the TICLK input and is cleared to a logic 0 by a read of this register.

DS2TCACT:

The DS2 Transmit Clock Activity (DS2TCACT) bit indicates at least one low to high transition has occurred on the TD2CLK input since the last read of this register. The DS2TCACT bit is set to a logic 1 by a rising edge on the

TD2CLK input and is cleared to a logic 0 by a read of this register. Note that if the TD2CLK signal is absent for a period of time (i.e., TD2CLK clock failure), the D3MX must be reset once the TD2CLK signal is restored.

Register 01H: Revision/Global PMON Update

Bit	Type	Function	Default
Bit7	R	ID7	0
Bit6	R	ID6	0
Bit5	R	ID5	0
Bit4	R	ID4	0
Bit3	R	ID3	0
Bit2	R	ID2	0
Bit1	R	ID1	0
Bit0	R	ID0	0

The Revision/Global PMON Update Register is provided at D3MX read/write address 01H.

ID[7:0]

The version identification bits ID[7:0], are set to a fixed value representing the version number of the D3MX. These bits can be read by software to determine the version number.

Writing to this register causes all performance monitor counters (DS3 and DS2/G.747) to be updated simultaneously.

Register 02H: Master Bypass Configuration

Bit	Type	Function	Default
Bit7	R/W	EXD2CLK	0
Bit6	R/W	BYP7	0
Bit5	R/W	BYP6	0
Bit4	R/W	BYP5	0
Bit3	R/W	BYP4	0
Bit2	R/W	BYP3	0
Bit1	R/W	BYP2	0
Bit0	R/W	BYP1	0

The Master Bypass Configuration Register is provided at D3MX read/write address 02H.

BYP[7:1]:

The BYP[7:1] bits allow for each of the seven MX12 blocks to be individually bypassed so that an external DS2 may be multiplexed and demultiplexed directly without the intermediate M12 multiplexing. If BYP[n] is a logic 1, the following applies:

1. A nominally 6.312 MHz clock is expected on TD1CLK(4n).

2. A data stream synchronous to TD1CLK(4n) is expected on TD1DAT(4n).

3. The clocks on TD1CLK(4n-1), TD1CLK(4n-2) and TD1CLK(4n-3) have no effect.

4. The data streams on TD1DAT(4n-1), TD1DAT(4n-2) and TD1DAT(4n-3) are ignored.

5. A nominally 6.312 MHz clock is presented on RD1CLK(4n).

6. A data stream synchronous to RD1CLK(4n) is presented on RD1DAT(4n).

7. The signals on RD1CLK(4n-1), RD1CLK(4n-2), RD1CLK(4n-3), RD1DAT(4n-1), RD1DAT(4n-2) and RD1DAT(4n-3) are always low.

EXD2CLK bit:

The EXD2CLK bit selects between an internally generated DS2 clock and the clock input on the TD2CLK pin. If EXD2CLK is a logic 0, the DS2 clock for the multiplexing side becomes the generated clock derived from the DS3 transmit TICLK clock. The generated DS2 clock is nominally 6.306272 MHz while in C-bit parity mode and while in M23 mode, it is nominally 6.311993 MHz. If EXD2CLK is a logic 1, the transmit DS2 clock becomes TD2CLK.

Register 03H: Master HDLC Configuration

Bit	Type	Function	Default
Bit7	R/W	REXHDLC	0
Bit6	R/W	TEXHDLC	1
Bit5		Unused	X
Bit4		Unused	X
Bit3	R/W	REOMPOL	0
Bit2	R/W	TUDRPOL	0
Bit1	R/W	RINTPOL	0
Bit0	R/W	TINTPOL	0

The Master HDLC Configuration Register is provided at D3MX read/write address 03H.

REXHDLC:

The state of the receive external HDLC (REXHDLC) bit determines whether the C-bit parity path maintenance data link is terminated by the internal HDLC receiver or by an external HDLC receiver. When the REXHDLC bit is a logic 0, the internal HDLC receiver is selected; the RDLCLK/RDLINT pin is configured to output the interrupt signal (RDLINT) from the internal HDLC receiver and the RDLSIG/RDLEOM pin is configured to output the end-of-message signal (RDLEOM) from the internal HDLC receiver. When the REXHDLC bit is a logic 1, the use of an external HDLC receiver is selected; the RDLSIG/RDLEOM pin is configured to output the data link data stream (RDLSIG) and the RDLCLK/RDLINT pin is configured to output the data link clock signal (RDLCLK). The REXHDLC bit is cleared to logic 0 upon reset.

TEXHDLC:

The state of the transmit external HDLC (TEXHDLC) bit determines whether the C-bit parity path maintenance data link is sourced by the internal HDLC transmitter or by an external HDLC transmitter. When the TEXHDLC bit is a logic 0, the internal HDLC transmitter is selected; the TDLCLK/TDLINT pin is configured as an output to present the interrupt signal (TDLINT) from the internal HDLC transmitter and the TDLSIG/TDLUDR pin is configured to output the underrun signal (TDLUDR) from the internal HDLC transmitter. When the TEXHDLC bit is a logic 1, the use of an external HDLC transmitter is selected; the TDLSIG/TDLUDR pin is configured to input the data link data

stream (TDLSIG) and the TDLCLK/TDLINT pin is configured to output the data link clock signal (TDLCLK). The TEXHDLC bit is set to logic 1 upon reset.

REOMPOL:

The Receive End-of-Message Polarity (REOMPOL) bit determines the assertion level of the RDLEOM output. If REOMPOL is a logic 0, the RDLEOM output is an active low open-drain output. If REOMPOL is a logic 1, the RDLEOM output is asserted high and always has a strong drive. If the REXHDLC bit is a logic 1, this bit has no effect.

TUDRPOL:

The Transmit Underflow Polarity (TUDRPOL) bit determines the assertion level of the TDLUDR output. If TUDRPOL is a logic 0, the TDLUDR output is an active low open-drain output. If TUDRPOL is a logic 1, the TDLUDR output is asserted high and always has a strong drive. If the TEXHDLC bit is a logic 1, this bit has no effect.

RINTPOL:

The Receive Interrupt Polarity (RINTPOL) bit determines the assertion level of the RDLINT output. If RINTPOL is a logic 0, the RDLINT output is an active low open-drain output. If RINTPOL is a logic 1, the RDLINT output is asserted high and always has a strong drive. If the REXHDLC bit is a logic 1, this bit has no effect.

TINTPOL:

The Transmit Interrupt Polarity (TINTPOL) bit determines the assertion level of the TDLINT output. If TINTPOL is a logic 0, the TDLINT output is an active low open-drain output. If TINTPOL is a logic 1, the TDLINT output is asserted high and always has a strong drive. If the TEXHDLC bit is a logic 1, this bit has no effect.

Register 04H: Master Loopback Configuration

Bit	Type	Function	Default
Bit7		Unused	X
Bit6		Unused	X
Bit5		Unused	X
Bit4		Unused	X
Bit3	R/W	LINEAIS[1]	0
Bit2	R/W	LINEAIS[0]	0
Bit1	R/W	LLBE	0
Bit0	R/W	DLBE	0

The Master Loopback Configuration Register is provided at D3MX read/write address 04H.

DLBE:

The diagnostic loopback enable (DLBE) bit allows the looping back of the transmitted DS3 into the receive DS3 path for diagnostic purposes. If the DLBE bit is a logic 1, the TPOS, TNEG, and TCLK signals are connected internally to replace the signals normally input on the RPOS, RNEG, and RCLK pins.

LLBE:

The line loopback enable (LLBE) bit allows the looping back of the received DS3 into the transmit DS3 path. If the LLBE bit is a logic 1, the RPOS, RNEG, and RCLK signals are connected internally to replace the signals normally output on the TPOS, TNEG, and TCLK pins.

LINEAIS[1:0]

The line AIS (LINEAIS[1:0]) bits allow the generation of various AIS patterns on the TDAT output when TUNI is set to logic 1, or on the TPOS and TNEG outputs when TUNI is set to logic 0, independent of the data stream being transmitted. The LINEAIS[1:0] option is expected to be used when the diagnostic loopback is invoked, ensuring that only a valid DS3 stream enters the network. The LINEAIS[1:0] bits select one of the following AIS patterns for transmission:

LINEAIS[1:0]	AIS Transmitted
00	none
01	Framed, repetitive 1010… pattern with C-bits forced to logic 0
10	Framed, repetitive 1111… pattern with C-bits forced to logic 0
11	Unframed, all-ones pattern

The LINEAIS[1:0]= 01 option is compatible with TR-TSY-000009 Section 3.7 objectives. If the intention is to loopback the AIS, the AIS bit in the DS3 TRAN Configuration Register should be written instead.

Register 05H: Master Interface Configuration

Bit	Type	Function	Default
Bit7		Unused	X
Bit6		Unused	X
Bit5		Unused	X
Bit4	R/W	TINV	0
Bit3	R/W	TRISE	0
Bit2	R/W	TUNI	0
Bit1	R/W	RINV	0
Bit0	R/W	RFALL	0

The Master Interface Configuration Register is provided at D3MX read/write address 05H.

RFALL:

The receive falling edge select (RFALL) bit configures the sampling edge used on the DS3 receive interface. When RFALL is a logic 1, the DS3 receive interface is sampled on the falling edge of RCLK. When RFALL is a logic 0, the DS3 receive interface is sampled on the rising edge of RCLK.

RINV:

The receive invert (RINV) bit enables data inversion of the DS3 receive interface. When RINV is a logic 1, the RPOS and RNEG signals are active low. When RINV is a logic 0, the RPOS and RNEG signals are active high. Inversion only takes place when the DS3 receive interface is configured for dual rail operation.

TUNI:

The transmit unipolar (TUNI) bit configures the DS3 transmit interface for unipolar or dual rail operation. When TUNI is a logic 1, the DS3 transmit interface is configured as TDAT and TMFP. When TUNI is a logic 0, the DS3 transmit interface is configured as TPOS and TNEG.

TRISE:

The transmit falling edge select (TRISE) bit configures the updating edge used on the DS3 transmit interface. When TRISE is a logic 1, the DS3

transmit interface is updated on the rising edge of TCLK. When TRISE is a logic 0, the DS3 transmit interface is updated on the falling edge of TCLK.

TINV:

The transmit invert (TINV) bit enables data inversion of the DS3 transmit interface. When TINV is a logic 1, the TPOS and TNEG signals are active low. When TINV is a logic 0, the TPOS and TNEG signals are active high. Inversion only takes place when the DS3 transmit interface is configured for dual rail operation.

Register 06H: Master Alarm Enable/Network Requirement Bit

Bit	Type	Function	Default
Bit 7	R/W	TNR	1
Bit 6	R	RNR	X
Bit 5	R/W	ALTFEBE	0
Bit 4	R/W	REDO	0
Bit 3	R/W	RED2ALME	0
Bit 2	R/W	DS2ALME	0
Bit 1	R/W	RED3ALME	0
Bit 0	R/W	DS3ALME	0

The Master Alarm Enable/Network Requirement Bit Register is provided at D3MX read/write address 06H.

DS3ALME:

The DS3 Alarm Enable (DS3ALME) bit allows the automatic generation of AIS in all of the demultiplexed DS2s upon a DS3 alarm condition. If DS3ALME is a logic 1, a DS3 loss of signal (>175 zeros), a DS3 out-of-frame (OOF) condition (i.e. immediately after 3-of-n F-bit errors where n is 8 or 16, or 3-of-4 M-frames containing M-bit errors), DS3 idle code detection or DS3 AIS detection causes all of the DS2s to be replaced by an unframed all ones pattern immediately. Generation of AIS continues while the detected alarm condition persists. If DS3ALME is a logic 0, AIS can still be generated in the demultiplexed DS2s under software control by setting the bits in the MX23 Demux AIS Insert Register.

RED3ALME:

The RED DS3 Alarm Enable (RED3ALME) bit works in conjunction with the DS3ALME and enables detection of DS3 RED condition to be used in place of DS3 loss of signal and DS3 out-of-frame in the above criteria for demultiplexed AIS generation. When DS3ALME is set to logic 1 and REDALME is set to logic 1, the occurrence of LOS or OOF for 127 consecutive M-frames (or 21 consecutive M-frames, if FDET is set to logic 1 in the DS3 FRMR configuration register) causes a DS3 RED alarm condition and generates the DS2 AIS. When DS3ALME is set to logic 1 and REDALME is set to logic 0, any occurrence of LOS or OOF generates the DS2 AIS. If DS3ALME is a logic 0, the REDALME bit is ignored.

DS2ALME:

The DS2 Alarm Enable (DS2ALME) bit allows the automatic generation of AIS in the DS1s demultiplexed from a DS2 or G.747 stream which is in an alarm condition. If DS2ALME is a logic 1,a DS2 or G.747 out-of-frame (OOF) condition (i.e. immediately after 2-of-n F-bit errors where n is 4 or 5, or 3-of-4 M-frames containing M-bit errors for DS2, or immediately after 4 consecutive framing word errors for G.747) or detection of DS2 or G.747 AIS causes each of the associated DS1s to be replaced by an unframed all ones pattern immediately. If DS2ALME is a logic 0, AIS can still be generated in the demultiplexed DS1s under software control by setting the bits in the appropriate MX12 AIS Insert Register. Note that the removal of the auto all-ones insertion is performed upon the first DS2 M-frame or G.747 frame pulse after the DS2 FRMR has found frame alignment.

RED2ALME:

The RED DS2 Alarm Enable (RED2ALME) bit works in conjunction with the DS2ALME and enables detection of DS2 RED condition to be used in place of DS2/G.747 out-of-frame in the above criteria for demultiplexed AIS generation. When DS2ALME is set to logic 1 and RED2ALME is set to logic 1, the occurrence of OOF for 53 consecutive DS2/G.747 "M-frames" causes a DS2 RED alarm condition and generates the DS1 AIS. When DS2ALME is set to logic 1 and RED2ALME is set to logic 0, any occurrence of OOF generates the DS1 AIS. If DS2ALME is a logic 0, the RED2ALME bit is ignored.

REDO:

The RED Alarm Output Enable (REDO) bit selects the type of signal output on the ROOF/RRED pin. If REDO is a logic 1, the DS3 RED status signal is available on the ROOF/RRED output pin. If REDO is a logic 0, the DS3 OOF status signal is available on the ROOF/RRED output pin.

ALTFEBE:

The Alternate Far End Block Error (ALTFEBE) bit selects the error conditions detected to define a FEBE indication. If ALTFEBE is a logic 1, a FEBE indication is generated in the outgoing C-bit Parity DS3 transmit stream if a C-bit parity error occurred in the last received M-frame. If no C-bit parity error occurred, no FEBE is generated. If ALTFEBE is a logic 0, a FEBE indication is generated if either one or more framing bit errors or a C-bit parity error has occurred in the last received M-frame. If no framing bit errors nor C-bit parity errors have occurred, then no FEBE is generated.

RNR:

The Receive Network Requirement (RNR) bit reflects the real time value of the Network Requirement (N_r) bit presented in the second C-bit in M-subframe 1 when in DS3 C-bit parity mode. The RNR bit is a logic 1 if a logic one occurs in the N_r overhead bit timeslot. If C-bit parity is not selected, the value of RNR is meaningless and random.

TNR:

The Transmit Network Requirement (TNR) bit determines the value inserted into the Network Requirement (N_r) bit transmitted in the second C-bit in M-subframe 1 when in DS3 C-bit parity mode. A logic 1 in the TNR bit causes a one to be transmitted in the N_r overhead bit timeslot. The TNR bit is set to a logic 1 upon either a hardware or software reset. If C-bit parity is not selected, the TNR bit has no effect. Note that the serial control input, TOHEN, takes precedence over the effect of this bit when TOHEN is asserted during the Network Requirement Bit position. While TOHEN is asserted at the second C-bit position of M-subframe 1, the data on the TOH input is transmitted in the N_r bit.

When the device is set for transmission of AIS (Register 0CH Bit 6) in C-bit parity mode, all C-bits are forced to 0 except for the network requirement bit which is forced to the TNR register bit value. The TNR bit must be cleared when TRAN is enabled to generate AIS in C-bit parity mode.

Register 07H: Master Test

Bit	Type	Function	Default
Bit 7	R/W	VCLK_IOTST	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	X
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	X

The Master Test Register is provided at D3MX read/write address 07H.

This register is used to select D3MX test features. All bits, except for PMCTST, are reset to zero by a hardware reset of the D3MX; a software reset of the D3MX does not affect the state of the bits in this register.

VCLK_IOTST:

The VCLK_IOTST bit replaces the RCLK/VCLK input as the test clock when the IOTST bit is a logic 1. Some sense points require a rising edge on the test clock to clock in the value on the pin. This bit satisfies the requirement without needing the RCLK/VCLK input to toggle.

PMCTST:

The PMCTST bit is used to configure the D3MX for PMC's manufacturing tests. When PMCTST is set to logic 1, the D3MX microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin while IOTST is a logic 1. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the D3MX to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the

data bus driver pads. When IOTST and PMCTST are both logic 0, the DBCTRL bit is ignored.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the D3MX for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the D3MX . While the HIZIO bit is a logic 1, all output pins of the D3MX except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

Register 08H: Master Interrupt Source #1

Bit	Type	Function	Default
Bit 7	R	REG2	0
Bit 6	R	REG3	0
Bit 5	R	XFDLINT	0
Bit 4	R	MX23	0
Bit 3	R	DS3FRMR	0
Bit 2	R	RFDLINT	0
Bit 1	R	RFDLEOM	0
Bit 0	R	RBOC	0

This register allows software to determine which of the MX23, DS3 FRMR, or RBOC TSBs produced the interrupt on the INTB output pin and whether there are any pending interrupts in the other two Interrupt Source registers. Also, this register reports whether the RFDL or XFDL TSBs have generated interrupts on their respective HDLC Controller outputs (i.e. RDLINT, RDLEOM, TDLINT, TDLUDR). These four signals can be configured for active-low, open-drain output and wire-ORed together with the INTB output to generate a global microprocessor interrupt.

Reading this register does not remove the interrupt indication; the corresponding TSB's interrupt status register must be read to remove the interrupt indication.

RBOC:

If the RBOC bit is a logic 1, the FEAC RBOC TSB is generating an interrupt. Register 33H should be read to determine which event in RBOC has caused to interrupt.

RFDLEOM:

If the RFDLEOM bit is a logic 1, the RFDL TSB is generating an interrupt due to an end of message occurrence (also visible on the RDLEOM output when configured for internal HDLC, i.e. REXHDLC=0).

RFDLINT:

If the RFDLINT bit is a logic 1, the RFDL TSB is generating an interrupt (also visible on the RDLINT output when configured for internal HDLC, i.e. REXHDLC=0).

DS3FRMR:

If the DS3FRMR bit is a logic 1, the DS3 FRMR TSB is generating an interrupt. Register 36H should be read to determine which event in DS3 FRMR has caused to interrupt.

MX23:

If the MX23 bit is a logic 1, the MX23 TSB is generating an interrupt due to the detection of a DS2 loopback request.

XFDLINT:

If the XFDLINT bit is a logic 1, the XFDL TSB is generating an interrupt (also visible on the TDLINT output when configured for internal HDLC, i.e. TEXHDLC=0).

REG2:

If the REG2 bit is a logic 1, at least one bit in the Master Interrupt Source #2 Register is set, that is, at least one DS2 Framer or the XFDL is generating an interrupt.

REG3:

If the REG3 bit is a logic 1, at least one bit in the Master Interrupt Source #3 Register is set, that is, at least one M12 Multiplexer is generating an interrupt.

Register 09H: Master Interrupt Source #2

Bit	Type	Function	Default
Bit 7	R	XFDLUDR	0
Bit 6	R	DS2FRMR #7	0
Bit 5	R	DS2FRMR #6	0
Bit 4	R	DS2FRMR #5	0
Bit 3	R	DS2FRMR #4	0
Bit 2	R	DS2FRMR #3	0
Bit 1	R	DS2FRMR #2	0
Bit 0	R	DS2FRMR #1	0

This register allows software to determine which of the seven DS2 framer TSBs produced the interrupt on the INTB output pin, or whether the XFDL TSB produced an underrun condition.

Reading this register does not remove the interrupt indication; the corresponding TSB's interrupt status register must be read to remove the interrupt indication.

XFDLUDR:

If the XFDLUDR bit is a logic 1, the XFDL TSB is generating an interrupt due to an underrun of the transmit data buffer (also visible on the TDLUDR output when configured for internal HDLC, i.e. TEXHDLC=0).

Register 0AH: Master Interrupt Source #3

Bit	Type	Function	Default
Bit 7	R	DS3PMON	0
Bit 6	R	MX12 #7	0
Bit 5	R	MX12 #6	0
Bit 4	R	MX12 #5	0
Bit 3	R	MX12 #4	0
Bit 2	R	MX12 #3	0
Bit 1	R	MX12 #2	0
Bit 0	R	MX12 #1	0

This register allows software to determine which of the seven MX12 TSBs or the DS3 PMON TSB produced the interrupt on the INTB output pin.

Reading this register does not remove the interrupt indication; the corresponding TSB's interrupt status register must be read to remove the interrupt indication.

Register 0CH:DS3 TRAN Configuration

Bit	Type	Function	Default
Bit7	R/W	CBTRAN	0
Bit6	R/W	AIS	0
Bit5	R/W	IDL	0
Bit4	R/W	FERF	0
Bit3	R/W	SBOW	0
Bit2		Unused	X
Bit1		Unused	X
Bit0	R/W	CBIT	0

CBIT:

The CBIT bit enables the C-bit parity application. When CBIT is a logic 1, C-bit parity is enabled, and the associated functions are inserted in the C-bit positions of the incoming DS3 stream. When CBIT is a logic 0, the M23 application is selected, and the C-bits are passed transparently through the DS3 TRAN.

SBOW:

The SBOW bit selects whether to insert the bit from the TOH input into the stuff opportunity bit or into the F4 bit. When SBOW is a logic 1, the bit from the TOH input is inserted into the stuff opportunity bit. When SBOW is a logic 0, the bit from the TOH input is inserted into the F4 bit.

FERF:

The FERF bit enables transmission of far end receive failure in the outgoing DS3 stream. When FERF is a logic 1, the X1 and X2 overhead bit positions in the DS3 stream are set to logic 0. When FERF is a logic 0, the X1 and X2 overhead bit positions in the DS3 stream are set to logic 1.

AIS, IDL:

The AIS and IDL bits enable the transmission of the alarm indication signal and the idle signal. When AIS is a logic 1, the transmit DS3 payload (on the TDAT/TPOS and TNEG outputs) is overwritten with the pattern 1010... When IDL is a logic 1, the transmit DS3 payload is overwritten with the pattern 1100...

CBTRAN:

The CBTRAN bit controls the C-bits during AIS transmission. When CBTRAN is a logic 0, the C-bits are overwritten with zeros during AIS transmission (as is currently specified in ANSI T1.107a Section 8.1.3.1). The only exception is the network requirement bit, which is forced to the TNR register bit value. When CBTRAN is a logic 1 and the M23 application is enabled, the C-bits pass through transparently during AIS transmission. When CBTRAN is a logic 1, and the C-bit parity application is enabled, the C-bits are overwritten with the appropriate C-bit parity functions during AIS transmission.

Register 0DH:DS3 TRAN Diagnostic

Bit	Type	Function	Default
Bit7	R/W	DLOS	0
Bit6	R/W	DLCV	0
Bit5		Unused	X
Bit4	R/W	DFERR	0
Bit3	R/W	DMERR	0
Bit2	R/W	DCPERR	0
Bit1	R/W	DPERR	0
Bit0	R/W	DFEBE	0

DFEBE:

The DFEBE controls the insertion of far end block errors in the outgoing DS3 stream. When DFEBE is set to a logic 1, and the C-bit parity application is enabled, the three C-bits in M-subframe 4 are set to a logic 0.

DPERR:

The DPERR controls the insertion of parity errors (P-bit errors) in the outgoing DS3 stream. When DPERR is set to a logic 1, the P-bits are inverted before insertion in the DS3 stream.

DCPERR:

The DCPERR controls the insertion of C-bit parity errors in the outgoing DS3 stream. When DCPERR is set to a logic 1, and the C-bit parity application is enabled, the three C-bits in M-subframe 3 are inverted before insertion in the DS3 stream.

DMERR:

The DMERR controls the insertion of framing errors (M-bit errors) in the outgoing DS3 stream. When DMERR is set to a logic 1, the M-bits are inverted before insertion in the DS3 stream.

DFERR:

The DFERR controls the insertion of framing errors (F-bit errors) in the outgoing DS3 stream. When DFERR is set to a logic 1, the F-bits are inverted before insertion in the DS3 stream.

DLCV:

The DLCV controls the insertion of a single line code violation in the outgoing DS3 stream. When the DLCV is set to logic 1, a line code violation is inserted by generating an incorrect polarity of violation in the next B3ZS signature. The data being transmitted must therefore contain periods of three consecutive zeros in order for the line code violation to be inserted. For example line code violations may not be inserted when transmitting AIS, but will be inserted when transmitting the idle signal. This bit is automatically cleared upon insertion of the line code violation.

DLOS:

The DLOS controls the insertion of loss of signal in the outgoing DS3 stream. When DLOS is set to a logic 1, the data on outputs TPOS, TNEG, and TDAT are forced to continuous zeros.

10.1 DS3 PMON Registers

Latching Performance Data

The DS3 Performance Monitor (PMON) data registers (16H-1FH) are updated by the rising edge of an internal transfer clock signal. The time between successive rising edges of the transfer clock determines the accumulation interval, which is nominally one second. A microprocessor write to any of the PMON count data registers causes a transfer clock and an update of the PMON data registers. Only one register location need be written to cause an update of all PMON data registers. The PMON is loaded with new performance data within 3 ROHCLK periods of the trailing edge of a microprocessor write. With ROHCLK at its nominal frequency of 526 kHz, the PMON registers should not be read until 6 µs have elapsed since the microprocessor write was performed. The data contained in the holding registers are subsequently read from the PMON registers by the microprocessor. The loading is synchronized to the internal event timing so that no events are missed.

Register 11H: DS3 PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	0
Bit 0	R	OVR	0

OVR:

The overrun (OVR) bit indicates the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

INTR:

The interrupt (INTR) bit indicates the current status of the internal interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read. The value of the INTR bit is not affected by the value of the INTE bit.

INTE:

A logic 1 in the INTE bit position enables the DS3 PMON to generate a microprocessor interrupt and assert the INTB output when the counter values are transferred to the holding registers. A logic 0 in the INTE bit position disables the DS3 PMON from generating an interrupt. When the TSB is reset, the INTE bit is set to logic 0, disabling the interrupt. The interrupt is cleared when this register is read.

Register 14H: DS3 LCV Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 15H: DS3 LCV Count MSB

Bit	Type	Function	Default
Bit 7	R	LCV[15]	X
Bit 6	R	LCV[14]	X
Bit 5	R	LCV[13]	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

These registers indicate the number of DS3 Line Code Violation (LCV) events that occurred during the previous accumulation interval.

A transfer operation of all counter registers within the selected PMON can be triggered by writing to either LCV Count Register.

Register 16H: DS3 FERR Count LSB

Bit	Type	Function	Default
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

Register 17H: DS3 FERR Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FERR[9]	X
Bit 0	R	FERR[8]	X

These registers indicate the number of DS3 framing error (FERR) events that occurred during the previous accumulation interval.

A transfer operation of all counter registers within the selected PMON can be triggered by writing to either FERR Count Register.

Register 18H: DS3 EXZS Count LSB

Bit	Type	Function	Default
Bit 7	R	EXZS[7]	X
Bit 6	R	EXZS[6]	X
Bit 5	R	EXZS[5]	X
Bit 4	R	EXZS[4]	X
Bit 3	R	EXZS[3]	X
Bit 2	R	EXZS[2]	X
Bit 1	R	EXZS[1]	X
Bit 0	R	EXZS[0]	X

Register 19H: DS3 EXZS Count MSB

Bit	Type	Function	Default
Bit 7	R	EXZS[15]	X
Bit 6	R	EXZS[14]	X
Bit 5	R	EXZS[13]	X
Bit 4	R	EXZS[12]	X
Bit 3	R	EXZS[11]	X
Bit 2	R	EXZS[10]	X
Bit 1	R	EXZS[9]	X
Bit 0	R	EXZS[8]	X

These registers indicate the number of summed Excessive Zeros (EXZS) that occurred during the previous accumulation interval. One or more excessive zeros occurrences within an 85 bit block is counted as one summed excessive zero.

A transfer operation of all counter registers within the selected PMON can be triggered by writing to either EXZS Count Register.

Register 1AH: DS3 PERR Count LSB

Bit	Type	Function	Default
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Register 1BH: DS3 PERR Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	PERR[13]	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

These registers indicate the number of P-bit parity error (PERR) events that occurred during the previous accumulation interval.

A transfer operation of all counter registers within the selected PMON can be triggered by writing to either PERR Count Register.

Register 1CH: DS3 CPERR Count LSB

Bit	Type	Function	Default
Bit 7	R	CPERR[7]	X
Bit 6	R	CPERR[6]	X
Bit 5	R	CPERR[5]	X
Bit 4	R	CPERR[4]	X
Bit 3	R	CPERR[3]	X
Bit 2	R	CPERR[2]	X
Bit 1	R	CPERR[1]	X
Bit 0	R	CPERR[0]	X

Register 1DH: DS3 CPERR Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	CPERR[13]	X
Bit 4	R	CPERR[12]	X
Bit 3	R	CPERR[11]	X
Bit 2	R	CPERR[10]	X
Bit 1	R	CPERR[9]	X
Bit 0	R	CPERR[8]	X

These registers indicate the number of C-bit parity error (CPERR) events that occurred during the previous accumulation interval.

A transfer operation of all counter registers within the selected PMON can be triggered by writing to either CPERR Count Register.

Register 1EH: DS3 FEBE Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 1FH: DS3 FEBE Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers indicate the number of far end block error (FEBE) events that occurred during the previous accumulation interval.

A transfer operation of all counter registers within the selected PMON can be triggered by writing to either FEBE Count Register.

Register 20H: XFDL TSB Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	EOM	0
Bit 3	R/W	INTE	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	0
Bit 0	R/W	EN	0

EN:

The enable bit (EN) controls the overall operation of the XFDL TSB. When the EN bit is set to a logic 1, the XDFL TSB is enabled and flag sequences are sent until data is written into the Transmit Data register. When the EN bit is set to logic 0, the XFDL TSB is disabled.

CRC:

The CRC enable bit controls the generation of the CCITT-CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and the appends the 16 bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial = $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 11111110 code to be transmitted after the last byte from the Transmit Data Register is transmitted. Aborts are continuously sent until this bit is reset to a logic 0.

INTE:

The INTE bit enables the generation of an interrupt via the TDLINT output. Setting the INTE bit to logic 1 enables the generation of an interrupt by asserting the TDLINT output; setting INTE to logic 0 disables the generation of an interrupt.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared before transmission of the next data packet begins. The EOM register bit value can also be set to logic 1 by pulsing the TDLEOMI input pin.

Register 21H: XFDL TSB Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	INT	0
Bit 0	R/W	UDR	0

INT:

The INT bit indicates when the XFDL TSB is ready to accept a new data byte for transmission. The INT bit is set to a logic 1 when the previous byte in the Transmit Data register has been loaded into the parallel to serial converter and a new byte can be written into the Transmit Data register. The INT bit is set to a logic 0 while new data is in the Transmit Data register. The INT bit is not disabled by the INTE bit in the configuration register.

UDR:

The UDR bit indicates when the XFDL TSB has underrun the data in the Transmit Data register. The UDR bit is set to a logic 1 if the parallel to serial conversion of the last byte in the Transmit Data register has completed before the new byte was written into the Transmit Data register. Once an underrun has occurred, the XFDL transmits an ABORT, followed by a flag, and waits to transmit the next valid data byte. If the UDR bit is still set after the transmission of the flag the XFDL will continuously transmit the all-ones idle pattern. The UDR bit can only be cleared by writing a logic 0 to the UDR bit position in this register.

Register 22H: XFDL TSB Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD7	X
Bit 6	R/W	TD6	X
Bit 5	R/W	TD5	X
Bit 4	R/W	TD4	X
Bit 3	R/W	TD3	X
Bit 2	R/W	TD2	X
Bit 1	R/W	TD1	X
Bit 0	R/W	TD0	X

Data written to this register is serialized and transmitted on the path maintenance data link least significant bit first. The XFDL TSB signals when the next data byte is required by asserting the TDLINT output (if enabled) and by setting the INT bit in the Status register high. When INT and/or TDLINT is set, the Transmit Data register must be written with the next message byte within 4 data bit periods to prevent the occurrence of an underrun. At a nominal 28.2 kbit/sec link data rate the required write interval is 110µsec.

Register 24H: RFDL TSB Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN:

The enable bit (EN) controls the overall operation of the RFDL TSB. When set, the RDFL TSB is enabled; when reset the RFDL TSB is disabled. When the TSB is disabled, the FIFO and interrupts are all cleared, however, the programming of the Interrupt Control/Status Register is not affected. When the TSB is enabled, it will immediately begin looking for flags.

Setting the terminate reception bit (TR) forces the RFDL TSB to immediately terminate the reception of the current LAPD frame, empty the FIFO, clear the interrupts, and begin searching for a new flag sequence. The RFDL handles the TR input in the same manner as if the EN bit had been cleared and then set. The TR bit in the Configuration register will reset itself after a rising and falling edge have occurred on the CLK input to the RFDL TSB once the write to this register has completed and WEB goes inactive. If the Configuration register is read after this time, the TR bit value returned will be zero.
The RFDL TSB handles the TR input in the same manner as clearing and setting the EN bit, therefore, the RFDL state machine will begin searching for flags and an interrupt will be generated when the first flag is detected.

Register 25H: RFDL TSB Interrupt Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTC1	0
Bit 1	R/W	INTC0	0
Bit 0	R	INT	0

INTC1, INTC0:

The INTC1 and INTC0 bits control when an interrupt is asserted based on the number of received data bytes in the FIFO as follows:

INTC1	INTC0	Description
0	0	Disable interrupts (All sources)
0	1	Enable interrupt when FIFO receives data
1	0	Enable interrupt when FIFO has 2 bytes of data
1	1	Enable interrupt when FIFO has 3 bytes of data

INT:

The INT bit reflects the status of the external RDLINT interrupt unless the INTC1 and INTC0 bits are set to disable interrupts. In that case, the RDLINT output is forced to 0 and the INT bit of the Interrupt Control/Status register will reflect the state of the internal interrupt latch.

FIFO:

In addition to the FIFO fill status, interrupts are also generated for EOM (end of message), OVR (FIFO overrun), detection of the abort sequence while not

receiving all ones and on detection of the first flag while receiving all ones. The interrupt is reset by a Receive Data Register read that empties the FIFO, unless the cause of the interrupt was due to a FIFO overrun. The interrupt due to a FIFO overrun is cleared on a Status register read, by disabling the TSB, or by setting TR high.

The contents of the Interrupt Control/Status register should only be changed when the RFDL TSB is disabled to prevent any erroneous interrupt generation.

Register 26H: RFDL TSB Status

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	FLG	X
Bit 4	R	EOM	X
Bit 3	R	CRC	X
Bit 2	R	NVB2	X
Bit 1	R	NVB1	X
Bit 0	R	NVB0	X

NVB[2:0]

The NVB[2:0] bit positions indicate the number of valid bits in the Receive Data Register byte. It is possible that not all of the bits in the Receive Data Register are valid when the last data byte is read since the data frame can be any number of bits in length and not necessarily an integral number of bytes. The Receive Data Register is filled from the MSB to the LSB bit position, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0]. A NVB[2:0] value of 000 binary indicates that only the MSB in the register is valid. NVB[2:0] is only valid when the EOM bit is a logic 1 and the FLG bit is a logic 1 and the OVR bit is a logic 0.

CRC:

The CRC bit is set if a CRC error was detected in the last received LAPD frame. The CRC bit is only valid when EOM is logic 1 and FLG is a logic 1 and OVR is a logic 0.

On an interrupt generated from the detection of first flag, reading the Status register will return invalid NVB[2:0] and CRC bits, even though the EOM bit is logic 1 and the FLG bit is logic 1.

EOM:

The End of Message bit (EOM) follows the RDLEOM output. It is set when:

1. The last byte in the LAPD frame (EOM) is being read from the Receive Data Register,

2. An abort sequence is detected while not in the receiving all-ones state and the byte, written to the FIFO due to the detection of the abort sequence, is being read from the FIFO,

3. The first flag has been detected and the dummy byte, written into the FIFO when the RFDL changes from the receiving all-ones state to the receiving flags state, is being read from the FIFO,

4. Immediately on detection of FIFO overrun.

The EOM bit is passed through the FIFO with the Data so that the Status will correspond to the Data just read from the FIFO.

FLG:

The flag bit (FLG) is set if the RFDL TSB has detected the presence of the LAPD flag sequence (01111110) in the data. FLG is reset only when the LAPD abort sequence (01111111) is detected in the data or when the RFDL TSB is disabled. This bit is passed through the FIFO with the Data so that the Status will correspond to the Data just read from the FIFO. The reception of bit-oriented codes over the data link will also force an abort due to its eight ones pattern.

OVR:

The Receiver Overrun bit (OVR) is set when data is written over unread data in the FIFO. This bit is not reset until after the Status register is read. While OVR is high, the RFDL and FIFO are held in the reset state, causing the FLG and EOM bits in the status register to be reset also.

FE:

The FIFO Empty bit (FE) is high when the last FIFO entry is read and goes low when the FIFO is loaded with new data.

If the Receive Data register is read while there is no valid data, then a FIFO underrun condition occurs. The underrun condition is reflected in the Status register by forcing all bits to logic zero on the first Status register read immediately following the Received Data register read which caused the underrun condition.

Register 27H: RFDL TSB Receive Data

Bit	Type	Function	Default
Bit 7	R	RD7	X
Bit 6	R	RD6	X
Bit 5	R	RD5	X
Bit 4	R	RD4	X
Bit 3	R	RD3	X
Bit 2	R	RD2	X
Bit 1	R	RD1	X
Bit 0	R	RD0	X

RD0

RD0 corresponds to the first bit of the serial byte received by the RFDL.

This register is actually a 4 level FIFO. If data is available, the FE bit in the Status register is low. If INTC[1:0] (in the Enable/Status register) is set to 01, the Receive Data register must be read within 31 data bit periods to prevent an overrun. If INTC[1:0] is set to 11 the Receiver Data register must be read within 15 data bit periods.

When an overrun is detected, an interrupt is generated and the FIFO is held cleared until the Status register is read. When the LAPD abort sequence (01111111) is detected in the data an ABORT interrupt is generated and the data that has been shifted into the serial to parallel converter is written into the FIFO.

A read of the Receive Data register increments the FIFO pointer at the end of the read. If the Receive Data register read causes an FIFO underrun, then the pointer is inhibited from incrementing. The underrun condition will be signaled in the next Status read by returning all zeros.

Register 28H: MX23 Configuration

Bit	Type	Function	Default
Bit7		Unused	X
Bit6		Unused	X
Bit5		Unused	X
Bit4		Unused	X
Bit3	R/W	LBCODE[1]	0
Bit2	R/W	LBCODE[0]	0
Bit1	R/W	CBE	0
Bit0	R/W	INTE	0

INTE:

When set high, the INTE bit enables the MX23 to activate the interrupt output, INTB, whenever any of the LBRI[7:1] bits are set high in the MX23 Loopback Request Interrupt register. MX23 interrupts are masked when INTE is cleared low.

CBE:

When set high, the CBE bit enables C-bit parity operation. When CBE is low, M23 operation is enabled. While in C-bit parity mode, loopback request detection and loopback request insertion are disabled. The generated DS2 clock, GD2CLK, is nominally 6.3062723 MHz while in C-bit parity mode, received C bits are ignored, and transmitted C bits are set to 1. While in M23 mode, the generated DS2 clock, GD2CLK, is nominally 6.311993 MHz and C bit decoding and encoding is fully operational.

LBCODE[1:0]:

The LBCODE[1:0] bits select the valid state for a loopback request coded in the C-bits of the DS3 signals. Transmit and receive are not independent; the same code is expected in the receive DS3 as is inserted in the transmitted DS3. The following table gives the correspondence between LBCODE[1:0] bits and the valid codes:

LBCODE[1:0]	Loopback Code
00	C1 = C2 and C1 = $\overline{C3}$
01	C1 = C3 and C1 = $\overline{C2}$
10	C2 = C3 and C1 = $\overline{C2}$
11	C1 = C2 and C1 = $\overline{C3}$

If LBCODE[1:0] is 'b00 or 'b11, the loopback code is as per ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7. Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported.

LBCODE[1:0]:

The LBCODE[1:0] bits become logical 0 upon either a hardware or software reset.

Register 29H: MX23 Demux AIS Insert Register

Bit	Type	Function	Default
Bit7		Unused	X
Bit6	R/W	DAIS[7]	0
Bit5	R/W	DAIS[6]	0
Bit4	R/W	DAIS[5]	0
Bit3	R/W	DAIS[4]	0
Bit2	R/W	DAIS[3]	0
Bit1	R/W	DAIS[2]	0
Bit0	R/W	DAIS[1]	0

DAIS[7:1]:

Setting any of the DAIS[7:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding DS2 stream demultiplexed from the DS3 signal input on RDAT. Demux AIS insertion takes place after the point where per DS2 loopback may be invoked using the Loopback Activate register thus allowing demux AIS to be inserted into the through path while a DS2 loopback is activated, if desired.

Register 2AH: MX23 Mux AIS Insert Register

Bit	Type	Function	Default
Bit7		Unused	X
Bit6	R/W	MAIS[7]	0
Bit5	R/W	MAIS[6]	0
Bit4	R/W	MAIS[5]	0
Bit3	R/W	MAIS[4]	0
Bit2	R/W	MAIS[3]	0
Bit1	R/W	MAIS[2]	0
Bit0	R/W	MAIS[1]	0

MAIS[7:1]:

Setting any of the MAIS[7:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding DS2 stream multiplexed into the DS3 signal output on TDAT. Mux AIS insertion takes place before the point where per DS2 loopback may be invoked using the Loopback Activate register and thus mux AIS cannot be inserted while a DS2 loopback is activated.

Register 2BH: MX23 Loopback Activate Register

Bit	Type	Function	Default
Bit7		Unused	X
Bit6	R/W	LBA[7]	0
Bit5	R/W	LBA[6]	0
Bit4	R/W	LBA[5]	0
Bit3	R/W	LBA[4]	0
Bit2	R/W	LBA[3]	0
Bit1	R/W	LBA[2]	0
Bit0	R/W	LBA[1]	0

LBA[7:1]:

Setting any of the LBA[7:1] bits activates loopback of the corresponding DS2 stream from the input DS3 signal to the output DS3 signal.

The demultiplexed DS2 signals continue to present valid payloads while loopbacks are activated. The MX23 Demux AIS Insert Register allows insertion of DS2 AIS if required.

Register 2CH: MX23 Loopback Request Insert Register

Bit	Type	Function	Default
Bit7		Unused	X
Bit6	R/W	ILBR[7]	0
Bit5	R/W	ILBR[6]	0
Bit4	R/W	ILBR[5]	0
Bit3	R/W	ILBR[4]	0
Bit2	R/W	ILBR[3]	0
Bit1	R/W	ILBR[2]	0
Bit0	R/W	ILBR[1]	0

ILBR[7:1]:

Setting any of the ILBR[7:1] bits enables the insertion of a loopback request in the corresponding DS2 stream in the output DS3 signal. The format of the loopback request is determined by the LBCODE[1:0] bits in the MX23 Configuration Register.

Register 2DH: MX23 Loopback Request Detect Register

Bit	Type	Function	Default
Bit7		Unused	X
Bit6	R	LBRD[7]	X
Bit5	R	LBRD[6]	X
Bit4	R	LBRD[5]	X
Bit3	R	LBRD[4]	X
Bit2	R	LBRD[3]	X
Bit1	R	LBRD[2]	X
Bit0	R	LBRD[1]	X

LBRD[7:1]

The LBRD[7:1] bits are set high while a loopback request is detected for the corresponding DS2 stream in the input DS3 signal. The LBRD[7:1] bits are set low otherwise.

The format of the loopback request expected is determined by the LBCODE[1:0] bits in the MX23 Configuration Register. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames.

Register 2EH: MX23 Loopback Request Interrupt Register

Bit	Type	Function	Default
Bit7		Unused	X
Bit6	R	LBRI[7]	X
Bit5	R	LBRI[6]	X
Bit4	R	LBRI[5]	X
Bit3	R	LBRI[4]	X
Bit2	R	LBRI[3]	X
Bit1	R	LBRI[2]	X
Bit0	R	LBRI[1]	X

LBRI[7:1]:

The LBRI[7:1] bits are set high when a loopback request is asserted or deasserted for the corresponding DS2 stream in the input DS3 signal. The LBRI[7:1] bits are set high whenever the corresponding LBRD[7:1] bits change state. If interrupts are enabled using the INTE bit in the Configuration register then the interrupt output, INTB, is activated. The LBRI[7:1] bits are to logic 0 immediately following a read of the register, acknowledging the interrupt and deactivating the INTB output.

Register 31H: FEAC XBOC TSB Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BC[5]	1
Bit 4	R/W	BC[4]	1
Bit 3	R/W	BC[3]	1
Bit 2	R/W	BC[2]	1
Bit 1	R/W	BC[1]	1
Bit 0	R/W	BC[0]	1

This register enables the XBOC TSB to generate a bit oriented code and selects the 6-bit code to be transmitted.

When this register is written with any 6-bit code other than 111111, that code will be transmitted repeatedly in the far-end alarm and control (FEAC) channel with the format 111111110[BC0][BC1][BC2][BC3][BC4][BC5]0. When the register is written with 111111, the XBOC TSB is disabled.

Register 32H: RBOC Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	BOCE	0

This register selects the validation criteria to be used in determining a valid bit-oriented code (BOC) on the far-end alarm and control (FEAC) channel and enables generation of an interrupt at code validation.

BOCE:

The BOCE bit position enables or disables the generation of an interrupt when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation. When the D3MX is reset, BOCE is reset to logic 0; therefore, interrupt generation is disabled.

AVC:

The AVC bit position selects the validation criterion used in determining a valid BOC. A logic 0 selects the 8 out of 10 matching BOC criterion; a logic 1 in the AVC bit position selects the "alternative" validation criterion of 4 out of 5 matching BOCs.

IDLE:

The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

Register 33H: RBOC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	IDLEI	X
Bit 6	R	BOCI	X
Bit 5	R	BOC[5]	X
Bit 4	R	BOC[4]	X
Bit 3	R	BOC[3]	X
Bit 2	R	BOC[2]	X
Bit 1	R	BOC[1]	X
Bit 0	R	BOC[0]	X

BOC[5:0]

The bit positions BOC[5:0] contain the received bit-oriented codes. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. Since the bit-oriented code "111111" is not recognized by the RBOC, the BOC[5:0] bits are set to all ones ("111111") if no valid code has been detected. The BOCI bit position is cleared to logic 0 and the interrupt is deasserted when this register is read.

IDLEI:

The IDLEI bit position indicates whether an interrupt was generated by the detection of the transition from a valid BOC to idle code. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.

Register 34H: DS3 FRMR Configuration

Bit	Type	Function	Default
Bit7	R/W	AISPAT	1
Bit6	R/W	FDET	0
Bit5	R/W	MBDIS	0

Bit	Type	Function	Default
Bit4	R/W	M3O8	0
Bit3	R/W	UNI	0
Bit2	R/W	REFR	0
Bit1	R/W	AISC	0
Bit0	R/W	CBE	0

CBE:

The CBE bit selects whether the C-bit parity application is enabled. When a logic 1 is written to CBE, C-bit parity mode is enabled. When a logic 0 is written, C-bit parity mode is disabled.

AISC:

The AISC bit controls the algorithm used to detect the alarm indication signal (AIS). When a logic 1 is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic 0 is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic 0 is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

REFR:

The REFR bit is used to trigger reframing. If a logic 1 is written to REFR when it was previously logic 0, the FRMR is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low to high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

UNI:

The UNI bit is used to configure the FRMR to accept either unipolar or bipolar data streams. When a logic 1 is written to UNI, the FRMR accepts unipolar data and line code violation indication on its inputs. When a logic 0 is written to UNI, the FRMR accepts bipolar data on its inputs and performs B3ZS decoding and line code violation reporting.

M3O8:

The M3O8 bit configures the out of frame decision criteria. If M3O8 is a logic 1, out of frame is declared if at least 3 of 8 framing bits are in error. If M3O8 is a logic 0, the standard 3 of 16 bits in error criteria is used.

MBDIS:

The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic 1, M-bit errors are disabled from causing an OOF; the loss of frame criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is set to logic 0, errors in either M-bits or F-bits are enabled to cause an OOF. When MBDIS is logic 0, an OOF can occur when one or more M-bit errors occur in 3 out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit. is exceeded.

FDET:

The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic 1, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic 0, the detection time is 13.5 ms.

AISPAT:

The AISPAT bit controls the pattern used to detect the alarm indication signal (AIS). When a logic 1 is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010... is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic 0 is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

Register 35H: DS3 FRMR Interrupt Enable (ACE=0)

Bit	Type	Function	Default
Bit7	R/W	COFAE	0
Bit6	R/W	REDE	0
Bit5	R/W	CBITE	0
Bit4	R/W	FERFE	0
Bit3	R/W	IDLE	0
Bit2	R/W	AISE	0
Bit1	R/W	OOFE	0
Bit0	R/W	LOSE	0

LOSE:

The LOSE bit enables an interrupt to be generated when a change of state of the loss of signal detector occurs. The state of the detector is visible in the LOSV bit position in the DS3 FRMR Status register and on the RLOS pin. When LOSE is set to logic 1, the interrupt output, INTB, is set low when the state of the LOS indication changes.

OOFE:

The OOFE bit enables an interrupt to be generated when a change of state of the DS3 FRMR frame alignment acquisition circuitry occurs. The state of the frame alignment acquisition circuitry is visible in the OOFV bit location in the DS3 FRMR Status register and on the ROOF/RRED pin when the REDO bit in the Master Alarm Enable register is logic 0. When the circuitry has lost frame alignment and is searching for the new alignment, an out of frame is indicated and the OOFV bit and ROOF pin are set to logic 1. When the circuitry has found frame alignment, the OOFV bit and ROOF pin are set to logic 0. When OOFE is set to logic 1, the interrupt output, INTB, is set low when the state of the OOF indication changes.

AISE:

The AISE bit enables an interrupt to be generated when a change of state of the DS3 AIS signal detector occurs. The state of the AIS detector is visible in the AISV bit location in the DS3 FRMR Status register and on the RAIS pin. When AISE is set to logic 1, the interrupt output, INTB, is set low when the state of the AIS detector changes.

IDLE:

The IDLE bit enables an interrupt to be generated when a change of state of the DS3 IDLE signal detector occurs. When IDLE is set to logic 1, the interrupt output, INTB, is set low when the state of the IDLE detector changes.

FERFE:

The FERFE bit enables an interrupt to be generated when a change of state of the FERF indication occurs. The FERF indication is visible in the FERFV bit location of the DS3 FRMR Status register and on the RFERF pin. When FERFE is set to logic 1, the interrupt output, INTB, is set low when the state of the FERF output changes.

CBITE:

The CBITE bit enables an interrupt to be generated when change of state in the C-bit Identification indication internal to the DS3 FRMR occurs. When CBITE is set to logic 1, the interrupt output, INTB, is set low when the state of the C-bit Identification indication changes.

REDE:

The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register and on the ROOF/RRED pin when the REDO bit in the Master Alarm Enable register (register 06Hex) is set to logic 1. When REDE is set to logic 1, the interrupt output, INTB, is set low when the state of the RED indication changes.

COFAE:

The COFAE bit enables an interrupt to be generated when a change of frame alignment (i.e. a COFA event) occurs. When COFAE is set to logic 1, the interrupt output, INTB, is set low when the COFA event occurs.

A FRMR-generated interrupt is cleared when the FRMR Interrupt Status Register is read.

Register 35H: DS3 FRMR Additional Configuration Register (ACE=1)

Bit	Type	Function	Default
Bit7		Unused	X
Bit6		Unused	X
Bit5	R/W	AISONES	0
Bit4	R/W	BPVO	0
Bit3	R/W	EXZSO	0
Bit2	R/W	EXZDET	0
Bit1	R/W	SALGO	0
Bit0	R/W	DALGO	0

DALGO:

The DALGO bit determines the criteria used to decode a valid B3ZS signature. When DALGO is set to logic 1, a valid B3ZS signature is declared and 3 zeros substituted whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen. When the DALGO bit is set to logic 0, a valid B3ZS signature is declared and the 3 zeros are substituted whenever a zero followed by a bipolar violation is observed.

SALGO:

The SALGO bit determines the criteria used to establish a valid B3ZS signature used to map BPVs to line code violation indications. Any BPV that is not part of a valid B3ZS signature is indicated as an LCV. When the SALGO bit is set to logic 1, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation is observed. When SALGO is set to logic 0, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen.

EXZDET:

The EXZDET bit determines the type of zero occurrences to be included in the LCV indication. When EXZDET is set to logic 1, the occurrence of an excessive zero generates a single pulse indication that is used to indicate an LCV. When EXZDET is set to logic 0, every occurrence of 3 consecutive zeros generates a pulse indication that is used to indicate an LCV. For example, if a sequence of 15 consecutive zeros were received, with EXZDET=1 only a single LCV would be indicated for this string of excessive zeros; with

EXZDET=0, five LCVs would be indicated for this string (i.e. one LCV for every 3 consecutive zeros).

EXZSO:

The EXZSO bit enables only summed zero occurrences to be accumulated in the PMON EXZS Count Registers. When EXZSO is set to logic 1, any excessive zeros occurrences over an 85 bit period increments the PMON EXZS counter by one. When EXZSO is set to logic 0, summed LCVs are accumulated in the PMON EXZS Count Registers. A summed LCV is defined as the occurrence of either BPVs not part of a valid B3ZS signature or 3 consecutive zeros (or excessive zeros if EXZDET=1) occurring over an 85 bit period; each summed LCV occurrence increment the PMON EXZS counter by one.

BPVO:

The BPVO bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPVO is set to logic 1, only BPVs not part of a valid B3ZS signature generate an LCV indication and increment the PMON LCV counter. When BPVO is set to logic 0, both BPVs not part of a valid B3ZS signature, and either 3 consecutive zeros or excessive zeros generate an LCV indication and increment the PMON LCV counter.

AISONES:

The AISONES bit controls the pattern used to detect the alarm indication signal (AIS) when both AISPAT and AISC bits in DS3 FRMR Configuration register (34H) are logic 0; if either AISPAT or AISC are logic 1, the AISONES bit is ignored. When a logic 0 is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111...) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored. When a logic 1 is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111...) signal is observed for a period of time before declaring AIS. In this case all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized below:

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010… pattern; overhead bits ignored.
0	1	X	Framed DS3 stream containing C-bits all logic 0; payload bits ignored.
1	1	X	Framed DS3 stream containing repeating 1010… pattern and C-bits all logic 0.
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

Register 36H: DS3 FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	X
Bit 6	R	REDI	X
Bit 5	R	CBITI	X
Bit 4	R	FERFI	X
Bit 3	R	IDLI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0	R	LOSI	X

LOSI:

The LOSI bit indicates that a change of state of the loss of signal detector has occurred. The state of the detector is visible in the LOSV bit position in the DS3 FRMR Status register and on the RLOS pin. When the LOSI bit is a logic 1, a change in the LOS state has occurred. When the LOSI bit is logic 0, no change in the LOS state has occurred.

OOFI:

The OOFI bit indicates that a change of state of the DS3 FRMR frame alignment acquisition circuitry has occurred. The state of the frame alignment acquisition circuitry is visible in the OOFV bit location in the DS3 FRMR Status register and on the ROOF/RRED pin when the REDO bit in the Master Alarm Enable register is logic 0. When the circuitry has lost frame alignment and is searching for the new alignment, an out of frame is indicated and the OOFV bit and ROOF pin are set to logic 1. When the circuitry has found frame alignment, the OOFV bit and ROOF pin are set to logic 0. When the OOFI bit is a logic 1, a change in the OOF state has occurred. When the OOFI bit is logic 0, no change in the OOF state has occurred.

AISI:

The AISI bit indicates that a change of state of the DS3 AIS signal detector has occurred. The state of the AIS detector is visible in the AISV bit location in the DS3 FRMR Status register and on the RAIS pin. When the AISI bit is a logic 1, a change in the AIS detector state has occurred. When the AISI bit is logic 0, no change in the AIS detector state has occurred.

IDLI:

The IDLI bit indicates that a change of state of the DS3 IDLE signal detector has occurred. When the IDLI bit is a logic 1, a change in the IDLE detector state has occurred. When the IDLI bit is logic 0, no change in the IDLE signal detector state has occurred.

FERFI:

The FERFI bit indicates that a change of state of the FERF indication has occurred. The FERF indication is visible in the FERFV bit location of the DS3 FRMR Status register and on the RFERF pin. When the FERFI bit is a logic 1, a change in the FERF state has occurred. When the FERFI bit is logic 0, no change in the FERF state has occurred.

CBITI:

The CBITI bit indicates that a change of state in the C-bit Identification indication internal to the DS3 FRMR has occurred. When the CBITI bit is a logic 1, a change in the internal CBIT state has occurred. When the CBITI bit is logic 0, no change in the CBIT state has occurred.

REDI:

The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register and on the ROOF/RRED pin when the REDO bit in the Master Alarm Enable register (register 06Hex) is set to logic 1. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.

COFAI:

The COFAI bit indicates that a change of frame alignment (i.e. a COFA event) has occurred. When the COFAI bit is a logic 1, the frame alignment acquisition circuitry has detected that the new alignment differs from the previous frame alignment. When the COFAI bit is logic 0, there was no difference from the current frame alignment and the previous frame alignment.

The interrupt status bits are cleared when the FRMR Interrupt Status Register is read.

Register 37H: DS3 FRMR Status

Bit	Type	Function	Default
Bit 7	R/W	ACE	0
Bit 6	R	REDV	X
Bit 5	R	CBITV	X
Bit 4	R	FERFV	X
Bit 3	R	IDLV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0	R	LOSV	X

LOSV:

The LOSV bit indicates the current state of the loss of signal detector. When the LOSV bit is a logic 1, a sequence of 175 consecutive zeros was detected on the dual-rail RPOS and RNEG DS3 inputs. When the LOSV bit is logic 0, a valid DS3 signal with a ones' density greater than 33% for 175 ± 1 bit periods was detected on the dual-rail inputs.

OOFV:

The OOFV bit indicates the current state of the DS3 FRMR frame alignment acquisition circuitry. When the circuitry has lost frame alignment and is searching for the new alignment, an out of frame is indicated and the OOFV bit is set to logic 1. When the circuitry has found frame alignment, the OOFV bit is set to logic 0.

AISV:

The AISV bit indicates the current state of the DS3 AIS signal detector. When the AISV bit is a logic 1, the DS3 AIS pattern has been received for 2.23ms (or for 13.5ms when FDET is logic 0). When the AISV bit is logic 0, the DS3 AIS pattern has not been received for either 2.23ms or 13.5ms.

IDLV:

The IDLV bit indicates the current state of the DS3 IDLE signal detector. When the IDLV bit is a logic 1, the DS3 IDLE pattern has been received for 2.23ms (or for 13.5ms when FDET is logic 0). When the IDLV bit is logic 0, the DS3 IDLE pattern has not been received for either 2.23ms or 13.5ms.

The FERFV bit indicates the current state of the FERF indication. When the FERFV bit is a logic 1, the FRMR detected that the second to last M-frame's X2=X1=0. When the FERFV bit is logic 0, the second to last M-frame's X2=X1=1.

CBITV:

The CBITV bit indicates the current state in the C-bit Identification indication. When the CBITV bit is a logic 1, the first C-bit of M sub-frame 1 has been observed to be logic 1 for 63 consecutive occasions. When the CBITV bit is logic 0, the first C-bit of sub-frame 1 has either not been logic 1 for 63 consecutive occasions or, if CBITV was previously logic 1, the first C-bit of sub-frame 1 has been observed to be logic 0 for 2 or more times within 15 consecutive occasions.

REDV:

The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic 1, the DS3 FRMR frame alignment acquisition circuitry has been out of frame for 2.23ms (or for 13.5ms when FDET is logic 0). When the REDV bit is logic 0, the frame alignment circuitry has found frame (i.e. OOFV=0) for 2.23ms (or 13.5ms if FDET=0).

ACE:

The ACE bit selects the Additional Configuration Register. This register is located at address 35H, and is only accessible when the ACE bit is set to logic 1. When ACE is set to logic 0, the Interrupt Enable register is accessible at address 35H.

Registers 40H, 50H, 60H, 70H, 80H, 90H and A0H: DS2 FRMR Configuration

Bit	Type	Function	Default
Bit7	R/W	G747	0
Bit6		Unused	X
Bit5	R/W	WORD	0
Bit4	R/W	M2O5	0
Bit3	R/W	MBDIS	0
Bit2	R/W	REFR	0
Bit1		Unused	X
Bit0		Unused	X

REFR:

The REFR bit is used to trigger reframing. If a logic 1 is written to REFR when it was previously logic 0, the FRMR is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low-to-high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

MBDIS:

The MBDIS bit disables the declaration of out-of-frame upon excessive M-bit errors. If MBDIS is a logic 0, out-of-frame is declared when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. If MBDIS is a logic 1, the state of the M-bits is ignored once in frame. Regardless of the state of the MBDIS bit, the F-bits are always monitored for invalid framing.

M2O5:

The M2O5 bit selects the error ratio for declaring out-of-frame (OOF) when in DS2 mode only. When a 1 is written to M2O5, the framer declares OOF when 2 F-bit errors out of 5 consecutive F-bits are observed. When a 0 is written, the framer declares OOF when 2 F-bit errors out of 4 consecutive F-bits are observed. (These two ratios are recommended in TR-TSY-000009 Section 4.1.2) When the FRMR is configured for G.747 operation (the G747 bit is set to logic 1), the OOF status is declared when 4 consecutive framing word errors occur (as per CCITT Rec. G747 Section 4), regardless of the M2O5 bit setting.

WORD:

The WORD bit determines the method of accumulating G.747 framing errors. If the WORD bit is a logic 0, each frame alignment signal (FAS) bit error results in a single FERR count. If the WORD bit is a logic 1, one or more bit errors in a FAS word result in a single FERR count.

G747:

The G747 bit configures the FRMR for G.747 operation. If the G747 bit is a logic 1, the FRMR will process a G.747 signal. If the G747 bit is a logic 0, the FRMR will process a DS2 signal as defined in ANSI T1.107 Section 7.

Registers 41H, 51H, 61H, 71H, 81H, 91H and A1H: DS2 FRMR Interrupt Enable

Bit	Type	Function	Default
Bit7	R/W	COFAE	0
Bit6		Unused	X
Bit5	R/W	REDE	0
Bit4	R/W	FERFE	0
Bit3	R/W	RESE	0
Bit2	R/W	AISE	0
Bit1	R/W	OOFE	0
Bit0		Unused	X

OOFE, AISE, FERFE, REDE:

The OOFE, AISE, FERFE and REDE bits are interrupt enables. A change of state on a corresponding DS2 FRMR status causes the interrupt output, INTB, to be asserted low when the corresponding interrupt enable bit is written with a logic 1.

COFAE:

The COFAE bit is an interrupt enable. A change of frame alignment (COFA) event causes the interrupt output to be set high when the COFAE bit is written with a logic 1.

RESE:

The RESE bit is an interrupt enable. A change in the debounced value of the reserved bit in Set II when in G.747 mode causes the interrupt output to be set high when the RESE bit is written with a logic 1. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames. The RESE bit has no effect in DS2 mode.

The interrupt output, INTB, is deasserted when the Interrupt Status Register is read if its assertion was a result an OOF, AIS, FERF, RED, RES, or COFA event.

Registers 42H, 52H, 62H, 72H, 82H, 92H and A2H: DS2 FRMR Interrupt Status

Bit	Type	Function	Default
Bit7	R	COFAI	X
Bit6		Unused	X
Bit5	R	REDI	X
Bit4	R	FERFI	X
Bit3	R	RESI	X
Bit2	R	AISI	X
Bit1	R	OOFI	X
Bit0		Unused	X

OOFI, AISI, FERFI, REDI:

The OOFI, AISI, FERFI and REDI bits are interrupt status indicators. A change of state on the corresponding DS2 FRMR status causes the corresponding interrupt status bit to be set to logic 1.

RESI:

The RESI bit is an interrupt status indicator. A change in the debounced value of the reserved bit in Set II when in G.747 mode causes this bit to be set to logic 1. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames. This bit has no effect in DS2 mode.

COFAI:

The COFAI bit is an interrupt status indicator. As per TR-TSY-000820, the Change of Frame Alignment (COFA) interrupt is only asserted if a frame search results in a frame alignment which is different from the prior frame alignment.

The interrupt status bits are cleared when the DS2 FRMR Interrupt Status Register is read.

Registers 43H, 53H, 63H, 73H, 83H, 93H and A3H: DS2 FRMR Status

Bit	Type	Function	Default
Bit7		Unused	X
Bit6		Unused	X
Bit5	R	REDV	X
Bit4	R	FERFV	X
Bit3	R	RESV	X
Bit2	R	AISV	X
Bit1	R	OOFV	X
Bit0		Unused	X

OOFV, AISV, FERFV, REDV:

The OOFV, AISV, FERFV and REDV bits in this register reflect the status of the corresponding DS2 FRMR value. The OOFV bit is a logic 1 if the DS2 framer is presently out-of-frame. The AISV bit is a logic 1 if AIS has been declared.

In DS2 mode, the FERFV bit reflects the debounced state of the X bit (first bit of the M4-Subframe). If the X-bit has been a zero for two consecutive M-frames, the FERFV bit becomes a logic 1. If the X-bit has been a one for two consecutive M-frames, the FERFV bit becomes a logic 0.

In G.747 mode, FERFV bit reflects the debounced state of the Remote Alarm Indication (RAI, bit 1 of Set II) bit. If the RAI bit has been a one for two consecutive frames, the FERFV bit becomes a logic 1. If the RAI bit has been a zero for two consecutive frames, the FERFV bit becomes a logic 0.

A six frame latency of the FERFV status ensures a virtually 100% probability of freezing correctly in DS2 mode upon an out-of-frame condition and a better than 99.9% probability of freezing correctly in G.747 mode.

REDV:

The REDV bit is a logic 1 if an out-of-frame condition has persisted for 9.9 ms (6.9ms in G.747 mode). This is less than 1.5 times the maximum average reframe time allowed. The REDV status will remain asserted for 9.9 ms (6.9ms in G.747 mode) after frame alignment has been declare and then become logic 0.

RESV:

The RESV bit reflects the debounced state of the reserved bit in Set II when in G.747 mode. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames.

Registers 44H, 54H, 64H, 74H, 84H, 94H and A4H: DS2 FRMR Monitor Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	0
Bit 0	R	OVR	0

INTE:

The interrupt enable (INTE) bit allows the DS2 FRMR to assert the INTB output upon register transfers. A logic 1 in the INTE bit position enables the DS2 FRMR to generate a microprocessor interrupt when the counter values are transferred to the Holding Registers. A logic 0 in the INTE bit position disables the DS2 FRMR from generating an interrupt. When the TSB is reset, the INTE bit is set to logic 0, disabling the interrupt. The interrupt is cleared when this register is read if its assertion was a result a transfer operation.

INTR:

The interrupt (INTR) bit indicates the current status of the internal interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the Holding Registers has occurred; a logic 0 indicates that no transfer has occurred. This bit is set to logic 0 when this register is read. The value of the INTR bit is not affected by the value of the INTE bit.

OVR:

The overrun (OVR) bit indicates the overrun status of the Holding Registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the Holding Registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

To generate a transfer of the counters to the holding registers, a microprocessor write to the Global PMON Update Register is required.

Registers 45H, 55H, 65H, 75H, 85H, 95H and A5H: DS2 FRMR FERR Count

Bit	Type	Function	Default
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

This register indicates the number of DS2 framing bit error events or G.747 framing word errors that occurred during the previous accumulation interval. A DS2 framing bit error event is either an M-bit or and F-bit error. One or more bit errors in a G.747 frame alignment signal results in a single framing word error.

A transfer operation can be triggered by writing to the Global PMON Update Register.

Registers 46H, 56H, 66H, 76H, 86H, 96H and A6H: DS2 FRMR PERR Count (LSB)

Bit	Type	Function	Default
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Registers 47H, 57H, 67H, 77H, 87H, 97H and A7H: DS2 FRMR PERR Count (MSB)

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

These registers indicate the number of G.747 parity error events that occurred during the previous accumulation interval.

A transfer operation can be triggered by writing to the Global PMON Update Register.

Registers 48H, 58H, 68H, 78H, 88H, 98H and A8H: MX12 Configuration and Control

Bit	Type	Function	Default
Bit7	R/W	G747	0
Bit6	R/W	PINV	0
Bit5	R/W	MINV	0
Bit4	R/W	FINV	0
Bit3	R/W	XAIS	0
Bit2	R/W	XFERF	0
Bit1	R/W	XRES	0
Bit0	R/W	INTE	0

INTE:

When set high, the INTE bit enables the activation of the interrupt output, INTB, whenever any of the LBRI[4:1] bits are set high in the Loopback Request Interrupt register. Interrupts are masked when INTE is cleared low.

XRES:

The XRES bit only has effect in G.747 mode. When XRES is set high and AIS is not being transmitted, the reserved bit (Set II, bit 3) is set to 0; otherwise, the transmitted reserved bit is set to 1.

XFERF:

When set high, the XFERF bit enables the transmission of the far end receive failure (FERF) signal in the DS2 output stream when in DS2 mode (i.e. G747 bit low). When XFERF is set high, the transmitted X bit is set to 0, provided that AIS is not being transmitted; otherwise the transmitted X bit is set to 1. When in G.747 mode (i.e. G747 bit high), the remote alarm indication (RAI) is set to 1 when XFERF is set high; otherwise, the transmitted RAI bit is set to 0 unless AIS is being transmitted.

XAIS:

When set high, the XAIS bit enables the transmission of the alarm indication signal (AIS) in the 6312 kbit/s output stream. When XAIS is set high, the transmitted data is set to all ones; otherwise the transmitted data is not affected.

FINV:

When FINV is set high and G747 is low, all the transmitted F bits in the DS2 output stream are logically inverted for diagnostic purposes. If G747 is low when FINV is set high, the nine bit frame alignment signal (111010000) is logically inverted (i.e. 000101111).

MINV:

When MINV is set high, the transmitted M bits in the DS2 output stream are inverted for diagnostic purposes. This only has effect when the G747 bit is low.

PINV:

When PINV is set high, the transmitted parity bit in the G.747 formatted output stream is inverted for diagnostic purposes. This only has effect when the G747 bit is high.

G747:

When G747 is high, the MX12 supports CCITT Recommendation G.747. In this mode, three 2048 kbit/s tributaries are multiplexed into and demultiplex out of a 840 bit frame. If G747 is low, the frame format is compatible with DS2 as specified in the ANSI T1.107 Standard.

Registers 49H, 59H, 69H, 79H, 89H, 99H and A9H: MX12 Loopback Code Select Register

Bit	Type	Function	Default
Bit7		Unused	X
Bit6		Unused	X
Bit5		Unused	X
Bit4		Unused	X
Bit3		Unused	X
Bit2		Unused	X
Bit1	R/W	LBCODE[1]	0
Bit0	R/W	LBCODE[0]	0

LBCODE[1:0]:

The LBCODE[1:0] bits select the valid state for a loopback request coded in the C-bits of the DS2 signals. Transmit and receive are not independent; the same code is expected in the demultiplexed DS2 as is inserted in the DS2 to be multiplexed. The following table gives the correspondence between LBCODE[1:0] bits and the valid codes:

LBCODE[1:0]	Loopback Code
00	C1 = C2 and C1 = $\overline{C3}$
01	C1 = C3 and C1 = $\overline{C2}$
10	C2 = C3 and C1 = $\overline{C2}$
11	C1 = C2 and C1 = $\overline{C3}$

If LBCODE[1:0] is 'b00 or 'b11, the loopback code is as per ANSI T1.107 Section 7.2.1.1 and TR-TSY-000009 Section 3.7. Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported.

The LBCODE[1:0] bits will also select the valid state for a loopback request coded in the C-bits of the G.747 formatted signal. Again, the transmit and

receive are not independent; the same code is expected in the demultiplexed G.747 stream as is inserted in the G.747 stream to be multiplexed. The valid codes are the same as those for the DS2 formatted stream given in the table above.

The LBCODE[1:0] bits become logical 0 upon either a hardware or software reset.

Registers 4AH, 5AH, 6AH, 7AH, 8AH, 9AH and AAH: MX12 AIS Insert Register

Bit	Type	Function	Default
Bit7	R/W	MAIS[4]	0
Bit6	R/W	MAIS[3]	0
Bit5	R/W	MAIS[2]	0
Bit4	R/W	MAIS[1]	0
Bit3	R/W	DAIS[4]	0
Bit2	R/W	DAIS[3]	0
Bit1	R/W	DAIS[2]	0
Bit0	R/W	DAIS[1]	0

DAIS[4:1]:

Setting any of the DAIS[4:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding low speed stream demultiplexed from the 6312 kbit/s high speed input signal. Demux AIS insertion takes place after the point where remote loopback may be invoked using the Loopback Activate register thus allowing demux AIS to be inserted into the through path while a loopback is activated, if desired.

MAIS[4:1]:

Setting any of the MAIS[4:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding low speed stream multiplexed into the 6312 kbit/s high speed output signal. Mux AIS insertion takes place before the point where remote loopback may be invoked using the Loopback Activate register and thus mux AIS cannot be inserted while a loopback is activated.

Registers 4BH, 5BH, 6BH, 7BH, 8BH, 9BH and ABH: MX12 Loopback Activate Register

Bit	Type	Function	Default
Bit7	R/W	ILBR[4]	0
Bit6	R/W	ILBR[3]	0
Bit5	R/W	ILBR[2]	0
Bit4	R/W	ILBR[1]	0
Bit3	R/W	LBA[4]	0
Bit2	R/W	LBA[3]	0
Bit1	R/W	LBA[2]	0
Bit0	R/W	LBA[1]	0

LBA[4:1]:

Setting any of the LBA[4:1] bits activates loopback of the corresponding low speed stream from the high speed input signal to the high speed output signal. LBA[4] has no effect in G.747 mode, but LBA[3:1] activates the loopback of the corresponding 2048 kbit/s signal.

The demultiplexed DS1 signals continue to present valid payloads while loopbacks are activated. The MX12 AIS Insert Register allows insertion of DS1 AIS if required.

ILBR[4:1]

In DS2 mode, setting any of the ILBR[4:1] bits enables the insertion of a loopback request in the corresponding DS1 stream in the DS2 output signal. The format of the loopback request is determined by the LBCODE[1:0] bits in the Loopback Code Select MX12 Register. In G.747 mode, ILBR[j] inverts bit C_{j1}, C_{j2} or C_{j3} in the G.747 frame in an analogous fashion.

Registers 4CH, 5CH, 6CH, 7CH, 8CH, 9CH and ACH: MX12 Loopback Interrupt Register

Bit	Type	Function	Default
Bit7	R	LBRI[4]	X
Bit6	R	LBRI[3]	X
Bit5	R	LBRI[2]	X
Bit4	R	LBRI[1]	X
Bit3	R	LBRD[4]	X
Bit2	R	LBRD[3]	X
Bit1	R	LBRD[2]	X
Bit0	R	LBRD[1]	X

LBRD[4:1]:

The LBRD[4:1] bits are set high while a loopback request is detected for the corresponding low speed stream in the high speed input signal. The LBRD[4:1] bits are set low otherwise.

The format of the loopback request expected is determined by the LBCODE[1:0] bits in the MX12 Loopback Code Select Register. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames.

LBRI[4:1]:

The LBRI[4:1] bits are set high when a loopback request is asserted or deasserted for the corresponding low speed stream in the high speed input signal. The LBRI[4:1] bits are set high whenever the corresponding LBRD[4:1] bits change state. If interrupts are enabled using the INTE bit in the Configuration register then the interrupt output, INTB, is activated. The LBRI[4:1] bits are cleared low immediately following a read of the register, acknowledging the interrupt and deactivating the INTB output.

11 TEST FEATURES DESCRIPTION

The D3MX contains test features for both production testing and board testing.

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the D3MX. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[8]) is high.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the D3MX are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

11.1 Test Mode Register Memory Map

Address	Register
100H-10CH	Reserved
10CH	TRAN Test Register 0
10DH	TRAN Test Register 1
10EH	TRAN Test Register 2
10FH	Reserved
110H	PMON Test Register 0
111H	PMON Test Register 1
112H	PMON Test Register 2
113H - 11FH	Reserved
120H	XFDL Test Register 0
121H	XFDL Test Register 1
122H - 123H	Reserved
124H	RFDL Test Register 0
125H	RFDL Test Register 1
126H-127H	Reserved

Address	Register
128H	MX23 Test Register 0
129H	MX23 Test Register 1
12AH	MX23 Test Register 2
12BH	MX23 Test Register 3
12CH - 12FH	Reserved
130H	XBOC Test Register 0
131H	XBOC Test Register 1
132H	RBOC Test Register 0
133H	RBOC Test Register 1
134H	DS3 FRMR Test Register 0
135H	DS3 FRMR Test Register 1
136H	DS3 FRMR Test Register 2
137H	DS3 FRMR Test Register 3
138H - 13FH	Reserved
140H	DS2 #1 FRMR Test Register 0
141H	DS2 #1 FRMR Test Register 1
142H	DS2 #1 FRMR Test Register 2
143H - 147H	Reserved
148H	DS2 #1 MX12 Test Register 0
149H	DS2 #1 MX12 Test Register 1
14AH	DS2 #1 MX12 Test Register 2
14BH - 14FH	Reserved
150H	DS2 #2 FRMR Test Register 0
151H	DS2 #2 FRMR Test Register 1
152H	DS2 #2 FRMR Test Register 2
153H - 157H	Reserved
158H	DS2 #2 MX12 Test Register 0
159H	DS2 #2 MX12 Test Register 1

Address	Register
15AH	DS2 #2 MX12 Test Register 2
15BH - 15FH	Reserved
160H	DS2 #3 FRMR Test Register 0
161H	DS2 #3 FRMR Test Register 1
162H	DS2 #3 FRMR Test Register 2
163H - 167H	Reserved
168H	DS2 #3 MX12 Test Register 0
169H	DS2 #3 MX12 Test Register 1
16AH	DS2 #3 MX12 Test Register 2
16BH - 16FH	Reserved
170H	DS2 #4 FRMR Test Register 0
171H	DS2 #4 FRMR Test Register 1
172H	DS2 #4 FRMR Test Register 2
173H - 177H	Reserved
178H	DS2 #4 MX12 Test Register 0
179H	DS2 #4 MX12 Test Register 1
17AH	DS2 #4 MX12 Test Register 2
17BH - 17FH	Reserved
180H	DS2 #5 FRMR Test Register 0
181H	DS2 #5 FRMR Test Register 1
182H	DS2 #5 FRMR Test Register 2
183H - 187H	Reserved
188H	DS2 #5 MX12 Test Register 0
189H	DS2 #5 MX12 Test Register 1
18AH	DS2 #5 MX12 Test Register 2
18BH - 18FH	Reserved
190H	DS2 #6 FRMR Test Register 0
191H	DS2 #6 FRMR Test Register 1

Address	Register
192H	DS2 #6 FRMR Test Register 2
193H - 197H	Reserved
198H	DS2 #6 MX12 Test Register 0
199H	DS2 #6 MX12 Test Register 1
19AH	DS2 #6 MX12 Test Register 2
19BH - 19FH	Reserved
1A0H	DS2 #7 FRMR Test Register 0
1A1H	DS2 #7 FRMR Test Register 1
1A2H	DS2 #7 FRMR Test Register 2
1A3H - 1A7H	Reserved
1A8H	DS2 #7 MX12 Test Register 0
1A9H	DS2 #7 MX12 Test Register 1
1AAH	DS2 #7 MX12 Test Register 2
1ABH - 1FFH	Reserved
00-FFH	Normal Mode Registers
07H	Master Test Register

Notes on Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2. Writeable register bits are not initialized upon reset unless otherwise noted.

Address 07H: Master Test

Bit	Type	Function	Default
Bit 7	R/W	VCLK_IOTST	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	X
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	X

The Master Test Register is provided at D3MX read/write address 07H.

This register is used to select D3MX test features. All bits, except for PMCTST, are reset to zero by a hardware reset of the D3MX; a software reset of the D3MX does not affect the state of the bits in this register.

VCLK_IOTST:

The VCLK_IOTST bit replaces the RCLK/VCLK input as the test clock when the IOTST bit is a logic 1. Some sense points require a rising edge on the test clock to clock in the value on the pin. This bit satisfies the requirement without needing the RCLK/VCLK input to toggle.

PMCTST:

The PMCTST bit is used to configure the D3MX for PMC's manufacturing tests. When PMCTST is set to logic 1, the D3MX microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the D3MX to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The

DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the D3MX for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the D3MX . While the HIZIO bit is a logic 1, all output pins of the D3MX except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

11.2 Test Mode 0

In test mode 0, the D3MX allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the IOTST bit in the Test Mode Select Register is set to logic 1 and the following addresses must be written with 00H: 10DH, 111H, 121H, 125H, 129H, 131H, 133H, 135H, 141H, 149H, 151H, 159H, 161H, 169H, 171H, 179H, 181H, 189H, 191H, 199H, 1A1H and 1A9H.

Reading the following address locations returns the values for the indicated inputs :

Table 1 - Test Mode Address Locations – Read from Inputs

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10EH	TDLSIG/ TDLUDR[3]						TOH	TOHEN
120H						TDLEOMI		
128H			TIMFP[4]	TICLK				
134H						RNEG/ RLCV[1,4]	RPOS/ RDAT[1,4]	RCLK[2]
14AH	TD1DAT4	TD1DAT3	TD1DAT2	TD1DAT1	TD1CLK4	TD1CLK3	TD1CLK2	TD1CLK1
15AH	TD1DAT8	TD1DAT7	TD1DAT6	TD1DAT5	TD1CLK8	TD1CLK7	TD1CLK6	TD1CLK5
16AH	TD1DAT12	TD1DAT11	TD1DAT10	TD1DAT9	TD1CLK12	TD1CLK11	TD1CLK10	TD1CLK9
17AH	TD1DAT16	TD1DAT15	TD1DAT14	TD1DAT13	TD1CLK16	TD1CLK15	TD1CLK14	TD1CLK13
18AH	TD1DAT20	TD1DAT19	TD1DAT18	TD1DAT17	TD1CLK20	TD1CLK19	TD1CLK18	TD1CLK17
19AH	TD1DAT24	TD1DAT23	TD1DAT22	TD1DAT21	TD1CLK24	TD1CLK23	TD1CLK22	TD1CLK21
1AAH	TD1DAT28	TD1DAT27	TD1DAT26	TD1DAT25	TD1CLK28	TD1CLK27	TD1CLK26	TD1CLK25

Notes:

1. If the RINV and the DS3 FRMR UNI register bits are logic one, the values read are active low.
2. If the RFALL register bit is a logic 1, the value read is inverted.
3. The TEXHDLC register bit must be a logic 1 to sense this input.
4. These inputs must be clocked by the VCLK_IOTST bit before being read. This requires writing a logic 0 then a logic 1 to the VCLK_IOTST bit .

Writing the following address locations forces the outputs to the value in the corresponding bit position:

Table 2 - Test Mode Address Locations – Write to Outputs

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10CH				TNEG/ TMFP[1,3]	TPOS/ TDAT[2,3]	TNEG/ TMFP[2,3]	TPOS TDAT[1,3]/	TCLK[4]
10EH					TDLCLK/ TDLINT[5]		TOHFP	TOHCLK
110H								INTB[7]

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
120H						TDLSIG/ TDLUDR[6]	TDLCLK/ TDLINT[6]	
124H							RDLSIG/ RDLEOM[9]	RDLCLK/ RDLINT[9]
128H				GD2CLK				INTB[7]
134H	INTB[7]		RLOS	ROHP	RMSFP	RMFP	RODAT	ROCLK
136H			ROHDAT					ROHCLK
137H	ROOF	REXZ		ROHFP			RDLCLK/ RDLINT[8]	RDLSIG/ RDLEOM[8]
140H	INTB[7]							
148H								INTB[7]
14AH	RD1DAT4	RD1DAT3	RD1DAT2	RD1DAT1	RD1CLK4	RD1CLK3	RD1CLK2	RD1CLK1
150H	INTB[7]							
158H								INTB[7]
15AH	RD1DAT8	RD1DAT7	RD1DAT6	RD1DAT5	RD1CLK8	RD1CLK7	RD1CLK6	RD1CLK5
160H	INTB[7]							
168H								INTB[7]
16AH	RD1DAT12	RD1DAT11	RD1DAT10	RD1DAT9	RD1CLK12	RD1CLK11	RD1CLK10	RD1CLK9
170H	INTB[7]							
178H								INTB[7]
17AH	RD1DAT16	RD1DAT15	RD1DAT14	RD1DAT13	RD1CLK16	RD1CLK15	RD1CLK14	RD1CLK13
180H	INTB[7]							
188H								INTB[7]
18AH	RD1DAT20	RD1DAT19	RD1DAT18	RD1DAT17	RD1CLK20	RD1CLK19	RD1CLK18	RD1CLK17
190H	INTB[7]							
198H								INTB[7]
19AH	RD1DAT24	RD1DAT23	RD1DAT22	RD1DAT21	RD1CLK24	RD1CLK23	RD1CLK22	RD1CLK21
1A0H	INTB[7]							
1A8H								INTB[7]
1AAH	RD1DAT28	RD1DAT27	RD1DAT26	RD1DAT25	RD1CLK28	RD1CLK27	RD1CLK26	RD1CLK25

Notes:

1. This bit only has effect if the TUNI register bit is logic one.

2. This bit only has effect if the TUNI register bit is logic zero.

3. These bits are only presented on the output after being clocked by the TCLK output. This requires writing a logic 0 then a logic 1 to the TCLK bit .

4. The TCLK output is inverted if the TRISE bit is a logic 0.

5. This bit only has effect if the TEXHDLC register bit is logic 1.

6. This bit only has effect if the TEXHDLC register bit is logic 0. The polarity of the signal forced on the output pin is determined by the state of the TINTPOL and TUDRPOL register bits.

7. Writing a logic 1 to any INTB bit asserts the INTB output low.

8. This bit only has effect if the REXHDLC register bit is logic 1.

9. This bit only has effect if the REXHDLC register bit is logic 0. The polarity of the signal forced on the output pin is determined by the state of the RINTPOL and REOMPOL register bits.

The state of the configuration registers must be considered. To make board testing more straight forward, it is recommended that the normal mode registers be initialized to the following state:

Write register 02H with 00H	(Clears BYP[7:1])
Write register 03H with C0H	(Sets REXHDLC and TEXHDLC)
or with 0FH	(Sets REOMPOL,TUDRPOL,RINTPOL, TINTPOL).
Write register 04H with 00H	(Clears LINEAIS[1:0], LLBE and DLBE.)
Write register 05H with 08H	(Sets TRISE. Clears TINV, TUNI, RINV, RFALL.)
Write register 07H with 04H	(Sets IOTST to put device into test mode.)
Write register 34H with 00H	(Clears DS3 FRMR UNI bit.)

If the registers are in a different state than this, adjustments must be made for inversion of assertion levels.

12 OPERATION

12.1 Using the Internal Data Link Transmitter

Upon reset of the D3MX, the XFDL should be disabled by setting the EN bit in the Configuration/Control Register to logic 0. If data is not ready to be transmitted, the TDLINT output should also be masked by setting the INTE bit to logic 0.

When a frame (or frames) of data are ready to be transmitted, the Configuration/ Control Register should be initialized for transmission: if the FCS is desired, the CRC bit should be set to logic 1; if the block is to be used in interrupt driven mode, interrupts should be enabled by setting the INTE bit to logic 1. Finally, the XFDL can be enabled by setting the EN bit to logic 1.

The XFDL can be used in a polled, interrupt driven, or DMA-controlled mode for the transfer of frame data. In the polled mode, the TDLINT and TDLUDR outputs of the XFDL are not used, and the processor controlling the XFDL must periodically read the Status Register to determine when to write to the Transmit Data Register. In the interrupt driven mode, the processor controlling the XFDL uses the TDLINT output to determine when to write to the Transmit Data Register. In the DMA controlled mode, the TDLINT output of the XFDL is used as a DMA request input to the DMA controller, and the TDLUDR output is used as an interrupt to the processor to allow handling of exceptions.

If the XFDL data transfer is operating in the polled mode, then a timer periodically starts up a service routine, which should process data as follows:

1. Read the XFDL Status Register and check the UDR and INTR bits.

2. If UDR=1, then clear the Status Register, set the UDR bit in the XFDL Configuration Register to logic 0, and restart the current frame.

3. If INTR=1, then:

   a) If there is still data to send, then write the next data byte to the Transmit Data Register;

   b) f all bytes in the frame have been sent, then set the EOM bit in the XFDL Configuration Register to logic 1, and set the INTE bit to logic 0. Alternatively, assert the TDLEOMI input.

4. Read the Status Register and check the UDR bit.

5. If UDR=1, then clear the Status Register, clear the UDR bit (deassert the TDLEOMI input and clear EOM, if set) in the XFDL Configuration Register to logic 0. Restart the current frame.

In the case of interrupt driven data transfer, the TDLINT output of the XFDL is connected to the interrupt input of the processor, and the interrupt service routine should process the data exactly as described above for the polled mode.

The XFDL can also be used with a DMA controller to process the frame data. In this case, the TDLUDR output is connected to the processor interrupt input. The TDLINT output of the XFDL is connected to the DMA request input of the DMA controller. The DMA "end" signal from the controller can be connected to the TDLEOMI input. The DMA controller writes a data byte to the XFDL whenever the TDLINT output is asserted. Upon writing the last byte of the packet to XFDL, the DMA asserts the TDLEOMI input. Note that the TDLEOMI input is expected to be "glitch-free" and, when pulsed high, sets the EOM register bit in the transmitter configuration register. The EOM register bit is used by the transmitter to determine the course of action when the current data byte is exhausted. If there is a problem during transmission and an underrun condition occurs, then the TDLUDR output goes high and the processor is interrupted. The processor can then halt the DMA controller, clear the problem condition, reset the frame data pointers, and restart the DMA controller to resend the data frame.

12.2 Using the Internal Data Link Receiver

On power up of the D3MX, the RFDL should be disabled by setting the EN bit in the Configuration Register to logic 0. The Interrupt Control/Status Register should then be initialized to select the FIFO buffer fill level at which an interrupt will be generated.

After the Interrupt Control/Status Register has been written to, the RFDL can be enabled at any time by setting the EN bit in the Configuration Register to logic 1. When the RFDL is enabled, it will assume that the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated (if enabled), and the byte received before the first flag was detected will be written into the FIFO buffer. Because the FLG and EOMR bits are passed through the buffer, this dummy write allows the Status Register to accurately reflect the current state of the data link. A Status Register read after a Data Register read of the dummy byte will return EOMR as logic 1 and FLG as logic 1. The first interrupt and data byte read after the RFDL is enabled (or TR bit set to logic 1) is an indication of the link status, and the data byte should therefore be discarded. It is up to the controlling processor to keep track of the

link state as idle (all ones or bit-oriented messages active) or active (flags received).

The RFDL can be used in a polled, interrupt driven, or DMA controlled mode for the transfer of frame data. In the polled mode, the RDLINT and RDLEOM outputs of the RFDL are not used, and the processor controlling the RFDL must periodically read the Status Register to determine when to read the Data Register. In the interrupt driven mode, the processor controlling the RFDL uses the RDLINT output to determine when to read the Data Register. In the DMA controlled mode, the RDLINT output of the RFDL is used as a DMA request input to the DMA controller, and the RDLEOM output is used as an interrupt to the processor to allow handling of exceptions and as an indication of when to process a frame.

In the case of interrupt driven data transfer from the RFDL to the processor, the RDLINT output of the RFDL is connected to the interrupt input of the processor. The processor interrupt service routine should process the data in the following order:

1. Read the RFDL Data Register.

2. Read the RFDL Status Register to check for, in order, underrun, OVR, FLG, EOMR, and FE.

3. If the FIFO has underrun (i.e. the Status Register returns 00 Hex), then discard the last data byte and wait for the next interrupt.

4. If OVR=1, then discard the last frame and wait for the next interrupt.

5. If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the last frame, and wait for the next interrupt.

6. If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and wait for the next interrupt.

7. Otherwise, save the last data byte read.

8. If EOMR=1, then check the CRC, NVB and process the frame.

9. If FE=0, then go to step 1, else wait for the next interrupt.

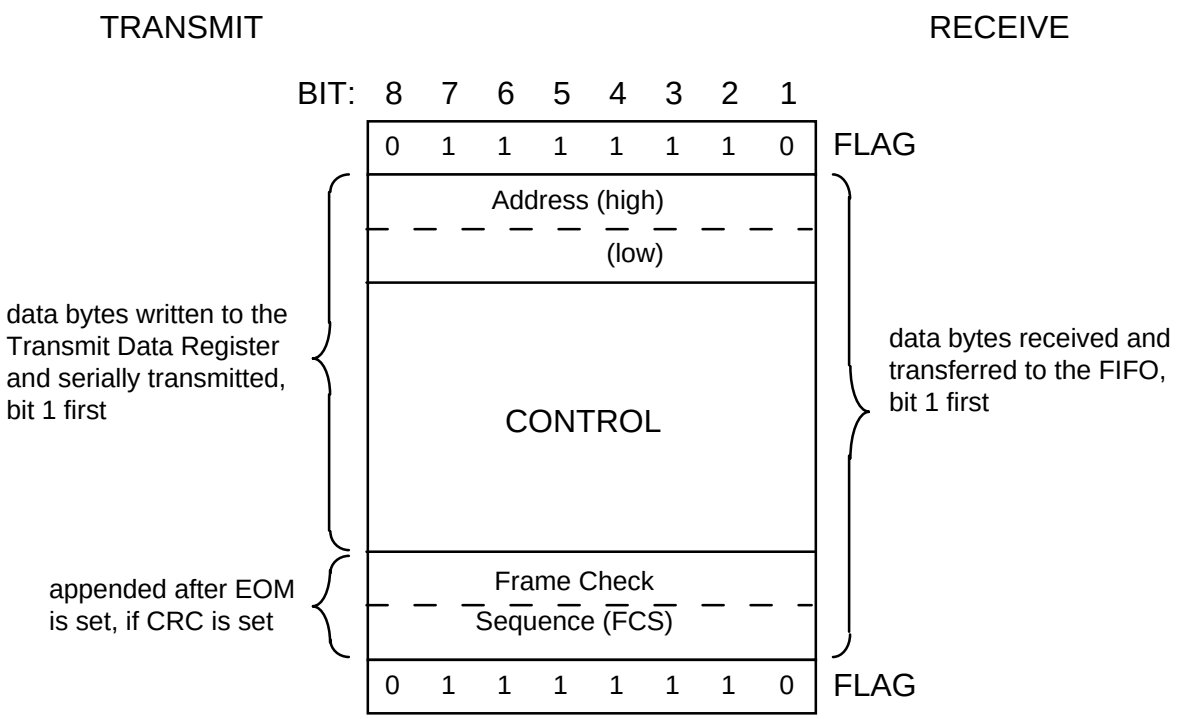
The interrupt service routine can optionally read the Status Register first to check for an overrun condition, and then for available data, before advancing to step one above.

The link state is typically a local software variable. The link state is inactive if the RFDL is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RFDL is receiving flags or data.

If the RFDL data transfer is operating in the polled mode, then processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt. In the polled mode, the option of reading the Status Register first should be used to avoid unnecessary reads of the Data Register.

The RFDL can also be used with a DMA controller to process the frame data. In this case, the RDLEOM output is connected to the processor interrupt input. The RDLINT output of the RFDL is connected through a gate to the DMA request input of the DMA controller. The gate optionally inhibits the DMA request if the RDLEOM output is high. The DMA controller reads the data bytes from the RFDL whenever the RDLINT output is asserted. When the current byte read from the Data Register is the last byte in a frame (due to an end-of-message or an abort), or an overrun condition occurs, then the RDLEOM output goes high. The DMA controller is inhibited from reading any more bytes, and the processor is interrupted. The processor can then halt the DMA controller, read the Status Register, process the frame, and finally reset the DMA controller to process the data for the next frame.

Figure 6 - Typical Data Frame



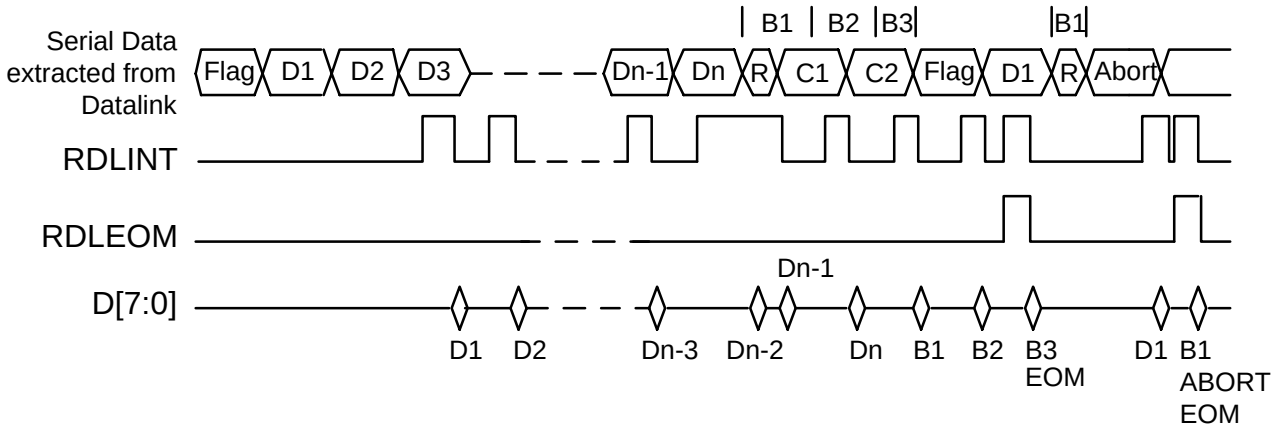
Bit 1 is the first serial bit to be transmitted or received.

Both the address and control bytes must be supplied by an external processor and are shown for reference purposes only.

12.2.1 Key used on subsequent diagrams:

Flag	- flag sequence (01111110)
Abort	- abort sequence (01111111)
D1 - Dn	- n frame data bytes
R	- remainder bits (less than 8)
C1, C2	- CRC-CCITT information
B1, B2, B3	- groupings of 8 bits

Figure 7 - RFDL Normal Data and Abort Sequence



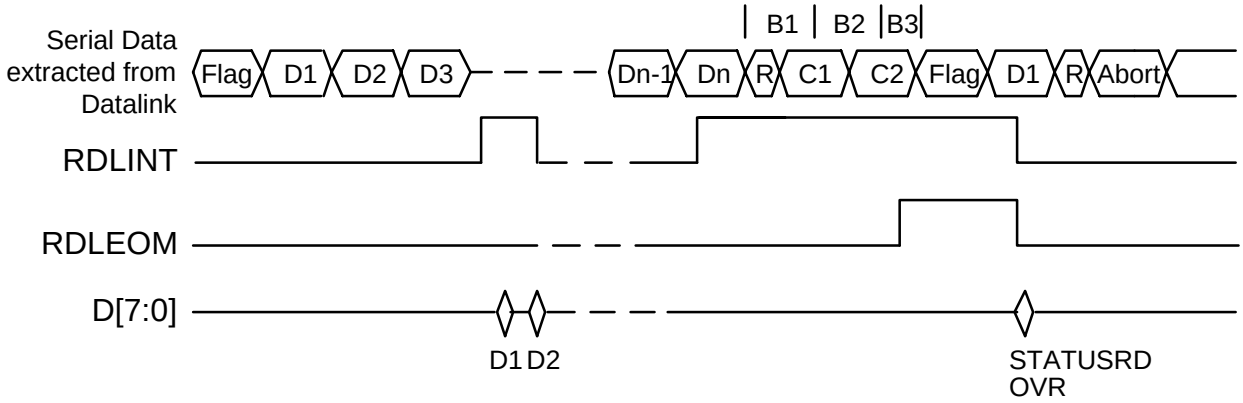
This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when one byte is present in the FIFO buffer. The RFDL is assumed to be operating in the interrupt driven mode. Each read shown is composed of two register reads: first a read of the Data Register, followed by a read of the Status Register. A read of the Data Register deasserts the RDLINT output if no more data exists in the FIFO buffer. The status of the FE bit returned in the Status Register read will indicate the FIFO buffer fill status as well. The Data Register read Dn-2 is shown to occur after two bytes have been written into the buffer. The RDLINT output is not deasserted after the first Data Register read because a data byte still remains to be read. The RDLINT output is deasserted after Data Register read Dn-1. The FE bit will be logic 0 in Status Register read Dn-2 and logic 1 in Status Register read Dn-1.

The RDLEOM output goes high as soon as the last byte in the frame is read from the Data Register. The RDLINT output will be deasserted if the FIFO buffer is empty. The next Status Register read will return a value of logic 1 for the EOMR and FLG bits, and cause the RDLEOM output of the RFDL to return low.

In the next frame, the first data byte is received, and after a delay of ten bit periods, it is written to the FIFO buffer, and read by the processor after the interrupt. When the abort sequence is detected, the data received up to the abort is written to the FIFO buffer and an interrupt generated. The processor then reads the partial byte from the Data Register and the RDLEOM output is set high. The processor then reads the Status Register which will return a value of logic 1 for the EOMR and FLG bits, and set the RDLEOM output low. The FIFO buffer is not cleared when an abort is detected. All bytes received up to the abort are available to be read.

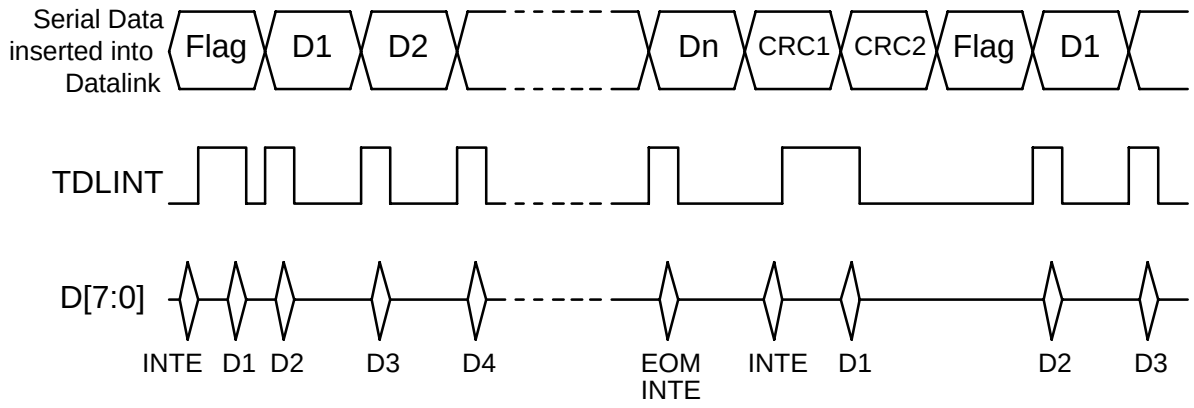
After an abort, the RFDL state machine will be in the receiving all ones state, and the data link status will be idle. When the first flag is detected, a new interrupt will be generated, with a dummy data byte loaded into the FIFO buffer, to indicate that the data link is now active.

Figure 8 - RFDL FIFO Overrun



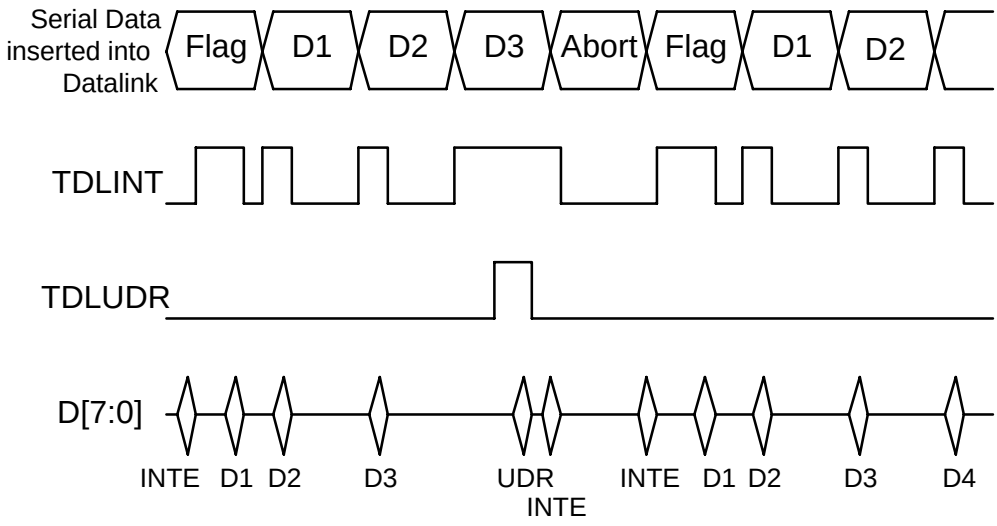
This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when two data bytes are present in the FIFO buffer. Each read is composed of two register reads, as described above. In this example, data is not read by the end of B2. An overrun occurs since unread data (Dn-3) has been overwritten by B1. This sets the RDLEOM output high, and resets both the RFDL and the FIFO buffer. The RFDL is held disabled until the Status Register is read. The start flag sequence is not detected since the RFDL is still held disabled when it occurs. Consequently, the RFDL will ignore the entire frame including the abort sequence (since it has not occurred in a valid frame or during flag reception, according to the RFDL).

Figure 9 - XFDL Normal Data Sequence



This diagram shows the relationship between XFDL inputs and outputs for the case where interrupts and CRC are enabled for regular data transmission. The process is started by setting the INTE bit in the Configuration/Control Register to logic 1, thus enabling the TDLINT signal. When TDLINT is asserted, the interrupt service routine is started, which writes the first byte (D1) of the data frame to the Transmit Data Register. When this byte begins to be shifted out on the data link, TDLINT is asserted. This restarts the interrupt service routine, and the next data byte (D2) is written to the Transmit Data Register. When D2 begins to be shifted out on the data link, TDLINT is asserted again. This cycle continues until the last data byte (Dn) of the frame is written to the Transmit Data Register. When Dn begins to be shifted out on the data link, TDLINT again is asserted. Since all the data has been sent, the interrupt service routine sets the EOM bit in the Configuration/Control Register to logic 1 (or alternatively asserts the TDLEOMI input). The TDLINT interrupt should also be disabled at this time by setting the INTE bit to logic 0. The XFDL will then shift out the two-byte CRC word and closing flag, which ends the frame. Whenever new data is ready, the TDLINT signal can be re-enabled by setting the INTE bit in the Configuration/Control Register to logic 1, and the cycle starts again.

Figure 10 - XFDL Underrun Sequence



This diagram shows the relationship between XFDL inputs and outputs in the case of an underrun error. An underrun error occurs if the XFDL finishes transmitting the current message byte before the processor writes the next byte into the Transmit Data Register; that is, the processor fails to write data to the XFDL in time. In this example, data is not written to the XFDL within five rising clock edges after TDLINT is asserted at the beginning of the transmission of byte D3. The TDLUDR interrupt becomes active at this point, and an abort, followed by a flag, is sent out on the data link. Meanwhile, the processor must clear the TDLUDR interrupt by setting the UDR bit in the Status Register to logic 0. The TDLINT interrupt should also be disabled at this time by setting the INTE bit in the Configuration/Control Register to logic 0. The data frame can then be restarted as usual, by setting the INTE bit logic to 1. Transmission of the frame then proceeds normally.

13 FUNCTIONAL TIMING

Figure 11 - Receive DS3 High Speed Output Timing

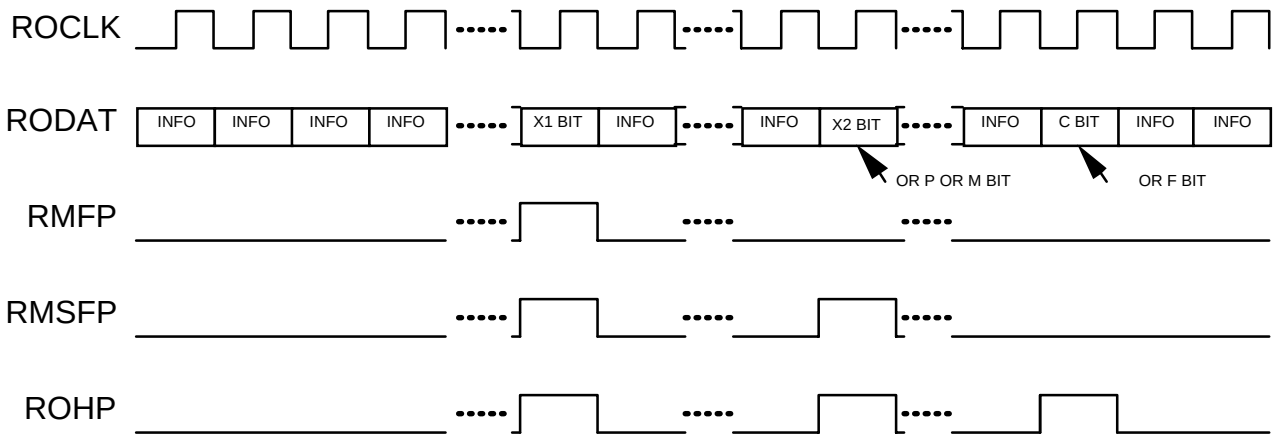


Figure 12 - Receive DS3 Low Speed Timing

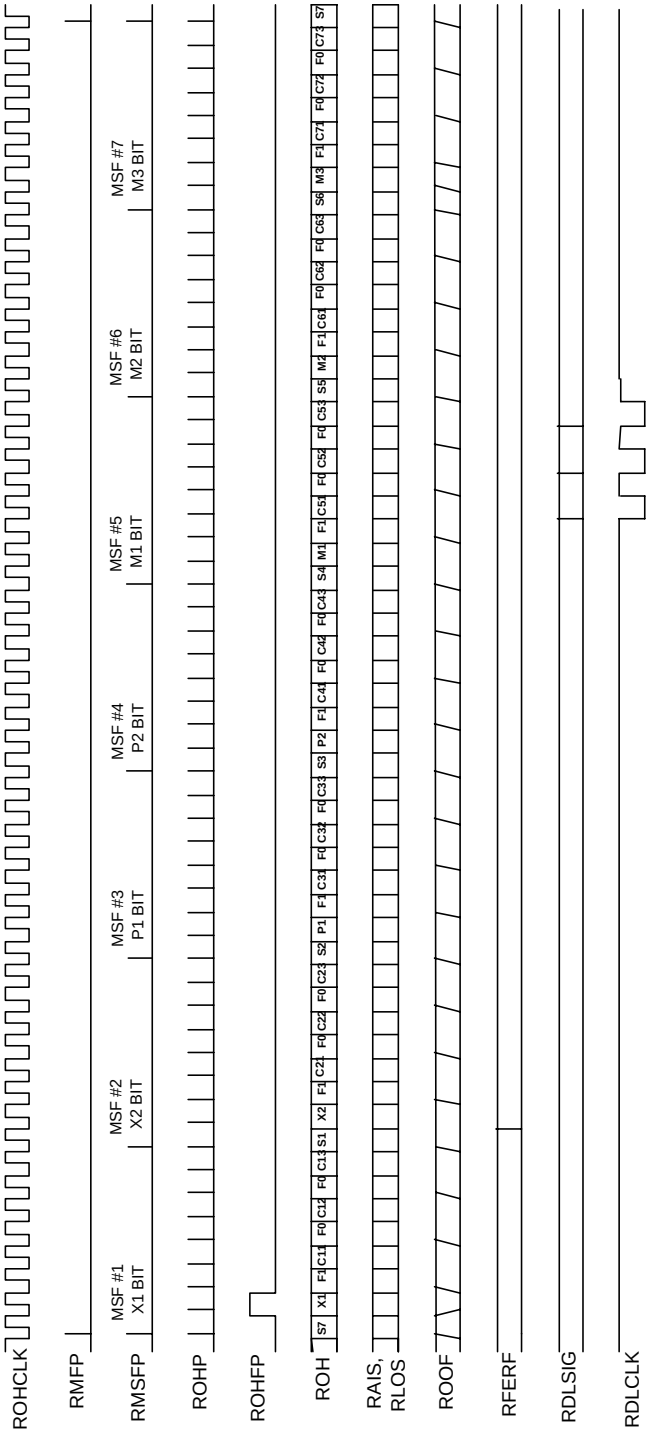


Figure 13 - Transmit DS3 Timing

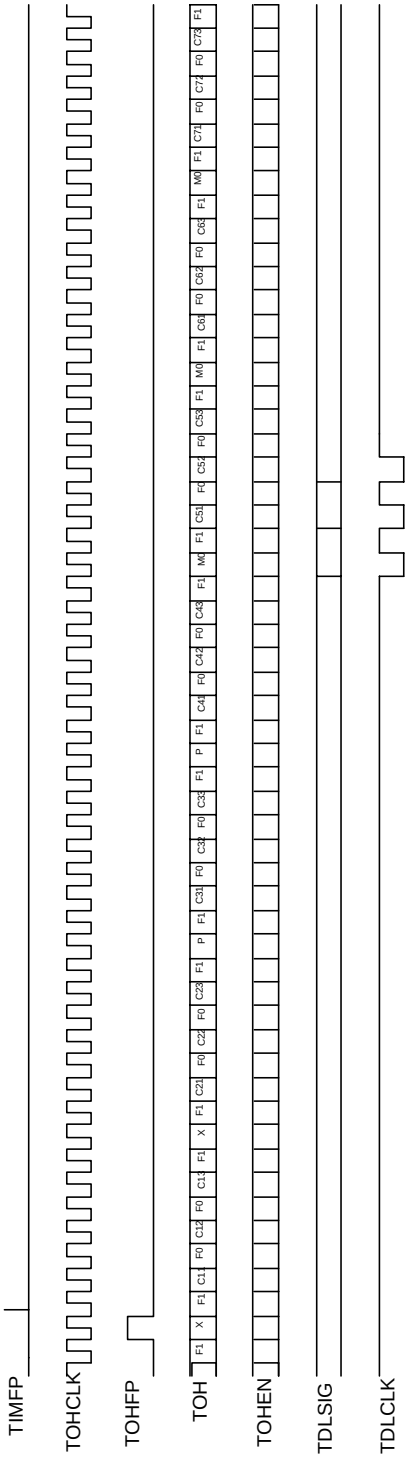
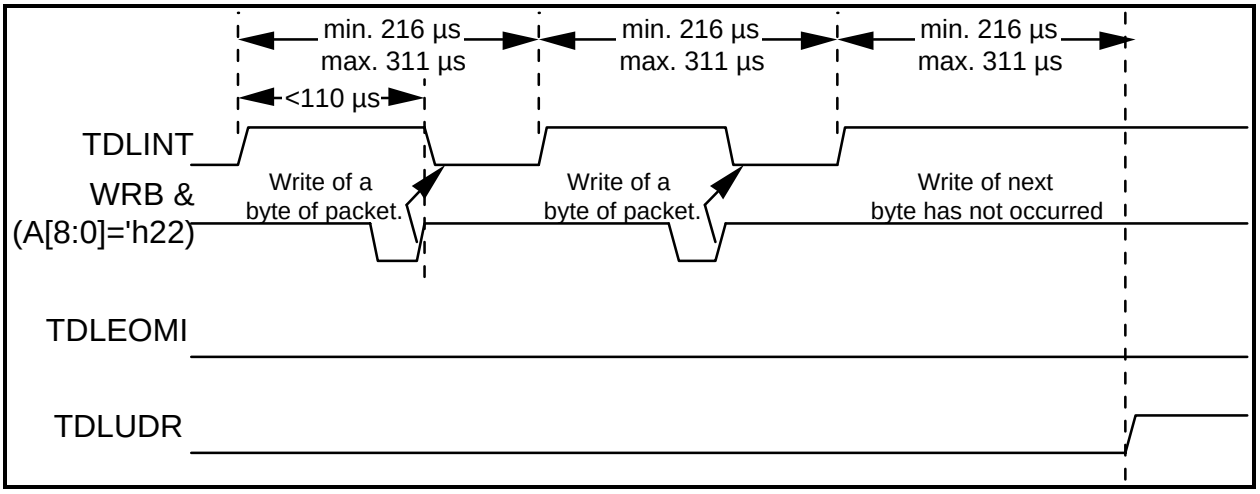
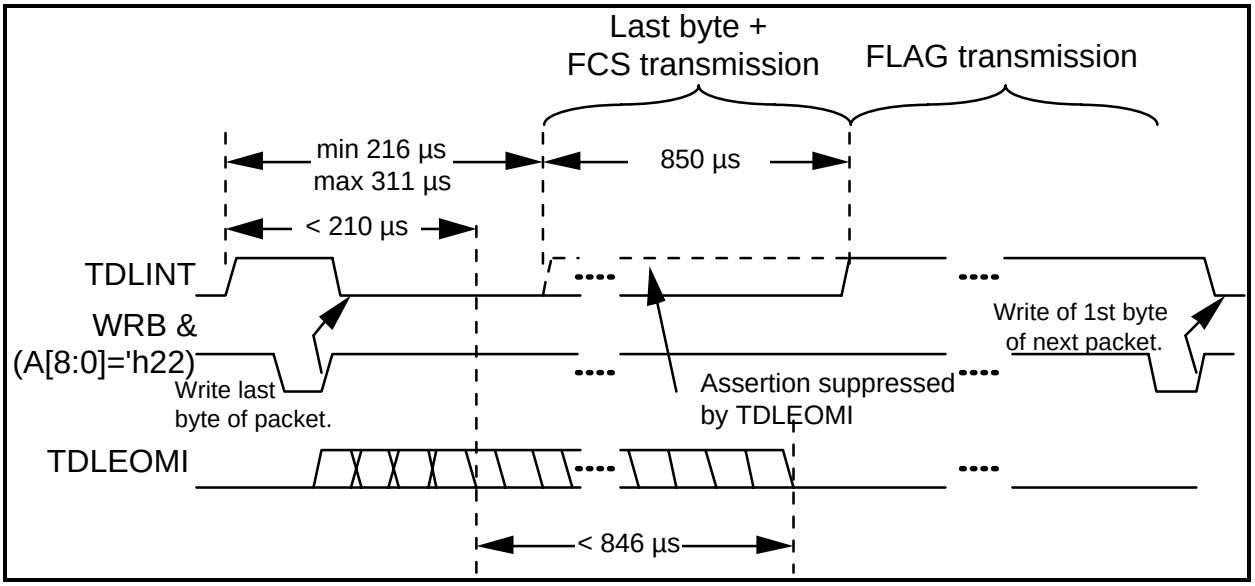


Figure 14 - TDLINT Timing - Normal Data Transmission



In this example successive bytes of a packet are written to the XFDL. Each byte must be written within 110µs from the TDLINT rising edge. Each subsequent assertion of TDLINT occurs once all 8 bits of the current data byte have been transmitted. The range in assertion times is due to the temporal spacing of the datalink bits (3 C-bits of M-subframe 5). If another byte is not written to the data register within 110µs of each TDLINT assertion, an underrun condition occurs. The underrun will be indicated on the TDLUDR output and in the UDR status bit within the XFDL Interrupt Status register.

Figure 15 - TDLEOMI Timing - With Removal of TDLEOMI Before Completion of FCS Transmission



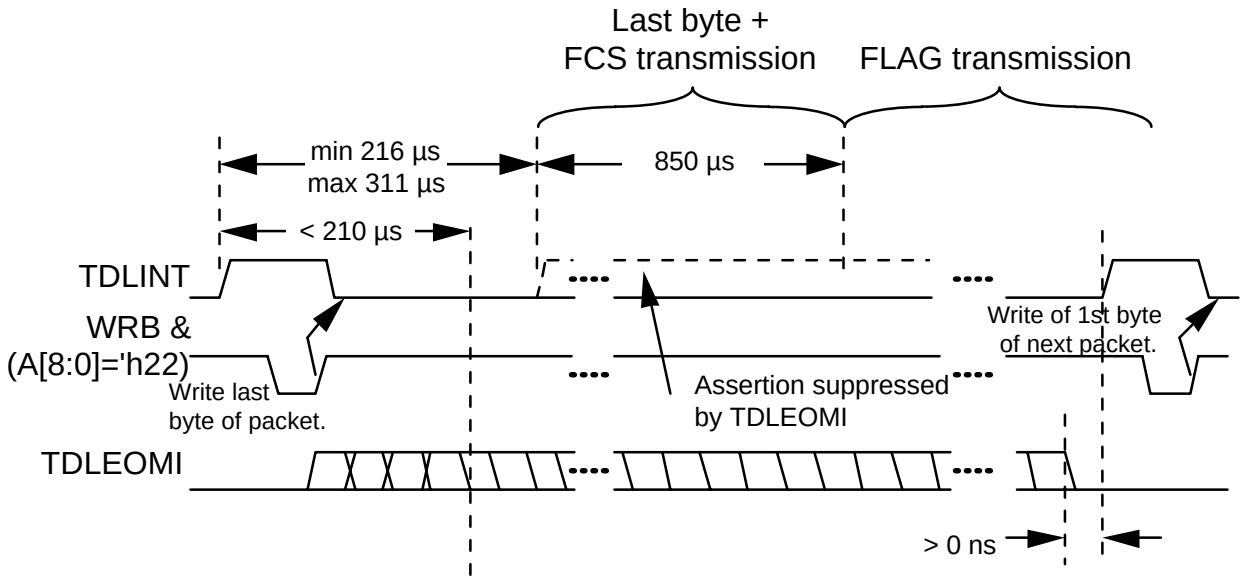
Assertion of the TDLEOMI input indicates the latest byte written to the XFDL Transmit Data Register is the last byte of the current packet. Upon assertion of TDLEOMI, the frame check sequence (FCS), if enabled, is appended to the packet once the last byte has been transmitted, and flags ("01111110") are transmitted in subsequent bytes until another byte is written. The TDLEOMI input accommodates a wide range of timing: the TDLEOMI input may be asserted as early as coincident with the falling edge of the write strobe for the last byte written, but must be asserted within 210 µs of the assertion of the TDLINT output (or INT bit in the XFDL Status Register). This ensures that the TDLEOMI input is recognized before the next TDLINT assertion. TDLEOMI must be deasserted before the write of the first byte of the next packet. If TDLEOMI falls too late, the first byte is also assumed to be the last, and the FCS (if enabled) and flags are appended immediately after.

In the example of Figure 15, the TDLEOMI is asserted anytime up to 210µs from the TDLINT rising edge and is deasserted before the FCS has been completely transmitted. The TDLINT signal is suppressed by the assertion of TDLEOMI and remains suppressed until the FCS has completed transmission. TDLINT is asserted coincident with the beginning of FLAG transmission and remains high until the first byte of a new packet is written into the data register. While TDLINT is asserted and the XFDL TSB is awaiting the first byte of a new packet, an underrun condition cannot occur. Once the first byte is written, however, the

XFDL must be serviced within 210µs of TDLINT assertion, otherwise an underrun condition occurs (see Figure 10).

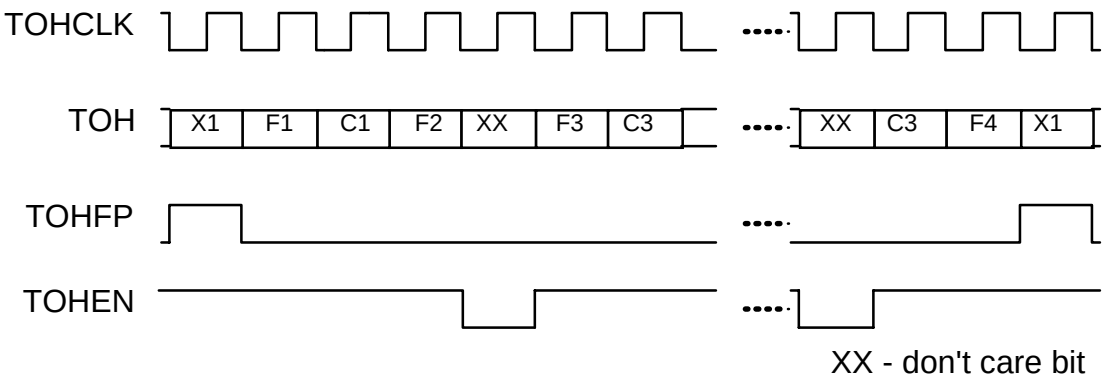
Note that TDLEOMI must be glitch free. If TDLEOMI is not used, it must be held low, and indication of end of message can be performed through the EOM bit of the XFDL Configuration Register. This bit may be set by a write to the configuration register any time after the write of the last data byte, but before 210 µs have elapsed since the TDLINT output (or INT bit in the XFDL Status Register) was last asserted.

Figure 16 - TDLEOMI Timing - With Removal of TDLEOMI After Completion of FCS Transmission



In this example, the TDLEOMI is asserted anytime up to 210µs from the TDLINT rising edge and is deasserted long after the FCS has been completely transmitted. The TDLINT signal is suppressed by the assertion of TDLEOMI and remains suppressed until TDLEOMI is deasserted. TDLINT is asserted immediately, indicating that the XFDL is ready to receive the first byte of a new packet. Again, while the XFDL is awaiting the first byte of a new packet, an underrun condition cannot occur. Once the first byte is written, however, the XFDL must be serviced within 210µs of each TDLINT assertion, otherwise an underrun condition occurs (see Figure 10).

Figure 17 - Input DS3 Overhead Serial Stream

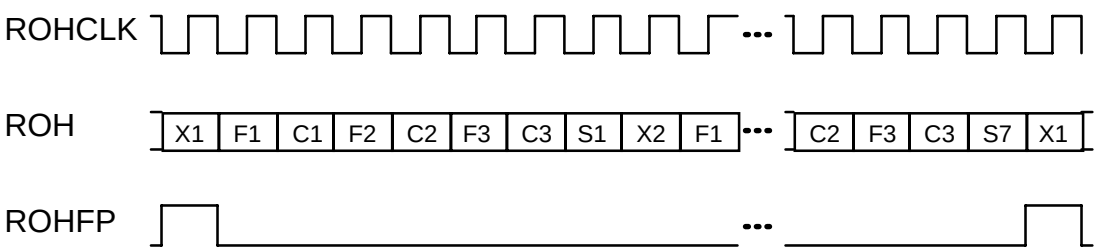


The TOHFP pulse indicates when the X1 overhead bit is sampled on the TOH input. Both TOH and TOHEN are sampled using the rising edge of TOHCLK. TOH bits are only inserted if TOHEN is asserted. At block 8 of each M-subframe either the F4 bits or the stuff opportunity bits are inserted depending on the setting of the SBOW bit in the DS3-TRAN Configuration Register. The format of the transmit overhead serial stream is as follows:

Table 3 - Transmitt Overhead Format

M-subframe	Block							
	1	2	3	4	5	6	7	8
1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4 or S_1
2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4 or S_2
3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4 or S_3
4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4 or S_4
5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4 or S_5
6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4 or S_6
7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	F_4 or S_7

Figure 18 - Output DS3 Overhead Serial Stream



The ROHFP pulse indicates when the X1 overhead bit is output on the ROH output stream. Both ROH and ROHFP are updated on the falling edge of ROHCLK. Within each M-subframe the stuff opportunity bits are extracted and output in place of the F4 framing bit. The format of the receive overhead serial stream is as follows:

Table 4 - Receive Overhead Format

M-subframe	Block							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	S_1
2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	S_2
3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	S_3
4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	S_4
5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	S_5
6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	S_6
7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	S_7

14 ABSOLUTE MAXIMUM RATINGS

Table 5 - D3MX Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±500 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C

15 D.C. CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 6 - D3MX D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{OL}	Output or Bidirectional Low Voltage			0.4	Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and high speed transmit outputs and 2 mA for all others, Note 3
V_{OH}	Output or Bidirectional High Voltage	2.4			Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and high speed transmit outputs and 2 mA for all others, Note 3
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			1.0	Volts	
V_{TH}	Reset Input Hysteresis Voltage		1.0		Volts	
IILPU	Input Low Current	+20		+200	µA	VIL = GND, Notes 1, 3
IIHPU	Input High Current	-10		+10	µA	VIH = VDD, Notes 1, 3
IIL	Input Low Current	-10		+10	µA	VIL = GND, Notes 2, 3

Symbol	Parameter	Min	Typ	Max	Units	Conditions
IIH	Input High Current	-10		+10	µA	VIH = VDD, Notes 2, 3
CIN	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
COUT	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
CIO	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
IDDOP	Operating Current		55	75	mA	VDD = 5.5 V, Outputs Unloaded, All Clocks At Nominal Frequencies

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

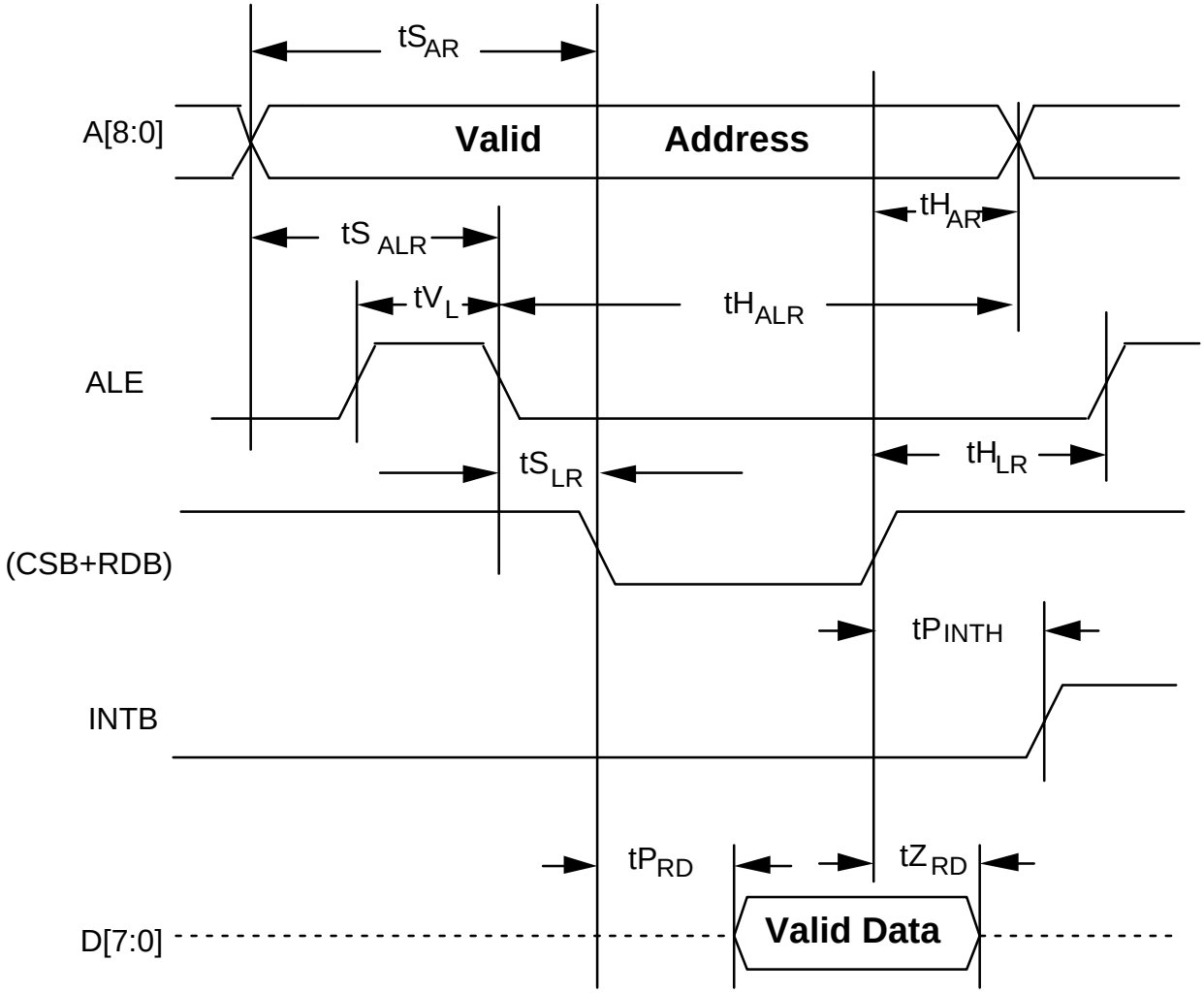
16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 7 - Microprocessor Read Access (Figure 19)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	20		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	20		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		100	ns
tZ_{RD}	Valid Read Deasserted to Output Tri-state		20	ns
tP_{INTH}	Valid Read Deasserted to INTB Tri-state		50	ns

Figure 19 - Microprocessor Read Access Timing



Notes on Microprocessor Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the microprocessor data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor timing applies to normal mode register accesses only.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

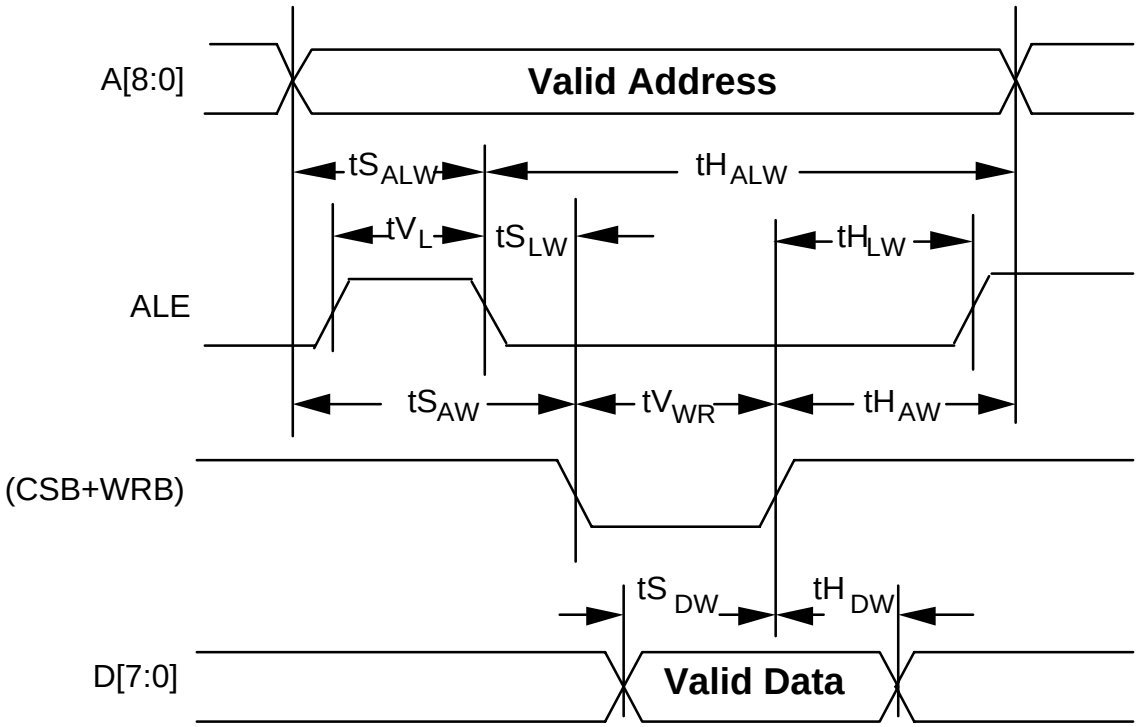
7. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, tH_{LR} and tS_{LR} are not applicable.

8. Parameters tH_{AR} and tS_{AR} are not applicable if address latching is used.

Table 8 - Microprocessor Write Access (Figure 20)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	20		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	20		ns
tH_{DW}	Data to Valid Write Hold Time	20		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 20 - Microprocessor Write Access Timing



Notes on Microprocessor Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. Microprocessor timing applies to normal mode register accesses only.
3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, tH_{LW} and tS_{LW} are not applicable.
4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.
5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

17 D3MX TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 9 - D3MX Receive DS3 Input (Figure 21)

Symbol	Description	Min	Max	Units
	RCLK Frequency (nominally 44.736 MHz)	-20	+20	ppm
	RCLK Duty Cycle	40	60	%
tS_{RPOS}	RPOS/RDAT Set-up Time	4		ns
tH_{RPOS}	RPOS/RDAT Hold Time	6		ns
tS_{RNEG}	RNEG/RLCV Set-Up Time	4		ns
tH_{RNEG}	RNEG/RLCV Hold Time	6		ns

Figure 21 - Receive DS3 Input Timing

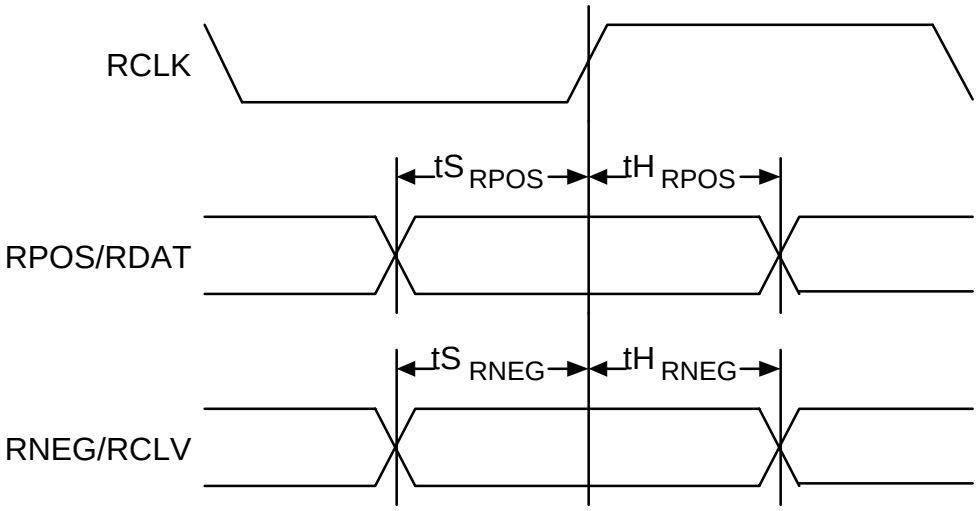


Table 10 - D3MX Transmit DS3 Input (Figure 22)

Symbol	Description	Min	Max	Units
	TICLK Frequency (nominally 44.736 MHz)	-20	+20	ppm
	TICLK Duty Cycle	40	60	%
tS_{TIMFP}	TIMFP Set-up Time	5		ns
tH_{TIMFP}	TIMFP Hold Time	5		ns

Figure 22 - Transmit DS3 Input Timing

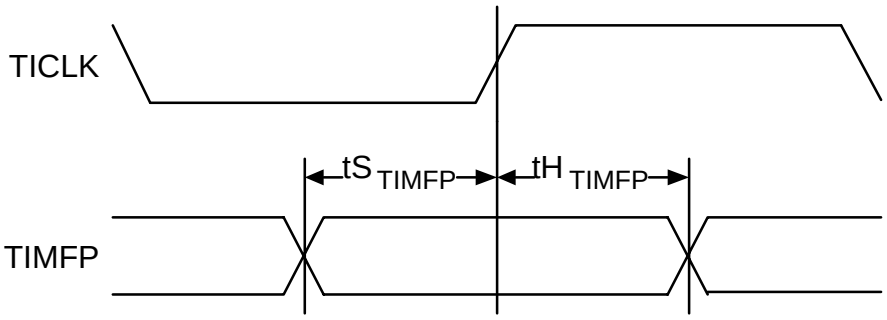


Table 11 - D3MX Transmit Overhead Input (Figure 23)

Symbol	Description	Min	Max	Units
tS_{TOH}	TOH Set-up Time	20		ns
tH_{TOH}	TOH Hold Time	20		ns
tS_{TOHEN}	TOHEN Set-up Time	20		ns
tH_{TOHEN}	TOHEN Hold Time	20		ns

Figure 23 - Transmit Overhead Input Timing

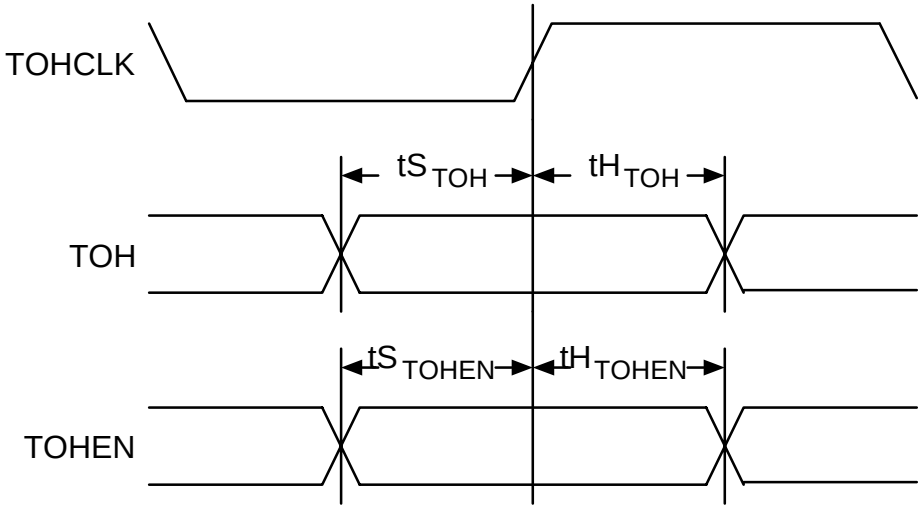


Table 12 - D3MX Transmit Tributary Input (Figure 24)

Symbol	Description	Min	Max	Units
	TD1CLKn Frequency (nominally 1.544 MHz, when configured for DS1 rate operation)[3]	-130	+130	ppm
	TD1CLKn Frequency (nominally 2.048 MHz, when configured for E1 rate operation; not applicable for n = 4, 8, 12, 16, 20, 24, 28)[3]	-50	+50	ppm
	TD1CLKn Frequency (nominally 6.312 MHz, when configured for DS2 rate operation; only applicable for n = 4, 8, 12, 16, 20, 24, 28)[3]	-33	+33	ppm
	TD1CLK Duty Cycle (all configurations)	33	67	%
	TD2CLK Frequency (nominally 6.312 MHz)[3]	-33	+33	ppm
	TD2CLK Duty Cycle	33	67	%
tS_{TD1DAT}	TD1DAT Set-up Time	20		ns
tH_{TD1DAT}	TD1DAT Hold Time	20		ns

Figure 24 - Transmit Tributary Input Timing

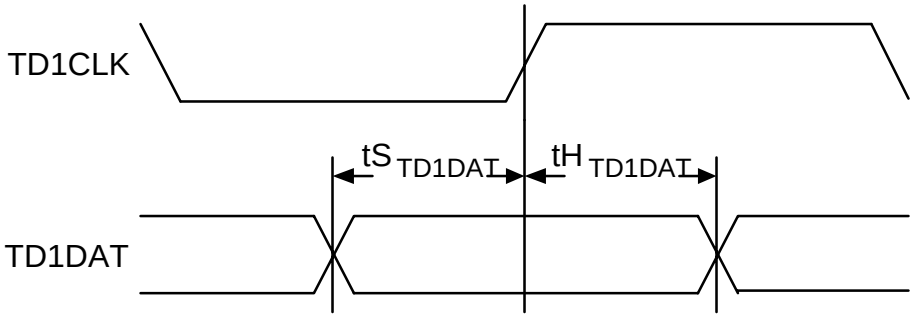


Table 13 - D3MX Transmit Data Link Input (Figure 25)

Symbol	Description	Min	Max	Units
tS_{TDLSIG}	TDLSIG to TDLCLK Set-up Time	20		ns
tH_{TDLSIG}	TDLSIG to TDLCLK Hold Time	20		ns

Figure 25 - Transmit Data Link Input Timing

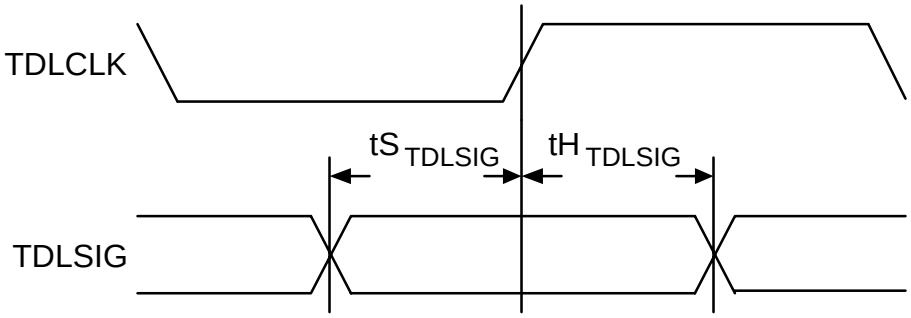
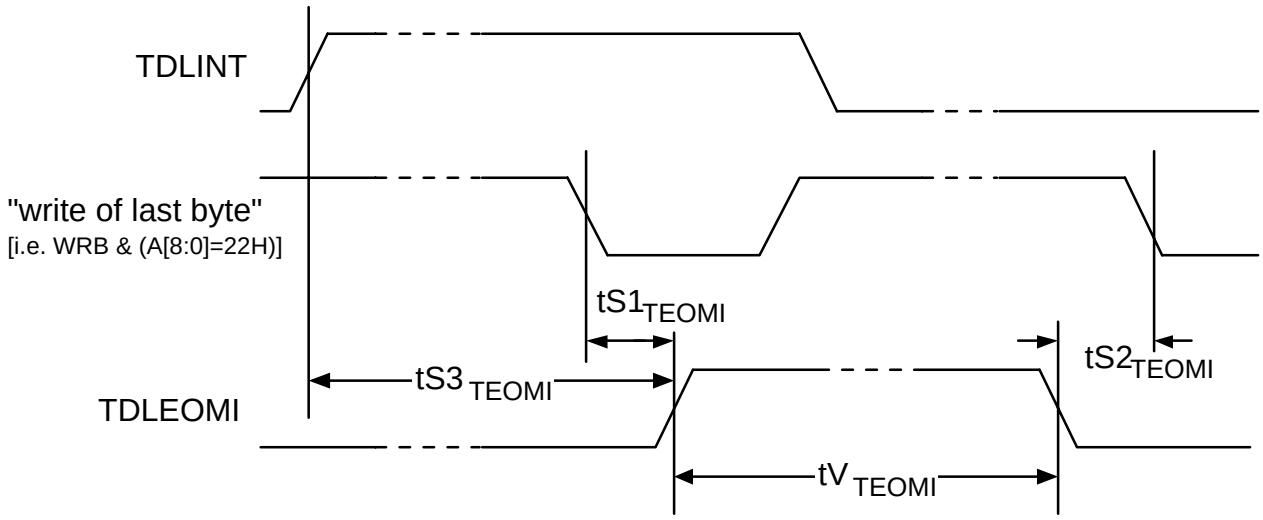


Table 14 - D3MX Transmit Data Link EOM Input (Figure 26)

Symbol	Description	Min	Max	Units
tV_{TEOMI}	TDLEOMI Pulse Width[3]	5		ns
$tS1_{TEOMI}$	TDLEOMI Pulse to Falling Edge of XFDL[3] Transmit Data Register Write Set-up Time	0		ns
$tS2_{TEOMI}$	TDLEOMI Pulse to Next Falling Edge of XFDL[3] Transmit Data Register Write Set-up Time	0		ns
$tS3_{TEOMI}$	TDLEOMI Pulse After TDLINT Assertion[3]		210	µs

Figure 26 - Transmit Data Link EOM Input Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. TD1CLKn frequency, TD2CLK frequency, $tS1_{TEOMI}$, $tS2_{TEOMI}$, $tS3_{TEOMI}$ and tV_{TEOMI} values are guaranteed by design - not measured.

Table 15 - D3MX Transmit DS3 Output (Figure 27)

Symbol	Description	Min	Max	Units
	TCLK Duty Cycle	TICLK-5	TICLK +5	%
tP_{TPOS}	TCLK Low to TPOS/TDAT Valid Prop. Delay	-2	5	ns
tP_{TNEG}	TCLK Low to TNEG/TMFP Valid Prop. Delay	-2	5	ns

Figure 27 - Transmit DS3 Output Timing

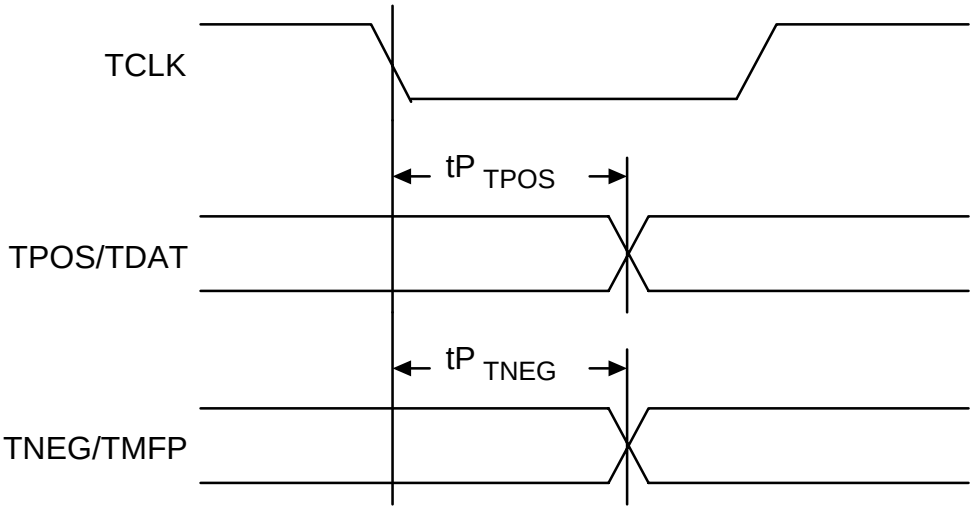


Table 16 - D3MX Receive DS3 Output (Figure 28)

Symbol	Description	Min	Max	Units
t_{PRODAT}	ROCLK Low to RODAT Valid Prop. Delay	-3	3	ns
t_{PRMFP}	ROCLK Low to RMFP Valid Propagation Delay	-3	3	ns
t_{PRMSFP}	ROCLK Low to RMSFP Valid Prop. Delay	-3	3	ns
t_{PROHP}	ROCLK Low to ROHP Valid Propagation Delay	-3	3	ns
t_{PRLOS}	ROCLK Low to RLOS Valid Propagation Delay	-3	3	ns

Figure 28 - Receive DS3 Output Timing

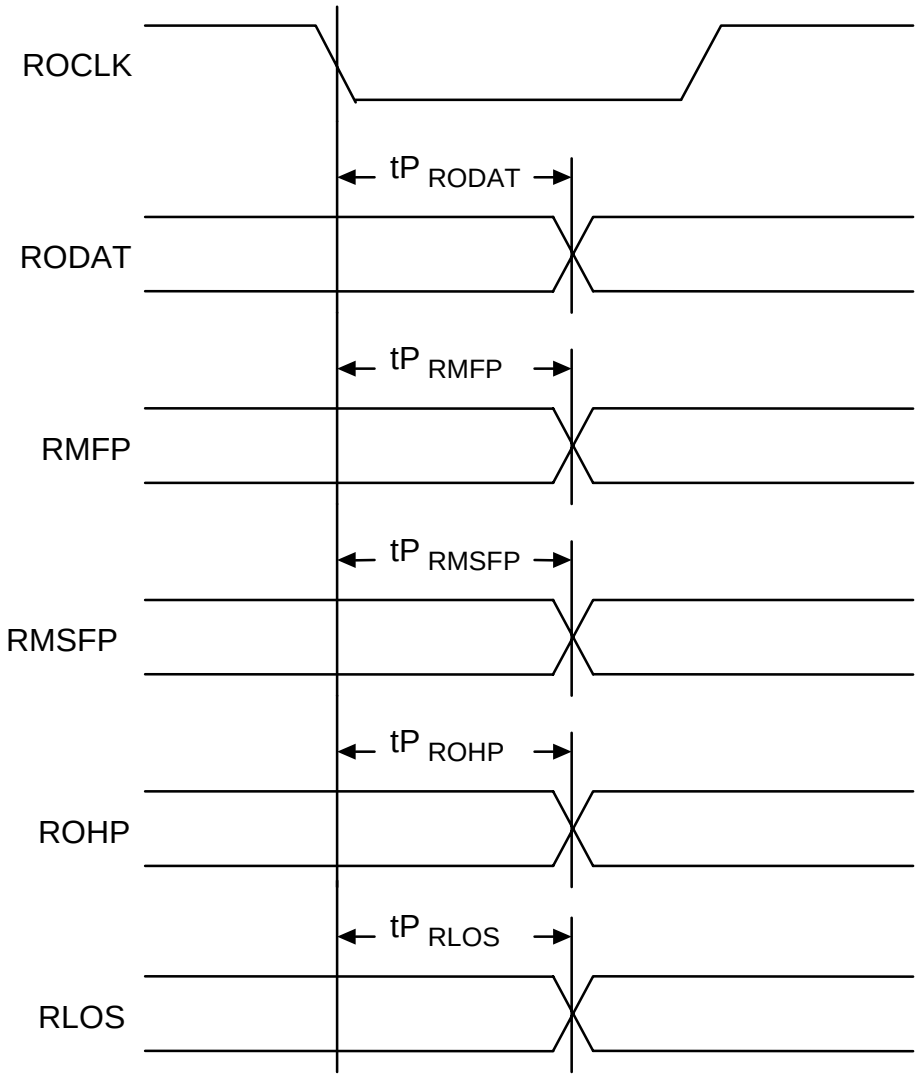


Table 17 - D3MX Receive Overhead Output (Figure 29)

Symbol	Description	Min	Max	Units
t_{PROH}	ROHCLK Low to ROH Valid Propagation Delay	-5	20	ns
t_{PROHFP}	ROHCLK Low to ROHFP Valid Prop. Delay	-5	20	ns
t_{PRAIS}	ROHCLK Low to RAIS Valid Propagation Delay	-5	20	ns
t_{PROOF}	ROHCLK Low to ROOF Valid Prop. Delay	-5	20	ns
t_{PRFERF}	ROHCLK Low to RFERF Valid Prop. Delay	-5	20	ns

Figure 29 - Receive Overhead Output Timing

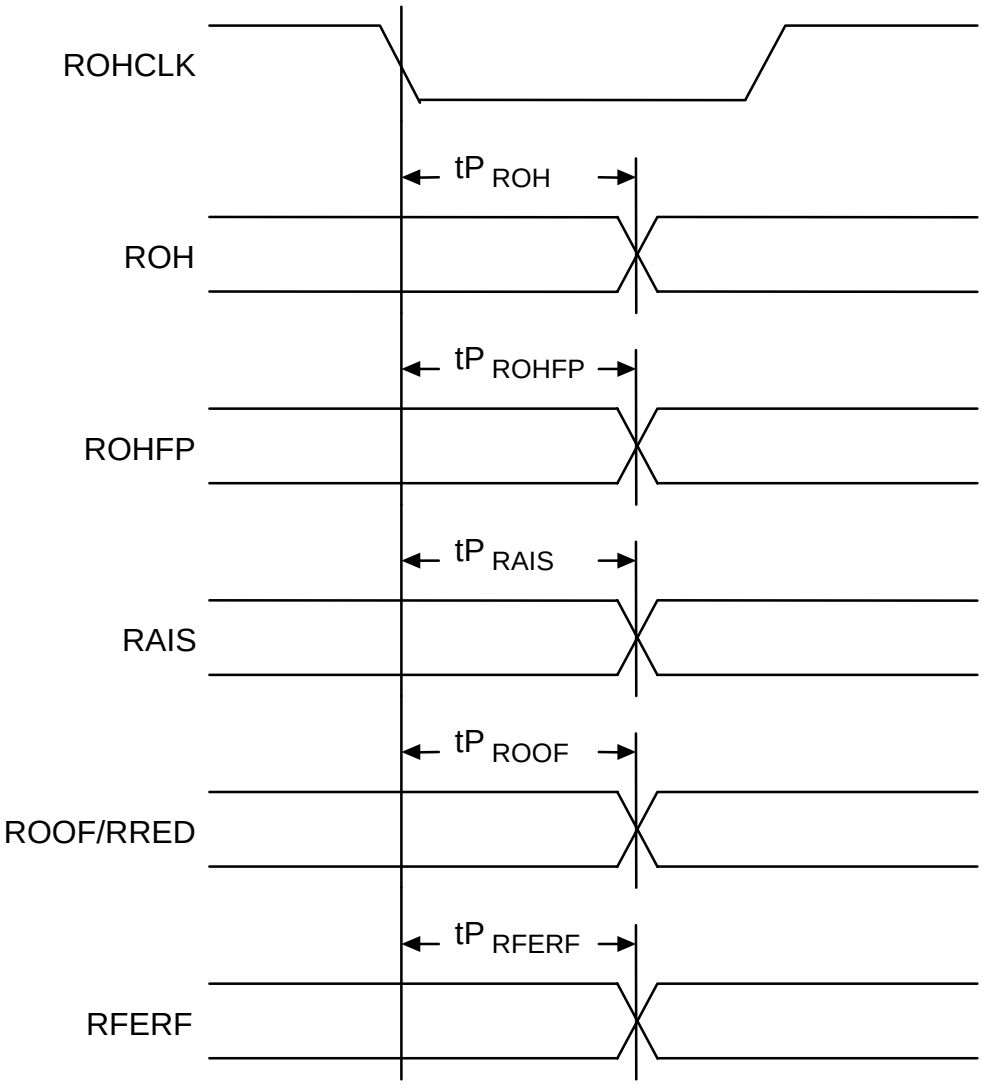


Table 18 - D3MX Transmit Overhead Output (Figure 30)

Symbol	Description	Min	Max	Units
tP_{TOHFP}	TOHCLK Low to TOHFP Valid Prop. Delay	-10	20	ns

Figure 30 - Transmit Overhead Output Timing

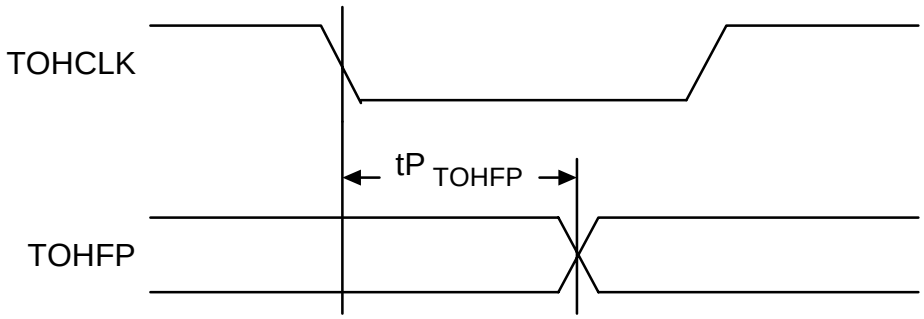


Table 19 - D3MX Receive Tributary Output (Figure 31)

Symbol	Description	Min	Max	Units
tP_{RD1DAT}	RD1CLK Low to RD1DAT Valid Prop. Delay	-10	20	ns

Figure 31 - Receive Tributary Output Timing

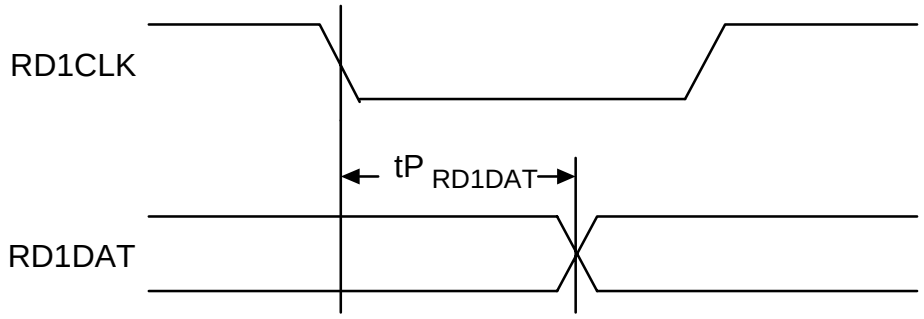
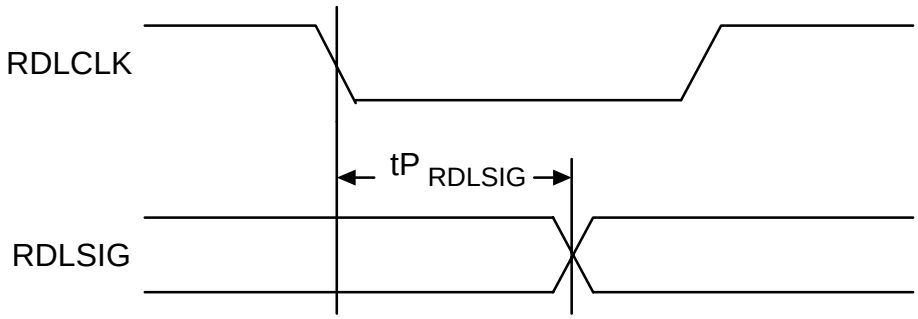


Table 20 - D3MX Receive Data Link Output (Figure 32)

Symbol	Description	Min	Max	Units
tP_{RDLSIG}	RDLCLK Low to RDLSIG Valid Prop. Delay	-10	20	ns

Figure 32 - Receive Data Link Output Timing



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 20 pF load on the high-speed DS3 outputs (TCLK, TPOS/TDAT, TNEG/TMFP, ROCLK, RODAT, RMFP, RMSFP, and ROHP) and a 50 pF load on the remaining outputs.

18 ORDERING AND THERMAL INFORMATION

Table 21 - D3MX Ordering Information

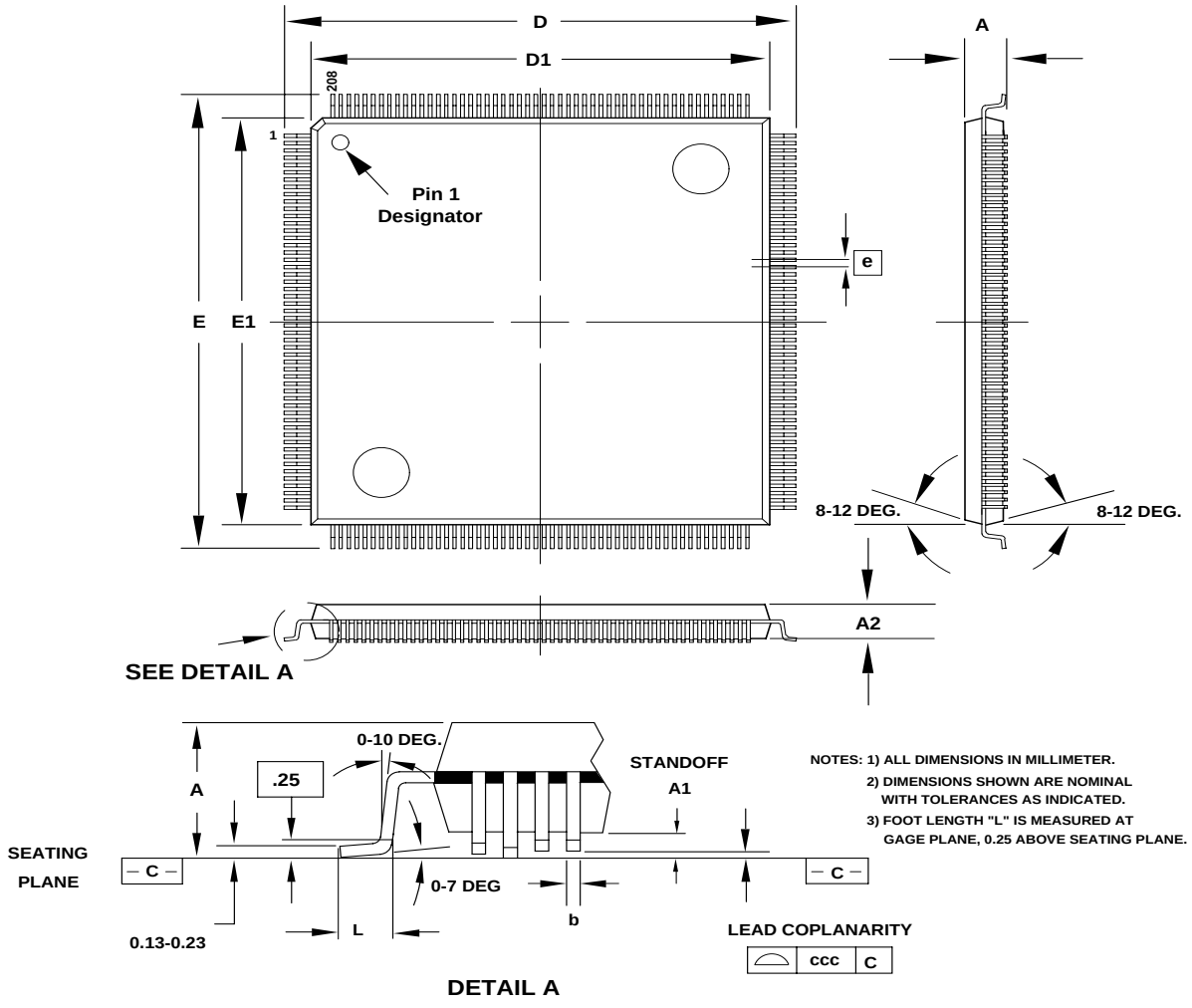
PART NO.	DESCRIPTION
PM8313-RI	208 Pin Copper Leadframe Plastic Quad Flat Pack

Table 22 - D3MX Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM8313-RI	-40°C to 85°C	50 °C/W	15 °C/W

19 MECHANICAL INFORMATION

Figure 33 - 208 Pin Copper Leadframe Plastic Quad Flat Pack (R Suffix):



PACKAGE TYPE: 208 PIN METRIC PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 28 x 28 x 3.49 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	3.64	0.25	3.39	30.40	27.90	30.40	27.90	0.50		0.17	
Nom.			3.49	30.60	28.00	30.60	28.00	0.60	0.50	0.22	
Max.	4.07	0.48	3.59	30.80	28.10	30.80	28.10	0.75		0.27	0.10

The 208 pin PQFP package lead length specification has been changed from 3.20mm to the industry standard length of 2.60 mm outlined above. This change applies on all devices shipped with date codes of 9514 or later.

NOTES

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

PMC-920702 (R5) ref 911105 (R13) Issue date: July 1998