PM6341

E1XC

E1 FRAMER/TRANSCEIVER

DATA SHEET

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PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
8	June 1998	Data Sheet Reformatted — No Change in Technical Content. Generated R8 data sheet from PMC-901204, R10
7	February 1996	Update to rev 9 of Eng Doc
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5		
4		
3		
2		
1		Creation of Document

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1 FEATURES

- Integrates a full-featured E1 transceiver in a single device with analog circuitry for receiving and transmitting G.703 2048 kbit/s compatible signals and digital circuitry for terminating the duplex digital signal.
- Pin compatible with the PMC PM4341A T1 Framer/Transceiver device.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power CMOS technology.
- Available in either a 68 pin PLCC or an 80 pin PQFP package.

The receiver section:

- Provides analog circuitry for receiving a G.703 2048 kbit/s signal with up to 6 dB of cable attenuation. Direct digital inputs are also provided to allow for by-passing the analog front-end.
- Recovers clock and data using a digital phase locked loop for high jitter tolerance. A direct clock input is provided to allow clock recovery to be by-passed.
- Accepts dual rail or single rail digital PCM inputs.
- Supports HDB3 or AMI line code.
- Accepts gapped data streams to support higher rate demultiplexing.
- Frames to a G.704 2048 kbit/s signal within 1 ms.
- Frames to the signalling multiframe alignment when enabled.
- Frames to the CRC multiframe alignment when enabled.
- Provides loss of signal detection, and indicates loss of frame alignment (OOF), loss of signalling multiframe alignment and loss of CRC multiframe alignment.
- Supports line and path performance monitoring according to ITU-T recommendations. Accumulators are provided for counting:
    - CRC-4 errors to 1000 per second;
    - Far end block errors to 1000 per second;
    - Frame sync errors to 127 per second; and
    - Line code violations to 8191 per second.

- Indicates the reception of remote alarm and remote multiframe alarm.
- Indicates the reception of alarm indication signal (AIS) and time slot 16 AIS.
- Declares RED and AIS alarms using Q.516 recommended integration periods.
- Provides an HDLC/LAPD interface for terminating a data link. Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Optionally extracts the data link from timeslot 16 (64 kbit/s), which may be used to receive common channel signalling, or from any combination of the national bits in timeslot 0 of non-frame alignment signal frames (4 kbit/s - 20 kbit/s).
- Provides a two-frame elastic store buffer for jitter and wander attenuation that performs controlled slips and indicates slip occurrence and direction.
- Provides channel associated signalling extraction, with optional data inversion, programmable idle code substitution, and up to 3 multiframes of signalling debounce on a per-timeslot basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signalling conditioning on all timeslots or on selected timeslots.
- Optionally provides dual rail digital PCM output signals to allow BPV transparency. Also supports unframed mode.
- Supports transfer of received PCM and signalling data to 2048 kbit/s backplane buses.

The transmitter section:

- Supports transfer of transmitted PCM and signalling data from 2048 kbit/s backplane buses.
- Formats data to create a G.704 2048 kbit/s signal. Optionally inserts signalling multiframe alignment signal. Optionally inserts CRC multiframe structure including optional transmission of far end block errors.
- Optionally accepts dual rail digital PCM inputs to allow BPV transparency. Also supports unframed mode.
- Provides channel associated signalling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per timeslot basis.

- Provides trunk conditioning which forces programmable trouble code substitution and signalling conditioning on all timeslots or on selected timeslots.
- Supports transmission of the alarm indication signal (AIS), timeslot 16 AIS, remote alarm signal or remote multiframe alarm signal.
- Provides an HDLC/LAPD interface for generating a data link. Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Optionally inserts the data link into timeslot 16 (64 kbit/s), which may be used to transmit common channel signalling, or into any combination of the national bits in timeslot 0 of non-frame alignment signal frames (4 kbit/s - 20 kbit/s).
- Provides a digital phase locked loop for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmitter. FIFO full or empty indication allows for bit-stuffing in higher rate multiplexing applications.
- Supports HDB3 or AMI line code.
- Provides analog circuitry for transmitting a G.703 compatible 2048 kbit/s signal on a 75 Ω coaxial line or a 120 Ω symmetrical line. Digitally programmable line build out is provided.
- Provides dual rail or single rail digital PCM output signals.

2 APPLICATIONS

- E1 ATM Interfaces
- E1 Frame Relay Interfaces
- E1 & E3 Multiplexers (MUX)
- Digital Private Branch Exchanges (DPBX)
- Digital Access and Cross-Connect Systems (DACS)
- Electronic Cross-Connect Systems (EDSX)
- E1 & E3 Test Equipment (TEST)
- ISDN Primary Rate Interfaces (PRI)
- E1 Channel Service Units (CSU) and Data Service Units (DSU)
- SONET/SDH Add/Drop Multiplexers (ADM)

3 REFERENCES

1. ITU-T Recommendation G.703, - "Physical/Electrical Characteristics of Hierarchical Digital Networks", Sept. 1991.

2. ITU-T Recommendation G.704, - "Synchronous Frame Structures Used at Primary and Secondary Hierarchical Levels", Oct. 1991.

3. ITU-T Recommendation G.706, - "Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704", Aug. 1991

4. ITU-T Recommendation G.711, - "Pulse Code Modulation (PCM) of Voice Frequencies", June 1990.

5. ITU-T Recommendation G.732, - "Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s", June 1990.

6. ITU-T Recommendation G.735, - "Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s and Offering Synchronous Digital Access at 384 kbit/s and/or 64 kbit/s", July 1990.

7. ITU-T Recommendation G.821, - "Error Performance of an International Digital Connection Forming Part of an Integrated Services Digital Network", July 1990.

8. ITU-T Recommendation G.823, - "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy", Jan. 1994.

9. ITU-T Recommendation O.151, - "Error Performance Measuring Equipment For Digital Systems at the Primary Bit Rate and Above", July 1993.

10. ITU-T Blue Book, Recommendation O.162, - "Equipment to Perform in Service Monitoring on 2048 kbit/s Signals", Vol. IV, Fascicle IV.4, 1988.

11. ITU-T Recommendation Q.506, - "Operations and maintenance functions", Vol. VI, Fascicle VI.5, 1984.

12. ITU-T Recommendation Q.516, - "Operations and maintenance functions", Vol. VI, Fascicle VI.5, 1984.

13. Transmission and Multiplexing (TM); Generic Functional Requirements for SDH Transmission Equipment, Part 1: Generic Processes and Performance", ETSI DE/TM-1015, November, 1993, Version 1.0.

14. American National Standard for Telecommunications, ANSI T1.102-1992 - "Digital Hierarchy - Electrical Interfaces".

4 APPLICATION EXAMPLES

Figure 1 - ATM E1 and DS1 User Network Interface

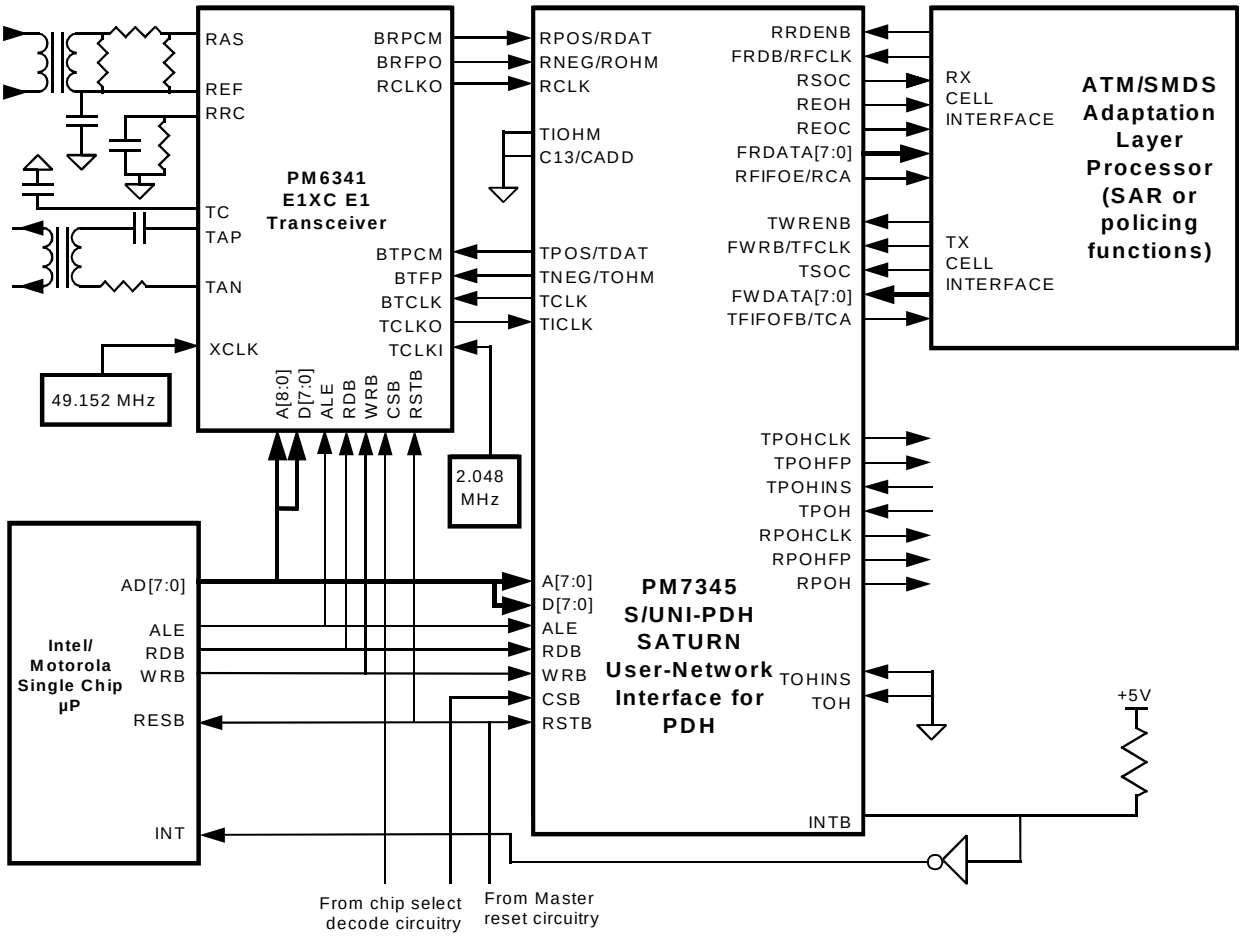


Figure 1 shows the PM6341 E1XC used with the PM7345 Saturn User Network Interface for PDH (S/UNI-PDH™) to implement an ATM wide area User Network Interface (UNI) or Network Node Interface (NNI).

In this example, the E1 LIU and framing functions are provided by the PM6341 E1XC. The combination of the E1XC with the S/UNI-PDH allows both PLCP formatted E1 signals and ITU-T G.804 compliant E1 signals to be processed. The G.804 specification defines ATM cell mappings for a variety of transmission formats, including the 2.048 Mbit/s E1 format.

Figure 2 - DS0 Cross-connect

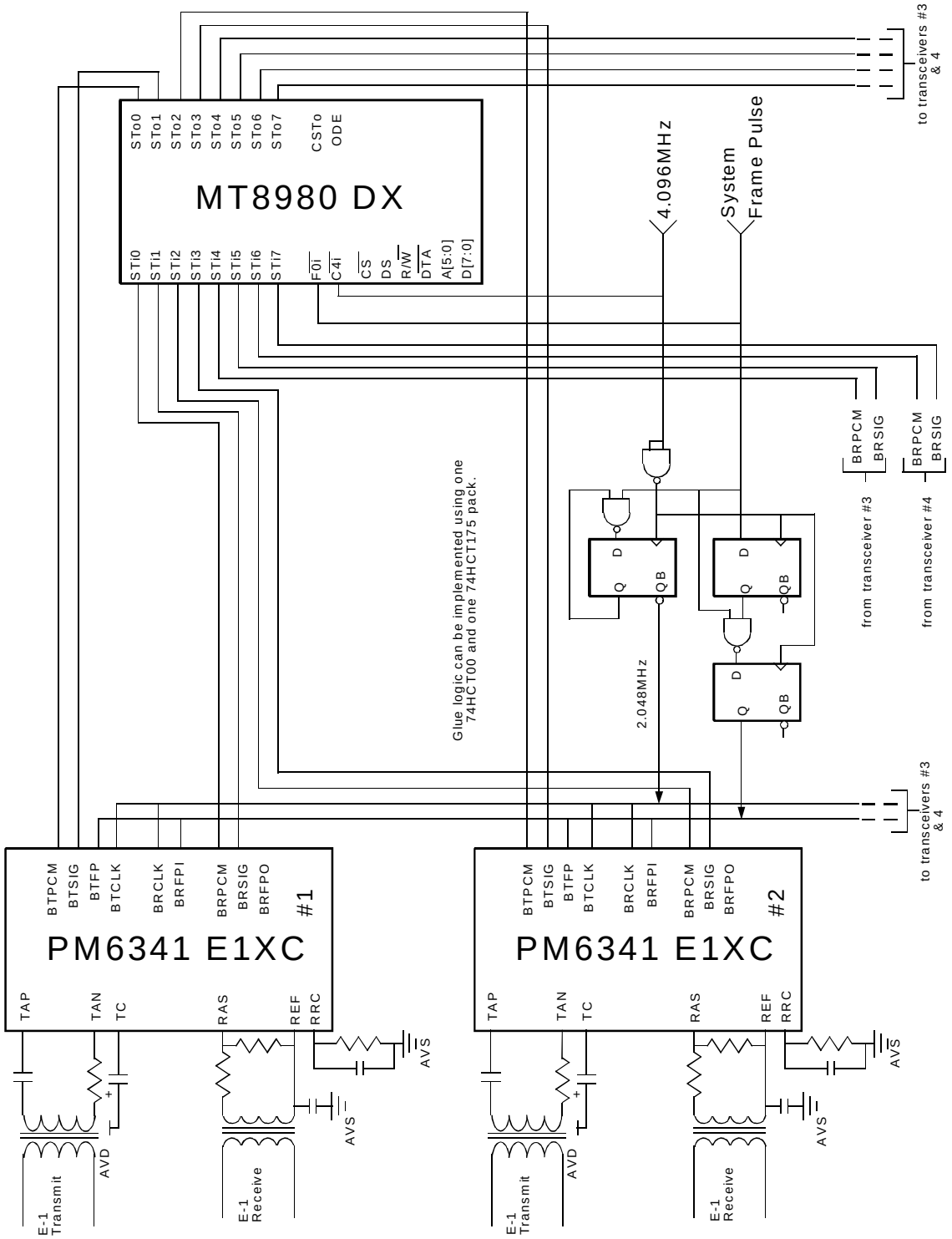
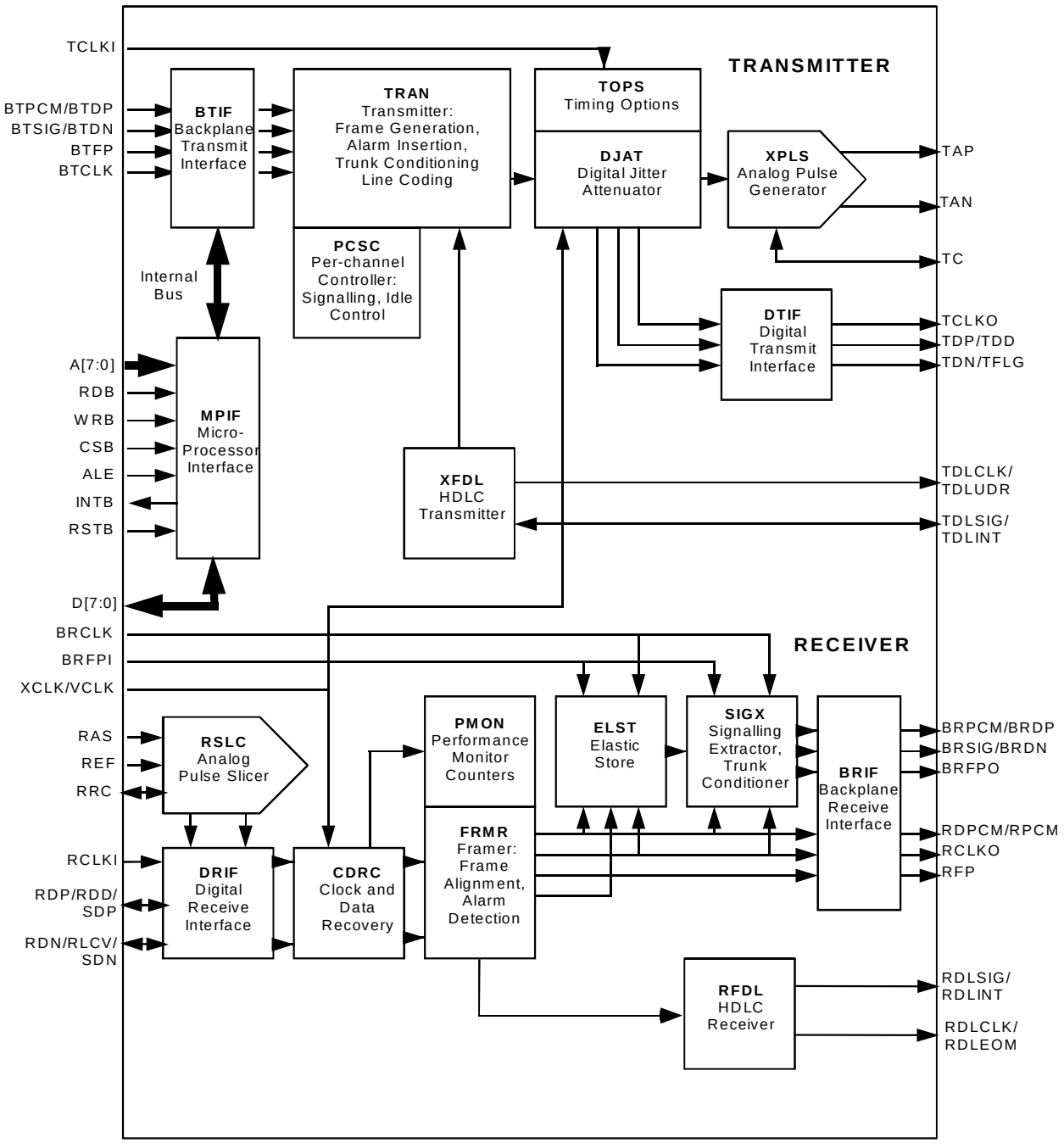


Figure 2 is an application utilizing 4 PM6341 E1XC chips and a Mitel MT8980 Digital Time/Space Switch to implement a simple DS0 cross-connect. An alternate architecture could use two MT8980, one as a voice switch and the other as a signalling switch, and 8 E1XCs to cross-connect 8 E1's. (Note: a true implementation would require redundancy in the switch core.)

The "system frame pulse" signal is stretched through the two D-FF into a pulse of 488ns duration, which is used to frame align the data out of each E1XC through the elastic store and to provide frame alignment indication to the transmitters. The raw system frame pulse signal is used to indicate frame alignment synchronization to the MT8980. Another D-FF is configured as a toggle to generate a 2.048MHz clock from the system 4.096MHz clock source, synchronized to the system frame pulse.

5 BLOCK DIAGRAM



6 DESCRIPTION

The PM6341 E1 Framer/Transceiver (E1XC) is a feature-rich device suitable for use in many E1 systems (such as CSU, DSU, CH BANK, MUX, DPBX, DACS, and ESDX) with a minimum of external circuitry. The E1XC is software configurable, allowing feature selection without changes to external wiring.

On the receive side, the E1XC recovers clock and data and can be configured to frame to a basic G.704 2048 kbit/s signal or also frame to the signalling multiframe alignment signal and the CRC multiframe alignment signal.

Analog circuitry is provided to allow direct reception of a G.703 2048 kbit/s signal with up to 6 dB of loss by using only an external transformer and passive components.

The E1XC also supports detection of various alarm conditions such as loss of signal, loss of frame, loss of signalling multiframe, loss of CRC multiframe, and reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and timeslot 16 alarm indication signal. The E1XC detects and indicates the presence of remote alarm and AIS patterns and also integrates red and AIS alarms as per industry specifications.

Performance monitoring with accumulation of CRC-4 errors, far end block errors, framing bit errors, and line code violation is provided. The E1XC also detects and terminates HDLC messages on a data link. The data link may be extracted from timeslot 16 and used for common channel signalling or may be extracted from the national bits.

An elastic store for slip buffering and adaptation to backplane timing is provided, as is a channel associated signalling extractor that supports signalling debounce, signalling freezing, idle code substitution, and data inversion on a per-timeslot basis. Receive side data and signalling trunk conditioning is also provided.

On the transmit side, the E1XC generates framing for a basic G.704 2048 kbit/s signal, or framing can be optionally disabled. The signalling multiframe alignment signal may be optionally inserted and the CRC multiframe structure may be optionally inserted.

Internal analog circuitry allows direct transmission of a G.703 2048 kbit/s signal into either a 75 Ω or 120 Ω line using only an external transformer.

Channel associated signalling insertion, idle code substitution, digital milliwatt tone substitution, and data inversion on a per-timeslot basis is also supported. Transmit side data and signalling trunk conditioning is provided.

HDLC messages on a data link can be transmitted. The data link may be inserted into timeslot 16 and used for common channel signalling or may be inserted into the national bits. The E1XC can generate a low jitter transmit clock and provides a FIFO for transmit jitter attenuation. When not used for jitter attenuation, the full or empty status of this FIFO is made available to facilitate higher order multiplexing applications by controlling bit-stuffing logic.

Interfaces include both a parallel microprocessor port for controlling the operation of the device and a serial PCM interface that allows 2048 kbit/s backplanes to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic.

7 PIN DIAGRAM

Figure 3 - 68 Pin PLCC (Q-Suffix):

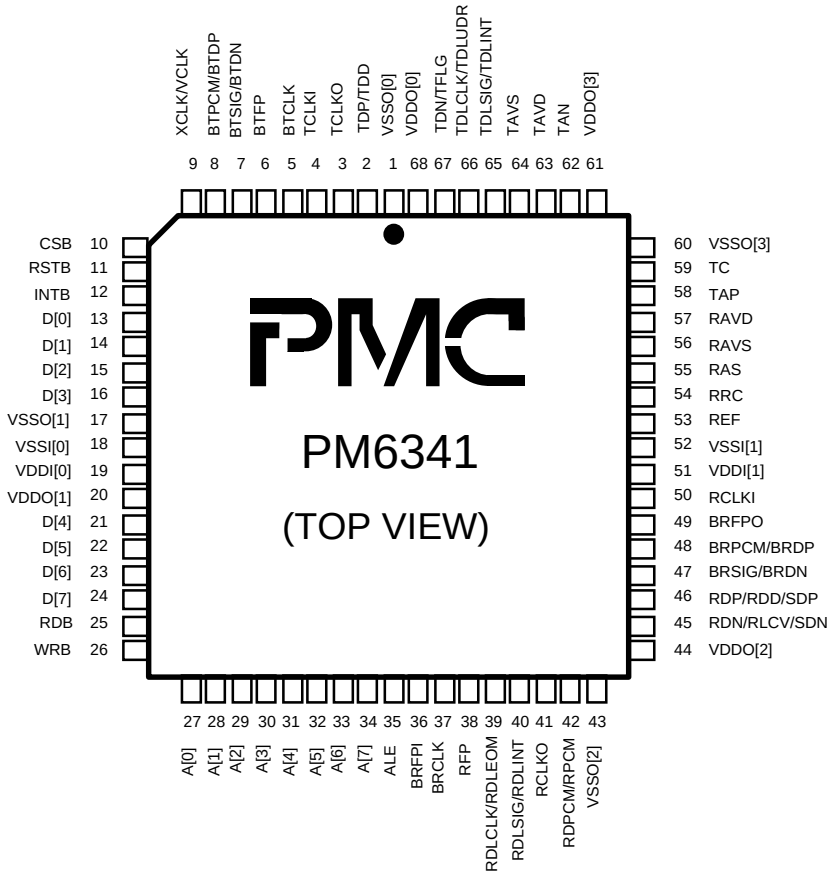
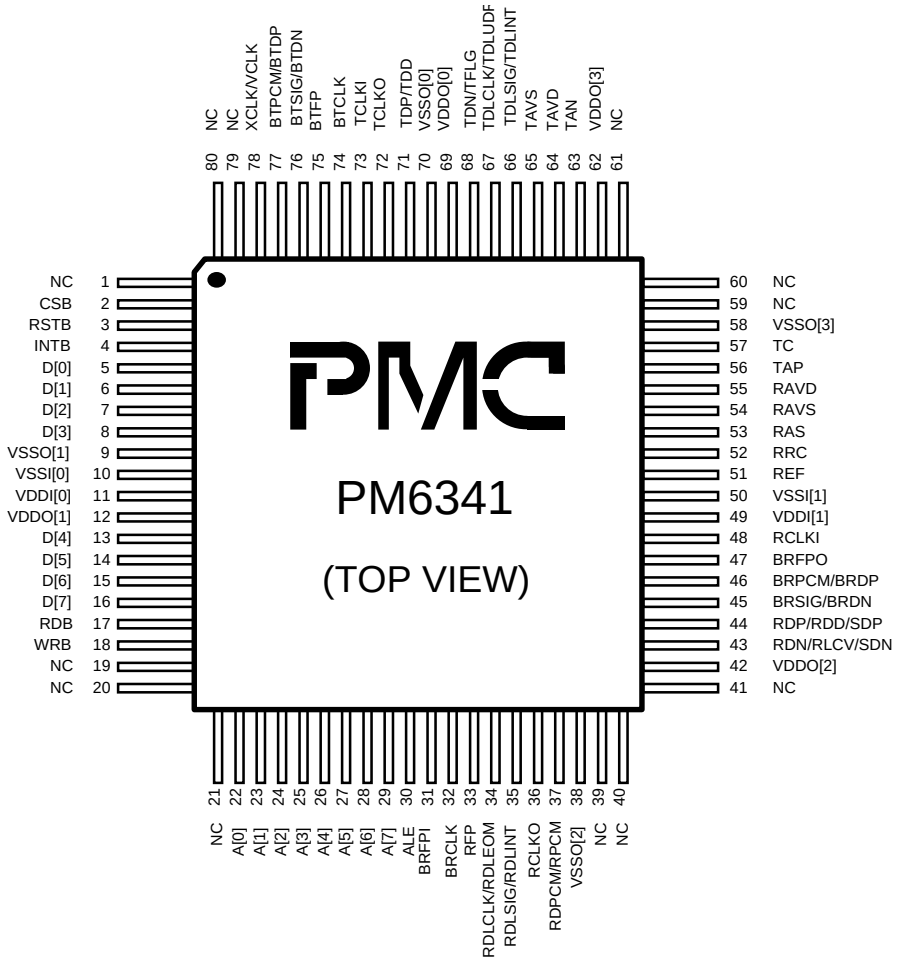


Figure 4 - 80 Pin PQFP (R-suffix):



8 PIN DESCRIPTION

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
RDP/	I/O	44	46	Receive Digital Positive Line Pulse (RDP). This input is available when the E1XC is configured to receive dual-rail formatted data. The RDP input can be enabled for either RZ or NRZ waveforms. When enabled for NRZ, this input may be enabled to be sampled on the rising or falling edge of RCLKI. When enabled for RZ, clock is recovered from the RDP and RDN inputs.
RDD/				Receive Digital Data (RDD). When the E1XC is configured to receive single-rail data, this input may be enabled to be sampled on the rising or falling edge of RCLKI.
SDP				Sliced Positive Line Pulse (SDP). This pin becomes an output when the receive analog line interface is powered up. A positive pulse on the SDP output corresponds to the sampled positive pulse excursion on the RAS input.
RDN/	I/O	43	45	Receive Digital Negative Line Pulse (RDN). This input is available when the E1XC is configured to receive dual-rail formatted data. The RDN input can be enabled for either RZ or NRZ waveforms. When enabled for NRZ, this input may be enabled to be sampled on the rising or falling edge of RCLKI. When enabled for RZ, clock is recovered from the RDP and RDN inputs.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
RLCV/ SDN	I/O	43	45	Receive Line Code Violation Indication (RLCV). When the E1XC is configured to receive single-rail data, this input may be enabled to be sampled on the rising or falling edge of RCLKI. Sliced Negative Line Pulse (SDN). This pin becomes an output when the receive analog line interface is powered up. A positive pulse on the SDN output corresponds to the sampled negative pulse excursion on the RAS input.
RCLKI	Input	48	50	Receive Line Clock Input (RCLKI). This input is an externally recovered 2.048 MHz line clock that may be enabled to sample the RDP and RDN inputs on its rising or falling edge when the input format is enabled for dual-rail NRZ; or to sample the RDD and RLCV inputs on its rising or falling edge when the input format is enabled for single-rail.
RAS	Input	53	55	Receive Analog Signal (RAS). This analog input samples the AC signal on an external isolation transformer. It is connected to the positive lead of the transformer secondary through a passive attenuation network.
REF	I/O	51	53	Receive Reference (REF). This analog bidirectional pin provides DC bias to an external isolation transformer. It is connected to the negative lead of the transformer secondary and to a decoupling capacitor to RAVS.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
RRC	I/O	52	54	Receive Peak Hold R-C Network (RRC). This analog bidirectional pin is connected to an external parallel resistor/capacitor network to RAVS. This network is necessary to the operation of the internal peak detector that tracks the incoming signal level.
RAVD	Power	55	57	Receive Analog Power (RAVD). This pin provides the +5V supply to the receive analog line interface. If the receive analog line interface is not used, the power consumption of the E1XC can be reduced by connecting the RAVD pin to the analog ground pin, RAVS. RAVD must be connected to a common, well decoupled +5 VDC supply together with the VDDO[3:0] and VDDI[1:0] pins. Care must be taken to avoid coupling noise induced on the VDDO and VDDI pins into the RAVD pin.
RAVS	Ground	54	56	Receive Analog Ground (RAVS). This pin provides the ground supply to the receive analog line interface. RAVS must be connected to a common ground together with the VSSO[3:0] and VSSI[1:0] pins. Care must be taken to avoid coupling noise induced on the VSSO and VSSI pins into the RAVS pin.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
RCLKO	Output	36	41	Recovered PCM Clock Output (RCLKO). This output signal is the recovered 2.048 MHz clock, synchronized to the XCLK signal. The RCLKO signal is recovered from the received analog inputs (if the interface is powered up), from the RDP and RDN inputs (if the input format is dual-rail RZ), or from the RCLKI input (if the input format is NRZ).
RDPCM/	Output	37	42	Recovered Decoded PCM (RDPCM). This output is available when the E1XC is configured for decoded data output. This NRZ output signal is the recovered data stream with HDB3 decoding applied, if HDB3 decoding is enabled. It is updated on the falling edge of RCLKO. The RDPCM signal is not meant to be used when the digital receive interface is configured for unipolar operation (RUNI = 1 and RDIEN = 1), since the data should be available at the RDD input.
RPCM				Recovered PCM (RPCM). This output is available when the E1XC is configured for raw data output. This NRZ output signal is the recovered data stream without optional HDB3 decoding applied. It is updated on the falling edge of RCLKO.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
RFP	Output	33	38	Receive Frame Pulse (RFP). When the E1XC is configured for receive frame pulse output, RFP pulses high for 1 RCLKO cycle during bit 1 of each 256-bit frame, indicating the frame alignment of the RDPCM data stream. When configured for receive signalling multiframe output, RFP pulses high for 1 RCLKO cycle during bit 1 of frame 1 of the 16 frame signalling multiframe, indicating the signalling multiframe alignment of the RDPCM data stream. (Even when signalling multiframing is disabled, the RFP output continues to indicate the position of bit 1 of every 16th frame.) When configured for receive CRC multiframe output, RFP pulses high for 1 RCLKO cycle during bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the RDPCM data stream. (Even when CRC multiframing is disabled, the RFP output continues to indicate the position of bit 1 of the FAS frame every 16th frame.)

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
RFP	Output	33	38	When configured for composite multiframe output, RFP goes high on the falling RCLKO edge marking the beginning of bit 1 of frame 1 of every 16 frame signalling multiframe, indicating the signalling multiframe alignment of the RDPCM data stream, and returns low on the falling RCLKO edge marking the ending of bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the RDPCM data stream. This mode allows both multiframe alignments to be decoded externally from the single RFP signal. Note that if the signalling and CRC multiframe alignments are coincident, RFP will pulse high for 1 RCLKO cycle every 16 frames. RFP does not indicate the frame or multiframe alignment of RDPCM when the digital receive interface is configured for unipolar operation (RUNI = 1 and RDIEN = 1 in register 03H.) RFP is updated on the falling edge of RCLKO.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
RDLSIG/	Output	35	40	Receive Data Link Signal (RDLSIG). The RDLSIG signal is available on this output when the internal HDLC receiver (RFDL) is disabled from use. RDLSIG contains the data link stream extracted from the selected data link bits. The E1XC may be configured to utilize timeslot 16 as a data link or utilize any combination of the national bits as a data link. RDLSIG is updated on the falling edge of RDLCLK.
RDLINT				Receive Data Link Interrupt (RDLINT). The RDLINT signal is available on this output when RFDL is enabled. RDLINT goes high when an event occurs which changes the status of the HDLC receiver.
RDLCLK/	Output	34	39	Receive Data Link Clock (RDLCLK). The RDLCLK signal is available on this output when the internal HDLC receiver (RFDL) is disabled from use. RDLCLK is used to process the data stream contained on the RDLSIG output. When the E1XC is not configured to extract a data link, the RDLCLK output is held low. In all other formats the rising edge of RDLCLK can be used to sample the data on RDLSIG.
RDLEOM				Receive Data Link End of Message (RDLEOM). The RDLEOM signal is available on this output when RFDL is enabled. RDLEOM goes high when the last byte of a received sequence is read from the RFDL FIFO buffer, or when the FIFO buffer is overrun.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
BRPCM/	Output	46	48	Backplane Receive PCM (BRPCM). The BRPCM signal is available on this output when the backplane is configured for single-rail output. BRPCM contains the recovered data stream passed through ELST and the SIGX. When the ELST is not by-passed, the BRPCM stream is aligned to the backplane timing and is updated on the falling edge of BRCLK. When the ELST is by-passed, BRPCM is aligned to the receive line timing and is updated on the falling edge of RCLKO.
BRDP				Backplane Receive Positive Line Pulse (BRDP). The BRDP signal is available on this output when the backplane is configured for dual-rail output. The BRDP NRZ output represents the RZ receive digital positive pulse signal extracted from the input bipolar signal. BRDP is updated on the falling edge of RCLKO.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
BRSIG/	Output	45	47	Backplane Receive Signalling (BRSIG). The BRSIG signal is available on this output when the backplane is configured for single-rail output. BRSIG contains the extracted signalling bits for each timeslot in the frame, repeated for the entire signalling multiframe. Each timeslot's signalling bits are valid in bit locations 5,6,7,8 of the timeslot and are timeslot-aligned with the BRPCM data stream. When the ELST is not by-passed, the BRSIG stream is aligned to the backplane timing and is updated on the falling edge of BRCLK. When the ELST is by-passed, BRSIG is aligned to the receive line timing and is updated on the falling edge of RCLKO.
BRDN				Backplane Receive Negative Line Pulse (BRDN). The BRDN signal is available on this output when the backplane is configured for dual-rail output. The BRDN NRZ output represents the RZ receive digital negative pulse signal extracted from the input bipolar signal. BRDN is updated on the falling edge of RCLKO.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
BRFPO	Output	47	49	Backplane Frame Pulse Output (BRFPO). When the E1XC is configured for backplane receive frame pulse output, BRFPO pulses high for 1 BRCLK cycle (or 1 RCLKO cycle if ELST is by-passed) during bit 1 of each 256-bit frame, indicating the frame alignment of the BRPCM data stream. When configured for backplane receive signalling multiframe output, BRFPO pulses high for 1 BRCLK cycle (or 1 RCLKO cycle if ELST is by-passed) during bit 1 of frame 1 of the 16 frame signalling multiframe, indicating the signalling multiframe alignment of the BRPCM data stream. (Even when signalling multiframing is disabled, the BRFPO output continues to indicate every 16th frame.) When configured for backplane receive CRC multiframe output, BRFPO pulses high for 1 BRCLK cycle (or 1 RCLKO cycle if ELST is by-passed) during bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM data stream. (Even when CRC multiframing is disabled, the BRFPO output continues to indicate the position of bit 1 of the FAS frame every 16th frame.)

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
BRFPO	Output	47	49	When configured for backplane receive composite multiframe output, BRFPO goes high on the falling BRCLK edge (or RCLKO edge if ELST is by-passed) marking the beginning of bit 1 of frame 1 of every 16 frame signalling multiframe, indicating the signalling multiframe alignment of the BRPCM data stream, and returns low on the falling BRCLK edge (or RCLKO edge if ELST is by-passed) marking the end of bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM data stream. This mode allows both multiframe alignments to be decoded externally from the single BRFPO signal. If the signalling and CRC multiframe alignments are coincident, BRFPO will pulse high for 1 clock cycle. When configured for backplane receive overhead output, BRFPO is high for timeslot 0 and timeslot 16 of each 256-bit frame, indicating the overhead bit positions of the BRPCM data stream. BRFPO is updated on the falling edge of BRCLK or RCLKO.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
BRCLK	Input	32	37	Backplane Receive Clock (BRCLK). This clock should be 2.048MHz with optional gapping for adaptation to non-uniform backplane data streams. The E1XC may be configured to ignore the BRCLK input and use the RCLKO signal in its place when the ELST is bypassed.
BRFPI	Input	31	36	Backplane Frame Pulse Input (BRFPI). This input is used to frame align the received data to the system backplane. A pulse at least 1 BRCLK cycle wide must be provided on BRFPI at multiples of 256 bit periods. BRFPI is sampled on the rising edge of BRCLK.
BTPCM/	Input	77	8	Backplane Transmit PCM (BTPCM). When the backplane is configured for single-rail input, the BTPCM inputs the data stream to be transmitted, and is sampled on the rising edge of BTCLK.
BTDP				Backplane Transmit Positive Line Pulse (BTDP). When the backplane is configured for dual-rail input, the BTDP input by-passes the transmitter and is fed directly into the DJAT. BTDP is sampled on the rising edge of BTCLK.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
BTSIG/	Input	76	7	Backplane Transmit Signalling (BTSIG). When the backplane is configured for single-rail input, the BTSIG input signal contains the signalling bits for each timeslot in the transmit data frame, repeated for the entire signalling multiframe. Each timeslot's signalling bits are in bit locations 5,6,7,8 of the timeslot and are timeslot-aligned with the BTPCM data stream. BTSIG is sampled on the rising edge of BTCLK.
BTDN				Backplane Transmit Negative Line Pulse (BTDN). When the backplane is configured for dual-rail input, the BTDN input by-passes the transmitter and is fed directly into the DJAT. BTDN is sampled on the rising edge of BTCLK.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
BTFP	Input	75	6	Backplane Transmit Frame Pulse (BTFP). This input is used to frame align the transmitter to the system backplane. If basic frame alignment only is required, a pulse at least 1 BTCLK cycle wide must be provided on BTFP at multiples of 256 bit periods. If multiframe alignment is required, transmit multiframe alignment must be enabled, and BTFP must be brought high to mark bit 1 of frame 1 of every 16 frame signalling multiframe and brought low following bit 1 of frame 1 of every 16 frame CRC multiframe. This mode allows both multiframe alignments to be independently controlled using the single BTFP signal. Note that if the signalling and CRC multiframe alignments are coincident, BTFP must pulse high for 1 BTCLK cycle every 16 frames.
BTCLK	Input	74	5	Backplane Transmit Clock (BTCLK). This clock should be 2.048MHz with optional gapping for adaptation from non-uniform backplane data streams. The E1XC may be configured to ignore the BTCLK input and use the RCLKO signal in its place.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
TDLSIG/	I/O	66	65	Transmit Data Link Signal (TDLSIG). The TDLSIG signal is input on this pin when the internal HDLC transmitter (XFDL) is disabled from use. TDLSIG is the source for the data stream to be inserted into the selected data link bits. The E1XC may be configured to utilize timeslot 16 as a data link or utilize any combination of the national bits as a data link. TDLSIG is sampled on the rising edge of TDLCLK.
TDLINT				Transmit Data Link Interrupt (TDLINT). The TDLINT signal is output on this pin when XFDL is enabled. TDLINT goes high when the last data byte written to the XFDL has been set up for transmission and processor intervention is required to either write control information to end the message, or to provide more data.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
TDLCLK/	Output	67	66	Transmit Data Link Clock (TDLCLK). The TDLCLK signal is available on this output when the internal HDLC transmitter (XFDL) is disabled from use. The rising edge of TDLCLK is used to sample the data stream contained on the TDLSIG input. When the E1XC is not configured to insert a data link, the TDLCLK output is held low.
TDLUDR				Transmit Data Link Underrun (TDLUDR). The TDLUDR signal is available on this output when XFDL is enabled. TDLUDR goes high when the processor has failed to service the TDLINT interrupt before the transmit buffer is emptied.
TCLKO	Output	72	3	Transmit Clock Output (TCLKO). The TDP, TDN, and TDD outputs may be enabled to be updated on the rising or falling edge of TCLKO. The TAP and TAN outputs are also driven with timing derived from TCLKO. TCLKO is a 2.048 MHz clock that is adequately jitter and wander free in absolute terms to permit an acceptable G.703 2048 kbit/s signal to be generated. Depending on the configuration of the E1XC, TCLKO may be derived from TCLKI, RCLKO, or BTCLK, with or without jitter attenuation.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
TDP/	Output	71	2	Transmit Digital Positive Line Pulse (TDP). This signal is available on the output when the E1XC is configured to transmit dual-rail data. The TDP signal can be formatted for either RZ or NRZ waveforms, and can be enabled to be updated on the rising or falling edge of TCLKO.
TDD				Transmit Digital Data (TDD). This signal is available on the output when configured to transmit single-rail data. The TDD signal may be enabled to be updated on the rising or falling edge of TCLKO.
TDN/	Output	68	67	Transmit Digital Negative Line Pulse (TDN). This signal is available on the output when the E1XC is configured to transmit dual-rail data. The TDN signal can be formatted for either RZ or NRZ waveforms, and can be enabled to be updated on the rising or falling edge of TCLKO.
TFLG				Transmit FIFO Flag (TFLG). This signal is available when configured to transmit single-rail data. The TFLG output indicates when the transmit rate conversion FIFO in DJAT is nearing an empty or a full condition. Either indication may be selected. This output may be enabled to be updated on the rising or falling edge of TCLKO.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
TAP	Output	56	58	Transmit Analog Positive Pulse (TAP). This analog output drives an AC signal through an external matching transformer. It is connected to the positive lead of the transformer primary. An analog Transmit Monitor Positive point is internally bonded to this output and is used to monitor the positive pulses on the transmit line.
TAN	Output	63	62	Transmit Analog Negative Pulse (TAN). This analog output drives an AC signal through an external matching transformer. It is connected to the negative lead of the transformer primary. An analog Transmit Monitor Negative point is internally bonded to this output and is used to monitor the negative pulses on the transmit line.
TC	I/O	57	59	Transmit Reference Decoupling Capacitor (TC). This analog bidirectional provides decoupling for an internal reference generator. It is connected to a decoupling capacitor to TAVD.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
TAVD	Power	64	63	Transmit Analog Power (TAVD). This pin provides the +5 V supply to the transmit analog line interface. Even if the transmit analog line interface is not used, a +5 V supply must be provided. The transmit analog line interface remains in a low power consumption state after reset until enabled. TAVD must be connected to a common, well decoupled +5 VDC supply together with the VDDO[3:0] and VDDI[1:0] pins. Care must be taken to avoid coupling noise induced on the VDDO and VDDI pins into the TAVD pin.
TAVS	Ground	65	64	Transmit Analog Ground (TAVS). This pin provides the ground supply to the transmit analog line interface. TAVS must be connected to a common ground together with the VSSO[3:0] and VSSI[1:0] pins. Care must be taken to avoid coupling noise induced on the VSSO and VSSI pins into the TAVS pin.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
TCLKI	Input	73	4	Transmit Clock Input (TCLKI). This input signal is used to generate the TCLKO clock signal. Depending upon the configuration of the E1XC, TCLKO may be derived directly from TCLKI by dividing TCLKI by 8, or TCLKO may be derived from TCLKI after jitter attenuation and frequency multiplication (default is a frequency ratio of one). If TCLKI is jitter-free when divided down to 8 kHz, then it is possible to derive TCLKO from TCLKI when TCLKI is a multiple of 8 kHz (i.e. Nx8 kHz, for N equals 1 to 256). The E1XC may be configured to ignore the TCLKI input and utilize BTCLK or RCLKO instead. RCLKO is also substituted for TCLKI if line loopback is enabled.
XCLK/	Input	78	9	Crystal Clock Input (XCLK). This signal provides timing for many portions of the E1XC. Depending on the configuration of the E1XC, XCLK is nominally a 49.152 MHz or 16.384 MHz, 50% duty cycle clock. When transmit clock generation or jitter attenuation is not required, XCLK may be driven with a 16.384 MHz clock. When transmit clock generation or jitter attenuation are required, XCLK must be driven with a 49.152 MHz clock.
VCLK				Vector Clock (VCLK). The VCLK signal is used during E1XC production test to verify internal functionality.

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
INTB	Output	4	12	Active low open-drain Interrupt signal (INTB). This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources, including the internal HDLC transceiver. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.
CSB	Input	2	10	Active low chip select (CSB). This signal must be low to enable E1XC register accesses. Note that when not being used, CSB must be tied high. If CSB is not required (i.e. register accesses are controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input. In any case, CSB must be high at least once after a powerup in order to clear internal test modes.
D[0]	I/O	5	13	Bidirectional data bus (D[7:0]). This bus is used during E1XC read and write accesses.
D[1]		6	14	
D[2]		7	15	
D[3]		8	16	
D[4]		13	21	
D[5]		14	22	
D[6]		15	23	
D[7]		16	24	

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
RDB	Input	17	25	Active low read enable (RDB). This signal is pulsed low to enable a E1XC register read access. The E1XC drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
WRB	Input	18	26	Active low write strobe (WRB). This signal is pulsed low to enable a E1XC register write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB while CSB is low.
ALE	Input	30	35	Address latch enable (ALE). This signal latches the address bus, A[7:0], when low. This allows the E1XC to be interfaced to a multiplexed address/data bus. When ALE is high, the address latches are transparent.
RSTB	Input	3	11	Active low reset (RSTB). This signal asynchronously resets the E1XC.
A[0]	Input	22	27	Address bus (A[7:0]). This bus selects specific registers during E1XC register accesses.
A[1]		23	28	
A[2]		24	29	
A[3]		25	30	
A[4]		26	31	
A[5]		27	32	
A[6]		28	33	
A[7]		29	34	

Pin Name	Type	Pin No.		Function
		PQFP	PLCC	
VDDO[0] VDDO[1] VDDO[2] VDDO[3]	Power	69 12 42 62	68 20 44 61	Pad ring power pins (VDDO[3:0]). These pins must be connected to a common, well decoupled +5 VDC supply together with the VDDI[1:0] pins. Care must be taken to avoid coupling noise induced on the VDDO pins into the VDDI pins.
VDDI[0] VDDI[1]	Power	11 49	19 51	Core power pins (VDDI[1:0]). These pins must be connected to a common, well decoupled +5 VDC supply together with the VDDO[3:0] pins.
VSSO[0] VSSO[1] VSSO[2] VSSO[3]	Ground	70 9 38 58	1 17 43 60	Pad ring ground pins (VSSO[3:0]). These pins must be connected to a common ground together with the VSSI[1:0] pins. Care must be taken to avoid coupling noise induced on the VSSO pins into the VSSI pins.
VSSI[0] VSSI[1]	Ground	10 50	18 52	Core ground pins (VSSI[1:0]). These pins must be connected to a common ground together with the VSSO[3:0] pins.

Notes on Pin Description:

1. VDDI and VSSI are the +5 V and ground connections, respectively, for the core circuitry of the device. VDDO and VSSI are the +5 V and ground connections, respectively, for the pad ring circuitry of the device. TAVD and TAVS are the +5 V and ground connections, respectively, for the transmit analog circuitry of the device. These power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate. There is no low impedance connection within the PM6341 between the core, pad ring, and transmit analog supply rails. Failure to properly make these connections may result in improper operation or damage to the device. Care must be taken to avoid coupling of noise into the transmit analog supply rails.

2. RAVD and RAVS are the +5 V and ground connections, respectively, for the receive analog circuitry of the device. These power supply connections need

only be used if the receive analog function is desired and should then connect to a common +5 V or ground rail, as appropriate, with the core, pad ring, and transmit analog supply rails. There is no low impedance connection within the PM6341 between the receive analog supply rail and other supply rails. When the receive analog function is not desired, RAVD should be connected to RAVS. Care must be taken to avoid coupling of noise into the receive analog supply rails.

3. Inputs RSTB and ALE have integral pull-up resistors.

4. The TDLSIG/TDLINT pin has an integral pull-up resistor and defaults to being an input after a reset.

9 FUNCTIONAL DESCRIPTION

9.1 Digital Receive Interface (DRIF)

The Digital Receive Interface provides control over the various input options available on the multifunctional digital receive pins RDP/RDD/SDP and RDN/RLCV/SDN. When configured for dual-rail input, the multifunctional pins become the RDP and RDN inputs. These inputs can be enabled to receive either return-to-zero (RZ) or non-return-to-zero (NRZ) signals; the NRZ input signals can be sampled on either the rising or falling edge of RCLKI. When the interface is configured for single-rail input, the multifunctional pins become the RDD and RLCV inputs, which can be sampled on either the rising or falling RCLKI edge. Finally, when the analog interface is used, the multifunction pins become the SDP and SDN outputs, indicating the sliced pulses corresponding to the received positive and negative analog line pulses.

9.2 Analog Pulse Slicer (RSLC)

The Analog E1 Pulse Slicer function is provided by the RSLC block. The Receive Data Slicer (RSLC) block provides the first stage of signal conditioning for a G.703 2048 kbit/s serial data stream by converting bipolar line signals to dual rail RZ pulses. Before an RZ output pulse is generated by the RSLC block, bipolar input signals must rise to 50% (for G.703 2048 kbit/s) of their peak amplitude. This level is referred to as the Slicing Level. The threshold criteria insures accurate pulse or mark recognition in the presence of noise.

The RSLC block provides a squelch alarm, which occurs when input pulses are below the squelching level threshold. In this state, data is not sliced, which prevents the detection of noise on an idle transmission line. The SQ status bit in register 5DH goes high whenever the RSLC block is squelching the input signal. The RSLC can be configured (in register 5DH) to generate an interrupt whenever the SQ status bit goes high.

The RSLC block relies on an external network for compliance to G.703 120 Ω twisted pair or G.703 75 Ω coax. The RSLC block is configured via an off-chip attenuator pad (see Figure 5). The following network values are recommended for the two intended applications:

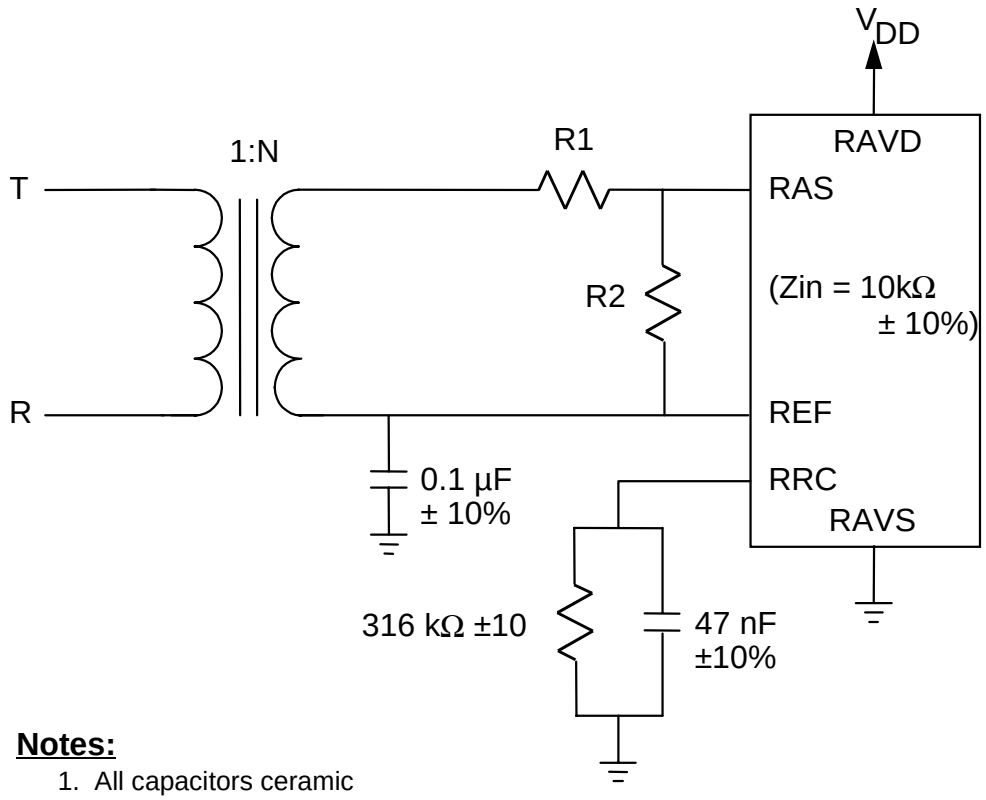
Table 1 - Recommended Rx Network Values

Signal Type	Turns Ratio (N ± 5%)	R1 (Ω ± 1%)	R2 (Ω ± 1%)	Squelch Level on the Primary
G.703				
Zo = 120Ω	1:2	357	121	276 mV ± 20%
Zo = 75Ω	1:2	205	95.3	220 mV ± 20%

Tight tolerances are required on the resistors and turns ratio to meet the return loss specification.

For details on how these values were determined, refer to the section entitled "Interfacing to the Analog Pulse Slicer" in the "Operation" section of this databook.

Figure 5 - External Analog Receive Interface Circuit



Notes:

1. All capacitors ceramic
2. Recommended Transformers:

   BH Electronics 500-1775 (1:1:1);
   Pulse Engineering PE 64931 (1:1:1); or
   Pulse Engineering PE 65341 (1:1:1) (for extended temp range)

3. Alternatively, a dual part containing both the 1:2CT & 1:1.36 transformers can be used, i.e.:

   BH Electronics 500-1777;
   Pulse Engineering PE64952; or
   Pulse Engineering PE65774 (for extended temp range)

The RSLC block can be disabled by strapping the receive analog power pin, RAVD to ground. When RLSC is disabled, the E1XC accepts RZ input pulses on the RDP/RDD and RDN/RLCV pins.

9.3 Clock and Data Recovery (CDRC)

The Clock and Data Recovery function is provided by a Data and Clock Recovery (CDRC) block that provides clock and PCM data recovery, HDB3 decoding, bipolar violation detection, and loss of signal detection. The CDRC block recovers the clock from the incoming RZ data pulses using a digital phase-

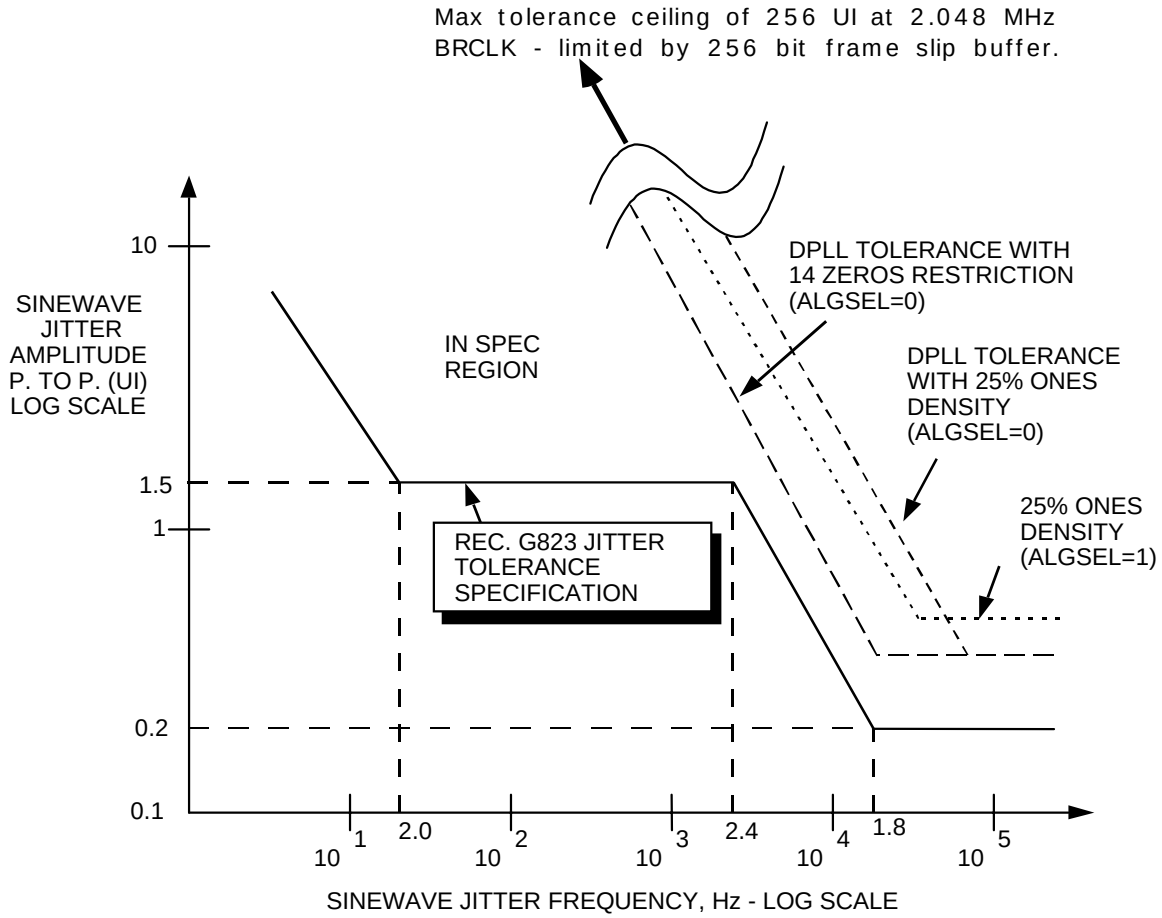
locked-loop and recovers the NRZ data. Loss of signal is indicated after exceeding a programmed threshold of 10, 31, 63 or 175 consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is cleared after the occurrence of a single line pulse. An alternate loss of signal indication is provided which is cleared only after 255 bit periods during which no sequence of four consecutive zeros has been received. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns.

The HDB3 decoding is summarized as follows: If a bipolar violation (BPV) preceded by two zeros is received, the violation and the preceding three bit periods are decoded as four zeros. If AMI line code is selected, no substitution is made.

If HDB3 line code is selected, a line code violation is declared if any bipolar violation is of the same polarity as the previous BPV or if the BPV is not preceded by two spaces (the second criteria is maskable). If AMI line code is selected, all bipolar violations are counted as line code violations.

The input jitter tolerance of CDRC complies with ITU-T Recommendation G.823.

Figure 6 - CDRC Jitter Tolerance



9.4 Framer (FRMR)

The Framer (FRMR) block searches for frame alignment, CRC multiframe alignment, and channel associated signalling (CAS) multiframe alignment in the incoming recovered PCM stream.

Once the FRMR has found basic (or FAS) frame alignment, the incoming PCM data is continuously monitored for FAS/NFAS framing bit errors. Framing bit errors are accumulated in the framing bit error counter contained in the PMON block. Once the FRMR has found CAS multiframe alignment, the PCM data is continuously monitored for CAS multiframe alignment pattern errors. Once the FRMR has found CRC multiframe alignment, the PCM data is continuously monitored for CRC multiframe alignment pattern errors, and CRC-4 errors. The FRMR also detects and indicates loss of frame, loss of CAS multiframe, and loss

of CRC multiframe, based on user-selectable criteria. The reframe operation can be initiated by software (via the FRMR Frame Alignment Options Register), by excessive CRC errors, or when CRC multiframe alignment is not found within 8 ms. The FRMR also identifies the position of the frame, the CAS multiframe, and the CRC multiframe.

The FRMR extracts timeslot 16 for optional use as a data link and also extracts the contents of the International bits (from both the FAS frames and the NFAS frames), the National bits, and the Extra bits (from timeslot 16 of frame 0 of the CAS multiframe), and stores them in the FRMR International/National Bits Register, and the FRMR Extra Bits Register respectively.

The FRMR identifies the raw bit values for the remote (or distant frame) alarm (bit 3 in timeslot 0 of NFAS frames) and the remote signalling multiframe (or distant multiframe) alarm (bit 6 of timeslot 16 of frame 0 of the CAS multiframe) via the FRMR International/National Bits Register, and the FRMR Extra Bits Register respectively. Access is also provided to the "debounced" remote alarm and remote signalling multiframe alarm bits which are set when the corresponding signals have been a logic 1 for 2 or 3 consecutive occurrences, as per Recommendation O.162. Detection of AIS and timeslot 16 AIS are provided; AIS is also integrated and an AIS Alarm is indicated if the AIS condition has persisted for at least 100 ms. The out of frame (OOF=1) condition is also integrated, indicating a red Alarm if the OOF condition has persisted for at least 100 ms.

An interrupt may be generated to signal a change in the state of any status bits (OOF, OOSMF, OOCMF, AIS, or RED), and to signal when any event (RRA, RRMA, AISD, T16AISD, COFA, FER, SMFER, CMFER, CRCE, or FEBE) has occurred.

9.4.1 Frame Find

The Frame Find Block searches for frame alignment using one of two user-selectable algorithms, as defined in Recommendation G.706. Optionally, a two frame check sequence can be added to either algorithm to provide protection against false frame alignment in the presence of random mimic patterns.

The first algorithm finds frame alignment by using the following sequence:

1. Search for the presence of the correct 7-bit FAS;

2. Check that the FAS is absent in the following frame by verifying that bit 2 of the assumed timeslot 0 byte is a logic 1;

3. Check that the correct 7-bit FAS is present in the assumed timeslot 0 byte of the next frame.

If either of the conditions in steps 2 or 3 are not met, a new search for frame alignment is initiated in the bit immediately following the errored timeslot 0 byte location.

The second algorithm is similar to the first, but adds a one frame "hold-off" in step 2 to begin a new search in the bit immediately following the second 7-bit FAS that is checked. This "hold-off" is performed only the condition in step 2 fails, providing a more robust algorithm which allows the framer to operate correctly in the presence of fixed timeslot data imitating the FAS pattern.

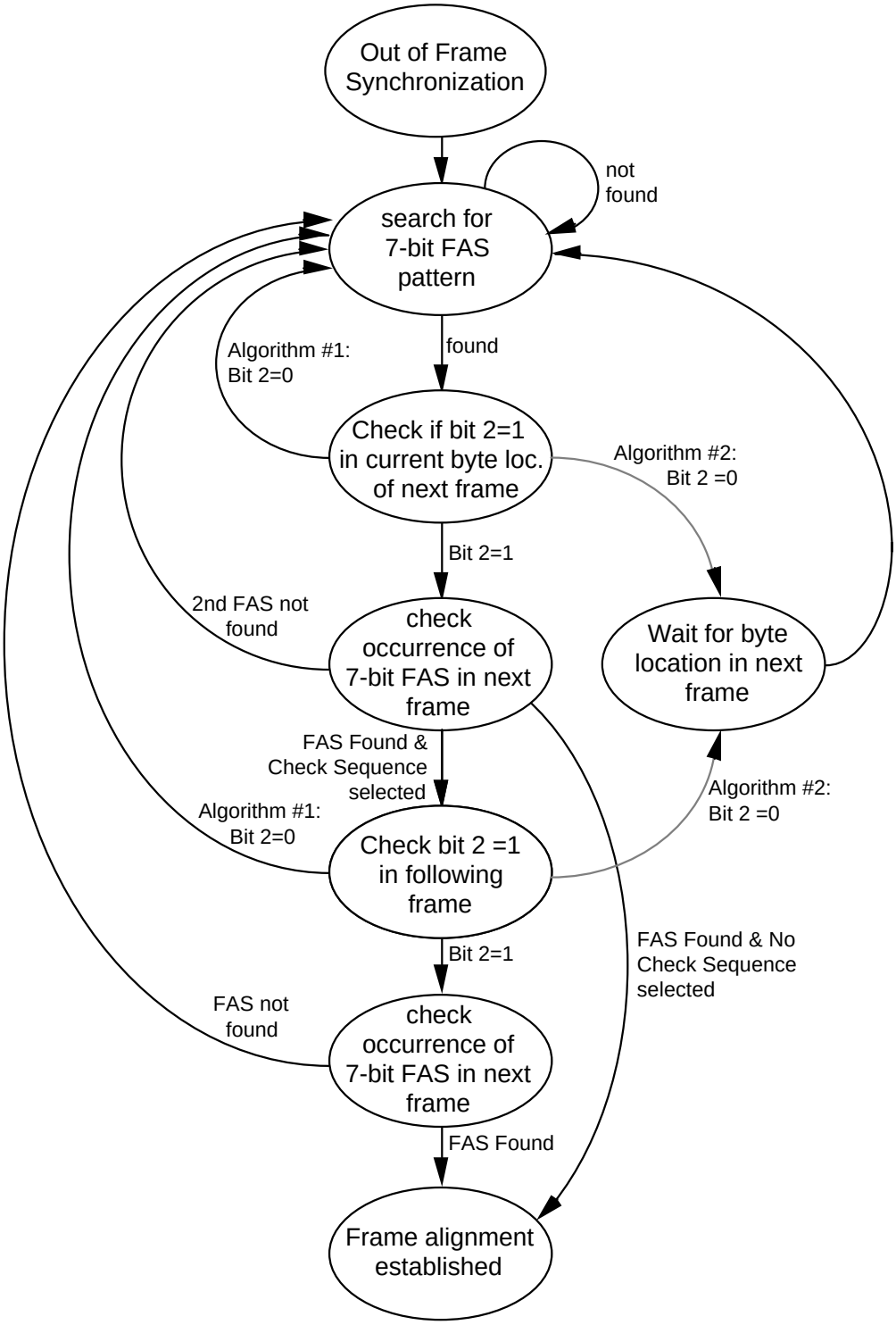
A check sequence can be added to either algorithm to verify correct frame alignment in the presence of random imitative FASs. Note that this check sequence should be enabled when monitoring an unframed 2^{15} -1 pseudo random sequence to avoid framing to the single mimic framing pattern contained in the sequence. The check consists of verifying correct frame alignment for an additional two frames, as follows:

- once frame alignment (in frame "n") is determined, check that the FAS is absent in the following frame (frame "n+1") by verifying that bit 2 of timeslot 0 is a logic 1;
- then, check that the correct 7-bit FAS is present in timeslot 0 of the next frame (frame "n+2").

If either of the two conditions in the check sequence are not met, a new search for frame alignment is initiated in the bit immediately following the errored byte location when using the first algorithm, and is initiated in the bit immediately following the byte location in frame "n+2" when using the second algorithm.

These algorithms are illustrated in Figure 7.

Figure 7 - Basic Framing Algorithm Flowchart



These algorithms provide robust framing operation even in the presence of random bit errors: framing with algorithm #1 or #2 provides a 99.98% probability of finding frame alignment within 1 ms in the presence of 10^{-3} bit error rate and no mimic patterns.

Once frame alignment is found, the block sets the OOF indication low, indicates a change of frame alignment (if it occurred), and monitors the frame alignment signal, indicating errors occurring in the 7-bit FAS pattern and in bit 2 of NFAS frames, and indicating the debounced value of the Remote Alarm bit (bit 3 of NFAS frames). Using debounce, the Remote Alarm bit has <0.00001% probability of being falsely indicated in the presence of a 10^{-3} bit error rate. The block declares loss of frame alignment if 3 or 4 consecutive FASs have been received in error or, additionally, if bit 2 of NFAS frames has been in error for 3 consecutive occasions. In the presence of a random 10^{-3} bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of >12 minutes.

The Frame Find Block can be forced to initiate a frame search at any time when any of the following conditions are met:

- the software re-frame bit in the Frame Alignment Options Register goes to logic 1;
- the CRC Frame Find Block is unable to find CRC multiframe alignment; or
- the CRC Frame Find Block accumulates excessive CRC evaluation errors (= 915 CRC errors in 1 second) and is enabled to force a re-frame.

9.4.2 CRC Frame Find

Once the basic frame alignment has been found, the CRC Frame Find Block searches for CRC multiframe alignment by observing whether the International bits (bit 1 of timeslot 0) of NFAS frames follow the CRC multiframe alignment pattern. Multiframe alignment is declared if at least two valid CRC multiframe alignment signals are observed within 8 ms, with the time separating two alignment signals being a multiple of 2 ms.

Once CRC multiframe alignment is found, the block sets the OOCMF indication low, and monitors the multiframe alignment signal, indicating errors occurring in the 6-bit pattern, and indicating the value of the FEBE bits (bit 1 of frames 13 and 15 of the multiframe).The block declares loss of CRC multiframe alignment if four consecutive CRC multiframe alignment signals have been received in error, or if frame alignment has been lost.

The CRC Frame Find Block will force the Frame Find Block to initiate a basic frame search when CRC multiframe alignment has not been found for 8 ms.

9.4.3 CRC Check and AIS Detection

The CRC Check and AIS Detect Block computes the 4-bit CRC checksum for each incoming sub-multiframe and compares this 4-bit result to the received CRC remainder bits in the subsequent sub-multiframe. The block also accumulates CRC errors over 1 second intervals, monitoring for excessive CRC errors and optionally, forcing the Frame Find Block to initiate a frame search when ≥ 915 CRC errors occur in 1 second. The number of CRC errors accumulated during the previous second is available by reading the FRMR CRC Error Counter Registers.

The block also detects the occurrence of an unframed all-ones receive data stream, indicating the AIS by setting the AISD indication when less than 3 zero bits are received in 2 frames (512 consecutive bits); the AISD indication is reset when 3 or more zeros in the E1 stream are observed, or when frame alignment is found.

9.4.4 Signalling Frame Find

Once the basic frame alignment has been found, the Signalling Frame Find Block searches for CAS multiframe alignment using one of two user-selectable algorithms, one of which is compatible with Recommendation G.732. Once frame alignment has been found, the first algorithm monitors timeslot 16 of each frame; it declares CAS multiframe alignment when 15 consecutive frames with bits 1-4 of timeslot 16 not containing the alignment pattern are observed to precede a frame with timeslot 16 containing the correct alignment pattern. The second algorithm, compatible with G.732, also monitors timeslot 16 of each frame, and declares CAS multiframe alignment when non-zero bits 1-4 of timeslot 16 are observed to precede a timeslot 16 containing the correct alignment pattern.

Once CAS multiframe alignment has been found, the block sets the OOSMF indication to logic 0, and monitors the CAS multiframe alignment signal, indicating errors occurring in the 4-bit pattern, and indicating the debounced value of the remote signalling multiframe alarm bit (bit 6 of timeslot 16 of frame 0 of the multiframe). Using debounce, the remote signalling multiframe alarm bit has

< 0.00001% probability of being falsely indicated in the presence of a 10^{-3} bit error rate. This block also indicates the reception of timeslot 16 AIS when timeslot 16 has been all-ones for two consecutive frames while out of CAS multiframe. The block declares loss of CAS multiframe alignment if two consecutive CAS multiframe alignment signals have been received in error, or

additionally, if all the bits in timeslot 16 are logic 0 for 1 or 2 (selectable) CAS multiframes. Loss of CAS multiframe alignment is also declared if frame alignment has been lost.

9.4.5 Alarm Integration

The Alarm Integrator Block monitors the OOF and the AIS indications, verifying that each condition has persisted for 104 ms (±6 ms) before indicating the alarm condition. The alarm is removed when the condition has been absent for 104 ms (±6 ms).

The AIS alarm algorithm accumulates the occurrences of AISD (AIS detection). AISD is defined as an unframed pattern with less than 3 zeros in two consecutive frame times (512 bits). The Alarm Integrator Block counts the occurrences of AISD over a 4 ms interval and indicates a valid AIS presence when 13 or more AISD indications (of a possible 16) have been received. Each interval with a valid AIS presence indication increments an interval counter which declares AIS Alarm when 25 valid intervals have been accumulated. An interval with no valid AIS presence indication decrements the interval counter; the AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.8% probability of declaring an AIS Alarm within 104 ms in the presence of a 10^{-3} mean bit error rate.

The TS16 AIS alarm algorithm accumulates the occurrences of T16AISD (TS16 AIS detection). T16AISD is defined as two consecutive all ones time slot 16 bytes while out of signalling multiframe. Each interval with a valid TS16 AIS presence indication increments an interval counter which declares TS16 AIS Alarm when 22 valid intervals have been accumulated. An interval with no valid TS16 AIS presence indication decrements the interval counter; the TS16 AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.1% probability of declaring an TS16 AIS Alarm within 3.1 ms after loss of signalling multiframe detection in the presence of a 10^{-3} mean bit error rate.

The red alarm algorithm monitors occurrences of OOF over a 4 ms interval, indicating a valid OOF interval when one or more OOF indications occurred during the interval, and indicating a valid in frame (INF) interval when no OOF indication occurred for the entire interval. Each interval with a valid OOF indication increments an interval counter which declares RED Alarm when 25 valid intervals have been accumulated. An interval with valid INF indication decrements the interval counter; the RED Alarm declaration is removed when the counter reaches 0. This algorithm biases OOF occurrences, leading to declaration of red alarm when intermittent loss of frame alignment occurs.

9.5 Performance Monitor Counters (PMON)

The Performance Monitor Counters function is provided by the Performance Monitor (PMON) block that accumulates CRC error events, frame synchronization bit error events, line code violation events, and far end block error events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second). When the transfer clock signal is applied, the PMON block transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If enabled, an interrupt is generated whenever counter data is transferred into the holding registers. If the holding registers are not read between successive transfer clocks, an OVERRUN register bit is asserted.

Generation of the transfer clock within the E1XC chip is performed by writing to any counter register location. The holding register addresses are contiguous to facilitate polling operations.

9.6 HDLC Receiver (RFDL)

The HDLC Receiver function is provided by the RFDL block. The RFDL is a microprocessor peripheral used to receive LAPD/HDLC frames on either Time Slot 16 or the National use bits of Time Slot 0.

The RFDL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives frame data, and calculates the CRC Q.921 frame check sequence (FCS).

Received data is placed into a 4-level FIFO buffer. The Status Register contains bits which indicate overrun, end of message, flag detected, and buffered data available.

On end of message, the Status Register also indicates the FCS status and the number of valid bits in the final data byte. Interrupts are generated when one, two or three bytes (programmable via the RFDL configuration register) are stored in the FIFO buffer. Interrupts are also generated when the terminating flag sequence, abort sequence, or FIFO buffer overrun are detected.

When the internal HDLC receiver is disabled, the serial data extracted by the FRMR TSB is output on the RDLSIG pin updated on the falling clock edge of the RDLCLK pin.

9.7 Elastic Store (ELST)

The Elastic Store function is provided by the ELST block.

The Elastic Store (ELST) block synchronizes incoming PCM frames to the local backplane clock, BRCLK. The frame data is buffered in a two frame circular data buffer. Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer.

When the backplane timing is derived from the receive line data (i.e. the RCLKO output is used), the elastic store can be bypassed to eliminate the 2 frame delay. In this configuration the elastic store can be used to measure frequency differences between the recovered line clock and another 2.048 MHz clock applied to the BRCLK input. A typical example might be to measure the difference in frequency between two received T1 streams (i.e. East-West frequency difference) by monitoring the number of SLIP occurrences of one direction with respect to the other.

When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane clock, the write pointer will catch up to the read pointer and the buffer will be filled. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The following frame of PCM data will be deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane clock, the read pointer will catch up to the write pointer and the buffer will be empty. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The last frame which was read will be repeated.

A slip operation is always performed on a frame boundary.

To allow for the extraction of signalling information in the PCM data timeslots, multiframe identification is also passed through the ELST.

9.8 Signalling Extractor (SIGX)

The Signalling Extraction function is provided by the Signalling Extractor (SIGX) block. The TSB provides channel associated signalling (CAS) extraction from an E1 signalling multiframe. Signalling data is extracted from timeslot (TS) 16 of each frame within a signalling multiframe and buffered. The SIGX selectively debounces the bits, and serializes the results onto the 2048 kbit/s serial stream BRSIG output. Buffered signalling data is aligned with its associated voice

timeslot in the E1 frame and output in PMC format. Both the output data stream and the output signalling stream are compatible with the TRAN E1 Transmitter block.

The SIGX provides user control over signalling freezing with a 95% confidence level of freezing with valid signalling data for a 50% ones density out-of-frame condition. The SIGX also provides control over timeslot data inversion, trunk conditioning, and signalling debounce on a per-timeslot basis directly, via the Common Bus Interface (CBI).

9.9 Backplane Receive Interface (BRIF)

The Backplane Receive Interface allows data to be presented to a backplane in a 2048 kbit/s serial stream, allows BPV transparency by outputting dual-rail data at 2048 kbit/s, and allows access to the recovered PCM stream (either the HDB3 decoded stream, or the undecoded stream) at 2048 kbit/s.

The block generates the output data stream on the BRPCM pin containing 32 timeslot bytes of data. The BRSIG output pin contains 30 bytes of signalling nibble data located in the least significant nibble of each byte. The framing alignment indication on the BRFPO pin can be configured to indicate the first bit of each 256-bit frame, the first bit of the first frame of the CRC multiframe, the first bit of the first frame of the signalling multiframe or all overhead bits.

9.10 Transmitter (TRAN)

The Transmitter function is provided by the TRAN block.

The TRAN generates a 2048 kbit/s data stream according to ITU-T recommendations, providing individual enables for frame generation, CRC multiframe generation, and channel associated signalling (CAS) multiframe generation.

In concert with Transmit Per-Channel Serial Controller (TPSC), the TRAN block provides per-timeslot control of idle code substitution, data inversion, digital milliwatt substitution, selection of the signalling source and CAS data. All timeslots can be forced into a trunk conditioning state (idle code substitution and signalling substitution) by use of the master trunk conditioning bit in the Configuration Register.

Common Channel Signalling (CCS) is supported in time slot 16 either through the internal HDLC Transmitter (XFDL) or through a serial data input and clock

output. Support is provided for the transmission of AIS and TS16 AIS, and the transmission of remote alarm and remote multiframe alarm signals.

PCM output signals may be selected to conform to HDB3 or AMI line coding.

9.11 Transmit Per-channel Serial Controller (TPSC)

The Transmit Per-channel Serial Controller allows data and signalling trunk conditioning or idle code to be applied on the transmit E-1 stream on a per-timeslot basis. It also allows per-timeslot control of data inversion and application of digital milliwatt.

The Transmit Per-channel Serial Controller function is provided by a Per-Channel Serial Controller (PCSC) block. The TPSC interfaces directly to the TRAN block and provides serial streams for signalling control, idle code data and PCM data control.

The registers are accessible from the µP interface in an indirect address mode. The BUSY indication signal can be polled from an internal status register to check for completion of the current operation.

9.12 HDLC Transmitter (XFDL)

The HDLC Transmitter function is provided by the XFDL block. The XFDL is designed to provide a serial data link for the TRAN E1 Transmitter block. The XFDL is used under microprocessor or DMA control to transmit HDLC data frames in Time Slot 16 or in the Time Slot 0 National Use bits when the E1XC is enabled to use the internal HDLC transmitter. The XFDL performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, idle, and abort sequence insertion. Data to be transmitted is provided on an interrupt-driven basis by writing to a double-buffered transmit data register. Upon completion of the frames, a CRC Q.921 frame check sequence is transmitted, followed by idle flag sequences. If the transmit data register underflows, an abort sequence is automatically transmitted.

When enabled for use (via the EN bit in the XFDL Configuration register), the XFDL continuously transmits the flag character (01111110). Data bytes to be transmitted are written into the Transmit Data Register. After the parallel-to-serial conversion of each data byte, an interrupt is generated to signal the controller to write the next byte into the Transmit Data Register. After the last data frame byte is transmitted, the CRC word (if CRC insertion has been enabled), or a flag (if CRC insertion has not been enabled) is transmitted. The XFDL then returns to the transmission of flag characters.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort characters.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the Transmit Data Register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the TDLUDR signal. Optionally, the interrupt and underrun signals can be independently enabled to also generate an interrupt on the INTB output, providing a means to notify the controlling processor of changes in the XFDL operating status.

When the internal HDLC transmitter is disabled, the serial data to be transmitted on data link can be input on the TDLSIG pin timed to the clock rate output on the TDLCLK pin.

9.13 Digital Jitter Attenuator (DJAT)

The Digital Jitter Attenuation function is provided by the Digital Jitter Attenuator (DJAT) block. The DJAT block receives jittered, dual-rail E1 data in NRZ format from TRAN on two separate inputs, which allows bipolar violations to pass through the block uncorrected. The incoming data streams are stored in a FIFO timed to the transmit clock (either BTCLK or RCLKO). The respective input data emerges from the FIFO timed to the jitter attenuated clock (TCLKO) referenced to either TCLKI, BTCLK, or RCLKO.

The jitter attenuator generates the jitter-free 2.048 MHz TCLKO output transmit clock by adaptively dividing the 49.152 MHz XCLK signal according to the phase difference between the generated TCLKO and input data clock to DJAT (either BTCLK or RCLKO). Jittered fluctuations in the phase of the input data clock are attenuated by the phase-locked loop within DJAT so that the frequency of TCLKO is equal to the average frequency of the input data clock. Phase fluctuations with a jitter frequency above 8.8 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 8.8 Hz are tracked by the generated TCLKO. To provide a smooth flow of data out of DJAT, TCLKO is used to read data out of the FIFO.

If the FIFO read pointer (timed to TCLKO) comes within one bit of the write pointer (timed to the input data clock, BTCLK or RCLKO), DJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

Jitter Characteristics

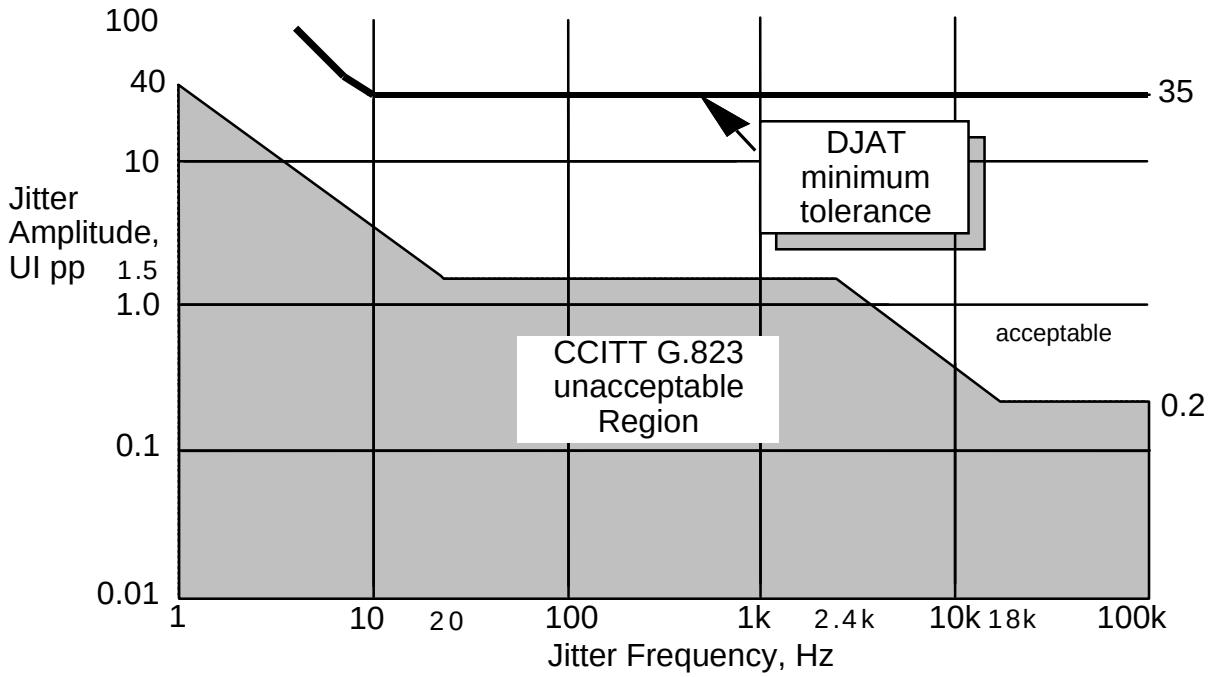
The DJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 35 UIpp of input jitter at jitter frequencies above 9 Hz. For jitter frequencies below 9 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In most applications the DJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The DJAT Block meets the low frequency jitter tolerance requirements of ITU-T Recommendation G.823.

DJAT exhibits negligible jitter gain for jitter frequencies below 8.8 Hz, and attenuates jitter at frequencies above 8.8 Hz by 20 dB per decade. In most applications the DJAT Block will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through DJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of 24X (49.152 MHz) digital phase locked loop for transmit clock generation. DJAT meets the jitter attenuation requirements of the ITU-T Recommendations G.737, G.738, G.739 and G.742.

Jitter Tolerance

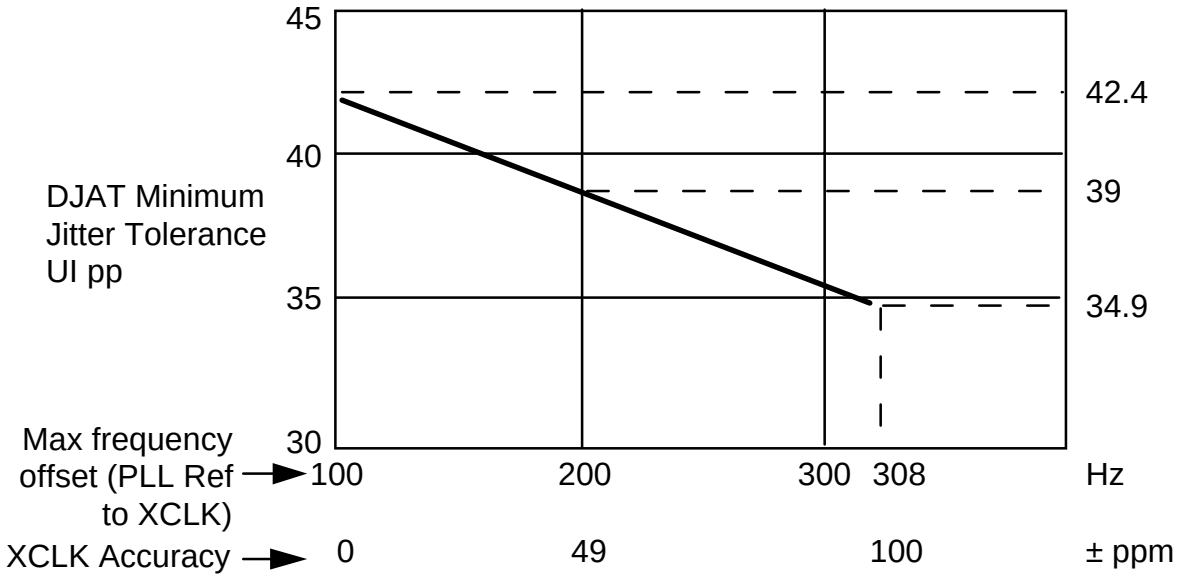
Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For DJAT, the input jitter tolerance is 35 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 308 Hz. It is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK divided by 24 and that of the input data clock.

Figure 8 - DJAT Jitter Tolerance



The accuracy of the XCLK frequency and that of the DJAT PLL reference input clock used to generate the jitter-free TCLKO have an effect on the minimum jitter tolerance. Given that the DJAT PLL reference clock accuracy can be ±103 Hz from 2.048 MHz, and that the XCLK input accuracy can be ±100 ppm from 49.152 MHz, the minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK/24 are shown in Figure 9.

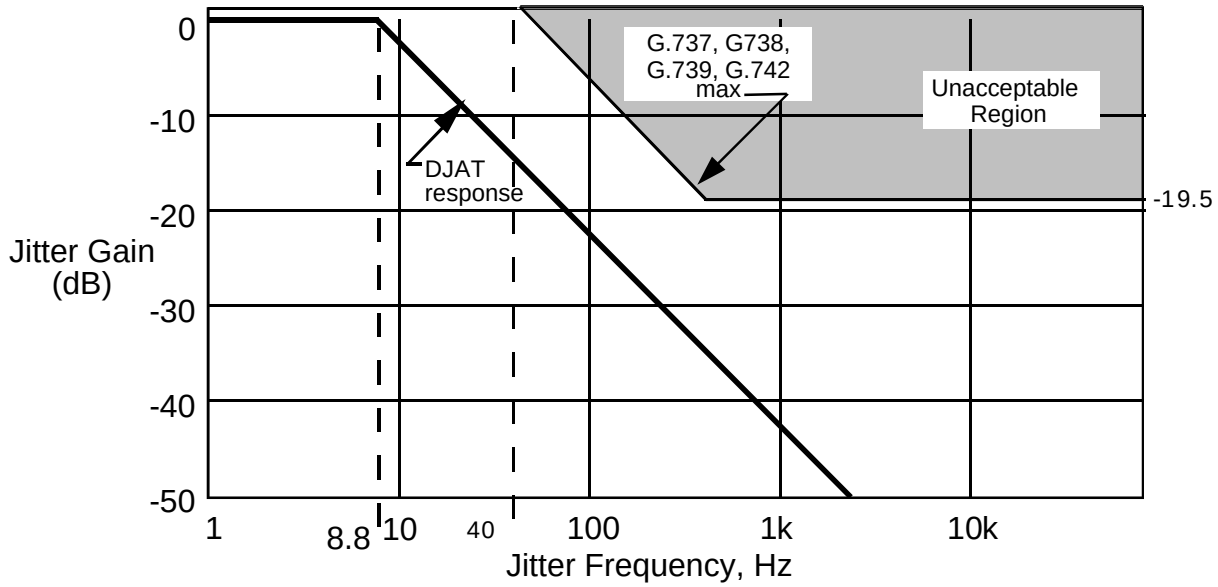
Figure 9 - DJAT Minimum Jitter Tolerance vs. XCLK Accuracy



Jitter Transfer

The output jitter for jitter frequencies from 0 to 8.8 Hz is no more than 0.1 dB greater than the input jitter, excluding residual jitter. Jitter frequencies above 8.8 Hz are attenuated at a level of 6 dB per octave, as shown in Figure 10.

Figure 10 - DJAT Jitter Transfer



Jitter Generation

When no jitter is applied to the input port, the jitter attenuator generates 0.042 UIpp (1/24 UIpp) of output jitter.

Frequency Range

In the non-attenuating mode, that is, when the FIFO is within one UI of overrunning or under running, the tracking range is 1.963 to 2.133 MHz. The guaranteed linear operating range for the jittered input clock is 2.048 MHz ± 1278 Hz with worst case jitter (42 UIpp) and maximum XCLK frequency offset (± 100 ppm). The nominal range is 2.048 MHz ± 103 Hz with no jitter or XCLK frequency offset.

9.14 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the internal input clock to the DJAT block, the reference signal for the digital PLL, and the clock source used to derive the output TCLKO signal.

9.15 Digital DS-1 Transmit Interface (DTIF)

The Digital DS-1 Transmit Interface provides control over the various output options available on the multifunctional digital transmit pins TDP/TDD and TDN/TFLG. When configured for dual-rail output, the multifunctional pins become the TDP and TDN outputs. These outputs can be formatted as either return-to-zero (RZ) or non-return-to-zero (NRZ) signals and can be updated on either the rising or falling edge of TCLKO. When the interface is configured for single-rail output, the multifunctional pins become the TDD and TFLG outputs, which can be enabled to be updated on either the rising or falling TCLKO edge. Further, the TFLG output can be enabled to indicate FIFO empty or FIFO full status.

The DTIF block also provides Alarm Indication Signalling (AIS) generation capability by generating alternating mark signals on the TDP/TDN outputs, or all-ones on the TDD output, when the TAISEN bit is set in the Transmit Interface Configuration register. This is useful when the internal loopback modes are used.

9.16 Analog Pulse Generator (XPLS)

The Analog Pulse Generator function is provided by the Transmit Pulse Generator block (XPLS) block that converts Non Return to Zero (NRZ) pulses into Alternate Mark Inversion (AMI) line signals suitable for use in a G.703 2048 kbit/s intra-office environment. The dual-rail NRZ pulses are supplied by the DJAT block. A logical "1" on the TDP output from DJAT causes a positive pulse to be transmitted; a similar signal on the TDN output from DJAT causes a negative pulse to be transmitted. If both TDP and TDN are logical "0" or "1," no output pulse is transmitted.

The output pulse shape is synthesized digitally with an internal Digital to Analog (D/A) converter. The converter is updated eight times per 2048 kbit/s period with words stored in a ROM. These words define the output pulse shape. The ROM words are ITU-T G.703 2048 kbit/s compatible. If an external circuit different from that recommended in Figure 10 is used, the pulse generator permits creation of custom pulse shapes. Refer to the Operations section for details.

AMI signalling is created by exciting either the internal TIP or RING DRIVERS that drive a line-coupling transformer differentially via the TAP and TAN outputs. This differential driving scheme insures a small positive to negative pulse imbalance. The drivers, with the step-up transformer, amplify the output pulses to their final levels. The TIP and RING drivers also supply the high current capability required to drive the low impedance output load.

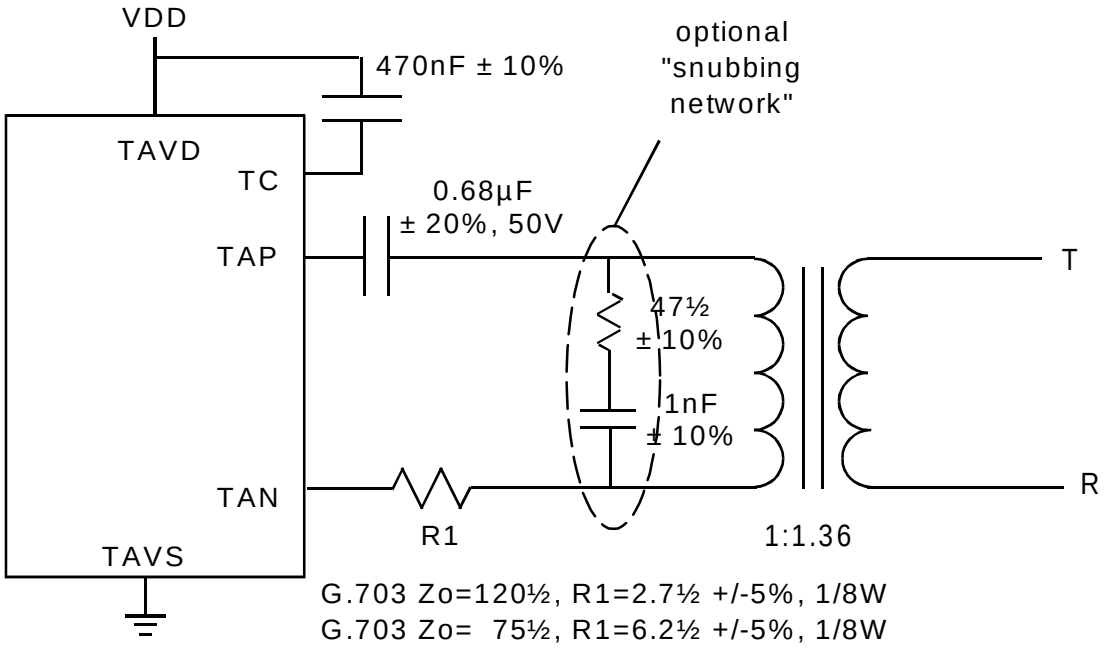
The default line build out is a 50% duty cycle square pulse compatible with the ITU-T G.703 specification for a 120 Ω symmetrical line. A separate build out is available for 75 Ω coaxial line.

A small, high-frequency negative-going spike may be observed on the falling edge of the transmit pulse. This spike can be filtered out by using the optional "snubbing" network shown in Figure 11.

The XPLS includes a driver performance monitor to detect nonfunctional links. Two monitor inputs, PM_TIP and PM_RING, are internally bonded to the XPLS's own TAP and TAN outputs. If no pulses are detected alternately across the PM_TIP or PM_RING monitor points for 62 consecutive TCLKO periods, the monitored link is declared failed. The XPLS can be programmed to produce an interrupt whenever the link monitor state changes.

The XPLS block provides Alarm Indication Signalling (AIS) generation capability by generating alternating mark signals on the link when the TAIS bit is programmed high. This is useful when the internal loopback modes are used.

Figure 11 - External Analog Transmit Interface Circuit



Recommended Transformers:

BH Electronics 500-1776 (1:1.36);
Pulse Engineering PE 64937 (1:1.36); or
Pulse Engineering PE 65340 (1:1.36)Ê(for extended temp range)

Alternatively, a dual part containing the 1:2CT & 1:1.36 transformers necessary for the receiver and the transmitter circuits can be used, i.e.:

BH Electronics 500-1777;
Pulse Engineering PE 64952; or
Pulse Engineering PE 65774Ê(for extended temp range)

9.17 Backplane Transmit Interface (BTIF)

The Backplane Transmit Interface allows data to be taken from a backplane in a 2048kbit/s serial stream and allows BPV transparency by accepting dual-rail data.

9.18 Microprocessor Interface (MPIF)

The Microprocessor Interface allows the E1XC to be configured, controlled and monitored via internal registers.

10 REGISTER DESCRIPTION

Table 2 - Normal Mode Register Memory Map

Address	Register
00H	E1XC Receive Options
01H	E1XC Receive Backplane Options
02H	E1XC Datalink Options
03H	E1XC Receive Interface Configuration
04H	E1XC Transmit Interface Configuration
05H	E1XC Transmit Backplane Options
06H	E1XC Transmit Framing Options
07H	E1XC Transmit Timing Options
08H	E1XC Master Interrupt Source
09H	E1XC Receive TS0 Data Link Enables
0AH	E1XC Master Diagnostics
0BH	E1XC Master Test
0CH	E1XC Revision/Chip ID
0DH	E1XC Master Reset
0EH	E1XC Phase Status Word (LSB)
0FH	E1XC Phase Status Word (MSB)
10H	CDRC block Configuration
11H	CDRC block Interrupt Enable
12H	CDRC block Interrupt Status
13H	Alternate Loss of Signal
14H	XPLS block Line Length Configuration
15H	XPLS block Control/Status
16H	XPLS block CODE Indirect Address
17H	XPLS block CODE Indirect Data
18H	DJAT block Interrupt Status

Address	Register
19H	DJAT block Reference Clock Divisor (N1) Control
1AH	DJAT block Output Clock Divisor (N2) Control
1BH	DJAT block Configuration
1CH	ELST block Configuration
1DH	ELST block Interrupt Enable/Status
1EH	ELST block Idle Code
1FH	ELST Reserved
20H	FRMR block Framing Alignment Options
21H	FRMR block FRMR Maintenance Mode Options
22H	FRMR block Framing Status Interrupt Enable
23H	FRMR block Maintenance/Alarm Status Interrupt Enable
24H	FRMR block Framing Status Interrupt Indication
25H	FRMR block Maintenance/Alarm Status Interrupt Indication
26H	FRMR block Framing Status
27H	FRMR block Maintenance/Alarm Status
28H	FRMR block International/National Bits
29H	FRMR block Extra Bits
2AH	FRMR block CRC Error Count - LSB
2BH	FRMR block CRC Error Count - MSB
2CH	TS16 AIS Alarm Status
2DH - 2FH	Reserved
30H	TPSC block Configuration
31H	TPSC block µP Access Status
32H	TPSC block Timeslot Indirect Address/Control
33H	TPSC block Timeslot Indirect Data Buffer
34H	XFDL block Configuration
35H	XFDL block Interrupt Status

Address	Register
36H	XFDL block Transmit Data
37H	XFDL Reserved
38H	RFDL block Configuration
39H	RFDL block Interrupt Control/Status
3AH	RFDL block Status
3BH	RFDL block Receive Data
3CH - 3FH	Reserved
40H	SIGX block Configuration
41H	SIGX block µP Access Status
42H	SIGX block Timeslot Indirect Address/Control
43H	SIGX block Timeslot Indirect Data Buffer
44H	TRAN block Configuration
45H	TRAN block Transmit Alarm/Diagnostic Control
46H	TRAN block International/National Control
47H	TRAN block Extra Bits Control
48H	PMON block Control/Status
49H	PMON block FER Count
4AH	PMON block FEBE Count (LSB)
4BH	PMON block FEBE Count (MSB)
4CH	PMON block CRC Count (LSB)
4DH	PMON block CRC Count (MSB)
4EH	PMON block LCV Count (LSB)
4FH	PMON block LCV Count (MSB)
50H-5BH	Reserved
5CH	RSLC block Configuration
5DH	RSLC block Interrupt Enable/Status

11 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the E1XC. Normal mode registers (as opposed to test mode registers) are selected when A[7] is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the E1XC to determine the programming state of the chip.

3. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect E1XC operation unless otherwise noted.

11.1 Internal Registers

Register 00H: E1XC Receive Options

Bit	Type	Function	Default
Bit 7	R/W	WORDERR	0
Bit 6	R/W	CNTNFAS	0
Bit 5	R/W	ELSTBYP	0
Bit 4	R/W	TRSLIP	0
Bit 3	R/W	SRPCM	0
Bit 2	R/W	SRSMFP	0
Bit 1	R/W	SRCMFP	0
Bit 0	R/W	TRKEN	0

This register allows software to configure the receive functions of the E1XC.

WORDERR:

The WORDERR bit determines how frame alignment signal (FAS) errors are reported. When WORDERR is logic 1, one or more errors in the seven bit FAS word results in a single framing error count. When WORDERR is logic 0, each error in a FAS word results in a single framing error count.

CNTNFAS:

When the CNTNFAS bit is a logic 1, a zero in bit 2 of time slot 0 of non-frame alignment signal (NFAS) frames results in an increment of the framing error count. If WORDERR is also a logic 1, the word is defined as the eight bits comprising the FAS pattern and bit 2 of time slot 0 of the next NFAS frame. When the CNTNFAS bit is a logic 0, only errors in the FAS affect the framing error count.

ELSTBYP:

The ELSTBYP bit allows the Elastic Store (ELST) block to be bypassed, eliminating the one frame delay incurred through the ELST. When set to logic 1, the received data and clock inputs to ELST are internally routed directly to the ELST outputs.

TRSLIP:

The TRSLIP bit allows the ELST block to be used to measure, through SLIP indications, the frequency difference between the recovered receive line clock

and the transmit clock driving the TRAN block when the ELST is bypassed. When TRSLIP is set to logic 1, the transmit clock input to TRAN is internally substituted for the BRCLK input to the system side of the ELST. When TRSLIP is set to logic 0, the BRCLK input is routed to the system side of the ELST. The TRSLIP bit should only be set if ELSTBYP is set to logic 1.

SRPCM:

The SRPCM bit selects the output signal seen on the multifunction output RPCM/ RDPCM. When set to logic 1, the multifunction output becomes RPCM, the undecoded PCM output from the Clock and Data Recovery (CDRC) block. When SRPCM is set to logic 0, the multifunction output becomes RDPCM, the HDB3-decoded PCM output from the CDRC block.

SRSMFP, SRCMFP:

The SRSMFP and SRCMFP bits select the output signal seen on the output RFP. The following table summarizes the four configurations:

SRSMFP	SRCMFP	Result
0	0	Receive frame pulse output: RFP pulses high for 1 RCLKO cycle during bit 1 of each 256-bit frame, indicating the frame alignment of the RDPCM/RPCM data stream.
0	1	Receive CRC multiframe output: RFP pulses high for 1 RCLKO cycle during bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the RDPCM/RPCM data stream. (Even when CRC multiframing is disabled, the RFP output continues to indicate the position of bit 1 of the FAS frame every 16th frame.)
1	0	Receive signalling multiframe output: RFP pulses high for 1 RCLKO cycle during bit 1 of frame 1 of the 16 frame signalling multiframe, indicating the signalling multiframe alignment of the RDPCM/RPCM data stream. (Even when signalling multiframing is disabled, the RFP output continues to indicate the position of bit 1 of every 16th frame.)

SRSMFP	SRCMFP	Result
1	1	Receive composite multiframe output: RFP goes high on the falling RCLKO edge marking the beginning of bit 1 of frame 1 of every 16 frame signalling multiframe, indicating the signalling multiframe alignment of the RPCM/RDPCM data stream, and returns low on the falling RCLKO edge marking the end of bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the RPCM/RDPCM data stream. This mode allows both multiframe alignments to be decoded externally from the single RFP signal. Note that if the signalling and CRC multiframe alignments are coincident, RFP will pulse high for 1 RCLKO cycle every 16 frames.

TRKEN:

The TRKEN bit enables receive trunk conditioning upon an out-of-frame-condition. If TRKEN is logic 1, the contents of the ELST Idle Code register are inserted into all time slots (including TS0 and TS16) of BRPCM if the framer is out-of-basic frame (i.e. the OOF status bit is logic 1). The TRKEN bit only has effect if the BRX2RAIL and ELSTBYP bits are both logic 0. If TRKEN is a logic 0, receive trunk conditioning can still be performed on a per-timeslot basis via the SIGX Per-Timeslot Trunk Conditioning Data Registers

Upon reset of the E1XC, these bits are cleared to zero.

Register 01H: E1XC Receive Backplane Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	RXDMAGAT	0
Bit 4	R/W	ROHM	0
Bit 3	R/W	BRX2RAIL	0
Bit 2	R/W	BRXSMFP	0
Bit 1	R/W	BRXCMFP	0
Bit 0		Unused	X

This register allows software to configure the Receive backplane interface format of the E1XC.

RXDMAGAT:

The RXDMAGAT bit selects the gating of the RDLINT output with the RDLEOM output when the internal HDLC receiver is used with DMA. When RXDMAGAT is set to logic 1, the RDLINT DMA output is gated with the RDLEOM output so that RDLINT is forced to logic 0 when RDLEOM is logic 1. When RXDMAGAT is set to logic 0, the RDLINT and RDLEOM outputs operate independently.

BRX2RAIL:

The BRX2RAIL bit selects whether the backplane receive data signal on the multifunction outputs BRPCM/BRDP and BRSIG/BRDN are in either dual rail or single rail format. When BRX2RAIL is set to logic 1, the multifunction pins become the BRDP and BRDN dual rail outputs, which contain the received positive and negative line pulses timed to the 2.048MHz receive line rate, RCLKO. When BRX2RAIL is set to logic 0, the multifunction pins become the BRPCM and BRSIG digital outputs.

ROHM, BRXSMFP, BRXCMFP:

The ROHM, BRXSMFP and BRXCMFP bits select the output signal seen on the backplane output BRFPO. The following table summarizes the configurations:

ROHM	BRXSMFP	BRXCMFP	Result
0	0	0	Backplane receive frame pulse output: BRFPO pulses high for 1 BRCLK cycle (or 1 RCLKO cycle if ELST is by-passed) during bit 1 of each 256-bit frame, indicating the frame alignment of the BRPCM data stream.
0	0	1	Backplane receive CRC multiframe output: BRFPO pulses high for 1 BRCLK cycle (or 1 RCLKO cycle if ELST is by-passed) during bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM data stream. (Even when CRC multiframing is disabled, the BRFPO output continues to indicate the position of bit 1 of the FAS frame every 16th frame).
0	1	0	Backplane receive signalling multiframe output: BRFPO pulses high for 1 BRCLK cycle (or 1 RCLKO cycle if ELST is by-passed) during bit 1 of frame 1 of the 16 frame signalling multiframe, indicating the signalling multiframe alignment of the BRPCM data stream. (Even when signalling multiframing is disabled, the BRFPO output continues to indicate the position of bit 1 of every 16th frame.)

ROHM	BRXSMFP	BRXCMFP	Result
0	1	1	Backplane receive composite multiframe output: BRFPO goes high on the falling BRCLK edge (or RCLKO edge if ELST is by-passed) marking the beginning of bit 1 of frame 1 of every 16 frame signalling multiframe, indicating the signalling multiframe alignment of the BRPCM data stream, and returns low on the falling BRCLK edge (or RCLKO edge if ELST is by-passed) marking the end of bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM data stream. This mode allows both multiframe alignments to be decoded externally from the single BRFPO signal. Note that if the signalling and CRC multiframe alignments are coincident, BRFPO will pulse high for 1 BRCLK cycle (or RCLKO cycle if ELST is by-passed) every 16 frames.
1	X	X	Backplane receive overhead output: BRFPO is high for timeslot 0 and timeslot 16 of each 256-bit frame, indicating the overhead of the BRPCM data stream.

Upon reset of the E1XC, these bits are cleared to zero.

Register 02H: E1XC Datalink Options

Bit	Type	Function	Default
Bit 7	R/W	RXDMASIG	0
Bit 6		Unused	X
Bit 5	R/W	TXDMASIG	0
Bit 4		Unused	X
Bit 3	R/W	RDLINTE	0
Bit 2	R/W	RDLEOME	0
Bit 1	R/W	TDLINTE	0
Bit 0	R/W	TDLUDRE	0

This register allows software to configure the datalink options of the E1XC.

RXDMASIG:

The RXDMASIG bit selects the internal HDLC receiver (RFDL) data-received interrupt (INT) and end-of-message (EOM) signals to be output on the RDLINT and RDLEOM pins. When RXDMASIG is set to logic 1, the RDLINT and RDLEOM output pins can be used by a DMA controller to process the datalink. When RXDMASIG is set to logic 0, the RFDL INT and EOM signals are no longer available to a DMA controller; the signals on RDLINT and RDLEOM become the extracted datalink data and clock, RDLSIG and RDLCLK. In this mode, the data stream available on the RDLSIG output corresponds to the extracted datalink from Time Slot 16 or the Time Slot 0 National Use bits depending on the state of the RXSAxEN bits of the Receive TS0 Data Link Enables register.

TXDMASIG:

The TXDMASIG bit selects the internal HDLC transmitter (XFDL) request for service interrupt (INT) and data underrun (UDR) signals to be output on the TDLINT and TDLUDR pins. When TXDMASIG is set to logic 1, the TDLINT and TDLUDR output pins can be used by a DMA controller to service the datalink. When TXDMASIG is set to logic 0, the XFDL INT and UDR signals are no longer available to a DMA controller; the signals on TDLINT and TDLUDR become the serial datalink data input and clock, TDLSIG and TDLCLK. In this mode an external controller is responsible for formatting the data stream presented on the TDLSIG input to correspond to the datalink in Time Slot 16 or the Time Slot 0 National Use bits. If the TRAN block Configuration DLEN bit is logic 1 and the TRAN block Configuration SIGEN

bit is a logic 0, the TDLSIG data stream is inserted into Time Slot 16 and the TDLCLK pin is a 50% duty cycle 64 kHz clock; otherwise, the TDLSIG data stream is inserted into the Time Slot 0 National Use positions enabled by the TXSAxEN bits.

In the default case TDLCLK is a bursted 4 kHz clock and TDLSIG is inserted into the TS0 Sa4 bit.

RDLINTE:

The RDLINTE bit enables the RFDL received-data interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the RFDL without needing to interface to the DMA control signals. When RDLINTE is set to logic 1, an event causing an interrupt in the RFDL (which is visible on the RDLINT output pin when RXDMASIG is logic 1) also causes an interrupt to be generated on the INTB output. When RDLINTE is set to logic 0, an interrupt event in the RFDL does not cause an interrupt on INTB.

RDLEOME:

The RDLEOME bit enables the RFDL end-of-message interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the RFDL without needing to interface to the DMA control signals. When RDLEOME is set to logic 1, an end-of-message event causing an EOM interrupt in the RFDL (which is visible on the RDLEOM output pin when RXDMASIG is logic 1) also causes an interrupt to be generated on the INTB output. When RDLEOME is set to logic 0, an EOM interrupt event in the RFDL does not cause an interrupt on INTB. NOTE: within the RFDL, an end-of-message event causes an interrupt on both the EOM and INT RFDL interrupt outputs. See the Operation section for further details on using the RFDL.

TDLINTE:

The TDLINTE bit enables the XFDL request for service interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the XFDL without needing to interface to the DMA control signals. When TDLINTE is set to logic 1, an request for service interrupt event in the XFDL (which is visible on the TDLINT output pin when TXDMASIG is logic 1) also causes and interrupt to be generated on the INTB output. When TDLINTE is set to logic 0, an interrupt event in the XFDL does not cause an interrupt on INTB.

TDLUDRE:

The TDLUDRE bit enables the XFDL transmit data underrun interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a

single microprocessor to service the XFDL without needing to interface to the DMA control signals. When TDLUDRE is set to logic 1, an underrun event causing an interrupt in the XFDL (which is visible on the TDLUDR output pin when TXDMASIG is logic 1) also causes and interrupt to be generated on the INTB output. When TDLUDRE is set to logic 0, an underrun event in the XFDL does not cause an interrupt on INTB.

Upon reset of the E1XC, these bits are cleared to zero.

Register 03H: E1XC Receive Interface Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SDOEN	0
Bit 5	R/W	RDIEN	0
Bit 4	R/W	RDNINV	0
Bit 3	R/W	RDPINV	0
Bit 2	R/W	RUNI	0
Bit 1	R/W	RFALL	0
Bit 0		Unused	X

This register enables the Receive Interface to handle the various input waveform formats.

SDOEN:

The SDOEN bit enables the sliced positive and negative pulses from the analog receive slicer to be visible on the SDP and SDN pins when the Analog G.703 E1 Receive Slicer is active. When SDOEN is set to logic 1, the multifunction pins SDP/RDP/RDD and SDN/RDN/RLCV become the sliced positive and negative pulse outputs, SDP and SDN. Pulses will be seen on the SDP and SDN outputs if RSLC is powered up. When SDOEN is set to logic 0, the multifunction pins SDP/RDP/RDD and SDN/RDN/RLCV become the digital inputs, RDP/RDD and RDN/RLCV. The function of the digital inputs is determined by the RUNI bit.

RDIEN:

The RDIEN bit enables data received on the digital inputs, RDP/RDD and RDN/RLCV, to be used internally instead of the outputs from the Analog G.703 E1 Receive Slicer. When RDIEN is set to logic 1 and SDOEN is set to logic 0, digital data input on the multifunction pins RDP/RDD and RDN/RLCV are handled in accordance with the remaining bit setting in this register and the resulting signals are used internally to drive the clock and data recovery block. When RDIEN is set to logic 0, the output signals from the analog RSLC are used internally to drive the CDRC block.

RDPINV,RDNINV:

The RDPINV and RDNINV bits enable the Receive Interface to logically invert the signals received on multifunction pins SDP/RDP/RDD and

SDN/RDN/RLCV, respectively. When RDPINV is set to logic 1, the interface inverts the signal on the RDP/RDD input. When RDPINV is set to logic 0, the interface passes the RDP/RDD signal unaltered. When RDNINV is set to logic 1, the interface inverts the signal on the RDN/RLCV input. When RDNINV is set to logic 0, the interface passes the RDN/RLCV signal unaltered.

RUNI:

The RUNI bit enables the interface to receive unipolar digital data and line code violation indications on the multifunction pins SDP/RDP/RDD and SDN/RDN/RLCV. When RUNI is set to logic 1, the SDP/RDP/RDD and SDN/RDN/RLCV multifunction pins become the data and line code violation inputs, RDD and RLCV, sampled on the selected RCLKI edge. When RUNI is set to logic 0, the SDP/RDP/RDD and SDN/RDN/RLCV multifunction pins become the positive and negative pulse inputs, RDP and RDN, sampled on the selected RCLKI edge.

RFALL:

The RFALL bit enables the Receive Interface to sample the multifunction pins on the falling RCLKI edge. When RFALL is set to logic 1, the interface is enabled to sample either the RDD and RLCV inputs, or the RDP and RDN inputs, on the falling RCLKI edge. When RFALL is set to logic 0, the interface is enabled to sample the inputs on the rising RCLKI edge.

Register 04H: E1XC Transmit Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	FIFOBYP	0
Bit 6	R/W	TAISEN	0
Bit 5	R/W	TDNINV	0
Bit 4	R/W	TDPINV	0
Bit 3	R/W	TUNI	0
Bit 2	R/W	FIFOFULL	0
Bit 1	R/W	TRISE	0
Bit 0	R/W	TRZ	0

This register enables the Transmit Interface to generate the required digital output waveform format.

FIFOBYP:

The FIFOBYP bit enables the transmit bipolar input signals to DJAT to be bypassed around the FIFO to the bipolar outputs. When jitter attenuation is not being used, and the XPLS pulse driver is being driven with a "jitter-free" 16.384MHz clock on TCLKI, the DJAT FIFO can be bypassed to reduce the delay through the transmitter section by typically 24 bits. NOTE: under this condition, the BTCLK signal must be synchronous to the TCLKI and the SMCLKO bit of the Transmit Timing Options register must be set. When FIFOBYP is set to logic 1, the bipolar inputs to DJAT are routed around the FIFO and directly into XPLS. When FIFOBYP is set to logic 0, the bipolar transmit data passes through the DJAT FIFO.

TAISEN:

The TAISEN bit enables the interface to generate an unframed all-ones AIS alarm on the TDP/TDD and TDN/TFLG multifunction pins. When TAISEN is set to logic 1 and TUNI is set to logic 0, the bipolar TDP and TDN outputs are forced to pulse alternately, creating an all-ones signal; when TAISEN and TUNI are both set to logic 1, the unipolar TDD output is forced to all-ones. When TAISEN is set to logic 0, the TDP/TDD and TDN/TFLG multifunction outputs operate normally. The transition to transmitting AIS on the TDP and TDN outputs is done in such a way as to not introduce any bipolar violations.

TDPINV,TDNINV:

The TDPINV and TDNINV bits enable the E1/DS1A Transmit Interface to logically invert the signals output on the TDP/TDD and TDN/TFLG multifunction pins, respectively. When TDPINV is set to logic 1, the TDP/TDD output is inverted. When TDPINV is set to logic 0, the TDP/TDD output is not inverted. When TDNINV is set to logic 1, the TDN/TFLG output is inverted. When TDNINV is set to logic 0, the TDN/TFLG output is not inverted.

TUNI:

The TUNI bit enables the transmit interface to generate unipolar digital outputs on the TDP/TDD and TDN/TFLG multifunction pins. When TUNI is set to logic 1, the TDP/TDD and TDN/TFLG multifunction pins become the unipolar outputs TDD and TFLG, updated on the selected TCLKO edge. When TUNI is set to logic 0, the TDP/TDD and TDN/TFLG multifunction pins become the bipolar outputs TDP and TDN, also updated on the selected TCLKO edge. When the TUNI is set to logic 1 (unipolar mode) the analog transmit data outputs, TAP and TAN, from the XPLS cannot be used.

FIFOFULL:

The FIFOFULL bit determines the indication given on the TFLG output pin. When FIFOFULL is set to logic 1, the TFLG output indicates when the Digital Jitter Attenuator's FIFO is within 4 bit positions of becoming full. When FIFOFULL is set to logic 0, the TFLG output indicates when the Digital Jitter Attenuator's FIFO is within 4 bit positions of becoming empty.

TRISE:

The TRISE bit configures the interface to update the multifunction outputs on the rising edge of TCLKO. When TRISE is set to logic 1, the interface is enabled to update the TDP/TDD and TDN/TFLG output pins on the rising TCLKO edge. When TRISE is set to logic 0, the interface is enabled to update the outputs on the falling TCLKO edge.

TRZ:

The TRZ bit configures the interface to transmit bipolar return-to-zero formatted waveforms. When TRZ is set to logic 1, the interface is enabled to generate the TDP and TDN output signals as RZ waveforms with duration equal to half the TCLKO period. When TRZ is set to logic 0, the interface is enabled to generate the TDP and TDN output signals as NRZ waveforms with duration equal to the TCLKO period, updated on the selected edge of TCLKO. The TRZ bit can only be used when TUNI and TRISE are set to logic 0.

When the system is reset, the contents of the register are set to logic 0, enabling the Transmit Interface to output NRZ formatted positive and negative pulse data on the TDP and TDN outputs, updated on the falling TCLKO edge.

Register 05H: E1XC Transmit Backplane Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	BTXCLK	0
Bit 2		Unused	X
Bit 1	R/W	BTX2RAIL	0
Bit 0	R/W	BTXMFP	0

This register allows software to configure the Transmit backplane interface format.

BTXCLK:

The BTXCLK bit selects the source of the TRAN transmit clock input signal. When BTXCLK is set to logic 1, the TRAN transmit clock is driven with the 2.048MHz recovered PCM output clock (RCLKO) from the receiver section. When BTXCLK is set to logic 0, the TRAN transmit clock is driven with the 2.048MHz backplane transmit clock (BTCLK). Note that this bit must be set to logic 1 when Line Loopback is enabled.

BTX2RAIL:

The BTX2RAIL bit selects whether the backplane transmit data signal presented to the transmitter on the multifunction inputs BTPCM/BTDP and BTSIG/BTDN are in either dual-rail or single-rail format. When BTX2RAIL is set to logic 1, the multifunction pins become the BTDP and BTDN dual-rail inputs, which bypass the TRAN and input directly into the jitter attenuator. It is expected that the framing bits be already inserted into the dual-rail streams before they are input on BTDP and BTDN. When BTX2RAIL is set to logic 0, the multifunction pins become the BTPCM and BTSIG digital inputs.

BTXMFP:

The BTXMFP bit selects the type of backplane frame alignment signal presented to the transmitter BTFP input. When BTXMFP is set to logic 1, BTFP must be brought high to mark bit 1 of frame 1 of every 16 frame signalling multiframe and brought low following bit 1 of frame 1 of every 16 frame CRC multiframe. This mode allows both multiframe alignments to be

independently controlled using the single BTFP signal. Note that if the signalling and CRC multiframe alignments are coincident, BTFP must pulse high for 1 BTCLK cycle at a multiple of 16 frames. When BTXMFP is set to logic 0, a rising edge on the BTFP indicates the first bit in each frame.

Upon reset of the E1XC, these bits are cleared to zero.

Register 06H: E1XC Transmit Framing Options

Bit	Type	Function	Default
Bit 7	R/W	PATHCRC	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TXSA4EN	1
Bit 3	R/W	TXSA5EN	0
Bit 2	R/W	TXSA6EN	0
Bit 1	R/W	TXSA7EN	0
Bit 0	R/W	TXSA8EN	0

PATHCRC:

The PATHCRC bit allows upstream block errors to be preserved in the transmit CRC bits. If PATHCRC is a logic 1, the CRC-4 bits are modified to reflect any bit values in BTPCM which have changed prior to transmission. When PATHCRC is set to logic 0, the TRAN block is allowed to generate a new CRC-4 value which overwrites the incoming CRC-4 word. For the PATHCRC bit to be effective, the BTXMFP bit of the Transmit Backplane Options register must be a logic 1; otherwise, the identification of the incoming CRC-4 bits would be impossible. The PATHCRC bit only takes effect if the GENCRC bit of the TRAN Configuration register (44H) is a logic 1 and either the INDIS or FDIS bit in the same register are set to logic1.

TXSA4EN, TXSA5EN, TXSA6EN, TXSA7EN and TXSA8EN:

The TXSAxEN bits control the insertion of a data link into the Time Slot 0 National Use bits (Sa4 through Sa8).

These bits only have effect if the TRAN block Configuration DLEN bit is logic 0 or if the TRAN block Configuration SIGEN bit is logic 1. The TXSAxEN bits take priority over the INDIS and FDIS bits of the TRAN block Configuration register. The data link bits are still inserted if either INDIS or FDIS is logic 1.

If the TXDMASIG bit is a logic 1, the data link bits are sourced by the internal HDLC transmitter; otherwise, the bits are sourced from the TDLSIG pin. If the TXSA4EN bit is logic 1, the TDLSIG value is written into bit 4 of Time Slot 0 of non-frame alignment signal frames. If the TXSA8EN bit is logic 1, the TDLSIG value is written into bit 8 of Time Slot 0 of non-frame alignment signal frames. The other enable bits operate in an analogous fashion. A clock pulse

is generated on TDLCLK for each enable that is logic 1. Any combination of enable bits is allowed, resulting in a data rate between 4 kbit/s and 20 kbit/s. Clearing all enables disables insertion. Any National Use bits which are not included in the data link are sourced from either BTPCM or the TRAN block International/National Control register.

Upon reset of the E1XC, all bits are logic 0 except TXSA4EN. By default, a 4 kbit/s data link is inserted into Sa4 from the TDLSIG input.

Register 07H: E1XC Transmit Timing Options

Bit	Type	Function	Default
Bit 7	R/W	HSBPSEL	0
Bit 6	R/W	XCLKSEL	0
Bit 5	R/W	OCLKSEL1	0
Bit 4	R/W	OCLKSEL0	0
Bit 3	R/W	PLLREF1	0
Bit 2	R/W	PLLREF0	0
Bit 1	R/W	TCLKISEL	0
Bit 0	R/W	SMCLKO	0

This register allows software to configure the options of the transmit timing section.

HSBPSEL:

The HSBPSEL bit selects the source of the high-speed clock used in the ELST, SIGX and TPSC blocks. This allows the E1XC to interface to higher rate backplanes (>2.048MHz) that are externally gapped; however, the instantaneous backplane clock frequency must not exceed 3.0MHz. When HSBPSEL is set to logic 1, the XCLK input signal is divided by 2 and used as the high-speed clock to these blocks. XCLK must be driven with 49.152MHz. When HSBPSEL is set to logic 0, the block high-speed clock is driven with the internal 16.384MHz clock source selected by the XCLKSEL bit.

XCLKSEL:

The XCLKSEL bit selects the source of the high-speed clock used in the CDRC, FRMR, and PMON blocks. When XCLKSEL is set to logic 1, the XCLK input signal is used as the high-speed clock to these blocks. XCLK must be driven with 16.384MHz. When XCLKSEL is set to logic 0, the block high-speed clock is driven with the internal DJAT generated smooth 16.384MHz clock source. XCLK must be driven with 49.152MHz.

OCLKSEL1, OCLKSEL0:

The OCLKSEL[1:0] bits select the source of the Digital Jitter Attenuator FIFO output clock signal. When OCLKSEL1 is set to logic 1, the DJAT FIFO output clock is driven with the input data clock driving the DJAT ICLK input. In this mode the jitter attenuation is disabled and the input clock must be jitter-free. When OCLKSEL1 is set to logic 0, the DJAT FIFO output clock is driven with

either the TCLKI input clock or an internal smooth 2.048MHz clock, as selected by the OCLKSEL0 bit. When OCLKSEL0 is set to logic 1, the DJAT FIFO output clock is driven with the TCLKI input clock. When OCLKSEL0 is set to logic 0, the DJAT FIFO output clock is driven with the internal smooth 2.048 MHz clock selected by the TCLKISEL and SMCLKO bits.

PLLREF1, PLLREF0:

The PLLREF[1:0] bits select the source of the Digital Jitter Attenuator phase locked loop reference signal as follows:

PLLREF1	PLLREF0	Source of PLL Reference
0	0	Transmit clock used by TRAN (either the 2.048MHz BTCLK or the 2.048MHz RCLKO, as selected by BTXCLK)
0	1	BTCLK input
1	0	RCLKO output
1	1	TCLKI input

TCLKISEL,SMCLKO:

The TCLKISEL and SMCLKO bits select the source of the internal smooth 2.048MHz and 16.384MHz output clock signals. When TCLKISEL and SMCLKO are set to logic 0, the internal 2.048MHz and 16.384MHz clock signals are driven by the smooth 2.048MHz and 16.384MHz clock sources generated by DJAT. When TCLKISEL is set to logic 0 and SMCLKO is set to logic 1, the internal 2.048MHz clock signal is driven by the TCLKI input signal divided by 8, and the internal 16.384MHz clock signal is driven by the TCLKI input signal. When TCLKISEL and SMCLKO are set to logic 1, the internal 2.048MHz clock signal is driven by the XCLK input signal divided by 8, and the internal 16.384MHz clock signal is driven by the XCLK input signal. The combination of TCLKISEL set to logic 1 and SMCLKO set to logic 0 should not be used.

The following table illustrates the required bit settings for these various clock sources to affect the transmitted data:

Table 3 - Transmit Timing Options

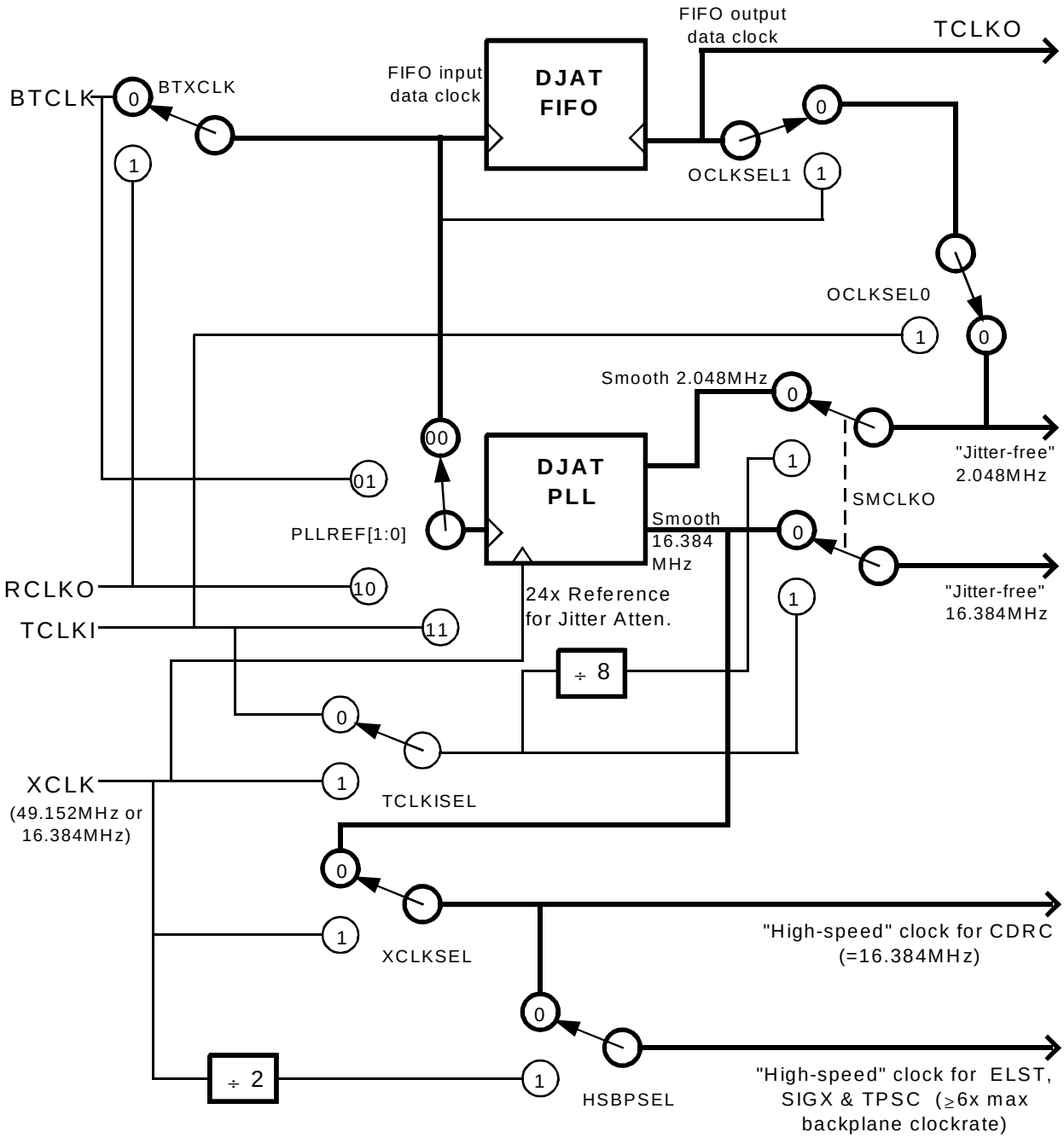
Input Transmit Data	Bit Settings	XCLK Freq	Effect on Output Transmit Data
Backplane transmit data timed to 2.048 MHz BTCLK.	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =0 PLLREF0 =X TCLKISEL =0 SMCLKO =0 PLLREF1 =1 PLLREF0 =0 PLLREF1 =1 PLLREF0 =1	49.152MHz	Jitter attenuated. TCLKO is a smooth 2.048 MHz. TCLKO referenced to BTCLK. TCLKO referenced to RCLKO. TCLKO referenced to TCLKI.
Backplane transmit data timed to >2.048MHz backplane clock. BTCLK is externally "gapped".	HSBPSEL =1 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =0 PLLREF0 =X TCLKISEL =0 SMCLKO =0 PLLREF1 =1 PLLREF0 =0 PLLREF1 =1 PLLREF0 =1	49.152MHz	Jitter attenuated. TCLKO is a smooth 2.048MHz. TCLKO referenced to externally "gapped" transmit clock. TCLKO referenced to RCLKO. TCLKO referenced to TCLKI.

Input Transmit Data	Bit Settings	XCLK Freq	Effect on Output Transmit Data
Backplane transmit data timed to BTCLK.	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =1 OCLKSEL0 =X PLLREF1 =X PLLREF0 =X TCLKISEL =0 SMCLKO =0	49.152MHz	No jitter attenuation. TCLKO is equal to internal transmit clock, either BTCLK, gapped BTCLK, or RCLKO.
	XCLKSEL =1 TCLKISEL =1 SMCLKO =1 DJAT SYNC =0	16.384MHz	Same as above. These modes are only compatible with the digital transmit outputs. Do not use the analog pulse transmitter for these register bit combinations.
Backplane transmit data timed to BTCLK.	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =1 PLLREF1 =X PLLREF0 =X TCLKISEL =0 SMCLKO =0	49.152MHz	No jitter attenuation. TCLKO is equal to TCLKI (useful for higher rate MUX applications).
	XCLKSEL =1 TCLKISEL =1 SMCLKO =1	16.384MHz	Same as above.

Input Transmit Data	Bit Settings	XCLK Freq	Effect on Output Transmit Data
Backplane transmit data timed to BTCLK.	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =X PLLREF0 =X TCLKISEL =0 SMCLKO =1 XCLKSEL =1	49.152MHz 16.384MHz	TCLKI is a jitter-free 16.384MHz clock. TCLKO is equal to TCLKI÷8. Same as above.
Backplane transmit data timed to BTCLK.	HSBPSEL =0 XCLKSEL =1 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =X PLLREF0 =X TCLKISEL =1 SMCLKO =1	jitter-free 16.384MHz	XCLK is a jitter-free 16.384MHz clock. TCLKO is equal to XCLK÷8.

Upon reset of the E1XC, these bits are cleared to zero, selecting digital jitter attenuation with TCLKO referenced to the backplane transmit clock, BTCLK. The following Figure 12 illustrates the various bit setting options, with the reset condition highlighted.

Figure 12 - Transmit Timing Options



Register 08H: E1XC Master Interrupt Source

Bit	Type	Function	Default
Bit 7	R	DJAT	X
Bit 6	R	RSLC	X
Bit 5	R	FRMR/SA	X
Bit 4	R	XPLS	X
Bit 3	R	ELST	X
Bit 2	R	RFDL	X
Bit 1	R	XFDL	X
Bit 0	R	CDRC	X

This register allows software to determine the block which produced the interrupt on the INTB output pin. The FRMR/SA bit is a logic 1 if either the FRMR or the the SACI bit in the Receive TS0 Data Link Enable register (Register 09H) is the source of the interrupt.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 09H: Receive TS0 Data Link Enables

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SACE	0
Bit 5	R	SACI	X
Bit 4	R/W	RXSA4EN	1
Bit 3	R/W	RXSA5EN	0
Bit 2	R/W	RXSA6EN	0
Bit 1	R/W	RXSA7EN	0
Bit 0	R/W	RXSA8EN	0

SACE:

The SACE bit enables the generation of an interrupt whenever there is a change in the National bits that are not extracted to form a data link. Changes in the National bits are not debounced, i.e. the interrupt is generated immediately when the current value of the National bits differs from the previous value. The value of the National bits can be read in the FRMR International/National Bits Register.

SACI:

The SACI bit is set to logic one whenever there is a change in the National bits that are not extracted to form a data link. The SACI bit is cleared following a read of this register.

RXSA4EN, RXSA5EN, RXSA6EN, RXSA7EN and RXSA8EN:

The RXSAxEN bits control the extraction of a data link from the received Time Slot 0 National Use bits (Sa4 through Sa8).

If the RXDMASIG bit is a logic one, the data link bits are terminated by the internal HDLC receiver; otherwise, the data link is presented on RDLSIG. If the RXSA4EN is logic 1, the RDLSIG value is extracted from bit 4 of Time Slot 0 of non-frame alignment signal frames. If the RXSA8EN is logic 1, the RDLSIG value is extracted from bit 8 of Time Slot 0 of non-frame alignment signal frames. The other enable bits operate in an analogous fashion. A clock pulse is generated on RDLCLK for each enable that is logic 1. Any combination enable bits is allowed resulting in a data rate between 4 kbit/s and 20 kbit/s.

If all RXSAEN[4:0] bits are set to logic 0, Timeslot 16 is extracted and treated as a data link. If RXDMASIG is logic 0, Timeslot16 is made available on the RDLSIG output and RDLCLK is an associated 64 kHz clock. If RXDMASIG is logic 1, the data link is terminated by the HDLC receiver and the RDLINT/RDLSIG and RDLEOM/RDLCLK pins operate as a data link interrupt (RDLINT) and a end-of-message (RDLEOM) indication.

Upon reset of the E1XC, all bits are logic 0 except RXSA4EN. By default, a 4 kbit/s data link is extracted from Sa4 and presented on the RDLSIG output.

Register 0AH: E1XC Master Diagnostics

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PAYLB	0
Bit 4	R/W	LINELB	0
Bit 3	R/W	DMLB	0
Bit 2	R/W	DDLB	0
Bit 1		Unused	X
Bit 0		Unused	X

This register allows software to enable the diagnostic mode of the E1XC.

PAYLB:

The PAYLB bit selects the payload loopback mode, where the received data output from the ELST is internally connected to the transmit data input of the TRAN. The data read out of ELST is timed to the transmitter clock, and the transmit frame alignment is used to synchronize the output frame alignment of ELST. During payload loopback, the data output on BRPCM is forced to logic 1. When PAYLB is set to logic 1, the payload loopback mode is enabled. When PAYLB is set to logic 0, the loopback mode is disabled.

LINELB:

The LINELB bit selects the line loopback mode, where the recovered positive and negative pulse outputs from the CDRC block are internally connected to the digital inputs of the DJAT block. When LINELB is set to logic 1, the line loopback mode is enabled. When LINELB is set to logic 0, the line loopback mode is disabled. Note that when line loopback is enabled, the BTXCLK bit in register 05H must be set to logic 1 to select the RCLKO clock as the transmit clock source and the Timing Options Register settings should be reviewed to ensure the options are such that data will pass error-free and "jitter"-free through DJAT (typically, the default setting, 00H, for register 7 will be appropriate for line loopback).

DDLB:

The DDLB bit selects the diagnostic digital loopback mode, where the digital positive and negative RZ pulse outputs from DJAT are internally connected to the receive positive and negative pulse inputs of CDRC. When DDLB is set to

logic 1, the diagnostic digital loopback mode is enabled. When DDLB is set to logic 0, the diagnostic digital loopback mode is disabled.

DMLB:

The DMLB bit enables the diagnostic metallic loopback mode, where the digital, RZ positive and negative sliced versions of the analog signals output on the TAP and TAN pins from XPLS are internally connected to the receive positive and negative pulse inputs of CDRC. When DMLB is set to logic 1, the diagnostic metallic loopback mode is enabled. When DMLB is set to logic 0, the diagnostic metallic loopback mode is disabled.

Upon reset of the E1XC, these register bits are cleared to zero.

Register 0BH: E1XC Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	0
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select E1XC test features. All bits, except for PMCTST, are reset to zero by a hardware reset of the E1XC ; a software reset of the E1XC does not affect the state of the bits in this register.

PMCTST:

The PMCTST bit is used to configure the E1XC for PMC's manufacturing tests. When PMCTST is set to logic 1, the E1XC microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the E1XC to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit only has effect if either the IOTST or PMCTST bit is set. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the E1XC for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the

outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).HIZIO,HIZDATA:
The HIZIO and HIZDATA bits control the tristate modes of the E1XC . While the HIZIO bit is a logic 1, all output pins of the E1XC except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

Register 0CH: E1XC Revision/Chip ID

Bit	Type	Function	Default
Bit 7	R	TYPE	1
Bit 6	R	ID[6]	0
Bit 5	R	ID[5]	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	X

The version identification bits, ID[6:0], are set to a fixed value representing the version number of the E1XC. ID[6:0] = 0000000 binary indicates the E1XC rev A. ID[6:0] = 0000001 binary indicates the E1XC rev B.

The chip identification bit, TYPE, is set to logic 1 representing the E1XC.

Register 0DH: E1XC Master Reset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RESET	0

RESET:

The RESET bit implements a software reset. If the RESET bit is a logic 1, the entire E1XC is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the E1XC out of reset. Holding the E1XC in a reset state effectively puts it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

Register 0EH: E1XC Phase Status Word (LSB)

Bit	Type	Function	Default
Bit 7	R	PSB[7]	X
Bit 6	R	PSB[6]	X
Bit 5	R	PSB[5]	X
Bit 4	R	PSB[4]	X
Bit 3	R	PSB[3]	X
Bit 2	R	PSB[2]	X
Bit 1	R	PSB[1]	X
Bit 0	R	PSB[0]	X

This register contains the least significant byte, PSB[7:0], of the 9-bit phase status word. The 9-bit phase status word indicates the relative phase difference between the received E-1 line timing (available on RCLKO) and system timing. By utilizing the value of the phase status word, the system timing can be locked to the receive line timing via an external software controlled phase-locked-loop.

The least significant 8 bits contained in this register indicate a count value (0-255) of the number of system backplane clock cycles between successive 125µs frame pulses. The most significant 5 bits (PSB[7:3]) represent a time slot number (0-31) and the least significant 3 bits (PSB[2:0]) represent the bit number within the timeslot (0-7). The count value corresponds to the location within the system frame where the receive line-timed frame pulse occurred. If the received line clock frequency is higher on average than the system clock frequency, the phase status word value will be seen to decrease during successive register reads. If the received line clock frequency is lower on average than the system clock frequency, the phase status word value will be seen to increase during successive register reads.

The 9th bit of the Phase Status Word indicates the "frame count" and will toggle when two successive 8-bit counter values straddle a frame boundary. The PSB[8] bit will toggle when the bit and timeslot count indicated by PSB[7:0] exceeds timeslot 31, bit 7 or the count goes below timeslot 0, bit 0. This is determined by comparing the PSB[7:6] bits of the current phase status word value to those of the previous word value; PSB[8] is toggled only under the following conditions (all other bit value transitions leave PSB[8] unchanged):

Previous PSB[7:6]	Current PSB[7:6]	Effect on PSB[8]
00	11	toggle
11	00	toggle

The contents of the Phase Status Word registers (address 0EH and 0FH) are internally updated on each receive line data frame pulse; a write to either E1XC register address 0EH or 0FH must be performed to freeze the contents before this register and the Phase Status Word (MSB) register can be read. The correct sequence for reading the contents of the Phase Status Word are:

1. write to register address 0EH or 0FH

2. read register address 0FH (read Phase Status Word MSB)

3. read register address 0EH (read Phase Status Word LSB)

This write-before-read is analogous to the latching of performance monitor counter values in PMON, and is required to ensure that the phase status word value remains valid during the µP read. It is important to read the MSB register before the LSB register because, once the Phase Status Word (LSB) register has been read, the phase status word counter is unfrozen and the contents may change immediately.

Register 0FH: E1XC Phase Status Word (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	PSB[8]	X

This register contains the most significant bit of the 9-bit phase status word.

The PSB[8] bit toggles when the bit and timeslot count (from the Phase Status Word LSB register) exceeds time slot 31, bit 7 or goes below time slot 0, bit 0.

The contents of the Phase Status Word registers (address 0EH and 0FH) are internally updated on each receive line data frame pulse; a write to either E1XC register address 0EH or 0FH must be performed to freeze the contents before this register and the Phase Status Word (MSB) register can be read. The correct sequence for reading the contents of the Phase Status Word are:

1. write to register address 0EH or 0FH
2. read register address 0FH (read Phase Status Word MSB)
3. read register address 0EH (read Phase Status Word LSB)

This write-before-read is analogous to the latching of performance monitor counter values in PMON, and is required to ensure that the phase status word value remains valid during the µP read. It is important to read the MSB register before the LSB register because, once the Phase Status Word (LSB) register has been read, the phase status word counter is unfrozen and the contents may change immediately.

Register 10H: CDRC Block Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6	R/W	LOS1	0
Bit 5	R/W	LOS0	0
Bit 4	R/W	DCR	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ALGSEL	0
Bit 1	R/W	O162	0
Bit 0		Unused	X

AMI:

The active high AMI bit disables HDB3 decoding. With AMI low, an HDB3 signature on the RP and RN inputs is substituted with four zeros on the DRPCM output. The AMI bit has no affect on the RPCM output.

LOS1, LOS0

The loss of signal threshold is set by the state of the AMI, LOS1 and LOS0 bits:

AMI	LOS1	LOS0	Threshold (PCM periods)
0	0	0	10
1	0	0	15
X	0	1	31
X	1	0	63
X	1	1	175

If the number of consecutive spaces exceeds the programmed threshold, loss of signal is declared.

DCR:

Asserting the DCR bit disables clock recovery. With DCR high, the recovered clock (RCLKO) is derived from RCLKI instead of being recovered from the RDP and RDN inputs.

Reserved:

The reserved bit must be cleared to logic 0 for correct operation.

ALGSEL:

The algorithm select (ALGSEL) bit determines the DPLL phase adjustment algorithm. A logic 0 selects the original phase adjustment algorithm which has 0.41 UIpp of high frequency jitter tolerance. When ALGSEL is logic 1, the high frequency jitter tolerance is 0.50 UIpp, but the low frequency tolerance is approximately 20% lower than the first algorithm.

O162:

If the AMI bit is logic 0, the ITU-T Recommendation O.162 compatibility select bit (O162) allows selection between two line code definitions:

1. If O162 is a logic 0, a line code violation is indicated if the serial stream does not match the verbatim HDB3 definition given in Recommendation G.703. A bipolar violation that is not part of an HDB3 signature or a bipolar violation in an HDB3 signature that is the same polarity as the last bipolar violation results in a line code violation indication.

2. If O162 is a logic 1, a line code violation is indicated if a bipolar violation is of the same polarity as the last bipolar violation, as per ITU-T Recommendation O.162.

Register 11H: CDRC Block Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LCVE	0
Bit 6	R/W	LOSE	0
Bit 5	R/W	HDB3E	0
Bit 4	R/W	Z4DE	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The Interrupt Control Register is provided at CDRC read/write address 1.

The Z4DE, HDB3E, LOSE, and LCVE bits of this register are interrupt enable bits used to select which of the indications (four consecutive zeros, HDB3 pattern, loss of signal, or line code violation) will generate an interrupt when their status changes.

The occurrence of any of these events will generate an interrupt if there is a logic 1 in the corresponding bit position. When the E1XC is reset, Z4DE, HDB3E, LOSE, and LCVE bits are set to logic 0, disabling any interrupt generation.

Register 12H: CDRC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	LCVI	X
Bit 6	R	LOSI	X
Bit 5	R	HDB3I	X
Bit 4	R	Z4DI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOS	X

The LCVI, LOSI, HDB3I and Z4DI bits indicate which of the status events have occurred since the last read of this register. A logic 1 indicates the corresponding event was detected. These bits are cleared when the CDRC Status Register is read.

LCVI:

The LCVI bit is asserted if a line code violation is detected. If the AMI bit of the CDRC Configuration Register is a logic 1, LCVI becomes a logic 1 if two consecutive marks are of the same polarity (i.e. on the same pin, RDP or RDN). If the AMI and O162 bits of the CDRC Configuration Register is a logic 0, LCVI becomes a logic 1 if a bipolar violation (BPV) is of the same polarity as the previous BPV or if the BPV is not preceded by two spaces. If the AMI bit is a logic 0 and the O162 bit is a logic 1, LCVI becomes a logic 1 if two consecutive bipolar violations are of the same polarity.

LOSI:

The LOSI bit is set high when the LOS status bit changes state.

HDB3I:

The HDB3I bit is set high if an HDB3 signature, which is a bipolar violation of the opposite polarity of the previous bipolar violation following two spaces, is detected in the received data stream.

Z4DI:

The Z4DI bit is set high if four consecutive spaces occur.

LOS:

The LOS bit is the loss of signal status. It is a logic 1 if the number of consecutive spaces exceeds the programmed threshold. The status is deasserted upon the reception of a single mark.

Register 13H: Alternate Loss of Signal Status

Bit	Type	Function	Default
Bit 7	R/W	ALTLOSE	0
Bit 6	R	ALTLOSI	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ALTLOS	X

The alternate loss of signal status provides a more stringent criteria for the deassertion of the alarm.

ALTLOSE:

If the ALTLOSE bit is a logic 1, an interrupt is generated when the ALTLOS status bit changes state.

ALTLOSI:

The LOSI bit is set high when the ALTLOS status bit changes state. It is cleared when this register is read.

ALTLOS:

The ALTLOS bit is asserted when the number of consecutive zeros exceeds the threshold specified by the CDRC Configuration register. The ALTLOS bit is deasserted only after 255 bit periods during which no sequence of four zeros has been received.

Register 14H: XPLS Block Line Length Configuration

Bit	Type	Function	Default
Bit 7	R/W	RPT	0
Bit 6	R/W	SM	0
Bit 5	R	1	1
Bit 4	R	0	0
Bit 3	R	0	0
Bit 2	R/W	ILS[2]	0
Bit 1	R/W	ILS[1]	0
Bit 0	R/W	ILS[0]	0

This register allows software to select the length of cable that XPLS is required to drive and to enable generation of user-programmable output templates.

RPT:

The RPT bit enables the 4-bit DAC codes contained in the Register Programmable Template CODE registers to generate the output waveform. When RPT is set to a logic 1, the internal user-programmable XPLS CODE registers supply the DAC codes used to generate the waveform. When RPT is set to logic 0, the DAC codes contained in the internal ROM generate the output waveform in accordance with the line length selected.

The internal ROM DAC codes are compatible with ITU-T G.703 provided that a 1:1.36 transformer is used in conjunction with external interface components per Figure 10. If a different external network is used, a user-programmable line build-out is necessary. The Operation Section contains the required details.

SM:

The SM bit allows software to select one of eight waveform templates by enabling the ILS[2:0] select bits. When SM is set to logic 1, the ILS[2:0] bit positions select one of eight waveform templates. When SM is set to logic 0, the ILS[2:0] bits are ignored and the default G.703 120 Ω waveform template is selected.

The eight available templates are selected via the following values of ILS[2:0]:

ILS[2:0]	Build-out
000	Reserved
001	Reserved
011	Reserved
010	Reserved
110	Reserved
111	Reserved
101	G.703 75 Ω
100	G.703 120 Ω

Register 15H: XPLS Block Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	TAIS	0
Bit 2	R	DPMV	X
Bit 1	R	DPMI	X
Bit 0	R/W	DPME	0

TAIS:

The TAIS bit enables the XPLS to generate an unframed all-ones AIS alarm on the TAP and TAN output pins. When TAIS is set to logic 1, the outputs are forced to pulse alternately, creating an all-ones signal. When TAIS is set to logic 0, the outputs operate normally. The transition to transmitting AIS is done in such a way as to not introduce any bipolar violations.

DPMV:

The DPMV bit reflects the current state of the DPM alarm signal.

DPMI:

The DPMI bit is set to logic 1 when any change of state occurs on the Driver Performance Monitor (DPM) alarm signal. This bit is cleared when the register is read.

DPME:

The DPME bit controls the generation of an interrupt on the microprocessor INTB pin by the driver performance monitor portion of XPLS. When DPME is set to logic 1, an interrupt is generated on INTB whenever an alarm condition occurs on the driver performance monitor points. A driver performance monitor alarm is declared whenever a period of 63 consecutive bit periods with no pulses on either the TAN or TAN output pins occurs. When DPME is set to logic 0, detection of a driver performance monitor alarm condition is disabled from generating an interrupt.

Register Register 16H: XPLS Block CODE Indirect Address

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	CRA2	0
Bit 1	R/W	CRA1	0
Bit 0	R/W	CRA0	0

This register allows software to select any one of the eight internal waveform CODE registers, addressed by the CRA[2:0] bits, for subsequent access through the CODE Indirect Data register. When accessing the internal CODE registers, the address of the desired register must first be written to this register. Then, by reading or writing the Indirect Data register (Register 17H), the microprocessor can either read from or write to the internal register identified by the CRA[2:0] bits.

The CRA[2:0] bits address the internal registers as follows:

Table 4 - XPLS Code Register Memory Map

CRA2	CRA1	CRA0	Internal Code Register
0	0	0	CODE register #0 - first code applied
0	0	1	CODE register #1
0	1	0	CODE register #2
0	1	1	CODE register #3
1	0	0	CODE register #4
1	0	1	CODE register #5
1	1	0	CODE register #6
1	1	1	CODE register #7 - last code applied

See the Operation section for more details on setting up custom waveform templates.

Register 17H: XPLS Block CODE Indirect Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	CRD3	0
Bit 2	R/W	CRD2	0
Bit 1	R/W	CRD1	0
Bit 0	R/W	CRD0	0

This register allows software to access the contents of any one of the eight internal waveform CODE registers, addressed by the CRA[2:0] bits in the CODE Indirect Address register. When accessing the internal CODE registers, the address of the desired register must first be written to the Indirect Address register (Register 16H). Then, by reading or writing the Indirect Data register, the microprocessor can either read from or write to the internal register identified by the CRA[2:0] bits.

The value read from or written to the internal CODE registers is contained in the CRD[3:0] bits. CRD3 is the most significant bit.

See the Operation section for more details on setting up custom waveform templates.

Register 18H: DJAT Block Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	X
Bit 0	R	UNDI	X

This register contains the indication of the DJAT FIFO status.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred.

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred.

Register 19H: DJAT Block Reference Clock Divisor (N1) Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

This register defines an 8-bit binary number, N1, which is one less than the magnitude of the divisor used to scale down the DJAT PLL reference clock input. The REF divisor magnitude, (N1+1), is the ratio between the frequency of REF input and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit in the DJAT Configuration register is high, will also reset the FIFO.

Upon reset of the E1XC, the default value of N1 is set to decimal 47 (2FH).

Consult the Operations section for clarification of divisor selection criteria.

Register 1AH: DJAT Block Output Clock Divisor (N2) Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

This register defines an 8-bit binary number, N2, which is one less than the magnitude of the divisor used to scale down the DJAT smooth output clock signal. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit is high, will also reset the FIFO.

Upon reset of the E1XC, the default value of N2 is set to decimal 47 (2FH).

Consult the Operations section for clarification of divisor selection criteria.

Register 1BH: DJAT Block Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	WIDEN	1
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	SYNC	1
Bit 0	R/W	LIMIT	1

This register controls the operation of the DJAT FIFO read and write pointers and controls the generation of interrupt by the FIFO status.

WIDEN:

The WIDEN bit controls the width of the generated pulse from the XPLS block. When WIDEN is set to logic 1, the high phase of one cycle of the 16.384 MHz clock generated by the DJAT PLL is modified to be nominally 20ns wider. This results in the XPLS producing a greater pulse width. When WIDEN is set to logic 0, the 16.384MHz clock from DJAT is not modified, resulting in pulses of approximately 50% duty cycle. These narrow pulses reduce the amount of energy sourced by E1XC into the line. The WIDEN bit has no effect when the DJAT PLL is not used (i.e. the SMCLKO bit in register 7 is set to logic 1).

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, then the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions. CENT can only be set to logic 1 if SYNC is logic 0.

OVRE,UNDE:

The OVRE and UNDE bits control the generation of an interrupt on the microprocessor INTB pin when a FIFO error event occurs. When OVRE or UNDE is set to logic 1, an overrun event or underrun event, respectively, is allowed to generate an interrupt on the INTB pin. When OVRE or UNDE is set to logic 0, the FIFO error events are disabled from generating an interrupt.

SYNC:

The SYNC bit enables the PLL to synchronize the phase delay between the FIFO input and output data to the phase delay between reference clock input and smooth output clock at the PLL. For example, if the PLL is operating so that the smooth output clock lags the reference clock by 24 UI, then the synchronization pulses that the PLL sends to the FIFO will force its output data to lag its input data by 24 UI.

LIMIT:

The LIMIT bit enables the PLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one unit interval (UI) of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 1, the PLL jitter attenuation is limited. When LIMIT is set to logic 0, the PLL is allowed to operate normally.

Upon reset of the E1XC, the LIMIT and SYNC bits are set to logic 1, and the OVRE, UNDE, and CENT bits are set to logic 0.

Register 1CH: ELST Configuration

Bit	Type	Function	Default
Bit 7	R/W	ACCEL	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IR	1
Bit 0	R/W	OR	1

This register controls the format of the expected input frame to the ELST block and the format of the generated output frame from the ELST block.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

IR:

The IR bit selects the input frame format. The IR bit must be set to logic 1 to properly handle the E1 frame format being input into the ELST. SETTING IR TO LOGIC 0 IS A RESERVED SETTING AND SHOULD NOT BE USED.

OR:

The OR bit selects the output frame format. The OR bit must be set to logic 1 to properly generate the E1 frame format output from the ELST. SETTING OR TO LOGIC 0 IS A RESERVED SETTING AND SHOULD NOT BE USED.

Register 1DH: ELST Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	SLIPE	0
Bit 1	R	SLIPD	X
Bit 0	R	SLIPI	X

SLIPE:

The SLIPE bit position is an interrupt enable that when set, allows the INT output to go HIGH when a slip occurs. When the block is reset the SLIPE bit position is cleared and interrupt generation is disabled.

SLIPD:

The SLIPD bit indicates the direction of the last slip. If the Interrupt Status Register is read and the SLIPD bit is a logic 1 then the last slip was due to the frame buffer becoming full. If the Interrupt Status Register is read and the SLIPD bit is a logic 0 then the last slip was due to the frame buffer becoming empty.

SLIPI:

The SLIPI bit is set if a slip occurred since the last read of the Interrupt Status register. The SLIPI bit is cleared just after the Interrupt Status register read operation.

Register 1EH: ELST Idle Code

Bit	Type	Function	Default
Bit 7	R/W	D7	1
Bit 6	R/W	D6	1
Bit 5	R/W	D5	1
Bit 4	R/W	D4	1
Bit 3	R/W	D3	1
Bit 2	R/W	D2	1
Bit 1	R/W	D1	1
Bit 0	R/W	D0	1

The contents of the IDLE CODE register replace the timeslot data in the BRPCM serial data stream when the framer is out of frame and the TRKEN bit in the E1 Configuration Register is a logic 1. Since the transmission of all ones timeslot data is a common requirement, the IDLE CODE register is set to all ones when the CBI reset signal is active. Bit 7 is the first to be transmitted.

The writing of the idle code pattern is asynchronous with respect to the output data clock. One timeslot of idle code data will be corrupted if the register is written to when the framer is out of frame.

Register Register 20H: FRMR Frame Alignment Options

Bit	Type	Function	Default
Bit 7	R/W	CRCEN	0
Bit 6	R/W	CASDIS	0
Bit 5	R/W	AFAA	0
Bit 4	R/W	CHKSEQ	0
Bit 3	R/W	CASA	0
Bit 2	R/W	REFR	0
Bit 1	R/W	REFCRCE	0
Bit 0	R/W	REFRDIS	0

This register selects the various framing formats and framing algorithms supported by the FRMR block.

CRCEN:

The CRCEN bit enables the FRMR to frame to the CRC multiframe. When the CRCEN bit is logic 1, the FRMR searches for CRC multiframe alignment and monitors for errors in the alignment. A logic 0 in the CRCEN bit position disables searching for multiframe and suppresses the OOCMF, CRCE, CMFER, and FEBE FRMR statuses, forcing them to logic 0.

CASDIS:

The CASDIS bit enables the FRMR to frame to the Channel Associated Signalling multiframe when set to a logic 0. When CAS is enabled, the FRMR searches for signalling multiframe alignment and monitors for errors in the alignment. A logic 1 in the CASDIS bit position disables searching for multiframe and suppresses the OOSMF and the SMFER FRMR outputs, forcing them to logic 0.

AFAA:

The AFAA bit enables an alternate framing algorithm. If AFAA is a logic zero, frame alignment is declared after a correct FAS, a logic 1 in bit 2 of time slot 0 of the next frame and finally another FAS in the third frame are found. If one of the conditions fails, the next bit position is checked for valid framing. If AFAA is a logic one, the framing is similar to the above, but adds a "hold-off" feature. If bit2 or the second 7-bit FAS conditions fail, the same byte location is checked again in the subsequent frames before checking the next bit position for frame alignment.

CHKSEQ:

The CHKSEQ bit enables the use of the check sequence to verify the correct frame alignment in the presence of random imitative frame alignment signals. A logic 1 in the CHKSEQ bit position enables the use of the check sequence algorithm in addition to the basic frame find algorithms; a logic 0 disables the use of the check sequence algorithm.

CASA:

The CASA bit selects one of the two algorithms used to find Channel Associated Signalling multiframe alignment. A logic 0 in the CASA bit position selects the G.732-compatible algorithm; a logic 1 selects the alternate framing algorithm.

REFR:

A transition from logic 0 to logic 1 in the REFR bit position forces the re-synchronization to a new frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to generate subsequent re-synchronizations.

REFCRCE:

The REFCRCE bit enables excessive CRC errors (≥ 915 errors in one second) to force a re-synchronization to a new frame alignment. Setting the REFCRCE bit position to logic 1 enables reframe due to excessive CRC errors; setting the REFCRCE bit to logic 0 disables CRC errors from causing a reframe.

REFRDIS:

The REFRDIS bit disables reframing under any error condition once frame alignment has been found; reframing can be initiated by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur based on the various error criteria (FER, excessive CRC errors, etc.).

Register 21H: FRMR Maintenance Mode Options

Bit	Type	Function	Default
Bit 7	R/W	FASC	0
Bit 6	R/W	BIT2C	0
Bit 5	R/W	SMFASC	0
Bit 4	R/W	T16C	0
Bit 3	R/W	RADEB	0
Bit 2	R/W	RMADEB	0
Bit 1	R	CMFACT	X
Bit 0	R	EXCRCE	X

FASC:

The FASC bit selects the criterion used to declare loss of frame alignment signal: a logic 0 in the FASC bit position enables declaration of loss of frame alignment when 3 consecutive frame alignment patterns have been received in error; a logic 1 in the FASC bit position enables declaration of loss of frame when 4 consecutive frame alignment pattern errors are detected.

BIT2C:

The BIT2C bit enables the additional criterion that loss of frame is declared when bit 2 in time slot 0 of NFAS frames has been received in error on 3 consecutive occasions: a logic 1 in the BIT2C position enables declaration of loss of frame alignment when bit 2 is received in error; a logic 0 in BIT2C enables declaration of loss of frame alignment based on the setting of FASC, only.

SMFASC:

The SMFASC bit selects the criterion used to declare loss of signalling multiframe alignment signal: a logic 0 in the SMFASC bit position enables declaration of loss of signalling multiframe alignment when 2 consecutive multiframe alignment patterns have been received in error; a logic 1 in the SMFASC bit position enables declaration of loss of signalling multiframe when 2 consecutive multiframe alignment patterns have been received in error or when time slot 16 contains logic 0 in all bit positions for 1 or 2 multiframes based on the criterion selected by T16C.

T16C:

The T16C bit selects the criterion used to declare loss of signalling multiframe alignment signal when enabled by the SMFASC: a logic 0 in the T16C bit position enables declaration of loss of signalling multiframe alignment when time slot 16 contains logic 0 in all bit positions for 1 multiframe; a logic 1 in the T16C bit position enables declaration of loss of signalling multiframe when time slot 16 contains logic 0 in all bit positions for 2 consecutive signalling multiframes.

RADEB:

The RADEB bit selects the amount of debouncing applied to the Remote Alarm Indication before the RRA is allowed to change state: a logic 0 in the RADEB bit position enables the RRA output to change to the logic value contained in the Remote Alarm bit position (bit 3 of NFAS frames) when the received Remote Alarm bit value has been in the same state for 2 consecutive NFAS frames; a logic 1 in the RADEB bit position enables the RRA output to change when the Remote Alarm bit has been in the same state for 3 consecutive NFAS frames.

RMADEB:

The RMADEB bit selects the amount of debouncing applied to the Remote Signalling Multiframe Alarm Indication before the RRMA is allowed to change state: a logic 0 in the RMADEB bit position enables the RRMA output to change to the logic value contained in the Remote Signalling Multiframe Alarm bit position (bit 6 of time slot 16 of frame 0 of the signalling multiframe) when the received Remote Signalling Multiframe Alarm bit value has been in the same state for 2 consecutive signalling multiframes; a logic 1 in the RMADEB bit position enables the RRMA output to change when the Remote Signalling Multiframe Alarm bit has been in the same state for 3 consecutive signalling multiframes.

CMFACT:

The CMFACT bit is an active high status bit indicating that the CRC Multiframe Find algorithm has been active for more than 8ms, thereby initiating a reframe if the CRCEN bit is set to logic 1. The CMFACT bit is reset to logic 0 after the register is read.

EXCRCE:

The EXCRCE bit is an active high status bit indicating that excessive CRC evaluation errors (i.e. ≥915 error in one second) have occurred, thereby initiating a reframe if enabled by the REFCRCE bit of the Frame Alignment Options register. The EXCRCE bit is reset to logic 0 after the register is read.

Register 22H: FRMR Framing Status Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	OOFE	0
Bit 5	R/W	OOSMFE	0
Bit 4	R/W	OOCMFE	0
Bit 3	R/W	COFAE	0
Bit 2	R/W	FERE	0
Bit 1	R/W	SMFERE	0
Bit 0	R/W	CMFERE	0

OOFE, OOSMFE and OOCMFE:

A logic one in bits OOFE, OOSMFE and OOCMFE enables the generation of an interrupt on a change of state of OOF, OOSMF and OOCMF bits of the FRMR Framing Status register.

COFAE:

A logic one in the COFAE bit enables the generation of an interrupt when the position of the frame alignment has changed.

FERE:

A logic one in the FERE bit enables the generation of an interrupt when an error has been detected in the frame alignment signal.

SMFERE:

A logic one in the SMFERE bit enables the generation of an interrupt when an error has been detected in the signalling multiframe alignment signal.

CMFERE:

A logic one in the CMFERE bit enables the generation of an interrupt when an error has been detected in the CRC multiframe alignment signal.

Register 23H: FRMR Maintenance/Alarm Status Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	RRAE	0
Bit 6	R/W	RRMAE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	T16AISDE	0
Bit 3	R/W	REDE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	FEBEE	0
Bit 0	R/W	CRCEE	0

RRAE, RRMAE, AISDE, T16AISDE, REDE and AISE:

A logic one in bits RRAE, RRMAE, AISDE, T16AISDE, REDE or AISE enables the generation of an interrupt on a change of state of the RRA, RRMA, AISD, T16AISD, RED and AIS bits of the FRMR Maintenance/Alarm Status register.

FEBEE:

When the FEBEE bit is a logic one, an interrupt is generated when a logic zero is received in the Si bits of frames 13 or 15.

CRCEE:

When the CRCEE bit is a logic one, an interrupt is generated when calculated CRC differs from the received CRC remainder.

Register 24H: FRMR Framing Status Interrupt Indication

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	OOFI	X
Bit 5	R	OOSMFI	X
Bit 4	R	OOCMFI	X
Bit 3	R	COFAI	X
Bit 2	R	FERI	X
Bit 1	R	SMFERI	X
Bit 0	R	CMFERI	X

A logic 1 in any bit position of this register indicates which framing status generated an interrupt by changing state.

OOFI, OOSMFI, OOCMFI, and COFAI:

OOFI, OOSMFI, OOCMFI, and COFAI indicate when the corresponding status has changed state from logic 0 to logic 1 or vice-versa.

FERI, SMFERI, CMFERI:

FERI, SMFERI, CMFERI indicate when a framing error, signalling multiframe error or CRC multiframe error event has been detected; these bits will be set if one or more errors have occurred since the last register read.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read; the interrupt is also cleared if it was generated by any of the Framing Status outputs.

Register 25H: FRMR Maintenance/Alarm Status Interrupt Indication

Bit	Type	Function	Default
Bit 7	R	RRAI	X
Bit 6	R	RRMAI	X
Bit 5	R	AISDI	X
Bit 4	R	T16AISDI	X
Bit 3	R	REDI	X
Bit 2	R	AISI	X
Bit 1	R	FEBEI	X
Bit 0	R	CRCEI	X

A logic 1 in any bit position of this register indicates which maintenance or alarm status generated an interrupt by changing state.

RRAI, RRMAI, AISDI, T16AISDI, REDI, and AISI:

RRAI, RRMAI, AISDI, T16AISDI, REDI, and AISI indicate when the corresponding FRMR Maintenance/Alarm Status register bit has changed state from logic 0 to logic 1 or vice-versa.

FEBEI:

The FEBEI bit becomes a logic one when a logic zero is received in the Si bits of frames 13 or 15.

CRCEI:

The CRCEI bit becomes a logic one when a calculated CRC differs from the received CRC remainder.

The bits in this register are set by a single error event.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read; the interrupt is also cleared if it was generated by any of the Maintenance/Alarm Status events.

Register 26H: FRMR Framing Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	OOF	X
Bit 5	R	OOSMF	X
Bit 4	R	OOCMF	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Reading this register returns the current state value of the OOF, OOSMF and OOCMF FRMR framing statuses.

OOF:

The OOF bit is a logic one when basic frame alignment has been lost. The OOF bit goes to a logic zero once frame alignment has been regained.

OOSMF:

The OOSMF bit is a logic one when the signalling multiframe alignment has been lost. The OOSMF bit becomes a logic zero once signalling multiframe has been regained.

OOCMF:

The OOCMF bit is a logic one when the CRC multiframe alignment has been lost. The OOCMF bit becomes a logic zero once CRC multiframe has been regained.

Register 27H: FRMR Maintenance/Alarm Status

Bit	Type	Function	Default
Bit 7	R	RRA	X
Bit 6	R	RRMA	X
Bit 5	R	AISD	X
Bit 4	R	T16AISD	X
Bit 3	R	RED	X
Bit 2	R	AIS	X
Bit 1		Unused	X
Bit 0		Unused	X

Reading this register returns the current state value of the RRA, RRMA, AISD, T16AISD, RED, and AIS maintenance/alarm statuses.

RRA:

The RRA bit is a logic one when the "A" bit (bit 3 in time slot 0 of the non-frame alignment signal frame) has been a logic one for 2 or 3 consecutive non-frame alignment signal frames, as determined by the RADEB bit. The RRA output is updated every two frames.

RRMA:

The RRMA bit is a logic one when the "Y" bit (bit 6 in time slot 16 in frame 0 of the signalling multiframes) has been a logic one for 2 or 3 consecutive signalling multiframes, as determined by the RMADEB bit.. The RRMA bit is updated every 16 frames.

AISD:

The AISD bit is a logic one after an unframed pattern of all ones with less than 3 zeros in two consecutive frame times (512 bits) has been detected. The AISD bit is updated every 512 bit times.

T16AISD:

The T16AISD is a logic one after an all-ones byte has been detected in time slot 16 for 2 consecutive frames while out of signalling multiframe alignment.

RED:

The RED bit is a logic one if an out of frame condition has persisted for 100 ms. The RED bit returns to a logic zero when a out of frame condition has been absent for 100 ms.

AIS:

The AIS bit is a logic one when an out of frame all-ones condition has persisted for 100 ms. The AIS bit returns to a logic zero when the AIS condition has been absent for 100 ms.

Register 28H: FRMR International/National Bits

Bit	Type	Function	Default
Bit 7	R	Si1	X
Bit 6	R	Si0	X
Bit 5	R	RAWRA	X
Bit 4	R	Sn0	X
Bit 3	R	Sn1	X
Bit 2	R	Sn2	X
Bit 1	R	Sn3	X
Bit 0	R	Sn4	X

Reading this register returns the current bit value of the International and National bits collected over 2 consecutive frames. The Si1 bit position corresponds to the value contained in the International bit position in the FAS frame; the Si0, RAWRA, and Sn[4:0] bit positions correspond to the values contained in the International, Remote Alarm Indication, and National bit positions in the NFAS frame. This register is updated after time slot 0 of every NFAS frame and the contents are valid for 2 frames (250µs). The contents of this register are latched during the read, however the individual bits should not be considered to constitute a byte value (i.e. the 5 national bits should not be considered as indicating 1 of 32 possible values since it is possible that the individual bits are not all from the same time instant due to the asynchronous nature of the microprocessor reads). If the bits are to be interpreted as binary values, care should be taken to ensure a coherent set of bit values by reading the register at least twice.

The Si0, RAWRA and Sn0-Sn4 bits map to the TSO NFAS as follows:

Bit Position							
1	2	3	4	5	6	7	8
Si0	1	RAWRA	Sn0	Sn1	Sn2	Sn3	Sn4

Note that the TXSAEN[8:4] bits in the E1XC Transmit Framing Options Register (Register 06H) can cause a datalink to overwrite some or all of the National Use Bits.

Register 29H: FRMR Extra Bits

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	X3	X
Bit 2	R	RAWRMA	X
Bit 1	R	X1	X
Bit 0	R	X0	X

Reading this register returns the current bit value of the Extra bits and the Remote Signalling Multiframe Alarm collected from time slot 16 of frame 0 of signalling multiframes. The X3, RAWRMA, X1, X0 bit positions corresponds to the value contained in bit positions 5, 6, 7, and 8 in time slot 16 of frame 0 of the signalling multiframe. This register is updated once per signalling multiframe (the contents remain valid for 2ms). If the X3, X1, X0 bits are to be interpreted as binary values, care should be taken to ensure a coherent set of bit values by reading the register at least twice.

Register 2AH: FRMR CRC Error Counter – LSB

Bit	Type	Function	Default
Bit 7	R	CRCE7	X
Bit 6	R	CRCE6	X
Bit 5	R	CRCE5	X
Bit 4	R	CRCE4	X
Bit 3	R	CRCE3	X
Bit 2	R	CRCE2	X
Bit 1	R	CRCE1	X
Bit 0	R	CRCE0	X

This register contains the least significant byte of the 10-bit CRC error counter value, updated every second.

Register 2BH: FRMR CRC Error Counter – MSB

Bit	Type	Function	Default
Bit 7	R	OVR	X
Bit 6	R	NEWDATA	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CRCE9	X
Bit 0	R	CRCE8	X

This register contains the most significant two bits of the 10-bit CRC error counter value, updated every second.

NEWDATA:

The NEWDATA flag bit indicates that the counter register contents have been updated with a new count value accumulated over the last 1 second interval. It is set to logic 1 when the CRC error counter data is transferred into the counter registers, and is reset to logic 0 when this register is read. This bit can be polled to determine the 1 second timing boundary used by the FRMR.

OVR:

The OVR flag bit indicates that the counter register contents have not been read within the last 1 second interval, and therefore have been over-written. It is set to logic 1 if CRC error counter data is transferred into the counter registers before the previous data has been read out, and is reset to logic 0 when this register is read.

This CRC error count is distinct from that of PMON because it is guaranteed to be an accurate count of the number of CRC error in one second; whereas, PMON relies on externally initiated transfers which may not be one second apart.

Register 2CH: TS16 AIS Alarm Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	TS16AISE	0
Bit 5	R	TS16AISI	X
Bit 4	R	TS16AIS	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Reading this register returns the current value of the time slot 16 AIS status.

The TS16 AIS alarm algorithm accumulates the occurrences of T16AISD (TS16 AIS detection) events. T16AISD is defined as two consecutive all ones time slot 16 bytes while out of signalling multiframe. Each interval with a valid TS16 AIS presence indication increments an interval counter which declares TS16 AIS Alarm when 22 valid intervals have been accumulated. An interval with no valid TS16 AIS presence indication decrements the interval counter; the TS16 AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.1% probability of declaring an TS16 AIS Alarm within 3.1 ms after loss of signalling multiframe detection in the presence of a 10^{-3} mean bit error rate.

TS16AISE:

If the TS16AISE bit is a logic 1, an interrupt is generated when the TS16AIS status bit changes state.

TS16AISI:

The TS16AISI bit is set high when the TS16AIS status bit changes state. It is cleared when this register is read.

TS16AIS:

The TS16AIS bit is a logic one when an all ones condition has persisted in time slot 16 for 3 ms. The bit returns to a logic zero when the time slot 16 AIS condition has been absent for 3 ms.

Register 30H: TPSC Block Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

This register allows selection of the microprocessor read access type and output enable control for the Transmit Per-channel Serial Controller.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the E1XC is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-timeslot functions. When the PCCE bit is set to a logic 1, each timeslot's Data Control byte and IDLE Code byte are passed on to the TRAN block. When the PCCE bit is set to logic 0, the per-timeslot functions are disabled.

Register 31H: TPSC Block µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

BUSY:

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 480 ns.

Register 32: TPSC Block Timeslot Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

This register allows the µP to access the internal TPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal TPSC register is requested; when R/WB is set to a logic 0, an write to the internal TPSC register is requested.

The reserved bit must be set to 0 for proper operation.

Register 33H: TPSC Block Timeslot Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D7	0
Bit 6	R/W	D6	0
Bit 5	R/W	D5	0
Bit 4	R/W	D4	0
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

This register contains either the data to be written into the internal TPSC registers when a write request is initiated or the data read from the internal TPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 480 ns, this register will contain the requested data byte.

The internal TPSC registers control the per-timeslot functions on the Transmit PCM data, provide the per-timeslot Transmit IDLE Code, and provide the per-timeslot Transmit signalling control and the alternate signalling bits. The functions are allocated within the registers as follows:

Table 5 - TPSC Indirect Memory Map

20H	Data Control byte for Time Slot 0
21H	Data Control byte for Time Slot 1
22H	Data Control byte for Time Slot 2
•	•
•	•
•	•
3EH	Data Control byte for Time Slot 30

3FH	Data Control byte for Time Slot 31
40H	IDLE Code byte for Time Slot 0
41H	IDLE Code byte for Time Slot 1
42H	IDLE Code byte for Time Slot 2
•	•
•	•
•	•
5EH	IDLE Code byte for Time Slot 30
5FH	IDLE Code byte for Time Slot 31

The bits within each control byte are allocated as follows:

TPSC Internal Registers 20-3FH: Data Control byte

Bit	Type	Function
Bit 7	R/W	SUBS
Bit 6	R/W	DS[0]
Bit 5	R/W	DS[1]
Bit 4	R/W	SIGSRC
Bit 3	R/W	A'
Bit 2	R/W	B'
Bit 1	R/W	C'
Bit 0	R/W	D'

SUBS, DS[1], and DS[0]:

The SUBS, DS[1], and DS[0] bits select one of the following data manipulations to be performed on the timeslot:

SUBS	DS[0]	DS[1]	Function
0	0	0	OFF - no change to PCM timeslot data
0	0	1	ADI - data inversion on timeslot bits 1,3,5,7
0	1	0	ADI - data inversion on timeslot bits 2,4,6,8
0	1	1	INV - data inversion on all timeslot bits
1	0	X	Data substitution on - IDLE code replaces PCM timeslot data
1	1	0	Data substitution on - A-Law digital milliwatt pattern* replaces TPCM timeslot data.
1	1	1	Data substitution on - µ-Law digital milliwatt pattern* replaces TPCM timeslot data.

* The A-Law digital milliwatt pattern used is that defined in Recommendation G.711 for A-law:

Table 6 - A-law Digital Milliwatt Pattern

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
0	0	1	1	0	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	0	0
1	0	1	1	0	1	0	0
1	0	1	0	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	0	0

* The µ-Law digital milliwatt pattern used is that defined in Recommendation G.711 for µ-law:

Table 7 - µ-law Digital Milliwatt Pattern

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
0	0	0	1	1	1	1	0
0	0	0	0	1	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	1	1	1	0
1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	1	1	1	0

SIGSRC:

The SIGSRC bit is valid only if Channel Associated Signalling (CAS) is selected in the Configuration Register; otherwise, it is ignored. When valid, the SIGSRC bit selects the source of the timeslot signalling bits: if SIGSRC is a logic 0, the signalling bits are taken from the incoming BTSIG stream in the format specified by the SIGEN and DLEN bits in the Configuration Register; if SIGSRC is a logic 1, the signalling bits are taken from the A',B',C', and D' bit .

TPSC Internal Registers 40-5FH: IDLE Code byte

Bit	Type	Function
Bit 7	R/W	IDLE7
Bit 6	R/W	IDLE6
Bit 5	R/W	IDLE5
Bit 4	R/W	IDLE4
Bit 3	R/W	IDLE3
Bit 2	R/W	IDLE2
Bit 1	R/W	IDLE1
Bit 0	R/W	IDLE0

The contents of the IDLE Code byte register are substituted for the timeslot data on BTPCM when the SUBS bit in the PCM Control Byte is set to a logic 1 and the DS[0] bit in the PCM Control Byte is set to a logic 0. The IDLE Code is transmitted from MSB (bit 7) to LSB (bit 0).

Register 34H: XFDL Block Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	EOM	0
Bit 3	R/W	INTE	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	0
Bit 0	R/W	EN	0

EN:

The enable bit (EN) controls the overall operation of the XFDL block. When the EN bit is set to a logic 1, the XDFL block is enabled and flag sequences are sent until data is written into the Transmit Data register. When the EN bit is set to logic 0, the XFDL block is disabled.

CRC:

The CRC enable bit controls the generation of the ITU-T-CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the ITU-T-CRC generator and the appends the 16 bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the ITU-T-CRC with generator polynomial = $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 11111110 code to be transmitted after the last byte from the Transmit Data Register is transmitted. Aborts are continuously sent until this bit is reset to a logic 0.

INTE:

The INTE bit enables the generation of an interrupt via the TDLINT output. Setting the INTE bit to logic 1 enables the generation of an interrupt; setting INTE to logic 0 disables the generation of an interrupt. If the TDLINTE bit is also set to logic 1 in the Datalink Options register, the interrupt generated on the TDLINT output is also generated on the microprocessor INTB pin.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared before transmission of the next data packet begins.

Register 35H: XFDL Block Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	INT	X
Bit 0	R/W	UDR	0

INT:

The INT bit indicates when the XFDL block is ready to accept a new data byte for transmission. The INT bit is set to a logic 1 when the previous byte in the Transmit Data register has been loaded into the parallel to serial converter and a new byte can be written into the Transmit Data register. The INT bit is set to a logic 0 while new data is in the Transmit Data register. The INT bit is not disabled by the INTE bit in the configuration register.

UDR:

The UDR bit indicates when the XFDL block has underrun the data in the Transmit Data register. The UDR bit is set to a logic 1 if the parallel to serial conversion of the last byte in the Transmit Data register has completed before the new byte was written into the Transmit Data register. Once an underrun has occurred, the XFDL transmits an ABORT, followed by a flag, and waits to transmit the next valid data byte. If the UDR bit is still set after the transmission of the flag the XFDL will continuously transmit the all-ones idle pattern. The UDR bit can only be cleared by writing a logic 0 to the UDR bit position in this register.

Register 36H: XFDL Block Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD7	X
Bit 6	R/W	TD6	X
Bit 5	R/W	TD5	X
Bit 4	R/W	TD4	X
Bit 3	R/W	TD3	X
Bit 2	R/W	TD2	X
Bit 1	R/W	TD1	X
Bit 0	R/W	TD0	X

Data written to this register is serialized and transmitted on the facility data link least significant bit first. The XFDL block signals when the next data byte is required by setting the TDLINT output high (if enabled) and by setting the INT bit in the Status register high. When INT and/or TDLINT is set, the Transmit Data register must be written with the new data within 4 data bit periods to prevent the occurrence of an underrun.

Register 38H: RFDL Block Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN:

The enable bit (EN) controls the overall operation of the RFDL block. When set, the RDFL block is enabled; when reset the RFDL block is disabled. When the block is disabled, the FIFO and interrupts are all cleared, however, the programming of the Enable/Status Register is not affected. When the block is enabled, it will immediately begin looking for flags.

TR:

Setting the terminate reception bit (TR) forces the RFDL block to immediately terminate the reception of the current LAPD frame, empty the FIFO, clear the interrupts, and begin searching for a new flag sequence. The RFDL handles the TR input in the same manner as if the EN bit had been cleared and then set. The TR bit in the Configuration register will reset itself after a rising and falling edge have occurred on the CLK input to the RFDL block once the write to this register has completed and WRB goes inactive. If the Configuration register is read after this time, the TR bit value returned will be zero.

The RFDL block handles the TR input in the same manner as clearing and setting the EN bit, therefore, the RFDL state machine will begin searching for flags and an interrupt will be generated when the first flag is detected.

Register 39H: RFDL Block Interrupt Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTC1	0
Bit 1	R/W	INTC0	0
Bit 0	R	INT	0

INTC1,INTC0:

The INTC1 and INTC0 bits control when an interrupt is asserted based on the number of received data bytes in the FIFO as follows:

INTC1	INTC0	Description
0	0	Disable interrupts (All sources)
0	1	Enable interrupt when FIFO receives data
1	0	Enable interrupt when FIFO has 2 bytes of data
1	1	Enable interrupt when FIFO has 3 bytes of data

INT:

The INT bit reflects the status of the external RDLINT interrupt unless the INTC1 and INTC0 bits are set to disable interrupts. In that case, the RDLINT output is forced to 0 and the INT bit of the Enable/Status register will reflect the state of the internal interrupt latch.

In addition to the FIFO fill status, interrupts are also generated for EOM (end of message), OVR (FIFO overrun), detection of the abort sequence while not receiving all ones and on detection of the first flag while receiving all ones. The interrupt is reset by a Receive Data Register read that empties the FIFO, unless the cause of the interrupt was due to a FIFO overrun. The interrupt due to a FIFO overrun is cleared by a Status register read, by disabling the block, or by setting TR high.

The contents of the Enable/Status register should only be changed when the RFDL block is disabled to prevent any erroneous interrupt generation.

Register 3AH: RFDL Block Status

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	FLG	X
Bit 4	R	EOM	X
Bit 3	R	CRC	X
Bit 2	R	NVB2	X
Bit 1	R	NVB1	X
Bit 0	R	NVB0	X

NVB[2:0]:

The NVB[2:0] bit positions indicate the number of valid bits in the RFDL Receive Data Register byte. It is possible that not all of the bits in the RFDL Receive Data Register are valid when the last data byte is read since the data frame can be any number of bits in length and not necessarily an integral number of bytes. The RFDL Receive Data Register is filled starting from the MSB bit position (RD7) and the data bits are shifted to lower bit positions as more bits are received, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0]. An NVB[2:0] value of 000 binary indicates that only the FE bit in this register is valid. An NVB[2:0] value of 011 indicates that RD[7:4] contain valid data bits where RD4 is the data bit that was received first. NVB[2:0] is only valid when the EOM bit is a logic 1 and the FLG bit is a logic 1 and the OVR bit is a logic 0.

CRC:

The CRC bit is set if a CRC error was detected in the last received LAPD frame. The CRC bit is only valid when EOM is logic 1 and FLG is a logic 1 and OVR is a logic 0.

On an interrupt generated from the detection of first flag, reading the Status register will return invalid NVB[2:0] and CRC bits, even though the EOM bit is logic 1 and the FLG bit is logic 1.

EOM:

The End of Message bit (EOM) follows the RDLEOM output. It is set when:

1. The last byte in the LAPD frame (EOM) is being read from the Receive Data Register,

2. An abort sequence is detected while not in the receiving all-ones state and the byte, written to the FIFO due to the detection of the abort sequence, is being read from the FIFO,

3. The first flag has been detected and the dummy byte, written into the FIFO when the RFDL changes from the receiving all-ones state to the receiving flags state, is being read from the FIFO,

4. Immediately on detection of FIFO overrun.

   The EOM bit is passed through the FIFO with the Data so that the Status will correspond to the Data just read from the FIFO.

FLG:

The flag bit (FLG) is set if the RFDL block has detected the presence of the LAPD flag sequence (01111110) in the data. FLG is reset only when the LAPD abort sequence (01111111) is detected in the data or when the RFDL block is disabled. This bit is passed through the FIFO with the Data so that the Status will correspond to the Data just read from the FIFO. The reception of bit-oriented codes over the data link will also force an abort due to its eight ones pattern.

OVR:

The Receiver Overrun bit (OVR) is set when data is written over unread data in the FIFO. This bit is not reset until after the Status register is read. While OVR is high, the RFDL and FIFO are held in the reset state, causing the FLG and EOM bits in the status register to be reset also.

FE:

The FIFO Empty bit (FE) is high when the last FIFO entry is read and goes low when the FIFO is loaded with new data.

If the Receive Data register is read while there is no valid data, then a FIFO underrun condition occurs. The underrun condition is reflected in the Status register by forcing all bits to logic zero on the first Status register read immediately following the Received Data register read which caused the underrun condition.

Register 3BH: RFDL Block Receive Data

Bit	Type	Function	Default
Bit 7	R	RD7	X
Bit 6	R	RD6	X
Bit 5	R	RD5	X
Bit 4	R	RD4	X
Bit 3	R	RD3	X
Bit 2	R	RD2	X
Bit 1	R	RD1	X
Bit 0	R	RD0	X

The RFDL Receive Data Register is filled starting from the MSB bit position (RD7) and the data bits are shifted to lower bit positions as more bits are received, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0] from the RFDL Status Register. An NVB[2:0] value of 111 indicates that RD[7:0] contain valid data bits where RD0 corresponds to the first bit of the serial byte received by the RFDL.

These registers are actually 4 level FIFOs. If data is available, the FE bit in the Status register is low. If INTC[1:0] (in the RFDL Interrupt Control/Status register) is set to 01, this register must be read within 31 data bit periods to prevent an overrun. If INTC[1:0] is set to 11, this register must be read within 15 data bit periods.

When an overrun is detected, an interrupt is generated and the FIFO is held cleared until the Status register is read. When the LAPD abort sequence (01111111) is detected in the data an ABORT interrupt is generated and the data that has been shifted into the serial to parallel converter is written into the FIFO.

A read of the Receive Data register increments the FIFO pointer at the end of the read. If the Receive Data register read causes an FIFO underrun, then the pointer is inhibited from incrementing. The underrun condition will be signalled in the next Status read by returning all zeros.

Register 40H: SIGX Block Configuration

Bit	Type	Function	Default
Bit 7	R/W	ACCEL	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MTKC	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

This register allows selection of the microprocessor access type, and allows enabling of the per-timeslot configuration registers.

ACCEL:

The ACCEL bit is used to enable an accelerated test mode for production purposes only. For proper operation the ACCEL bit must be set to logic 0.

MTKC:

The master trunk conditioning bit, MTKC, enables trunk conditioning for all timeslots, regardless of per-timeslot settings. A logic 1 in the MTKC bit position enables master trunk conditioning data from all of the timeslot Trunk Conditioning Data Registers (40H to 5FH) is output onto the data stream, BRPCM and the per-timeslot signalling trunk conditioning bits A',B',C' and D' are output onto the signalling data stream, BRSIG. The MTKC bit is ORed with the per-timeslot trunk conditioning enable bits in the Per-Timeslot Configuration Registers to form the applied per-timeslot trunk conditioning enables. When the E1XC is reset, the MTKC bit is set to logic 0, disabling master trunk conditioning.

The MTKC bit is independent of the TRKEN bit of the E1XC Receive Options register and takes precedence over it. If TRKEN is a logic 1, an out-of-frame condition causes the the contents of the ELST Idle Code register to be placed in all time slots on BRPCM. BRSIG presents the frozen signalling. If MTKC is a logic 1, each BRPCM and BRSIG time slot may have an unique idle code.

Reserved:

The reserved bit must be programmed to logic 0 to enable the correct output format.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the E1XC is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-timeslot functions. When the PCCE bit is set to a logic 1, data inversion, trunk conditioning and signalling debouncing are performed on a per-timeslot basis. When the PCCE bit is set to logic 0, the per-timeslot functions are disabled.

Upon reset of the E1XC, the ACCEL, MTKC, IND, and PCCE bits are all set to logic 0 disabling µP indirect access and per-timeslot functions.

Register 41H: SIGX Block µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

BUSY:

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 480 ns.

Register 42H: SIGX Block Time Slot Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

This register allows the µP to access to internal SIGX registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal SIGX register is requested, when R/WB is set to a logic 0, a write to the internal SIGX register is requested.

Register 43H: SIGX Block Time Slot Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D[7]	X
Bit 6	R/W	D[6]	X
Bit 5	R/W	D[5]	X
Bit 4	R/W	D[4]	X
Bit 3	R/W	D[3]	X
Bit 2	R/W	D[2]	X
Bit 1	R/W	D[1]	X
Bit 0	R/W	D[0]	X

In the case of an indirect write, the Indirect Data Register holds the value that will be written to the desired register when a write is initiated via the Timeslot Indirect Address Register. In the case of an indirect read, the Indirect Data Register will hold the contents of the indirectly addressed register, when the read has been completed. Please refer below to the per-timeslot register descriptions for the expected bit formats.

The signalling and per-timeslot functions are allocated within the registers as follows:

Table 8 - SIGX Indirect Memory Map

21H	Signalling Data Register for Time Slot 1
22H	Signalling Data Register for Time Slot 2
•	•
•	•
•	•
2FH	Signalling Data Register for for Time Slot 15
31H	Signalling Data Register for Time Slot 17
•	•
•	•
•	•

3EH	Signalling Data Register for Time Slot 30
3FH	Signalling Data Register for Time Slot 31
40H	PCM Trunk Conditioning byte for Time Slot 0
41H	PCM Trunk Conditioning byte for Time Slot 1
•	•
•	•
•	•
5EH	PCM Trunk Conditioning byte for Time Slot 30
5FH	PCM Trunk Conditioning byte for Time Slot 31
60H	Configuration and Signalling Trunk Conditioning data for Time Slot 0
61H	Configuration and Signalling Trunk Conditioning data for Time Slot 1
•	•
•	•
•	•
7EH	Configuration and Signalling Trunk Conditioning for Time Slot 30
7FH	Configuration and Signalling Trunk Conditioning for Time Slot 31

SIGX Indirect Registers 33 (21H)- 47 (2FH) - Segment 1: Typical Timeslot Signalling Data Register (TSs 1-15)

Bit	Type	Function	Default
Bit 7	R	A TS ‘n+16’	X
Bit 6	R	B TS ‘n+16’	X
Bit 5	R	C TS ‘n+16’	X
Bit 4	R	D TS ‘n+16’	X
Bit 3	R	A TS ‘n’	X
Bit 2	R	B TS ‘n’	X
Bit 1	R	C TS ‘n’	X
Bit 0	R	D TS ‘n’	X

SIGX Indirect Registers 49 (31H)- 63 (3FH) - Segment 2: Typical Timeslot Signalling Data Register (TSs 17-31)

Bit	Type	Function	Default
Bit 7	R	A TS ‘n-16’	X
Bit 6	R	B TS ‘n-16’	X
Bit 5	R	C TS ‘n-16’	X
Bit 4	R	D TS ‘n-16’	X
Bit 3	R	A TS ‘n’	X
Bit 2	R	B TS ‘n’	X
Bit 1	R	C TS ‘n’	X
Bit 0	R	D TS ‘n’	X

SIGX Indirect Registers 64 (40H) - 95 (5FH) - Segment 3: Typical Per-Timeslot PCM Trunk Conditioning Data Register

Bit	Type	Function	Default
Bit 6	R/W	TCD[6]	X
Bit 5	R/W	TCD[5]	X
Bit 4	R/W	TCD[4]	X
Bit 3	R/W	TCD[3]	X
Bit 2	R/W	TCD[2]	X
Bit 1	R/W	TCD[1]	X
Bit 0	R/W	TCD[0]	X

When trunk conditioning is enabled, PCM trunk conditioning bits TCD[7:0] replace timeslot bits 1 through 8 respectively for the referenced timeslot. TS0 and TS16 can be replaced with trunk conditioning data.

SIGX Indirect Registers 96 (60H) - 127 (7FH) - Segment 4:Typical Per-Timeslot Configuration and Signalling Trunk Conditioning Data Register

Bit	Type	Function	Default
Bit 7	R/W	RINV[1]	X
Bit 6	R/W	RINV[0]	X
Bit 5	R/W	RTKCE	X
Bit 4	R/W	RDEBE	X
Bit 3	R/W	A’	X
Bit 2	R/W	B’	X
Bit 1	R/W	C’	X
Bit 0	R/W	D’	X

RINV[1:0]:

The RINV[1:0] bits select whether the BRPCM stream is entirely or selectively inverted. The bit mapping is as follows.

- 00 - do not invert
- 01 - invert even bits (2,4,6,8)
- 10 - invert odd bits (1,3,5,7)
- 11 - invert all bits

RTKCE:

The RTKCE bit enables per-timeslot data stream and signal stream trunk conditioning. A logic 1 in this bit position enables trunk conditioning while a logic 0 disables trunk conditioning. When RTKCE is enabled, per-timeslot trunk conditioning data from one of the timeslot Trunk Conditioning Data Registers (one of 40H to 5FH) is output onto the data stream, BRPCM. In addition, the per-timeslot signalling trunk conditioning bits A’,B’,C’ and D’ are output onto the signalling data stream, BRSIG.

RDEBE:

The RDEBE bit enables debouncing of timeslot signalling bits. A logic 1 in this bit position enables signalling debouncing while a logic 0 disables it. When debouncing is selected, per-timeslot signalling transitions are ignored until two consecutive, equal values are sampled.

A',B',C' and D':

A',B',C' and D' are the per-timeslot signalling trunk conditioning bits. When trunk conditioning is enabled, these bits are used as signalling data, instead of the extracted timeslot signalling bits, and are output onto the SIG output.

To enable the RINV[1:0], RTKCE and RDEBE bits, the PCCE bit in the SIGX Configuration Register must be set to logic 1. When these bits are enabled, bits RINV[1:0] and RDEBE are ORed with their primary input equivalents to generate the applied configuration signals.

Register 44: TRAN Block Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6	R/W	SIGEN	1
Bit 5	R/W	DLEN	1
Bit 4	R/W	GENCRC	0
Bit 3	R/W	FDIS	0
Bit 2	R/W	FEBEDIS	0
Bit 1	R/W	INDIS	0
Bit 0	R/W	XDIS	0

AMI:

The AMI bit enables AMI line coding when set to logic 1; when it is set to logic 0, the HDB3 line coding is enabled.

SIGEN, DLEN:

The SIGEN and DLEN bits select the signalling data source for Time Slot 16 (TS16) as follows:

SIGEN	DLEN	MODE
0	0	Signalling insertion disabled. TS16 data is taken directly from the input BTPCM TS16.
0	1	CCS enabled. TS16 data is taken directly from the TDLSIG input or from the HDLC transmitter.
1	0	Reserved.
1	1	CAS enabled. TS16 data is taken from either BTSIG stream or from the TPSC Data Contol byte as selected on a per timeslot basis via the SIGSRC bit. The format of the BTSIG input data stream is PMC compatible.

When channel associated signalling (CAS) is enabled, the format of the input BTSIG stream is selected by the DLEN bit. A logic 1 in the DLEN bit position selects the PMC compatible format in which the BTSIG stream contains the

signalling data nibble in the lower four bits of the time slot byte. A logic 0 in the DLEN bit position is reserved and should not be used.

GENCRC:

The GENCRC bit enables generation of the CRC multiframe when set to logic 1. When enabled, the TRAN generates the CRC multiframe alignment signal, calculates and inserts the CRC bits, and if enabled by FEBEDIS, inserts the FEBE indication in the spare bit positions. The CRC bits transmitted during the first sub-multiframe (SMF) are indeterminate and should be ignored. The CRC bits calculated during the transmission of the 'n'th SMF (SMF n) are transmitted in the following SMF (SMF n+1). When GENCRC is set to logic 0, the CRC generation is disabled. The CRC bits are then set to the logic value contained in the Si[1] bit position in the International/National Bit Control Register and bit 1 of the NFAS frames are set to the value of Si[0] bit if enabled by INDIS, or, if not enabled by INDIS, are taken directly from BTPCM. When BTPCM or Si[1] are transmitted in lieu of the calculated CRC bits, there is no delay of one SMF (i.e., the BTPCM bits received in SMF n are transmitted in the same SMF). The same applies when substituting Si[1] in place of the calculated CRC bits.

FDIS:

The FDIS bit value controls the generation of the framing alignment signal. A logic 1 in the FDIS bit position disables the generation of the framing pattern in TS0 and allows the incoming data on BTPCM to pass through the TRAN transparently. A logic 0 in FDIS enables the generation of the framing pattern, replacing TS0 of frames 0,2,4,6,8,10,12,14 with the frame alignment signal, and if enabled by INDIS, replacing TS0 of frames 1,3,5,7,9,11,13,15 with the contents of the International/National Bits Control Register. When FDIS is a logic 1, framing is globally disabled and the values in controls bits GENCRC, FEBEDIS, INDIS, and XDIS are ignored.

Note that the above is true only if the AIS bit in the Transmit Alarm / Diagnostic Control Register is a logic 0. If AIS is logic 1, the output bit stream becomes all ones unconditionally.

INDIS, GENCRC and FEBEDIS:

The INDIS bit controls the insertion of the International and National bits into TS0. When INDIS is set to logic 0, the contents of the International/National Bit Control Register are inserted into TS0; when INDIS is a logic 1, the contents of the International/National Bit Control Register are ignored and the values for those bit positions in the output stream are taken directly from the BTPCM stream. When INDIS and FDIS are logic 0, the bit values used for the International and National bits are dependent upon the values of the GENCRC and FEBEDIS configuration bits, as follows:

GENCRC	FEBEDIS	Source of International/National bits
0	X	Bit position Si[1] in the International/National Control Register is used for the International bit in the frame alignment signal (FAS) frames and the Si[0] bit in the non-frame alignment signal (NFAS) frames if INDIS is logic 0. TPCM replaces Si[1:0] if INDIS is logic 1. Bit positions Sn[4:0] in the register are used for the National bits in NFAS frames.
1	0	The calculated CRC bits are used for the International bit in the FAS frames and the generated CRC multiframe alignment signal and the FEBE bits are used for the International bit in the NFAS frames. Bit positions Sn[4:0] in the International/National Control Register are used for the National bits in NFAS frames.
1	1	The calculated CRC bits are used for the International bit in the FAS frames and the generated CRC multiframe alignment signal is used for the International bit in the NFAS frames, with the Si[1:0] bits in the International/National Control Register used for the spare bits. Bit positions Sn[4:0] in the register are used for the National bits in NFAS frames.

XDIS:

If FDIS is logic 0 and SIGEN is logic 1, the XDIS bit controls the insertion of the Extra bits in TS16 of frame 0 of the signalling multiframe as follows. When XDIS is set to a logic 0, the contents of the Extra Bits Control Register are inserted into TS16, frame 0; when XDIS is a logic 1, the contents of the register are ignored and the values for those bits positions in the output stream are taken directly from the BTPCM stream. i.e., When XDIS and FDIS are logic 0, and SIGEN is logic 1, the X1,X3,X4 bit values from the Extra Bits Control Register are used for the Extra bits in TS16 of frame 0 of the signalling multiframe.

When the E1XC is reset, the contents of this register are set to logic 0, except SIGEN and DLEN which are set to logic 1.

Register 45: TRAN Block Transmit Alarm/Diagnostic Control

Bit	Type	Function	Default
Bit 7	R/W	MTRK	0
Bit 6	R/W	FPATINV	0
Bit 5	R/W	SPLRINV	0
Bit 4	R/W	SPATINV	0
Bit 3	R/W	REMAIS	0
Bit 2	R/W	MFAIS	0
Bit 1	R/W	TS16AIS	0
Bit 0	R/W	AIS	0

MTRK:

The MTRK bit forces trunk conditioning (i.e., idle code substitution and signalling substitution) when MTRK is a logic 1. This has the same effect as setting data substitution to IDLE code on time slots 1-15 and 17-31 (setting bits SUBS and DS[0] to binary 10 in time slots 1-15 and 17-31) and sourcing the signalling data from the TPCSC stream, if SIGEN is logic 1. When SIGEN is logic 0, TS16 will be treated the same as time slots 1-15 and 17-31 and will contain data sourced from TIDL. TS0 data is determined by the control bits associated with it and is independent of the value of MTRK.

FPATINV:

The FPATINV bit is a diagnostic control bit. When set to logic 1, FPATINV forces the frame alignment signal (FAS) written into TS0 to be inverted (i.e., the correct FAS, 0011011, is substituted with 1100100); when set to logic 0, the FAS is unchanged.

SPLRINV:

The SPLRINV bit is a diagnostic control bit. When set to logic 1, SPLRINV forces the "spoiler bit" written into bit 2 of TS0 of NFAS frames to be inverted (i.e., the spoiler bit is forced to 0); when set to logic 0, the spoiler bit is unchanged.

SPATINV:

The SPATINV bit is a diagnostic control bit. When set to logic 1, SPATINV forces the signalling multiframe alignment signal written into bits 1-4 of TS16 of frame 0 of the signalling multiframe to be inverted (i.e., the correct

signalling multiframe alignment signal, 0000, is substituted with 1111); when set to logic 0, the signalling multiframe alignment signal is unchanged.

REMAIS:

The REMAIS bit controls the transmission of the remote Alarm Indication Signal. A logic 1 in the REMAIS bit position causes bit 3 of NFAS frames to be forced to logic 1; otherwise, bit 3 of NFAS frames is a logic 1.

MFAIS:

The MFAIS bit controls the transmission of the signalling multiframe Alarm Indication Signal. A logic 1 in the MFAIS bit position causes the y-bit (bit 6) of TS16 of frame 0 of the signalling multiframe to be forced to logic 1; otherwise, the y-bit is a logic 1.

TS16AIS:

The TS16AIS bit controls the transmission of the Time Slot 16 Alarm Indication Signal (all-ones in TS16). A logic 1 in the TS16AIS bit position forces TS16 of all frames in the output stream to logic 1.

AIS:

The AIS bit controls the transmission of the Alarm Indication Signal (unframed all-ones). A logic 1 in the AIS bit position forces the output streams to logic 1.

When the E1XC is reset, the contents of this register are set to logic 0.

Register 46: TRAN Block International/National Control

Bit	Type	Function	Default
Bit 7	R/W	Si[1]	1
Bit 6	R/W	Si[0]	1
Bit 5		Unused	X
Bit 4	R/W	Sn[4]	1
Bit 3	R/W	Sn[3]	1
Bit 2	R/W	Sn[2]	1
Bit 1	R/W	Sn[1]	1
Bit 0	R/W	Sn[0]	1

Sn[4:0]:

Bits 4 to 0 of this register are substituted in bit positions 4 to 8, respectively, of TS0 of each NFAS frame when framing generation (FDIS = 0) and International/National bit control (INDIS = 0) is enabled. When FDIS or INDIS is logic 1, the contents of this register are ignored and replaced with the values received on the TPCM input.

The bits Sn[4:0] correspond to the 5 National bits; these can be programmed to any value and are inserted into the National bit positions in the NFAS frames when enabled by INDIS.

Si[1:0]:

The bits Si[1] and Si[0] correspond to the International bits. The Si[1] and Si[0] bits can be programmed to any value and will be inserted into bit 1 of each FAS frame and NFAS frame, respectively, when the block is configured for frame generation, INDIS is set to logic 0, and CRC multiframe generation is disabled. When CRC multiframe generation is enabled, both Si[1] and Si[0] are ignored if FEBE indication is enabled; if FEBEDIS is a logic 1 and INDIS = 0, the values programmed in the Si[1] and Si[0] bit positions are inserted into the spare bit locations of frame 13 and frame 15, respectively, of the CRC multiframe. If both FEBEDIS and INDIS are logic 1, then data from TPCM replaces the Si[0] and Si[1] bits in the CRC multiframe.

The Si[1], Si[0], and Sn[4:0] bits should be programmed to a logic 1 when not being used to carry information.

When the E1XC is reset, the contents of the register are set to logic 1.

Register 47: TRAN Block Extra Bits Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	X[1]	1
Bit 2		Unused	X
Bit 1	R/W	X[3]	1
Bit 0	R/W	X[4]	1

X[4:3,1]:

The X[1], X[3], and X[4] bits control the value programmed in the X[1], X[3], and X[4] bit locations (bits 5,7, and 8) in TS16 of frame 0 of the signalling multiframe, when enabled by XDIS. The X[1], X[3], and X[4] bits should be programmed to a logic 1 when not being used to carry information.

When the E1XC is reset, the contents of the register are set to logic 1.

Register 48H: PMON Block Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	XFER	X
Bit 0	R	OVR	X

This register contains status information indicating when counter data has been transferred into holding registers and indicating whether the holding registers have been overrun.

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the PMON count registers (49H - 4FH). A logic 1 in the INTE position enables the generation of an interrupt; a logic 0 disables the generation of an interrupt. Note: The INTE bit is not available if ID[6:0] = 0000000 binary in the E1XC Revision/Chip ID register, indicating the E1XC rev. A.

XFER:

The XFER bit indicates that a transfer of counter data has occurred (and an interrupt, if INTE is set to logic 1). A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations, was received and a transfer of the counter has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit and its interrupt are cleared (acknowledged) by reading this register.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

11.1.1 Registers 49-4FH: Latching Performance Data

All the Performance Data registers are updated as a group by writing to any of the PMON block count registers (addresses 49H-4FH). A write to any of these locations loads performance data located in the PMON block into the internal holding registers. The data contained in the holding registers can then be subsequently read by µP accesses into the PMON block count register address space. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed. NOTE: it is necessary to write to one, and only one, count register address to latch all the count data register values into the holding registers and to reset all the counters for each polling cycle.

The PMON block is loaded with new performance data within 27 internal high-speed clock periods of the latch performance data register write. With the XCLK frequency at the nominal 16.384 MHz (or with the XCLK frequency at 49.152 MHz when using the jitter attenuator), the PMON registers should not be polled until 1.7µsec have elapsed from the "latch performance data" register write.

When the E1XC is reset, the contents of the PMON count registers are unknown until the first latching of performance data is performed.

Register 49: Framing Bit Error Count

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FER[6]	X
Bit 5	R	FER[5]	X
Bit 4	R	FER[4]	X
Bit 3	R	FER[3]	X
Bit 2	R	FER[2]	X
Bit 1	R	FER[1]	X
Bit 0	R	FER[0]	X

This register indicates the number of framing bit error events that occurred during the previous accumulation interval. The FER counts are suppressed when the FRMR has lost frame alignment (OOF in the FRMR Framing Status register is set).

Register 4A: Far End Block Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 4B: Far End Block Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers indicate the number of far end block error events that occurred during the previous accumulation interval. The FEBE counts are suppressed when the FRMR has lost frame alignment (OOF in the FRMR Framing Status register is set).

Register 4C: CRC Error Count LSB

Bit	Type	Function	Default
Bit 7	R	CRCE[7]	X
Bit 6	R	CRCE[6]	X
Bit 5	R	CRCE[5]	X
Bit 4	R	CRCE[4]	X
Bit 3	R	CRCE[3]	X
Bit 2	R	CRCE[2]	X
Bit 1	R	CRCE[1]	X
Bit 0	R	CRCE[0]	X

Register 4D: CRC Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CRCE[9]	X
Bit 0	R	CRCE[8]	X

These registers indicate the number of CRC error events that occurred during the previous accumulation interval. CRC error events are suppressed when the FRMR is out of CRC-4 multiframe alignment (OOCMF bit in the FRMR Framing Status register is set).

Register 4E: Line Code Violation Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 4F: Line Code Violation Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

These registers indicate the number of LCV error events that occurred during the previous accumulation interval.

Register 5CH: RSLC Block Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	THS	0

THS:

The bit THS controls the selection of slicing threshold. The analog pulse slicer generates a logic one on either the SDP or SDN output if the amplitude (positive or negative) of the line voltage exceeds the adaptive slicing threshold. The THS bit selects between two fractions of the pulse amplitude for the slicing threshold.

When THS is set to logic 0, the slicing threshold is 67% of the peak amplitude.

When THS is set to logic 1, the slicing threshold is 50% of the peak amplitude and is intended for G.703 2048 kbit/s applications.

Register 5DH: RSLC Block Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	SQ	X
Bit 1	R	SQI	X
Bit 0	R/W	SQE	0

SQ:

The SQ bit reflects the current state of the squelch alarm.

SQI:

The SQI bit is set to logic 1 when the squelch alarm is either asserted or deasserted. The bit is cleared to logic 0 when the register is read.

SQE:

The SQE bit enables the generation of an interrupt when the squelch alarm changes state. When SQE is set to logic 1, the squelch alarm event is enabled to generate an interrupt on the microprocessor INTB pin.

When the E1XC is reset, the SQE bit is set to logic 0, disabling a squelch event from generating an interrupt.

12 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the E1XC. Test mode registers (as opposed to normal mode registers) are mapped into addresses 80H-FFH.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the E1XC are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Table 9 - Test Mode Register Memory Map

Address	Register
80H-8FH	E1XC Reserved
90H	CDRC TREG 0
91H	CDRC TREG 1
92H	CDRC Reserved
93H	CDRC Reserved
94H	XPLS TREG 0
95H	XPLS TREG 1
96H	XPLS TREG 2
97H	XPLS TREG 3
98H	DJAT TREG 0

Address	Register
99H	DJAT TREG 1
9AH	DJAT TREG 2
9BH	DJAT Reserved
9CH	ELST TREG 0
9DH	ELST TREG 1
9EH	ELST TREG 2
9FH	ELST Reserved
A0H	FRMR TREG 0
A1H	FRMR TREG 1
A2H	FRMR TREG 2
A3H	FRMR TREG 3
A4H - ABH	FRMR Reserved
ACH - AFH	Reserved
B0H	TPSC TREG 0
B1H	TPSC TREG 1
B2H	TPSC Reserved
B3H	TPSC Reserved
B4H	XFDL TREG 0
B5H	XFDL TREG 1
B6H	XFDL Reserved
B7H	XFDL Reserved
B8H	RFDL TREG 0
B9H	RFDL TREG 1
BAH	RFDL Reserved
BBH	RFDL Reserved
BCH - BFH	Reserved
C0H	SIGX TREG 0
C1H	SIGX TREG 1

Address	Register
C2H	SIGX TREG 2
C3H	SIGX Reserved
C4H	TRAN TREG 0
C5H	TRAN TREG 1
C6H	TRAN TREG 2
C7H	Reserved
C8H	PMON TREG 0
C9H	PMON TREG 1
CAH-CFH	PMON Reserved
D0H - DBH	Reserved
DCH	RSLC TREG 0
DDH	RSLC TREG 1
DEH-FFH	Reserved

12.1 Internal Registers

Register 0BH: E1XC Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	0
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select E1XC test features. All bits, except for PMCTST, are reset to zero by a hardware reset of the E1XC ; a software reset of the E1XC does not affect the state of the bits in this register.

PMCTST:

The PMCTST bit is used to configure the E1XC for PMC's manufacturing tests. When PMCTST is set to logic 1, the E1XC microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the E1XC to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit only has effect if either the IOTST or PMCTST bit is set. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the E1XC for board level

testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in this section).

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tristate modes of the E1XC . While the HIZIO bit is a logic 1, all output pins of the E1XC except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

12.2 Test Mode 0

In test mode 0, the E1XC allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the IOTST bit in the Test Mode Select Register is set to logic 1 and the following addresses must be written with 00H: 91H, 99H, 9DH, A1H, B1H, B5H, B9H, C1H and C5H. Also, to enable input and output signals to propagate through the Interface blocks, the values 00H, 00H, 00H, 00H , and 02H must be written to addresses 01H, 02H, 03H, 04H, and 07H, respectively.

Reading the following address locations returns the values for the indicated inputs :

Table 21 - Test Mode 0 Read Memory Map

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
90H					RDP	RDN	RCLKI	
98H					XCLK	TCLKI		
9CH	BRFPI	BRCCK						
C4H		BTPCM			BTSIG			TDLSIG
C6H					BTFP			BTCLK

Writing the following address locations forces the outputs to the value in the corresponding bit position:

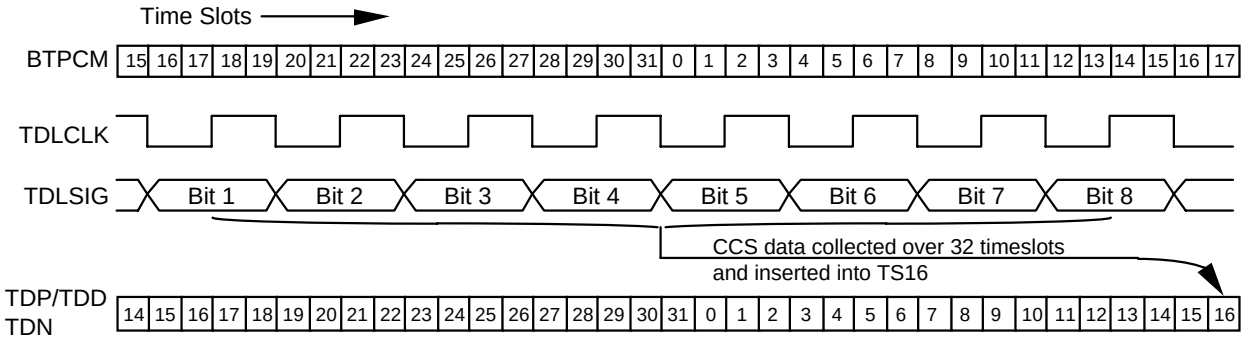
Table 22 - Test Mode 0 Write Memory Map

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
90H		INTB†					RDPCM	RCLKO
92H							BRPCM	BRSIG
98H	INTB†					TCLKO	TDN	TDP
9CH		INTB†						
A0H					RFP			
A3H								INTB†
B8H							RDLCLK	RDLSIG
C0H					BRFPO			
C4H								TDLCLK

Notes: †Writing a logic 1 to any of the block interrupt signals asserts the INTB output low.

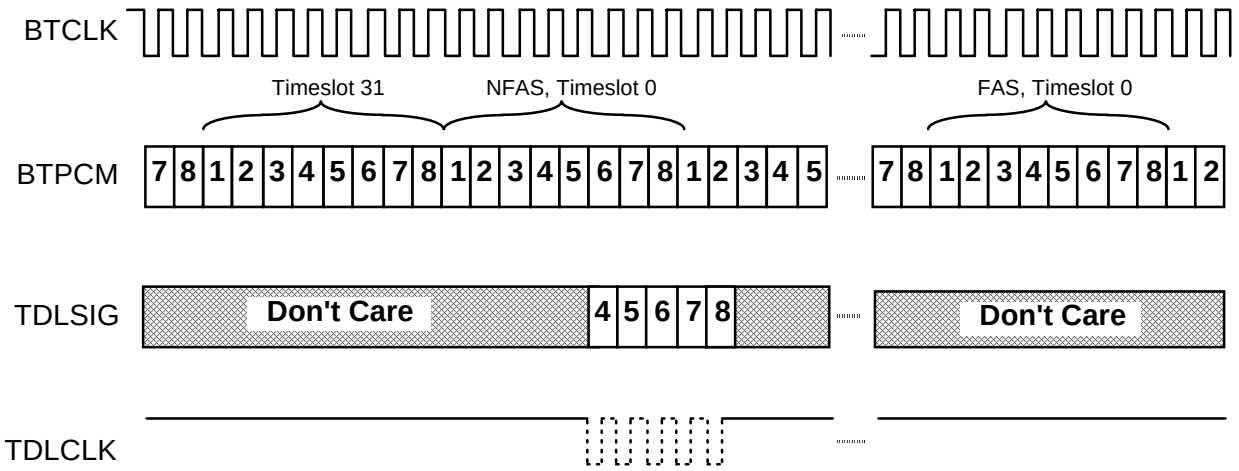
13 TIMING DIAGRAMS

Figure 13 - TS16 Transmit Datalink Interface



When Common Channel Signalling (CCS) data sourced from TDLSIG is selected (DLEN=1, SIGEN=0 and TXDMASIG=0), TDLCLK is active, producing one cycle every 4 time slots, aligned to the incoming TPCM. The data on TDLSIG is sampled on the rising edge of TDLCLK and put directly into TS16 on the outgoing data stream.

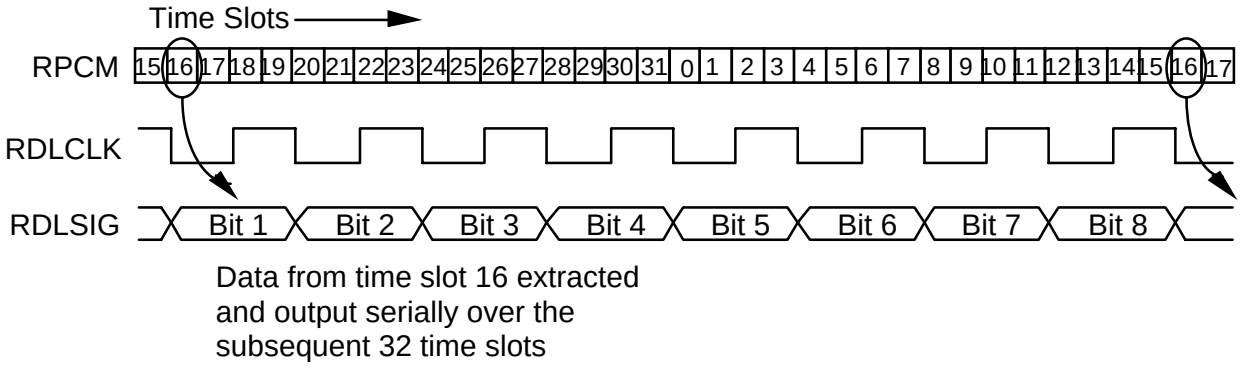
Figure 14 - TS0 Transmit Datalink Interface



When the TS0 maintenance datalink is active (DLEN=0 or SIGEN=1, TXDMASIG=0, at least one TXSAxEN bit is a logic 1), the data presented on TDLSIG is inserted into the National Use bits of the NFAS frames. A clock pulse is generated on TDLCLK for each National Use bit on TDLSIG which has the associated enable (TXSAxEN, x=4 to 8) set to logic 1. If the enable is logic 0,

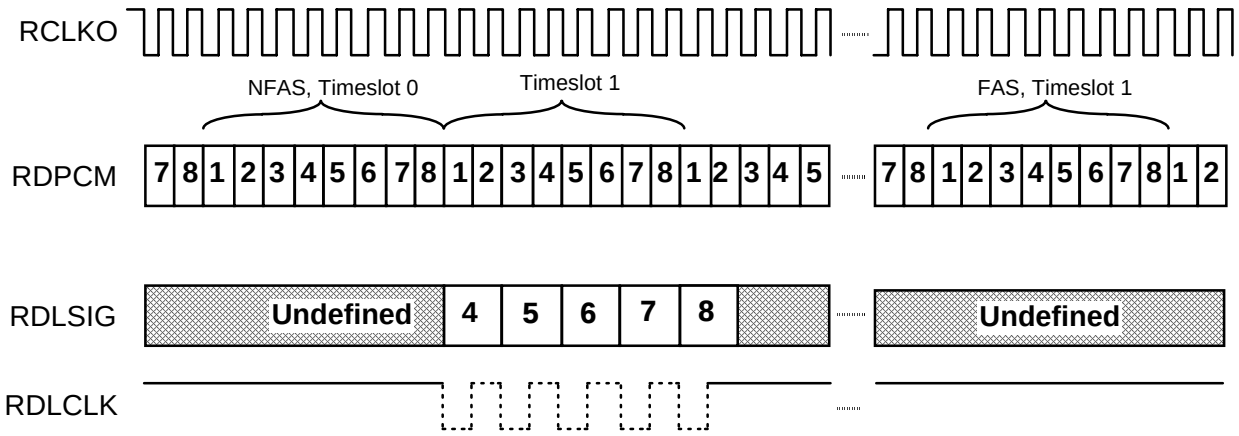
the specific bit value is sourced from the TRAN block International/National Control register. Depending on the settings of the TXSAxEN bits, the effective bit rate of the data link may range between 4 bit/s and 20 kbit/s. TDLSIG is sampled on the rising edge of TDLCLK.

Figure 15 - TS16 Receive Datalink Interface



When TS16 is selected as the source of the receive datalink (RXDMASIG=0 and all of RXSAxEN=0), the 64 kbit/s TS16 data is presented on RDLSIG with an accompanying RDLCLK with a period of 4 time slots. The data on RDLSIG is generated on the falling edge of RDLCLK.

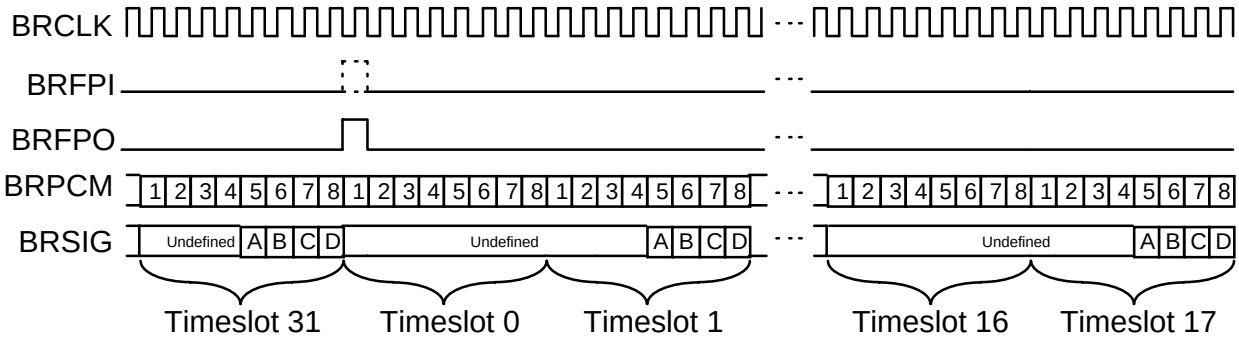
Figure 16 - TS0 Receive Datalink Interface



When TS0 is selected as the source of the receive datalink (RXDMASIG=0 and at least one RXSAxEN bit is a logic 1), the National Use bit of TS0 of the NFAS frames data is presented on RDLSIG with an accompanying RDLCLK. A clock pulse is generated on RDLCLK for each National Use bit on RDLSIG which has

the associated enable (RXSAxEN, x=4 to 8) set to logic 1. Depending on the settings of the RXSAxEN bits, the effective bit rate of the data link may range between 4 bit/s and 20 kbit/s. RDLSIG is generated on the falling edge of RDLCLK.

Figure 17 - Receive Backplane Interface



The Receive Backplane is configured to generate 2048 kbit/s, single-rail formatted data with frame alignment indication. The Receive Backplane Options register is programmed to BRX2RAIL=0, BRXSMFP=0 and BRXCMFP=0.

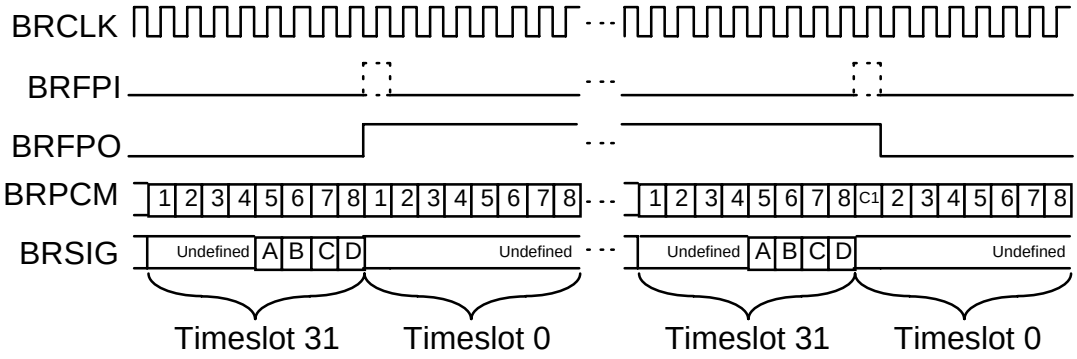
The BRFPI input pulse need not exist every frame; only one is required to align the backplane signals. If no BRFPI pulse has been presented since reset, the outputs will assume an arbitrary alignment.

If ROHM=0, BRXSMFP=0 and BRXCMFP=1, the BRFPO signal pulses high only during the first bit of the first frame in the CRC multiframe.

If ROHM=0, BRXSMFP=1 and BRXCMFP=0, the BRFPO signal pulses high only during the first bit of the frame containing the signalling multiframe alignment signal.

If ROHM=0, BRXSMFP=1 and BRXCMFP=1, the BRFPO signal becomes high on the falling BRCLK edge marking the beginning of bit 1 of frame 1 of every 16 frame signalling multiframe and returns low on the falling BRCLK edge marking the end of bit 1 of frame 1 of every 16 frame CRC multiframe.

Figure 18 - Receive composite multiframe output (BRXSMFP=1 and BRXCMFP=1):



If the ROHM bit is logic 1, the BRFPO signal marks the overhead by becoming high during timeslots 0 and 16.

Figure 19 - Receive overhead output (ROHM=1):

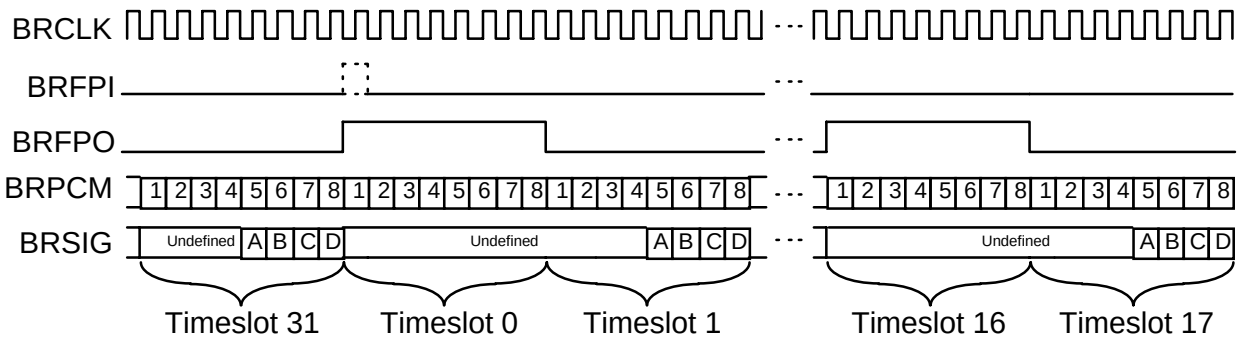
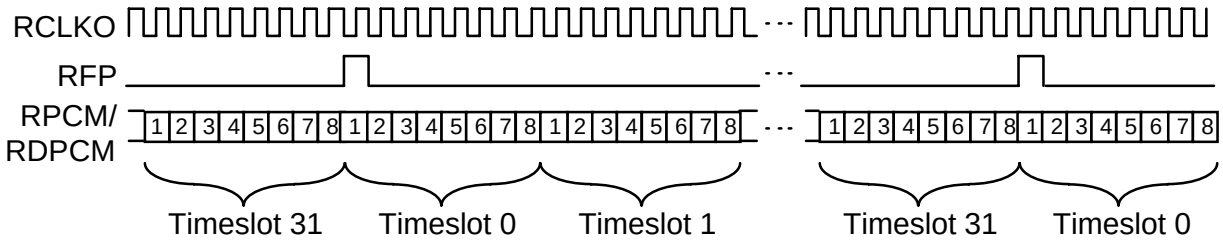


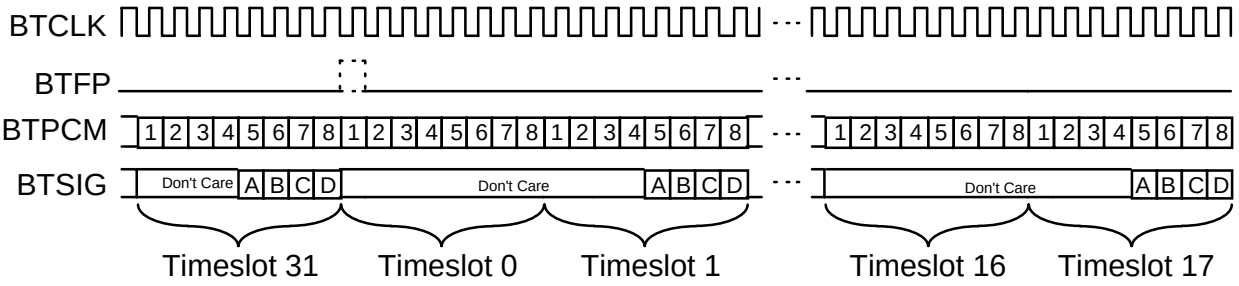
Figure 20 - Receive Line Data Interface



The Receive Options register is programmed to SRCMFP=0 and SRPCM=X. (If SRCMFP=1, the RFP output only pulses on the frame boundary indicating the

start of the CRC multiframe alignment). This diagram does not apply if the digital receive interface is configured for unipolar operation (i.e. RUNI=1 and RDIEN=1).

Figure 21 - Transmit Backplane Interface



The Transmit Backplane is configured to receive 2048 kbit/s, single-rail formatted data with frame alignment indication. The Transmit Backplane Options register is programmed to BTXCLK=0, BTX2RAIL=0, BTXMFP=0. (If BTXMFP=1, the BTFP input must be brought high to mark bit 1 of frame 1 of every 16 frame signalling multiframe and brought low following bit 1 of frame 1 of every 16 frame CRC multiframe. This mode allows both multiframe alignments to be independently controlled using the single BTFP signal. Note that if the signalling and CRC multiframe alignments are coincident, BTFP must pulse high for 1 BTCLK cycle every 16 frames.

14 OPERATIONS

14.1 Configuring the E1XC from Reset

After a system reset (either via the RSTB pin or via the RESET register bit), the E1XC will default to the following settings:

Table 10 - E1XC Default Settings

Setting	Receiver Section	Transmitter Section
Framing Format	Basic G.704 without CRC multiframe. Channel Associated Signalling is enabled.	Basic G.704 without CRC multiframe. Channel Associated Signalling is enabled.
Line Code	HDB3	HDB3
E1 interface	• RSLC active, outputs from RSLC used internally for clock and data recovery • Pins SDP/RDP/RDD and SDN/RDN/RLCV active as digital inputs RDP and RDN, but ignored	• XPLS active • Digital interface active • TDP, TDN outputs NRZ data updated on falling TCLKO edge
System Backplane	• BRPCM, BRSIG active • BRFPO indicates frame pulses	• BTPCM active BTSIG inactive • BTFP indicates frame alignment
Data Link	• internal RFDL disabled • RDLSIG and RDLCLK outputs present the Sa4 bit of TS0.	• internal XFDL disabled • TDLCLK output, TDLSIG input inserted into Sa4 bit of TS0.

Setting	Receiver Section	Transmitter Section
Options	• ELST not bypassed • RPCM outputs HDB3-decoded PCM • RFP indicates frame pulses	•
Timing Options	Not applicable	• Digital jitter attenuation enabled, with TCLKO referenced to BTCLK
Diagnostics	• All diagnostic modes disabled	• All diagnostic modes disabled

14.2 Using the Internal FDL Transmitter

Upon reset of the E1XC, the XFDL should be disabled by setting the EN bit in the XFDL Configuration Register to logic 0. If data is not ready to be transmitted, the TDLINT[x] output should also be masked by setting the INTE bit to logic 0.

When a frame (or frames) of data are ready to be transmitted, the XFDL Configuration Register should be initialized for transmission: if the FCS is desired, the CRC bit should be set to logic 1; if the block is to be used in interrupt driven mode, interrupts should be enabled by setting the INTE bit to logic 1. Finally, the XFDL can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, an underrun will occur.

The XFDL can be used in a polled, interrupt driven, or DMA-controlled mode for the transfer of frame data. In the polled mode, the TDLINT and TDLUDR outputs of the XFDL are not used, and the processor controlling the XFDL must periodically read the XFDL Status Register to determine when to write to the XFDL Transmit Data Register. In the interrupt driven mode, the processor controlling the XFDL uses either the TDLINT output, or the main processor INTB output and the interrupt source registers, to determine when to write to the XFDL Transmit Data Register. In the DMA controlled mode, the TDLINT output of the XFDL is used as a DMA request input to the DMA controller, and the TDLUDR output is used as an interrupt to the processor to allow handling of exceptions. The TDLUDR output can also be enabled to generate a processor interrupt through the common INTB output via the TDLUDRE bit in the Datalink Options register.

Polled Mode

If the XFDL data transfer is operating in the polled mode (TXDMASIG, TDLINTE, and TDLUDRE bits in the Datalink Options Register are set to logic 0), then a timer periodically starts up a service routine, which should process data as follows:

1. Read the XFDL Interrupt Status Register and poll the UDR and INT bits.

2. If UDR=1, then clear the UDR bit in the XFDL Interrupt Status Register to logic 0, and restart the current frame. Go to step 1.

3. If INT=1, then:

   a) If there is still data to send, then write the next data byte to the XFDL Transmit Data Register;

   b) If all bytes in the frame have been sent, then set the EOM bit in the XFDL Configuration Register to logic 1.

4. If EOM bit was set to logic 1 in step 3b, then:

   a) Read the XFDL Interrupt Status Register and check the UDR bit.

   b) If UDR=1 then reset the UDR bit in the XFDL Interrupt Status Register and the EOM bit in the XFDL Configuration Register to logic 0, and retransmit the last frame.

5. Go to step 1.

Interrupt Mode

In the case of interrupt driven data transfer, the TDLINT output is connected to the interrupt input of the processor, and the interrupt service routine should process the data exactly as described above for the polled mode. The INTE bit in the XFDL Configuration Register must be set to logic 1. Alternately, the INTB output can be connected to the interrupt input of the processor if the TDLINTE bit of the Datalink Options Register is set to logic 1. If this mode is used, additional polling of the Master Interrupt Source register must be performed to identify the cause of the interrupt before the initiating the interrupt service routine.

DMA-Controlled Mode

The XFDL can also be used with a DMA controller to process the frame data. In this case, the TDLUDR output is connected to the processor interrupt input. The TDLINT output of the XFDL is connected to the DMA request input of the DMA controller. The INTE bit in the XFDL Configuration Register must be set to logic 1 before enabling the XFDL. The DMA controller writes a data byte to the XFDL whenever the TDLINT output is high. If there is a problem during transmission and an underrun condition occurs, then the TDLUDR output goes high and the processor is interrupted. The processor can then halt the DMA controller, reset the UDR bit in the XFDL Interrupt Status Register, reset the frame data pointers, and restart the DMA controller to resend the data frame. After the message transmission is completed, the DMA controller must initiate a write to set the EOM bit in the XFDL Configuration Register and then verify that TDLUDR is not set prior to setting EOM.

14.3 Using the Internal FDL Receiver

On power up of the E1XC, the RFDL should be disabled by setting the EN bit in the Configuration Register to logic 0. The RFDL Interrupt Control/Status Register should then be initialized to select the FIFO buffer fill level at which time an interrupt will be generated.

After the Interrupt Control/Status Register has been written to, the RFDL can be enabled at any time by setting the EN bit in the Configuration Register to logic 1. When the RFDL is enabled, it will assume that the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated (if enabled), and the byte received before the first flag was detected will be written into the FIFO buffer. Because the FLG and EOM bits are passed through the buffer, this dummy write allows the RFDL Status Register to accurately reflect the current state of the data link. A RFDL Status Register read after a RFDL Data Register read of the dummy byte will return EOM as logic 1 and FLG as logic 1. The first interrupt and data byte read after the RFDL is enabled (or TR bit set to logic 1) is an indication of the link status, and the data byte should therefore be discarded. It is up to the controlling processor to keep track of the link state as idle (all ones or bit-oriented messages active) or active (flags received).

The RFDL can be used in a polled, interrupt driven, or DMA controlled mode for the transfer of frame data.

Polled Mode

In the polled mode, the RDLINT and RDLEOM outputs of the RFDL are not used, and the processor controlling the RFDL must periodically read the RFDL Interrupt/Status to determine when to read the Data Register. If the RFDL data transfer is operating in the polled mode, entry to the service routine is from a timer. The processor service routine should process the data in the following order:

1. Poll the INT bit in the RFDL Interrupt/Status Register until it is set to logic 1. Once INT is set to logic 1, then proceed to step 2.

2. Read the RFDL Data Register.

3. Read the RFDL Status Register to check for the following:

   a) If OVR=1, then discard the current frame and go to step 1.

   ELSE

   b) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the current frame, and go to step 1.

   c) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and go to step 1.

   ELSE

   d) Save the last data byte read.

   e) If EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register to process the frame properly.

   f) If FE=0, then go to step 2, else go to step 1.

The link state is typically a local software variable. The link state is inactive if the RFDL is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RFDL is receiving flags or data.

Interrupt Mode

In the interrupt driven mode, the processor controlling the RFDL uses the RDLINT output, the main processor INTB output (RDLINTE bit of the Datalink

Options Register is set to logic 1), or the Master Interrupt Source Register, to determine when to read the Data Register. The RXDMASIG bit in the Datalink Options Register should be set to logic 1. RDLINTE of the same register should be set to logic 1 if the INTB output is used as the interrupt source. The processor interrupt service routine should process the data in the following order:

1. Wait for an interrupt originating from the RFDL. Once the interrupt is set, then proceed to step 2.

2. Read the RFDL Data Register.

3. Read the RFDL Status Register to check for the following:

   a) If OVR=1, then discard the current frame and go to step 1.

   ELSE

   b) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the current frame, and go to step 1.

   c) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and go to step 1.

   ELSE

   d) Save the last data byte read.

   e) If EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register to process the frame properly.

   f) If FE=0, then go to step 2, else go to step 1.

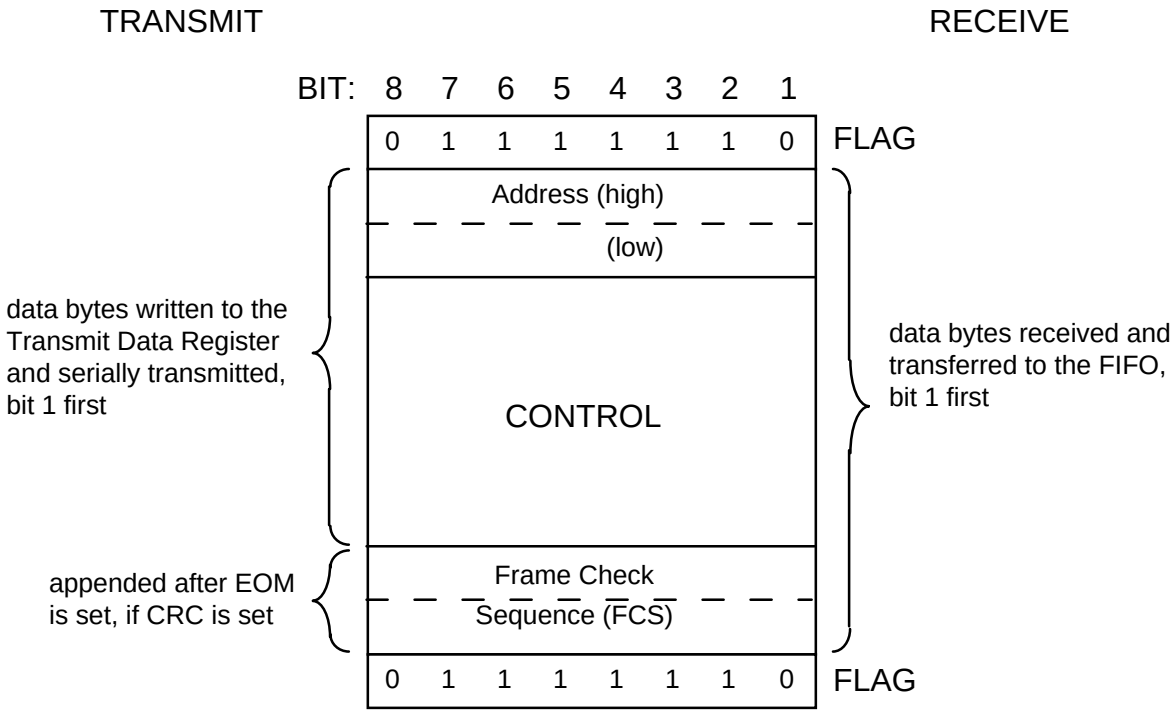
DMA-Controlled Mode

The RFDL can also be used with a DMA controller to process the frame data. In the DMA controlled mode, the RDLINT output of the RFDL is used as a DMA request input to the DMA controller, and the RDLEOM output is used as an interrupt to the processor to allow handling of exceptions and as an indication of when to process a frame. The RXDMASIG bit of the Datalink Options Register should be set to logic 1.

The RDLINT output of the RFDL is connected through a gate to the DMA request input of the DMA controller to optionally inhibit the DMA request if the RDLEOM output is high. The DMA controller reads the data bytes from the RFDL whenever the RDLINT output is high. When the current byte read from the

Data Register is the last byte in a frame (due to an end-of-message or an abort), or an overrun condition occurs, then the RDLEOM output goes high. The DMA controller is inhibited from reading any more bytes, and the processor is interrupted. The processor can then halt the DMA controller, read the Status Register, process the frame, and finally reset the DMA controller to process the data for the next frame. The RDLEOM output can optionally be enabled to generate a processor interrupt through the common INTB output via the RDLEOME bit in the Datalink Options register, rather than tying the RDLEOM output directly to the microprocessor. This allows a central microprocessor controlling the E1XC operation to also respond to conditions affecting the DMA servicing of RFDL. When using the INTB output, the central processor must poll the Interrupt ID/Clock Monitor, and the Interrupt Source Registers to identify the source of the interrupt before beginning any interrupt service routine.

Figure 22 - Typical Data Frame



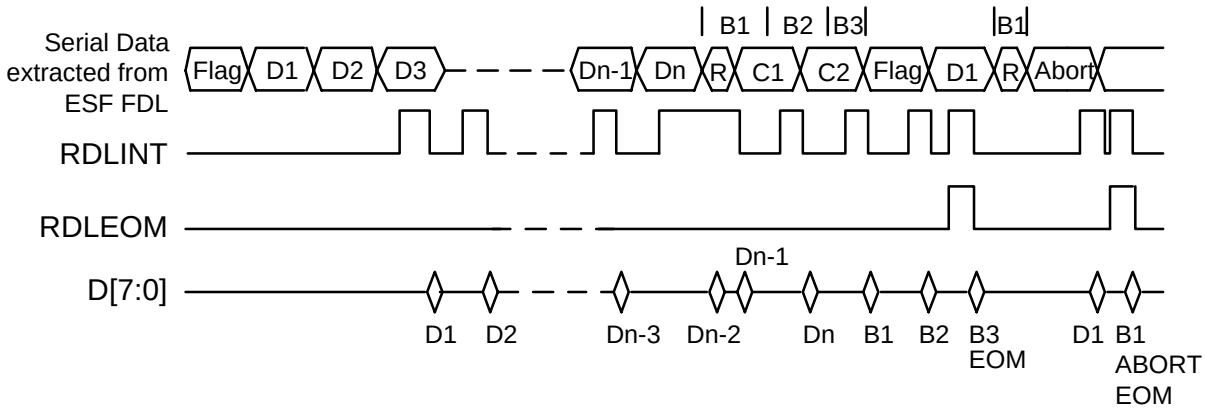
Bit 1 is the first serial bit to be transmitted or received.

Both the address and control bytes must be supplied by an external processor and are shown for reference purposes only.

14.3.1 Key used on subsequent diagrams:

Flag	- flag sequence (01111110)
Abort	- abort sequence (01111111)
D1 - Dn	- n frame data bytes
R	- remainder bits (less than 8)
C1, C2	- CRC-CCITT information
B1, B2, B3	- groupings of 8 bits

Figure 23 - RFDL Normal Data and Abort Sequence



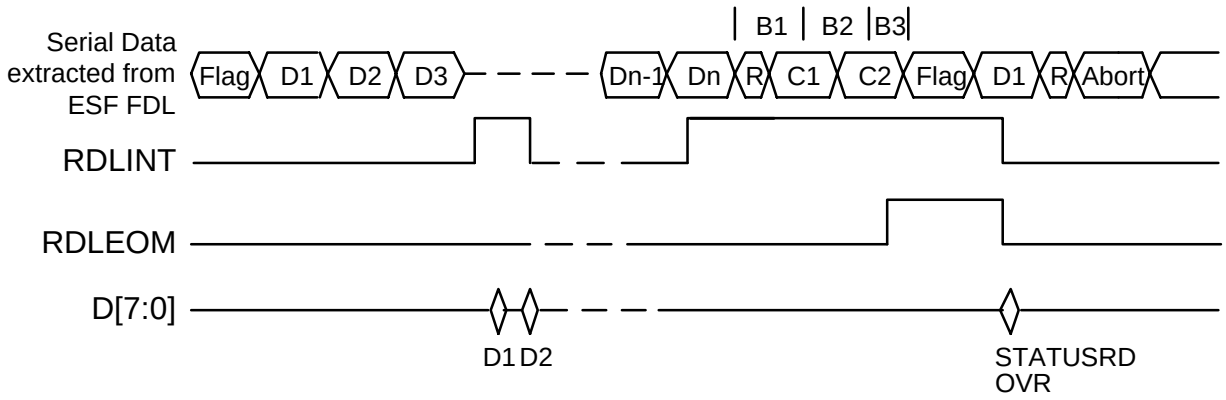
This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when one byte is present in the FIFO buffer. The RFDL is assumed to be operating in the interrupt driven mode. Each read shown is composed of two register reads: first a read of the RFDL Data Register, followed by a read of the RFDL Status Register. A read of the RFDL Data Register sets the RDLINT output to low if no more data exists in the FIFO buffer. The status of the FE bit returned in the RFDL Status Register read will indicate the FIFO buffer fill status as well. The RFDL Data Register read Dn-2 is shown to occur after two bytes have been written into the buffer. The RDLINT output does not go low after the first RFDL Data Register read because a data byte still remains to be read. The RDLINT output goes low after RFDL Data Register read Dn-1. The FE bit will be logic 0 in RFDL Status Register read Dn-2 and logic 1 in RFDL Status Register read Dn-1.

The RDLEOM output goes high as soon as the last byte in the frame is read from the RFDL Data Register. The RDLINT output will go low if the FIFO buffer is empty. The next RFDL Status Register read will return a value of logic 1 for the EOM and FLG bits, and cause the RDLEOM output of the RFDL to return low.

In the next frame, the first data byte is received, and after a delay of ten bit periods, it is written to the FIFO buffer, and read by the processor after the interrupt. When the abort sequence is detected, the data received up to the abort is written to the FIFO buffer and an interrupt generated. The processor then reads the partial byte from the RFDL Data Register and the RDLEOM output is set high. The processor then reads the RFDL Status Register which will return a value of logic 1 for the EOM and FLG bits, and set the RDLEOM output low. The FIFO buffer is not cleared when an abort is detected. All bytes received up to the abort are available to be read.

After an abort, the RFDL state machine will be in the receiving all ones state, and the data link status will be idle. When the first flag is detected, a new interrupt will be generated, with a dummy data byte loaded into the FIFO buffer, to indicate that the data link is now active.

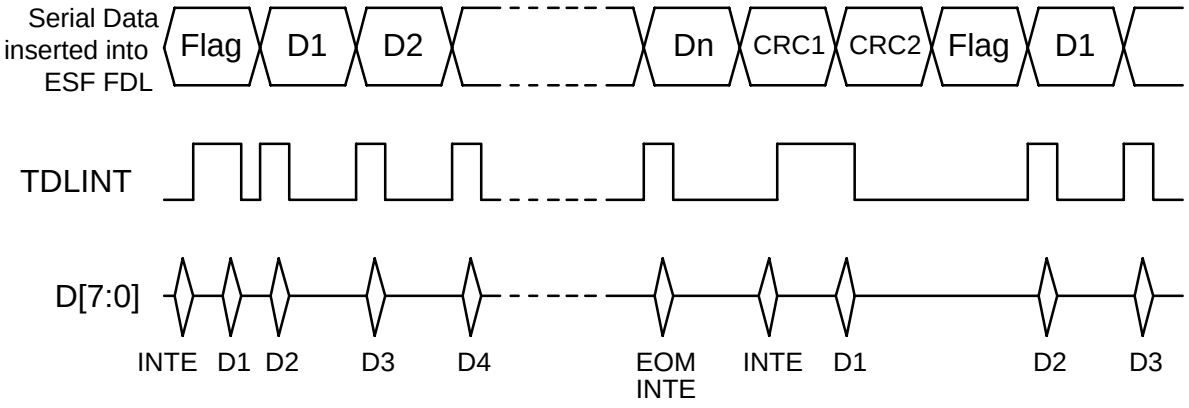
Figure 24 - RFDL FIFO Overrun



This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when two data bytes are present in the FIFO buffer. Each read is composed of two register reads, as described above. In this example, data is not read by the end of B2. An overrun occurs since unread data (Dn-3) has been overwritten by B1. This sets the RDLEOM output high, and resets both the RFDL and the FIFO buffer. The RFDL is held disabled until the RFDL Status Register is read. The start flag sequence is not detected since the RFDL is still held disabled when it occurs. Consequently, the

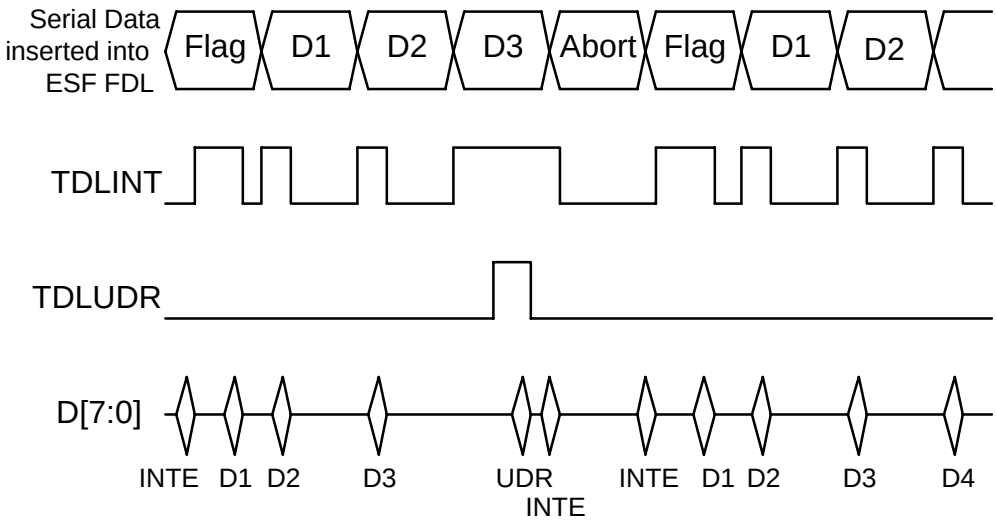
RFDL will ignore the entire frame including the abort sequence (since it has not occurred in a valid frame or during flag reception, according to the RFDL).

Figure 25 - XFDL Normal Data Sequence



This diagram shows the relationship between XFDL inputs and outputs for the case where interrupts and CRC are enabled for regular data transmission. The process is started by setting the INTE bit in the XFDL Configuration Register to logic 1, thus enabling the TDLINT signal. When TDLINT goes high, the interrupt service routine is started, which writes the first byte (D1) of the data frame to the XFDL Transmit Data Register. When this byte begins to be shifted out on the data link, TDLINT goes high. This restarts the interrupt service routine, and the next data byte (D2) is written to the XFDL Transmit Data Register. When D2 begins to be shifted out on the data link, TDLINT goes high again. This cycle continues until the last data byte (Dn) of the frame is written to the XFDL Transmit Data Register. When Dn begins to be shifted out on the data link, TDLINT again goes high. Since all the data has been sent, the interrupt service routine sets the EOM bit in the XFDL Configuration Register to logic 1. The TDLINT interrupt should also be disabled at this time by setting the INTE bit in the XFDL Configuration Register to logic 0. The XFDL will then shift out the two-byte CRC word and closing flag, which ends the frame. Whenever new data is ready, the TDLINT signal can be re-enabled by setting the INTE bit in the XFDL Configuration Register to logic 1, and the cycle starts again.

Figure 26 - XFDL Underrun Sequence



This diagram shows the relationship between XFDL inputs and outputs in the case of an underrun error. An underrun error occurs if the XFDL finishes transmitting the current message byte before the processor writes the next byte into the XFDL Transmit Data Register; that is, the processor fails to write data to the XFDL in time. In this example, data is not written to the XFDL within the time-out period after TDLINT goes high at the beginning of the transmission of byte D3. The TDLUDR interrupt becomes active at this point, and an abort, followed by a flag, is sent out on the data link. Meanwhile, the processor must clear the TDLUDR interrupt by setting the UDR bit in the XFDL Interrupt Status Register to logic 0. The TDLINT interrupt should also be disabled at this time by setting the INTE bit in the XFDL Configuration Register to logic 0. The data frame can then be restarted as usual, by setting the INTE bit logic to 1. Transmission of the frame then proceeds normally.

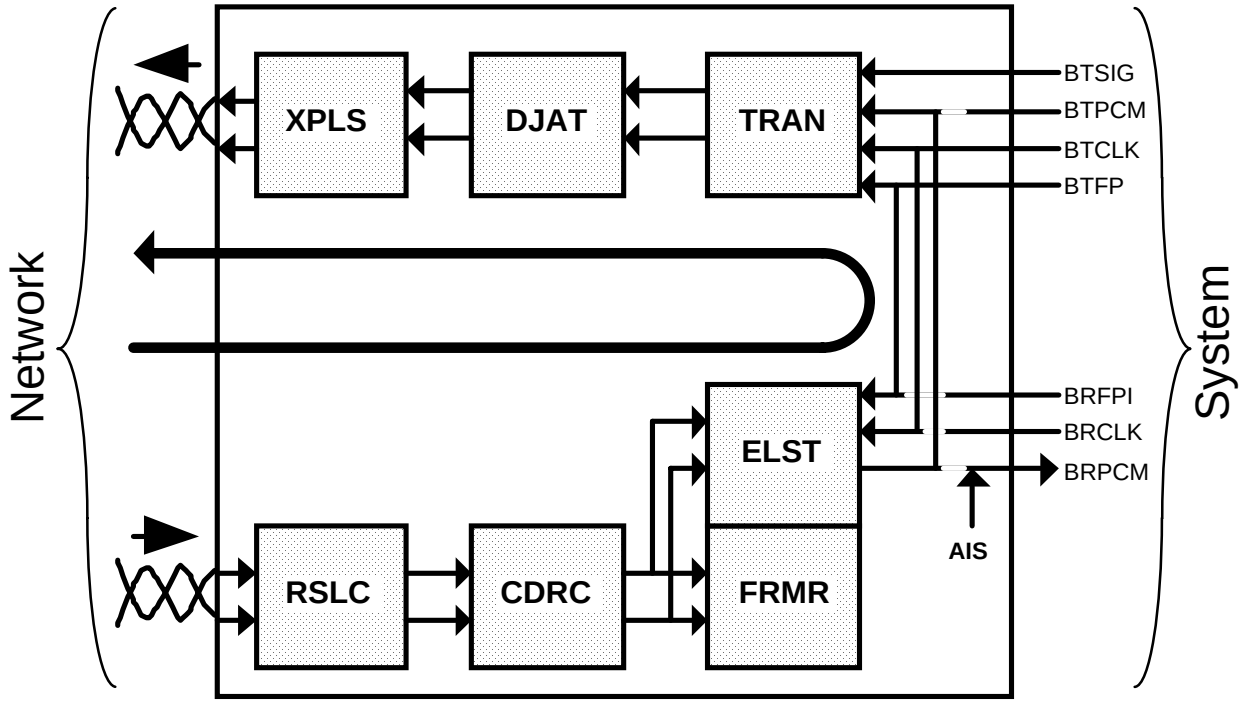
14.4 Using the Loopback Modes

The E1XC provides four loopback modes to aid in network and system diagnostics. The network loopbacks (PAYLOAD and LINE) can be initiated at any time via the µP interface, but are usually initiated once an inband loopback activate code is detected. The system loopbacks (Diagnostic DIGITAL and METALLIC) can be initiated at any time by the system via the µP interface to check the path of system data through the transceiver.

14.4.1 Payload Loopback

When PAYLOAD loopback (PAYLB) is initiated by writing 20H to the Master Diagnostics Register, the E1XC is configured to internally connect the output of the ELST to the PCM input of TRAN. The data is read out of ELST timed to the transmitter clock, and the transmit frame alignment indication is used to synchronize the output frame alignment of ELST. Note, that the BTSIG stream is still presented to the TRAN; therefore, the SIGEN and DLEN bits of the TRAN Configuration register should be cleared to logic 0 if the signalling is to be looped back. Conceptually, the data flow through E1XC in this loopback condition can be shown as follows:

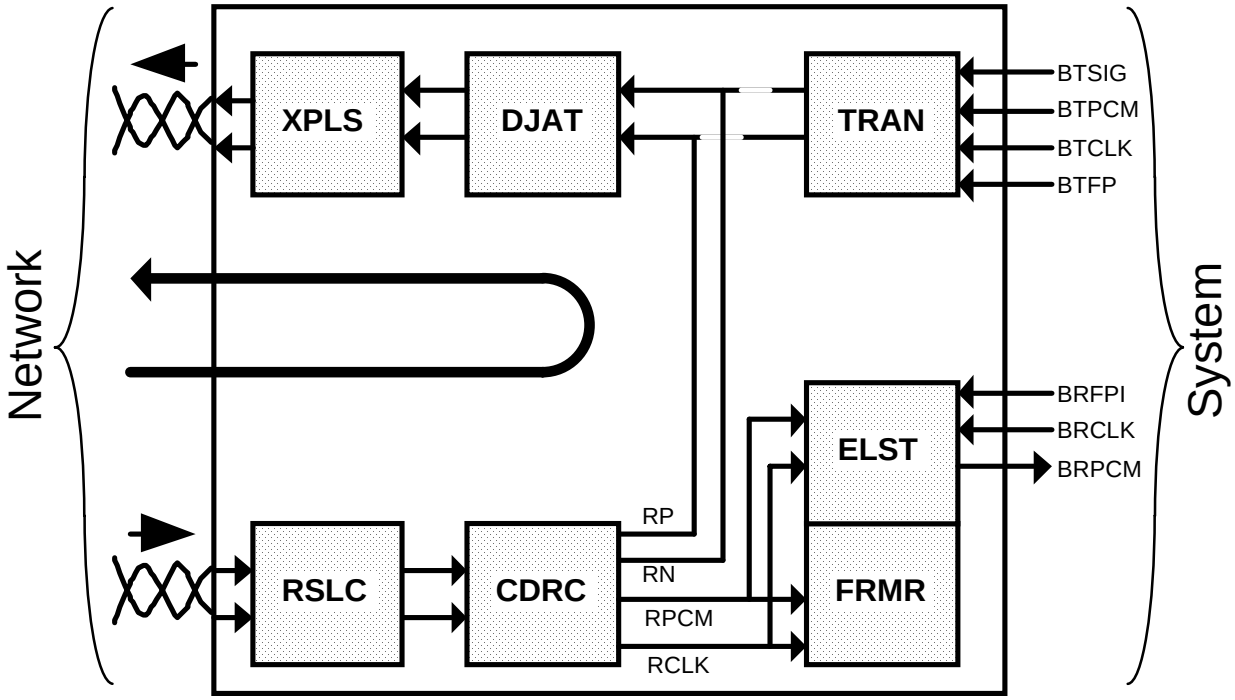
Figure 27 - Payload Loopback



14.4.2 Line Loopback

When LINE loopback (LINELB) is initiated by writing 10H to the Master Diagnostics Register, the E1XC is configured to internally connect the dual-rail positive and negative line data pulses output from CDRC to the dual-rail inputs of DJAT. If either the transmit or receive is in unipolar mode, the appropriate line decoding or encoding is performed. Conceptually, the data flow through E1XC in this loopback condition can be shown as follows:

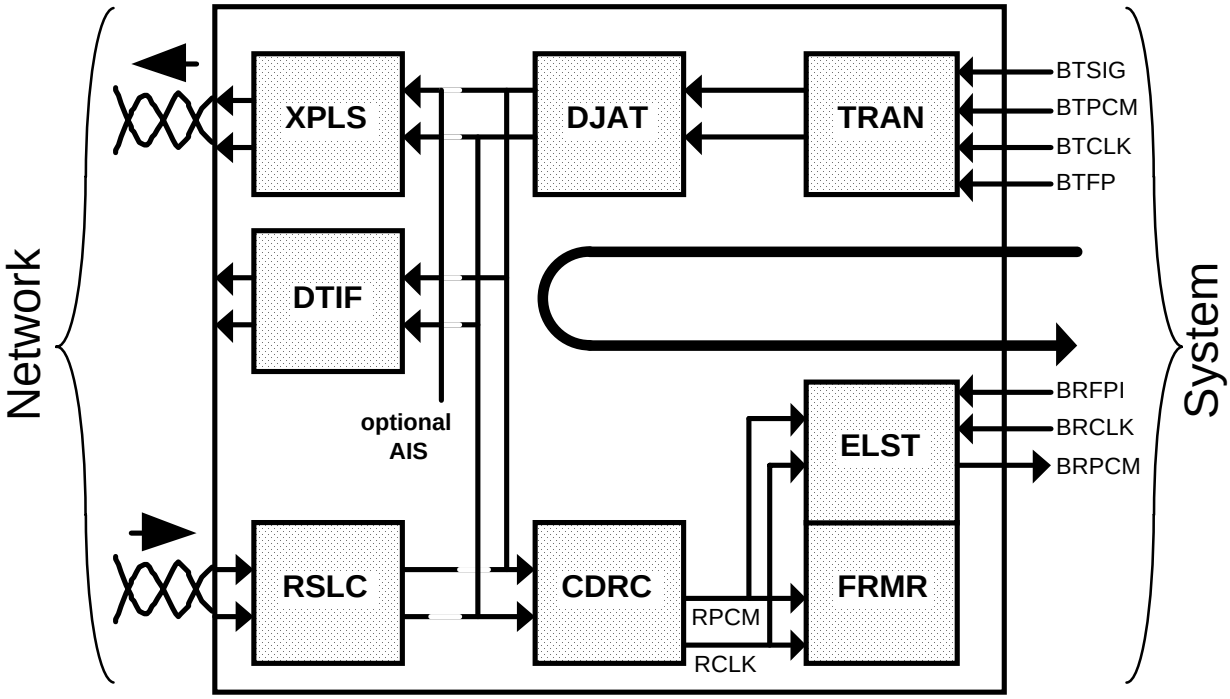
Figure 28 - Line Loopback



14.4.3 Diagnostic Digital Loopback

When Diagnostic Digital loopback (DDLB) is initiated by writing 04H to the Master Diagnostics Register, the E1XC is configured to internally connect the dual-rail positive and negative data pulses output from DJAT to the dual-rail inputs of CDRC. Conceptually, the data flow through E1XC in this loopback condition can be shown as follows:

Figure 29 - Diagnostic Digital Loopback

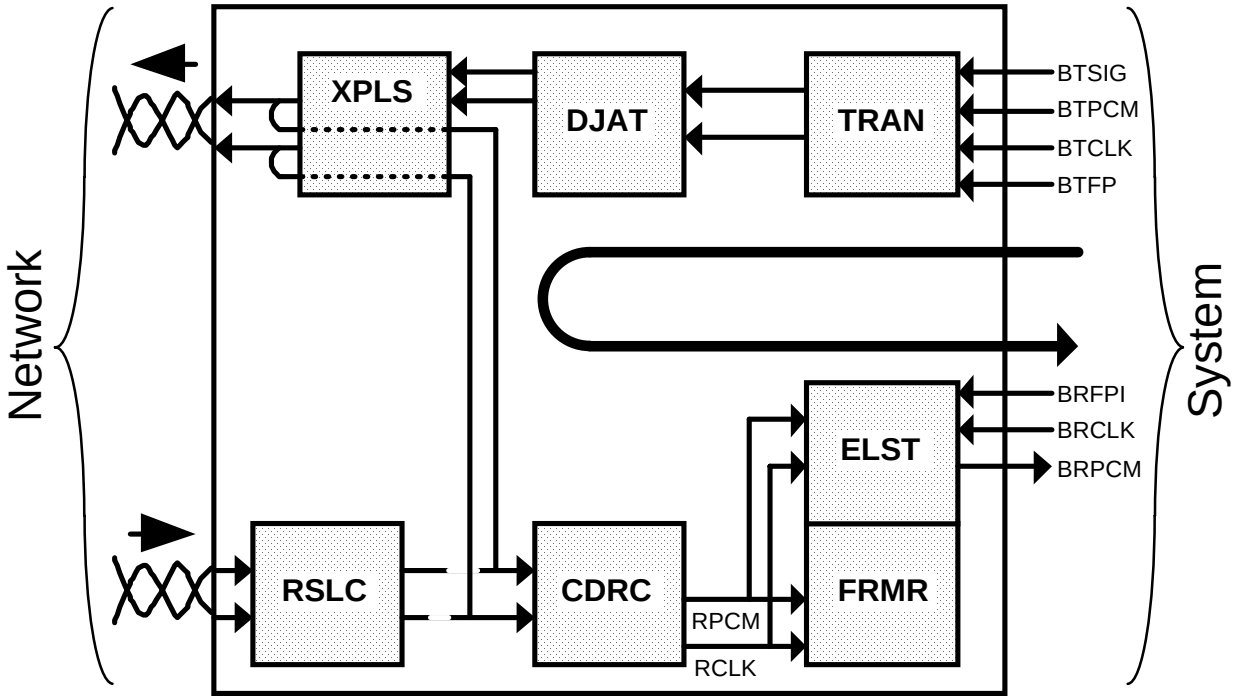


14.4.4 Diagnostic Metallic Loopback

When Diagnostic Metallic loopback (DMLB) is initiated by writing 08H to the Master Diagnostics Register, the E1XC is configured to internally connect the RZ dual-rail positive and negative data pulses from XPLS Performance Monitor, representing the sliced versions of the analog output signals on the TAP and TAN pins, to the dual-rail inputs of CDRC. The Performance Monitor inputs internal to XPLS have a fixed slicing threshold and their monitoring position is located at the driver outputs.

Conceptually, the data flow through E1XC in this loopback condition can be shown as follows:

Figure 30 - Diagnostic Metallic Loopback



14.5 Using the Per-Channel Serial Controllers

14.5.1 Initialization

Before the TPSC block can be used, a proper initialization of the internal registers must be performed to eliminate erroneous control data from being produced on the block outputs. The output control streams should be disabled by setting the PCCE bit in the TPSC Configuration Register to logic 0. Then, all 64 locations of the TPSC must be filled with valid data. Finally, the output streams can be enabled by setting the PCCE bit in the TPSC Configuration Register to logic 1.

14.5.2 Direct Access Mode

Direct access mode to the TPSC is not used in the E1XC. However, direct access mode is selected by default whenever the E1XC is reset. The IND bit within the TPSC Configuration Register must be set to logic 1 after a reset is applied.

14.5.3 Indirect Access Mode

Indirect access mode is selected by setting the IND bit in the TPSC Configuration Register to logic 1. When using the indirect access mode, the status of the BUSY indication bit should be polled to determine the status of the microprocessor access: when the BUSY bit is logic 1, the TPSC is processing an access request; when the BUSY bit is logic 0, the TPSC has completed the request.

The indirect write programming sequence for the TPSC is as follows:

1. Check that the BUSY bit in the TPSC µP Access Status Register is logic 0.
2. Write the timeslot data to the TPSC Timeslot Indirect Data Buffer register.
3. Write RWB=0 and the timeslot address to the TPSC Timeslot Indirect Address/Control Register.
4. Poll the BUSY bit until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 3 and remain at logic 1 until the request is complete.
5. If there is more data to be written, go back to step 1.

The indirect read programming sequence for the TPSC is as follows:

1. Check that the BUSY bit in the TPSC µP Access Status Register is logic 0.
2. Write RWB=1 and the timeslot address to the TPSC Timeslot Indirect Address/Control Register.
3. Poll the BUSY bit, waiting until it goes to a logic 0. The BUSY bit will go to logic 1 immediately after step 2 and remain at logic 1 until the request is complete.
4. Read the requested timeslot data from the TPSC Timeslot Indirect Data Buffer register.
5. If there is more data to be read, go back to step 1.

14.6 Interfacing to the Analog Pulse Slicer

The Receive Data Slicer (RSLC) block provides the first stage of signal conditioning for a G.703 2048 kbit/s serial data stream by converting bipolar line signals to dual rail RZ pulses. Before an RZ output pulse is generated by the

RSLC block, bipolar input signals must rise to 50% (for G.703 2048 kbit/s) of their peak amplitude. This level is referred to as the Slicing Level. The threshold criteria insures accurate pulse or mark recognition in the presence of noise.

The RSLC block relies on an external network for compliance to G.703 120 Ω twisted pair or G.703 75 Ω coax. The RSLC block is configured via an off-chip attenuator pad (see Fig. 4) to operate in one of two modes: terminating mode or bridging mode.

For determining the value of the components in Figure 4, the following constraints apply:

1. The receiver must match the line. ITU-T Recommendation G.703 specifies the minimum return loss allowable:

Frequency range (kHz)	Return loss (dB)
51 to 102	12
102 to 2048	18
2048 to 3072	14

The following constraint maximizes return loss:

$$\frac{R_1 + R_2 \| Z_{in}}{N^2} = Z_0 \qquad (1)$$

where Z_O is the line characteristic impedance,

Z_{in} is the differential input impedance between the RAS and REF input pins (≥ 10kΩ),

N is the transformer turns ratio (device-side to line-side).

The value of R_2 should be much smaller than Z_{in} to decrease the return loss sensitivity to the RSLC input impedance variability.

If Z_L is the terminating load (reflected through the transformer), then return loss is:

$$L_R = -20 \log \left| \frac{Z_L - Z_0}{Z_L + Z_0} \right|$$

$$Zo = \frac{R1(R2 + R3||Zin)}{N^2(R1+ R2+ R3||Zin)}$$ where Zo = line characteristic impedance.

The value of R3 should be much smaller than 10 kΩ to decrease the return loss sensitivity to the RSLC input impedance variability.

If Z_L is the reflected load, then return loss is

$$L_R = -20\log|(Z_L - Zo)/(Z_L + Zo)|$$

Provided tightly toleranced components are used, the ITU-T return loss specifications are easily met.

2. The signal should be attenuated to a level compatible with the slicer.

   The maximum potential between the RAS and REF pins must be less than 1.96V to prevent internal circuitry from saturating.

   The minimum peak amplitude between the RAS and REF pins must be large enough to ensure reliable operation; bit errors may occur if the amplitude is below 213 mV. If the amplitude drops below 105 mV for a 67% slicing threshold and 140 mV for a 50% slicing threshold, the RSLC outputs are forced to logic 0 and a squelch alarm is raised. The squelching prevents the slicing of noise on an idle transmission line. (The SQ status bit goes high whenever the RSLC block is squelching. The block can be configured to generate an interrupt whenever the SQ status bit goes high.)

   The RSLC was not designed for line lengths greater than 1000 ft. Although it can handle considerable flat loss, pulse spreading and inter-symbol interference results in unreliable operation for long line lengths.

   With the above limits in mind, it is recommended the attenuation shall be such that the differential signal level across RAS/REF be 1.96 V peak for the maximum expected signal level at the primary. The following table summarizes the limits:

Table 11 - RSLC Performance Limits

Signal Type	Squelch level between RAS – REF	Min. peak ampl. on the primary	Max. peak ampl. on the primary	Recommended signal gain
DSX-1A	105 mV	1.1	3.3	0.40 V/V
G.703				
120Ω	140 mV	1.35 V	3.96 V	0.50 V/V
75Ω	140 mV	1.07 V	3.10 V	0.63 V/V

ITU-T Recommendation G.703 states the pulse height at the output port must be 3.0V ± 10% for 120Ω twisted pair and 2.37V ± 10% for 75Ω coax with an allowed overshoot of 20% above nominal. The maximum peak amplitude of the primary assumes no transmission line losses and a maximum overshoot. The minimum peak amplitude of the primary assumes a minimum output level at the output port with 6 dB of transmission line loss.

The attenuation provides another constraint on the resistance values:

$$\frac{N\left(R_2 \| Z_{in}\right)}{R_1 + R_2 \| Z_{in}} \leq A_{\max} \qquad (2)$$

where A_{max} is the maximum signal gain allowable (Given in the table above) between the primary and the differential RAS/REF input pins.

This equation assumes that constraint (1) is satisfied (no signal reflection occurs).

Again, the value of R_2 should be much smaller than Z_{in} to decrease the sensitivity to the RSLC input impedance variability.

Based on the above constraints, the following network values are recommended for the two intended applications:

Table 12 - Recommended Rx Network Values

Signal Type	Turns ratio (N ± 5%)	R1 (Ω ± 1%)	R2 (Ω ± 1%)	Squelch level on the primary
G.703				
Zo = 120Ω	1:2	357	121	276 mV ± 20%
Zo = 75Ω	1:2	205	95.3	220 mV ± 20%

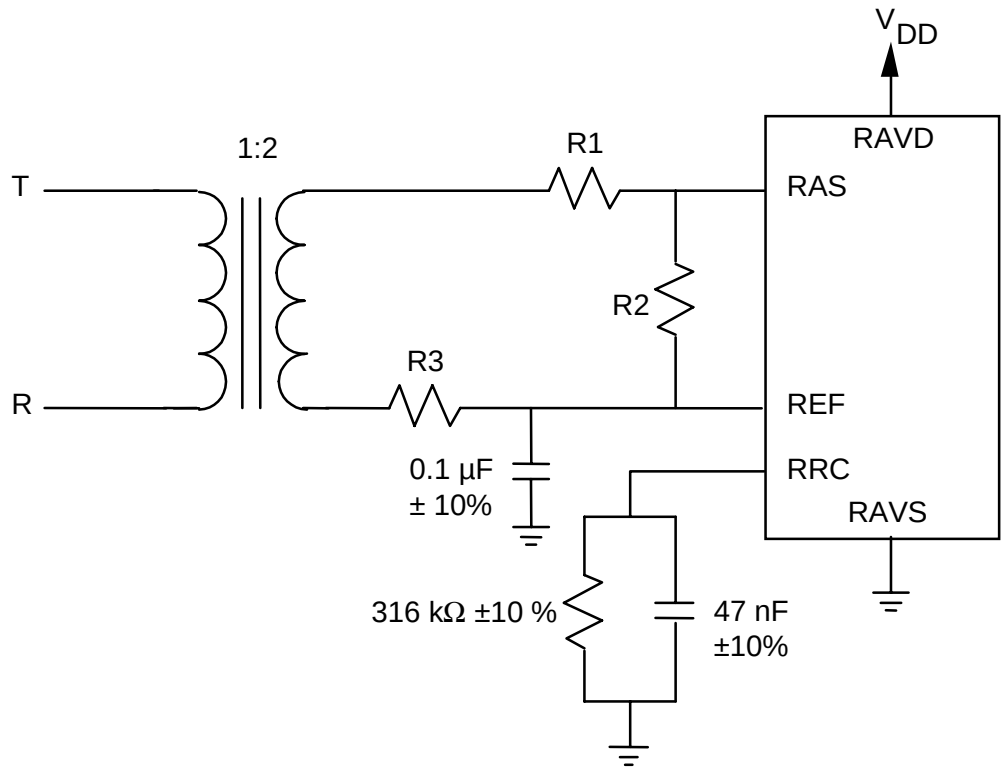
Tight tolerances are required on the resistors and turns ratio to meet the return loss specification.

14.7 Alternative Longitudinally Balanced Receive Interface

Although there is no specification that the E1 termination must be longitudinally balanced, it is sometimes preferable to have it so (e.g. if using controlled impedance PCB traces for connecting the line interface transformer to the PM6341 E1XC).

Therefore, for designs where longitudinal balance is preferred, the following receive line interface (shown in Figure 31) can be used.

Figure 31 - Longitudinally Balanced Receive Line Interface



Notes:

1. All capacitors ceramic
2. Recommended Transformers: BH Electronics 500-1775 (1:1:1);
   Pulse Engineering PE 64931 (1:1:1)
3. Alternatively, a dual part containing both the 1:2CT & 1:1.36 transformers can be used, i.e.:
   BH Electronics 500-1777;
   Pulse Engineering PE64952

There are three constraints on the values of R1, R2, and R3: Return loss must be maximized, the signal level must be attenuated to limit the differential input between RAS/REF, and the line must be longitudinally balanced.

To maximize return loss, the impedance presented by the terminating network must equal the characteristic impedance of the incoming E1 line:

$$\frac{R_1 + R_2 \| Z_{in} + R_3}{N^2} = Z_0 \qquad (1a)$$

where

Z_O is the line characteristic impedance,

Z_{in} is the differential input impedance between the RAS and REF input pins (≥ 10kΩ), and

N is the transformer turns ratio (device-side to line-side).

The value of R_2 should be much smaller than Z_{in} to decrease the sensitivity to the RSLC input impedance variability.

The overall gain of the terminating network must be such that the maximum signal swing between the RAS and REF inputs is less than 1.96Vpeak. The following table summarizes these limits:

Table 13 - Alternative Network RSLC Performance Limits

Signal Type	Squelch level between RAS - REF	Min. peak ampl. on the primary	Max. peak ampl. on the primary	Recommended signal gain
G.703				
120Ω	140 mV	1.35 V	3.96 V	0.50 V/V
75Ω	140 mV	1.07 V	3.10 V	0.63 V/V

Therefore, the component values in the termination network are constrained to:

$$\frac{N\left(R_2 \| Z_{in}\right)}{R_1 + R_2 \| Z_{in} + R_3} \leq A_{\max} \qquad (2a)$$

where

A_{max} is the maximum signal gain allowable (given in the table above) between the primary and the differential RAS/REF input pins.

This constraint assumes that constraint (1a) is met (no signal reflections occur).

Again, the value of R_2 should be much smaller than Z_{in} to decrease the sensitivity to the RSLC input impedance variability.

To meet the third constraint of longitudinal balance, the impedance to between each secondary pin of the transformer and the a.c. ground (through the 0.1µF capacitor attached to the REF input pin) must be equal. This is can be met if:

$$R_3 = R_1 + R_2 \| Z_{in} \quad (3)$$

Based on the above constraints, the following network values are recommended for the two intended applications:

Table 14 - Recommended Alternative Network Values

Signal Type	Turns ratio (N)	R1(Ω)	R2 (Ω)	R3(Ω)	Squelch level on the primary
G.703					
Zo = 120Ω	1:2	118	121	243	276 mV ± 20%
Zo = 75Ω	1:2	54.9	95.3	150	220 mV ± 20%

Tight tolerances are recommended on the resistors (e.g. 1%) and turns ratio (e.g. 5%) in order to maximize the realized return loss value.

14.8 Programming the XPLS Waveform Template

The internal XPLS CODE registers, at address 17H, can be used to create a custom waveform across the analog transmit outputs, TAP and TAN. These eight CODE registers are accessed indirectly through register 16H and contain 4-bit binary values corresponding to one of 16 quantized levels for the amplitude of the output pulse during each of eight synchronous, "high-speed" clock periods within a TCLKO cycle. The full swing of the amplifier outputs TAP and TAN ranges from 0 to 3.86 Volts. The codes select the voltage level as follows:

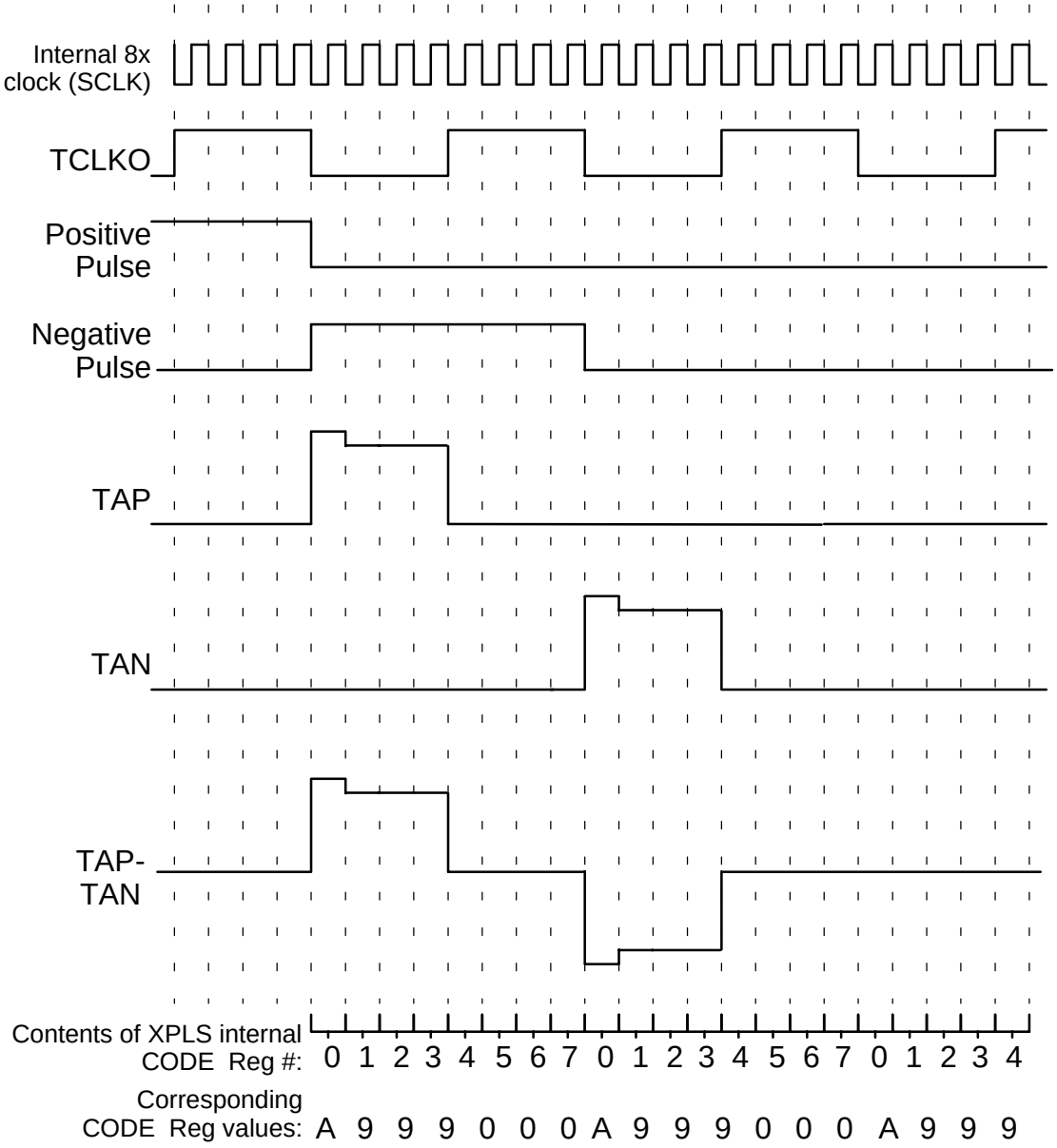
Table 15 - XPLS Typical Output Pulse Amplitudes

CODE (Reg 17H)	Typical Output Voltage	CODE (Reg 17H)	Typical Output Voltage
0000	0.00 V	1000	2.09 V
0001	0.31 V	1001	2.33 V
0010	0.57 V	1010	2.60 V

CODE (Reg 17H)	Typical Output Voltage	CODE (Reg 17H)	Typical Output Voltage
0011	0.82 V	1011	2.85 V
0100	1.08 V	1100	3.11 V
0101	1.33 V	1101	3.36 V
0110	1.59 V	1110	3.61 V
0111	1.84 V	1111	3.86 V

The contents of the CODE registers are used by XPLS and internally applied to the output D/A converter in sequence, beginning with CODE reg #0, on the first falling edge of the internal, synchronous high-speed clock once TCLKO has gone low. The first four codes determine the shape of the bulk of the pulse, whereas the last four codes determine the shape of the tail end of the pulse. Depending on the polarity of the input pulse (either on the positive pulse input or the negative pulse input to XPLS), the bulk of the pulse is generated on either TAP or TAN, with the tail generated on TAN or TAP, respectively. The pulse is produced differentially across the transformer primary so that, for example, while the first four codes are generating the pulse on TAP, TAN is grounded through the output amplifier. To generate the negative portion of the pulse, the last four codes generate the tail of the pulse on TAN while TAP is grounded through the other output amplifier. The ON-resistance of either TAP or TAN output amplifier is nominally 2.5Ω when acting as a ground for the transformer. The output impedance of the amplifier when driving the pulse is typically <0.5Ω at half the bit rate. Figure 17 shows the relationship between the TCLKO, the internal synchronous, high-speed clock SCLK timing, and the application of the CODE register contents for a positive pulse immediately followed by a negative pulse. The resultant waveform across TAP and TAN is also shown.

Figure 32 - CODE Register Sequence During G.803 (120Ω) Pulse Generation



The actual waveform produced at the transformer secondary depends upon the turns ratio of the transformer used, the series resistance on the primary side used to match the line, the output impedance of the amplifier, the on-resistance of the amplifier while providing the transformer ground, and the transformer winding resistance. To ensure that the amplifiers can drive the reflected load, it is

recommended that a transformer have a turns ratio of no more than 1:2. It is also recommended that the codes presented here be used as a guideline and that the actual code values be verified (and modified) on the bench with the device driving the actual transformer and termination expected in the application.

14.9 CODE Register Programming Sequence for Custom Waveforms

To program the XPLS CODE registers for a custom waveform template, the following sequence should be used:

1. Set the RPT bit in the XPLS Configuration Register to logic 0.
2. Write the CODE register address (0-7) in the XPLS CODE Indirect Address register.
3. Write the desired code value to the XPLS CODE Indirect Data Register (register 17H).
4. Repeat steps 2 and 3 until all 8 CODE registers are written.
5. Enable XPLS to generate the new waveform by setting RPT to logic 1.

The contents of the XPLS CODE registers can be reviewed at any time by using the following sequence:

1. Write the CODE register address (0-7) in the XPLS CODE Indirect Address register.
2. Read the XPLS CODE Indirect Data Register (register 17H). This returns the code contents of the desired code register.

14.10 Using the Digital Jitter Attenuator

The key to using DJAT lies in selecting the appropriate divisors for the phase comparison between the selected reference clock and the generated smooth TCLKO.

14.10.1 Default Application

Upon reset, the E1XC default condition provides jitter attenuation with TCLKO referenced to the transmit clock, BTCLK. The DJAT SYNC bit is also logic 1 by default. DJAT is configured to divide its input clock rate, BTCLK, and its output clock rate, TCLKO, both by 48, which is the maximum length of the FIFO. These divided down clock rates are then used by the phase comparator to update the

DJAT DPLL. The phase delay between BTCLK and TCLKO is synchronized to the physical data delay through the FIFO. For example, if the phase delay between BTCLK and TCLKO is 12UI, the FIFO will be forced to lag its output data 12 bits from its input data.

The default mode works well with the transmit backplane running at 2.048MHz.

14.10.2 Data Burst Application

In applications where a higher transmit backplane rate with external gapping is used, a few factors must be considered to adequately filter the resultant TCLKO into a smooth 2.048MHz clock. The magnitude of the phase shifts in the incoming bursty data can be too large to be properly attenuated by the PLL alone. However, the magnitudes, and the frequency components of these phase shifts are known, and are most often multiples of 8 kHz.

When using a gapped higher rate clock, the phase shifts of the input clock with respect to the generated TCLKO in this case can be large, but when viewed over a longer period, such as a frame, there is little net phase shift. Therefore, by choosing the divisors appropriately, the large phase shifts can be filtered out, leaving a stable reference for the DPLL to lock onto. In this application, the N1 and N2 divisors should be changed to FFH (i.e. divisors of 256). Consequently, the frequency of the clock inputs to the phase discriminator in the PLL is 8 kHz. The DJAT SYNC option must be disabled, since the divisor magnitude of 256 is not an integer multiple of the FIFO length, 48.

The self-centering circuitry of the FIFO should be enabled by setting the CENT register bit. This sets up the FIFO read pointer to be at least 4 UI away from the end of the FIFO registers, and then disengages. Should variations in the frequency of input clock or the output clock cause the read pointer to drift to within one unit interval of FIFO overflow or underflow, the pointer will be incrementally pushed away by the LIMIT control without any loss of data.

With SYNC disabled, CENT and LIMIT enabled, the maximum tolerable phase difference between the bursty input clock and the smooth TCLKO is 40UI. Phase wander between the two clock signals is compensated for by the LIMIT control.

14.10.3 Elastic Store Application

In multiplex applications where the jitter attenuation is not required, the DJAT FIFO can be used to provide an elastic store function. For example, in a M12 application, the data is written into the FIFO at 2.048MHz and the data is read out of the FIFO with a gapped DS2 rate clock applied on TCLKI. In this

configuration, the Timing Options OCLKSEL[1:0] bits should be programmed to 01, the TCLKISEL bit should be programmed to 1, and the SMCLKO bit should be programmed to 1. Also, the DJAT SYNC and LIMIT bits should be disabled and the CENT bit enabled. This provides the maximum phase difference between the input clock and the gapped output clock of 40UI. The maximum jitter and wander between the two clocks is 8UIpp.

14.10.4 Alternate TCLKO Reference Application

In applications where TCLKO is referenced to an Nx8 kHz clock source applied on TCLKI, DJAT can be configured by programming the output clock divisor, N2, to FFH and the input clock divisor, N1, to the value (N-1). The resultant input clocks to the phase comparator are both 8kHz. The DJAT SYNC and LIMIT bits should be disabled in this configuration.

14.10.5 Changing the Jitter Transfer Function

The DJAT phase lock loop has a single order low pass jitter transfer function. By default, the corner frequency is 8.8 Hz. The corner may be moved by the appropriate selection of clock divisors:

$$f_c = \frac{2048\,\text{kHz}}{1536\pi(N2+1)}$$

where

f_c = corner frequency

N2= value in the Output Clock Divisor Control register

Ensure the Reference Clock Divisor Control value (N1) is also modified to satisfy:

$$\frac{f_{REF}}{N1+1} \qquad \frac{2048}{N2+1}\ \text{kHz}$$

14.11 Using the Performance Monitor Counter Values

All PMON block event counters are of sufficient length so that the probability of counter saturation over a one second interval at a 10^{-3} BER is less than 0.001%. The odds of any one of the counters saturating during a one second sampling interval go up as the BER increases. At some point, the probability of counter saturation reaches 50%. This point varies, depending upon the framing format

and the type of event being counted. The BER at which the probability of counter saturation reaches 50% is shown below for various counters:

Table 16 - BER Required for PMON Counter Saturation

Counter	BER
LCV	4.0×10^{-3}
FER	4.0×10^{-3}
CRCE	cannot saturate
FEBE	cannot saturate

Below these 50% points, the relationship between the BER and the counter event count (averaged over many one second samples) is essentially linear. Above the 50% point, the relationship between BER and the average counter event count is highly non-linear due to the likelihood of counter saturation. Figures 18-20 show this relationship for various counters and framing formats. These graphs can be used to determine the BER, given the average event count. In general, if the BER is above 10^{-3}, the average counter event count cannot be used to determine the BER without considering the statistical effect of occasional counter saturation.

Figure 33 - LCV Count vs. BER

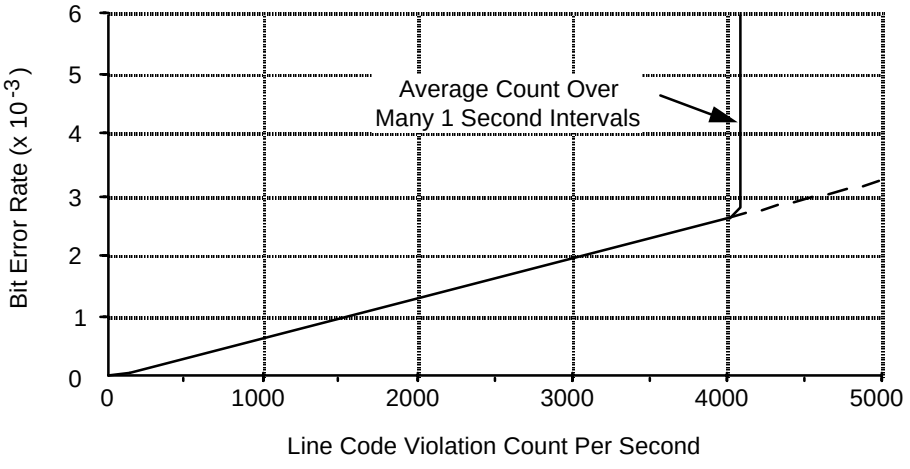
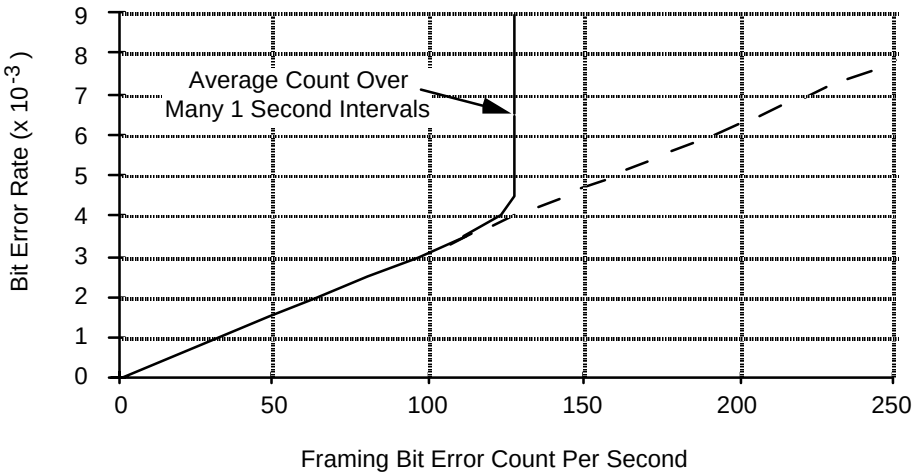
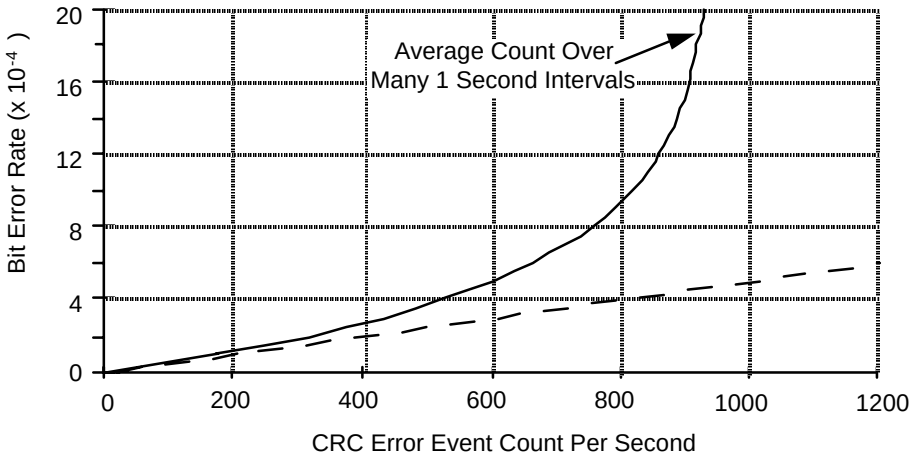


Figure 34 - FER Count vs. BER



Since the maximum number of CRC sub-multiframes that can occur in one second is 1000, the 10-bit FEBE and CRCE counters cannot saturate in one second. Despite this, there is not a linear relationship between BER and CRC-4 block errors due to the nature of the CRC-4 calculation. At BERs below 10^{-4}, there tends to be no more than one bit error per sub-multiframe, so the number of CRC-4 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above 10^{-4}, each CRC-4 error is often due to more than one bit error. Thus, the relationship between BER and CRCE count becomes non-linear above a 10^{-4} BER. This must be taken into account when using CRC-4 counts to determine the BER. Since FEBEs are indications of CRCEs at the far end, and are accumulated identically to CRCEs, the same explanation holds for the FEBE event counter.

Figure 35 - CRCE Count vs. BER



15 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on VDD with Respect to GND	-0.5V to +VDD
Voltage on Any Pin	-0.5V to +VDD
Latch-Up Current (T_A = -40°C to +85°C)	100 mA

16 CAPACITANCE

Symbol	Parameter	Typ	Units	Conditions
Cin	Input Capacitance	10	pF	T_A = 25°C, f = 1 MHz
Cout	Output Capacitance	10	pF	T_A = 25°C, f = 1 MHz
Cbidir	Bidirectional Capacitance	10	pF	T_A = 25°C, f = 1 MHz

17 D.C. CHARACTERISTICS

TA=-40° to +85°C, VDD=5V ±10%

Table 17 - E1XC D.C. Characteristics

Symbol	Parameter	Min	Typ.	Max	Units	Conditions
V_{DD},$^{RA}V_{D}$, $^{TA}V_{D}$	Power Supply	4.5	5.0	5.5	Volts	
V_{IL}	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0		V_{DD}+0.5	Volts	Guaranteed Input HIGH Voltage
V_{RAS}	Analog Input Voltage	A_{VS} -0.6		A_{VD} +0.6	Volts	
V_{OL} (TTL)	Output or Bidirectional Low Voltage		0.1	0.4	Volts	V_{DD} = 5.0V, I_{OL} = -4 mA for Data Bus Pins and -2 mA for others, Notes 3, 5
V_{OH} (TTL)	Output or Bidirectional High Voltage	2.4	4.7		Volts	V_{DD} = 5.0V, I_{OL} = 4 mA for Data Bus Pins and 2 mA for others, Notes 3, 5
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			1.0	Volts	
V_{TH}	Reset Input Hysteresis Voltage		1.0		Volts	
I_{ILPU}	Input Low Current	+20	+83	+200	µA	V_{IL} = GND, Notes 1, 3, 5
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}, Notes 1, 3, 5
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3, 5
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}, Notes 2, 3, 5
I_{DDOP1}	Operating Current			95	mA	V_{DD} = 5.5 V, Outputs Unloaded, XCLK = 49.152 MHz BTCLK = 2.048MHz, Notes 4, 5

Symbol	Parameter	Min	Typ.	Max	Units	Conditions
I_{DDOP2}	Operating Current		65		mA	VDD=5.0 V, Outputs Unloaded, transmitting all ones, Note 5
I_{DDOP3}	Operating Current		50		mA	VDD=5.0 V, Outputs Unloaded, transmitting 50% ones, Note 5
I_{DDOP4}	Operating Current		35		mA	VDD=5.0 V, Outputs Unloaded, transmitting all zeroes, Note 5

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. I_{DDOP} is the sum of all power supply currents when transmitting all ones from XPLS, producing 3.0 volt pulses across a 50 ohm load. RSLC is active.
6. Typical values are given as an aid to the system designer. This product is not tested to the typical values provided.

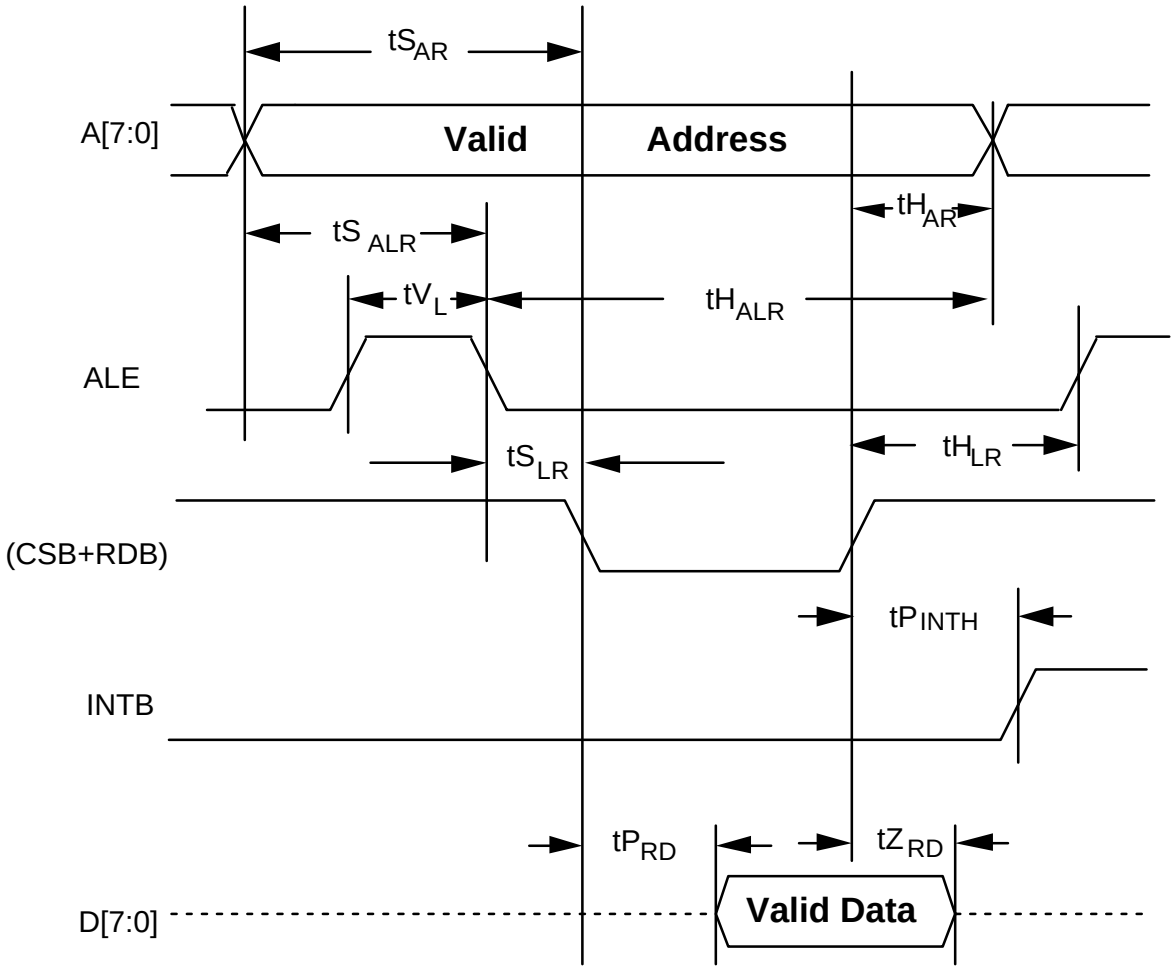
18 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

TA=-40° to +85°C, VDD=5V ±10%

Table 18 - Microprocessor Read Access (Figure 36)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	10		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Deasserted to Output Tri-state		20	ns
tP_{INTH}	Valid Read Deasserted to INTB High (Assumes a 2 kΩ pull up.)		100	ns

Figure 36 - Microprocessor Read Access Timing



Notes on Microprocessor Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor Interface timing applies to normal mode register accesses only.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

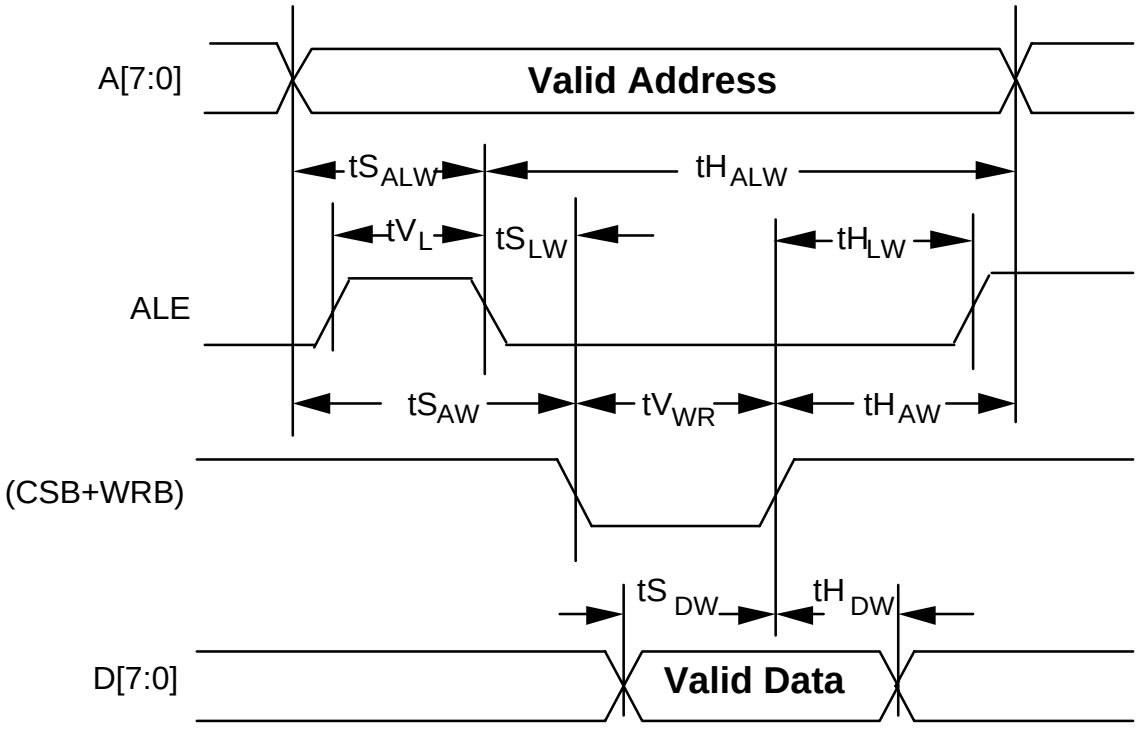
7. In non-multiplexed address/data bus architectures ALE should be held high; parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

8. Parameter tH_{AR} is not applicable when address latching is used.

Table 19 - Microprocessor Write Access (Figure 37)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	15		ns
tH_{ALW}	Address to Latch Hold Time	15		ns
tV_{L}	Valid Latch Pulse Width	15		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	13		ns
tH_{DW}	Data to Valid Write Hold Time	10		ns
tH_{AW}	Address to Valid Write Hold Time	13		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 37 - Microprocessor Write Access Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

19 E1XC I/O TIMING CHARACTERISTICS

TA=-40° to +85°C, VDD=5V ±10%

Table 20 - Backplane Transmit Input Timing (Figure 38)

Symbol	Description	Min	Max	Units
	Backplane Transmit Clock Frequency		2.1	MHz
	Backplane Transmit Clock Duty Cycle	30	70	%
tS_{TCLK}	BTCLK to Backplane Input Set-up Time	20		ns
tH_{TCLK}	BTCLK to Backplane Input Hold Time	20		ns

Figure 38 - Backplane Transmit Input Timing Diagram

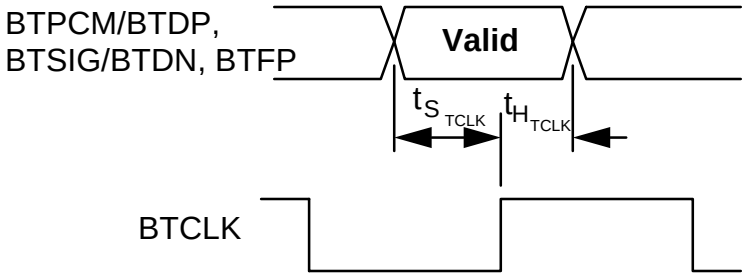
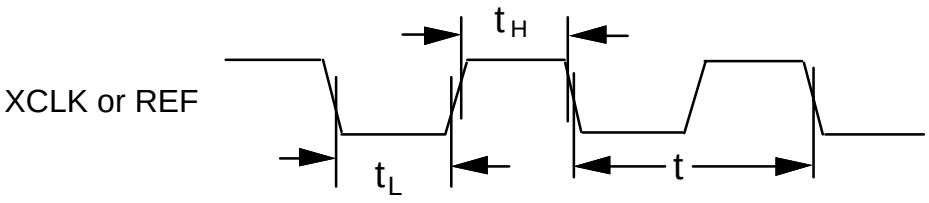


Table 21 - XCLK=49.152MHz Input (Figure 39)

Symbol	Description	Min	Max	Units
t_{LXCLK}	XCLK Low Pulse Width (note 1)	8		ns
t_{HXCLK}	XCLK High Pulse Width (note 1)	8		ns
tXCLK	XCLK Period (typically 1/49.152 MHz or 20.4 ns)	20		ns
	XCLK Duty Cycle (note 2)	40	60	%
t_{L}REF	REF Low Pulse Width (notes 1,3)	4		tXCLK
t_{H}REF	REF High Pulse Width (notes 1,3)	4		tXCLK
t_{REF}	REF Period	8		tXCLK

Figure 39 - XCLK=49.152MHz Input Timing



Notes on XCLK=49.152MHz Timing:

1. Input Clock high pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the rise and fall ramps.

2.

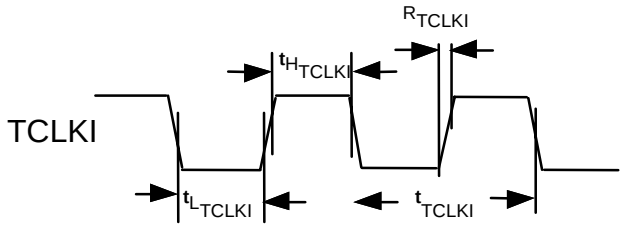
3. Duty cycle is measured at the 50% points of the rise and fall ramps.

4. The reference input (REF) timing applies to E1XC inputs BTCLK and TCLKI.

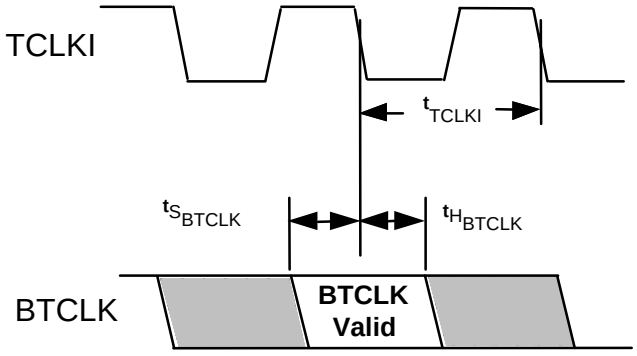
Table 22 - TCLKI Input (Figure 40)

Symbol	Description	Min	Max	Units
	TCLKI Instantaneous Frequency (when used for DJAT REF or for mux operation). Long term average frequency is typically 2.048MHz		4.10	MHz
	TCLKI Frequency (when DJAT PLL not used), typically 16.384MHz		16.8	MHz
t_{HTCLKI}	TCLKI High Duration (TCLKI=2.048MHz) (note 1)	100		ns
t_{LTCLKI}	TCLKI Low Duration (TCLKI=2.048MHz) (note 1)	100		ns
t_{RTCLKI}	TCLKI Rise Time		5	ns
t_{SBTCLK}	BTCLK falling to TCLKI falling Set-up Time (only applicable when Reg 04H FIFOBYP bit = 1)	45		ns
t_{HBTCLK}	BTCLK falling to TCLKI falling Hold Time (only applicable when Reg 04H FIFOBYP bit = 1)	0		ns

Figure 40 - TCLKI Input Timing



TCLKI = 2.048 MHz – Normal Mode



TCLKI = 16.238 MHz – FIFO Bypass Mode

Notes on TCLKI Input Timing:

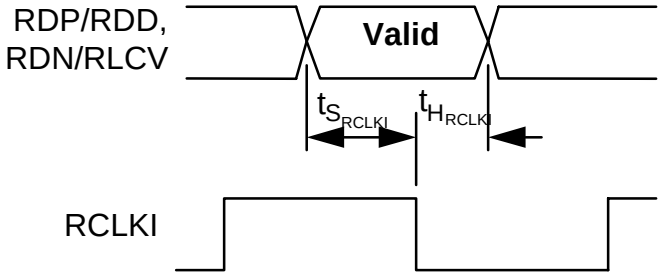
1. These parameters are guaranteed by design - not measured.

Table 23 - Digital Receive Interface Input Timing (Figure 41)

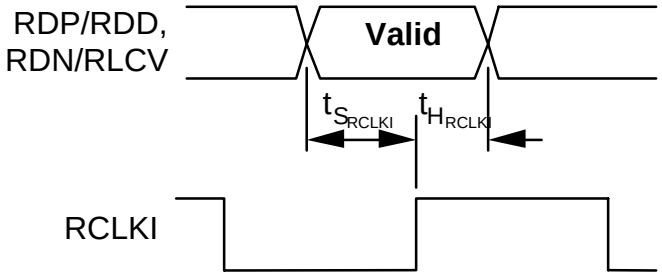
Symbol	Description	Min	Max	Units
	Digital Receive Clock Frequency (nom. 2.048)		2.1	MHz
	Digital Receive Clock Duty Cycle	30	70	%
tS_{RCLKI}	RCLKI to NRZ Digital Receive Input Set-up Time	20		ns

Symbol	Description	Min	Max	Units
tH_{RCLKI}	RCLKI to NRZ Digital Receive Input Hold Time	20		ns
tW_{RDPN}	RZ Digital Receive Input Pulse Width (note 3)	200	300	ns

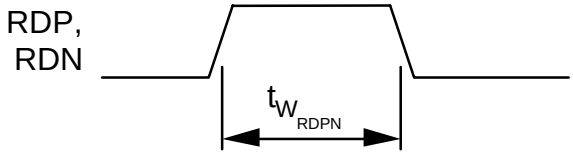
Figure 41 - Digital Receive Interface Input Timing Diagram



With RFALL bit =1, DCR or TUNI=1



With RFALL bit =0, DCR or TUNI=1



With DCR=0 & TUNI=0

Table 24 - Transmit Data Link Input Timing (Figure 42)

Symbol	Description	Min	Max	Units
tS_{DIN}	TDLCLK to TDLSIG Input Set-up Time (note 4)	80		ns
tH_{DIN}	TDLCLK to TDLSIG Input Hold Time	20		ns

Figure 42 - Transmit Data Link Input Timing Diagram

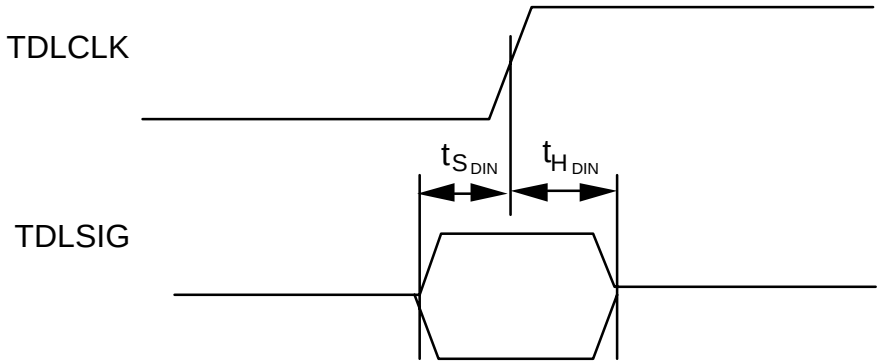
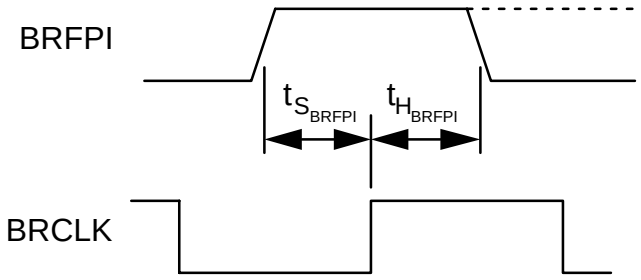


Table 25 - Backplane Receive Input Timing (Figure 43)

Symbol	Description	Min	Max	Units
t_{SBRFPI}	BRCLK to BRFPI Input Set-up Time	20		ns
t_{HBRFPI}	BRCLK to BRFPI Input Hold Time	20	1 frame -500ns	ns
	BRCLK freq - Reg 07H HSBPSEL=0 (note 3)		2.41	MHz
	BRCLK freq - Reg 07H HSBPSEL=1 (note 3)		3.00	MHz

Figure 43 - Backplane Receive Input Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. Parameter guaranteed by design, not production tested.

4. Parameter guaranteed by characterization, not production tested.

Table 26 - Receive Data Link Output Timing (Figure 44)

Symbol	Description	Min	Max	Units
$t_{PRDLCLK}$	RDLCLK to RDLSIG Propagation Delay		50	ns

Figure 44 - Receive Data Link Output Timing Diagram

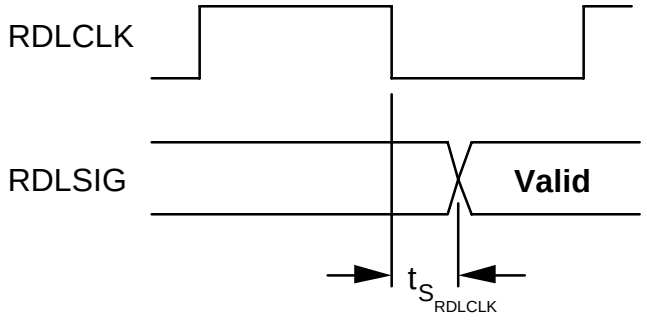


Table 27 - Backplane Receive Output Timing (Figure 45)

Symbol	Description	Min	Max	Units
t_{PBRCLK}	BRCLK to Backplane Output Signals Propagation Delay (note 3)		50	ns

Figure 45 - Backplane Receive Output Timing Diagram

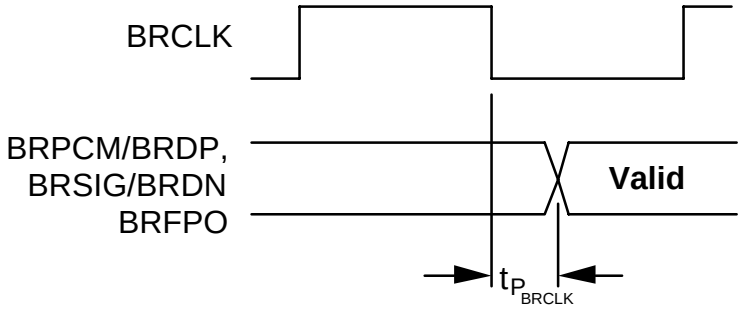


Table 28 - Recovered Data Output Timing (Figure 46)

Symbol	Description	Min	Max	Units
t_{PRCLKO}	RCLKO to Recovered Line Data Output Signals Propagation Delay (note 3)		50	ns

Figure 46 - Recovered Data Output Timing Diagram

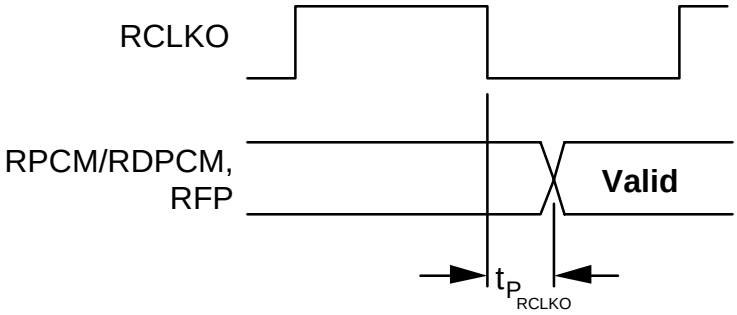
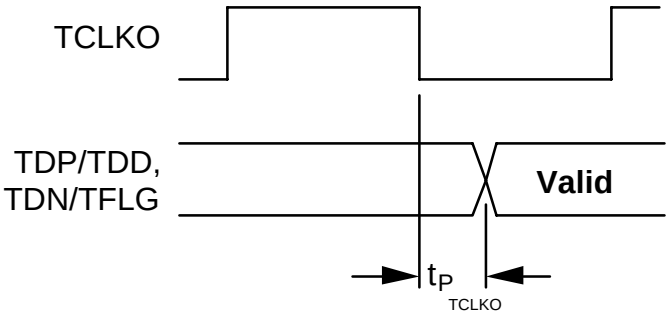


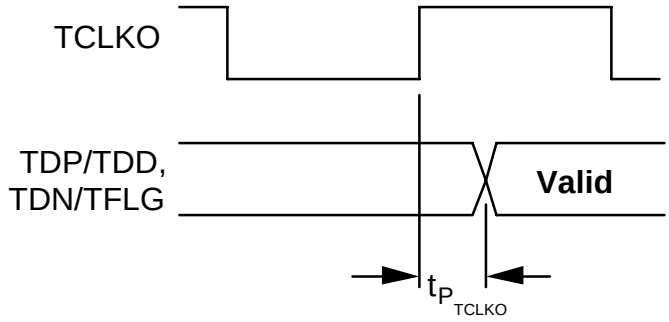
Table 29 - Transmit Interface Output Timing (Figure 47)

Symbol	Description	Min	Max	Units
t_{PTCLKO}	TCLKO to Digital Transmit Data Output Signals Propagation Delay (note 3)		50	ns

Figure 47 - Transmit Interface Output Timing Diagram



With TRISE bit=0



With TRISE bit= 1

Table 30 - Transmit Data Link DMA Interface Output Timing (Figure 48)

Symbol	Description	Min	Max	Units
t_{PTINT}	Transmit Data Register Serviced (WRB low) to TDLINT Low Propagation Delay		50	ns
t_{PUDR}	UDR bit written low (WRB high) to TDLUDR Low Propagation Delay		50	ns

Figure 48 - Transmit Data Link DMA Interface Output Timing Diagram

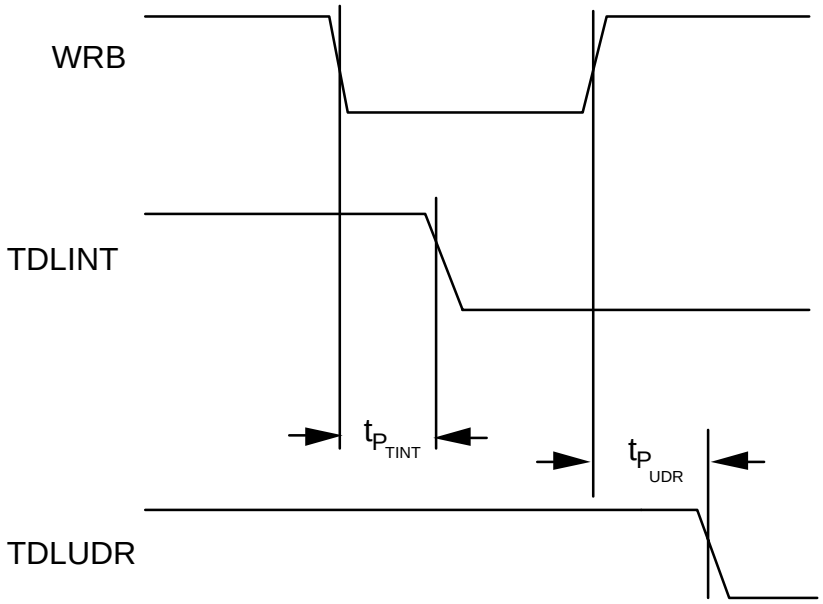
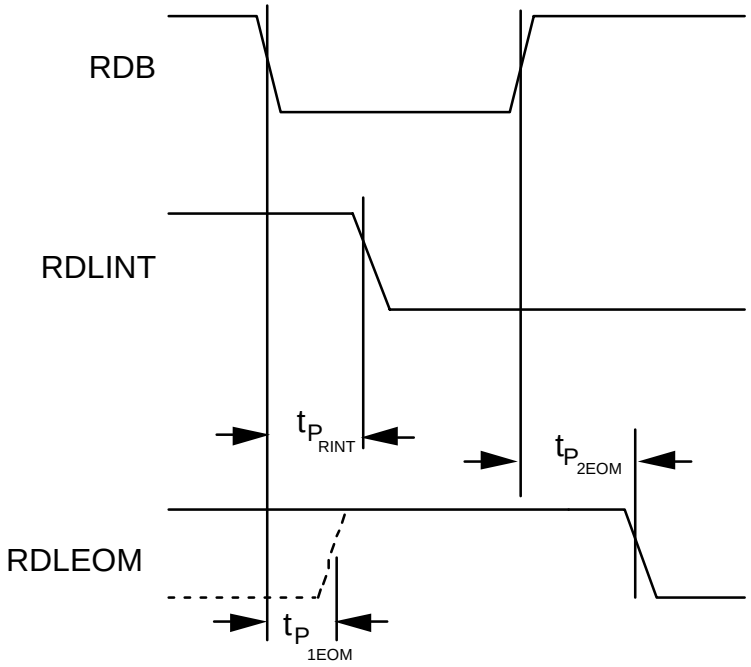


Table 31 - Receive Data Link DMA Interface Output Timing (Figure 49)

Symbol	Description	Min	Max	Units
t_{PRINT}	Receive Data Register Serviced (RDB low) to RDLINT Low Propagation Delay		70	ns
t_{P1EOM}	Receive Data Register Serviced (RDB low) to RDLEOM High Propagation Delay		80	ns
t_{P2EOM}	Receive Status Register Serviced (RDB high) to RDLEOM Low Propagation Delay		50	ns

Figure 49 - Receive Data Link DMA Interface Output Timing Diagram



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

3. Parameter guaranteed by characterization, not production tested.

20 ANALOG CHARACTERISTICS

TA=-40° to +85°C, VDD=5V ±10%

Typical Cond. TA=25°C, VDD = 5.0V

Table 32 - Receive Analog Input Threshold

Symbol	Description	Min	Typ	Max	Units
	E1 Slicing Threshold Voltage (note 1)	45	50	55	% of Peak

Table 33 - Analog Receive Data Input Timing (Figure 50)

Symbol	Description	Min	Max	Units
tW_{AIN}	Receive Analog Data Signal Pulse Width (note 2)	200	300	ns

Figure 50 - Analog Receive Data Input Timing Diagram

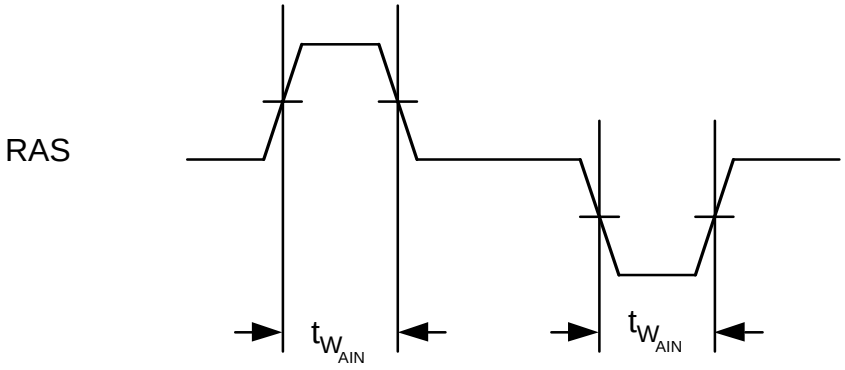


Table 34 - Transmit Pulse Symmetry

Symbol	Parameter	Min	Typ.	Max	Units	Conditions
	Positive/Negative Pulse Width Imbalance			5.0	%	Circuit per Figure 10, Measured at transformer secondary.
	Positive/Negative Pulse Amplitude Imbalance			5.0	%	Circuit per Figure 10, Measured at transformer secondary.

Notes on Analog Specifications:

1. Typical Values are given as an aid to the system designer. Products are not production tested to the typical values provided in the data sheet.

2. Parameter guaranteed by design not production tested.

21 ORDERING AND THERMAL INFORMATION

Table 35 - E1XC Ordering Information

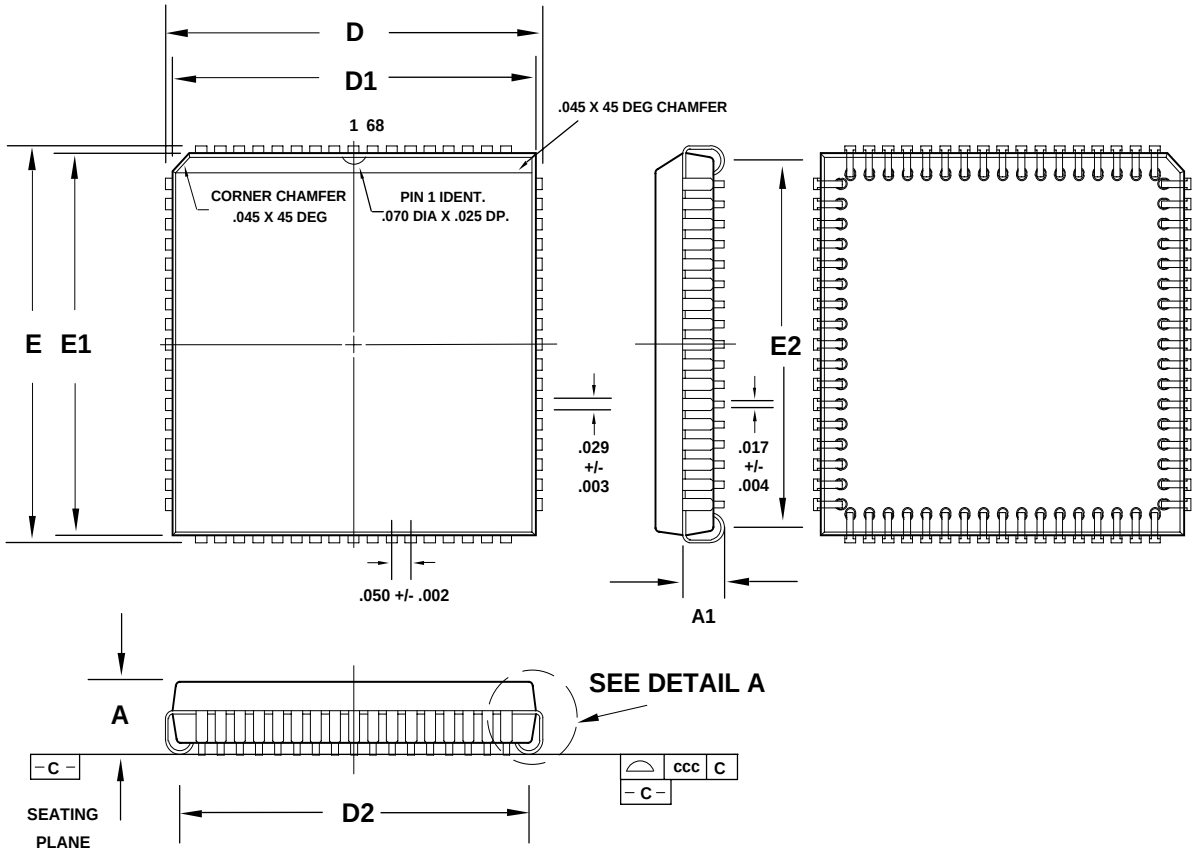
PART NO.	DESCRIPTION
PM6341-QI	68 Plastic Leaded Chip Carrier (PLCC)
PM6341-RI	80 Plastic Quad Flat Pack (PQFP)

Table 36 - E1XC Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM6341-QI	-40°C to 85°C	43 °C/W	13 °C/W
PM6341-RI	-40°C to 85°C	67 °C/W	15 °C/W

22 MECHANICAL INFORMATION

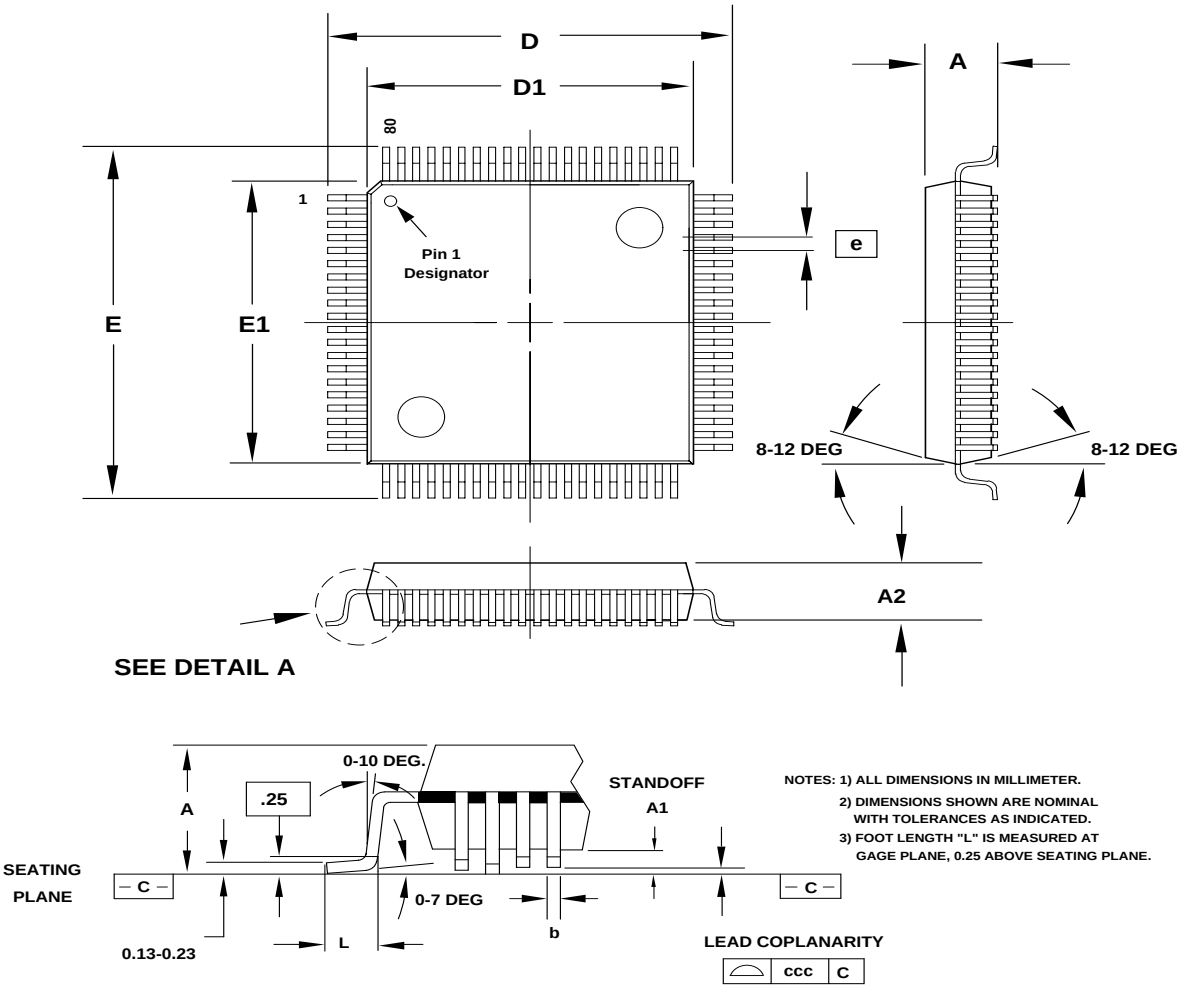
Figure 51 - 68 Pin Plastic Leaded Chip Carrier (Q Suffix)



NOTES : 1. ALL DIMENSIONS IN INCHES

PACKAGE TYPE: 68 PIN PLASTIC LEADED CHIP CARRIER-PLCC									
Dim.	A	A1	D	D1	D2	E	E1	E2	ccc
Min.	0.165	0.090	0.985	0.950	0.890	0.985	0.950	0.890	
Nom.	0.175		0.990	0.954	0.920	0.990	0.954	0.920	
Max.	0.200	0.130	0.995	0.958	0.930	0.995	0.958	0.930	0.004

Figure 52 - 80 Pin Copper Leadframe Plastic Quad Flat Pack (R Suffix):



PACKAGE TYPE: 80 PIN METRIC PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 14 x 14 x 2.0 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	2.00	0.05	1.95	16.95	13.90	16.95	13.90	0.73		0.22	
Nom.	2.15	0.15	2.00	17.20	14.00	17.20	14.00	0.88	0.65		
Max.	2.35	0.25	2.10	17.45	14.10	17.45	14.10	1.03		0.38	0.10

NOTES

NOTES

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