# Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter

The MC14569B is a programmable divide–by–N dual 4–bit binary or BCD down counter constructed with MOS P–channel and N–channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase–locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14568B, MC14522B or MC14526B for Frequency Synthesizer Applications
- · All Outputs are Buffered
- Schmitt Triggered Clock Conditioning

#### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

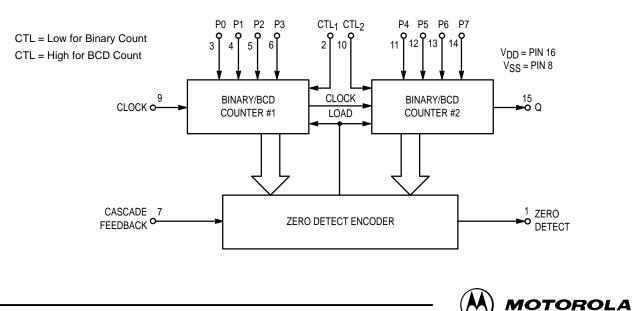
Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	– 0.5 to + 18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	$-$ 0.5 to V_DD + 0.5	V
l <sub>in</sub> , l <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	– 65 to + 150	°C
тլ	Lead Temperature (8–Second Soldering)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating:

Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

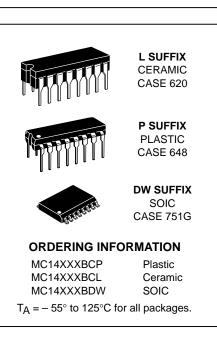
Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

#### **BLOCK DIAGRAM**





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MC14569B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

		V <sub>DD</sub>	- 5	5°C		25°C		125	S°C	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур #	Max	Min	Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V <sub>OL</sub>	5.0 10 15		0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub> "1" Level	VOH	5.0 10 15	4.95 9.95 14.95		4.95 9.95 14.95	5.0 10 15		4.95 9.95 14.95		Vdc
$\label{eq:VO} \begin{array}{ll} \mbox{Input Voltage} & "0" \mbox{ Level} \\ (V_O = 4.5 \mbox{ or } 0.5 \mbox{ Vdc}) \\ (V_O = 9.0 \mbox{ or } 1.0 \mbox{ Vdc}) \\ (V_O = 13.5 \mbox{ or } 1.5 \mbox{ Vdc}) \end{array}$	VIL	5.0 10 15		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	Vdc
$      (V_O = 0.5 \text{ or } 4.5 \text{ Vdc})  ``1" \text{ Level} \\       (V_O = 1.0 \text{ or } 9.0 \text{ Vdc}) \\       (V_O = 1.5 \text{ or } 13.5 \text{ Vdc}) $	VIH	5.0 10 15	3.5 7.0 11		3.5 7.0 11	2.75 5.50 8.25		3.5 7.0 11		Vdc
$\begin{array}{l} \text{Output Drive Current} \\ (V_{OH} = 2.5 \ \text{Vdc}) \\ (V_{OH} = 4.6 \ \text{Vdc}) \\ (V_{OH} = 9.5 \ \text{Vdc}) \\ (V_{OH} = 13.5 \ \text{Vdc}) \end{array}$	ЮН	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	  	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8		- 1.7 - 0.36 - 0.9 - 2.4		mAdc
	IOL	5.0 10 15	0.64 1.6 4.2		0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4	-	mAdc
Input Current	l <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	_	_	_	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0 10 15		5.0 10 20		0.005 0.010 0.015	5.0 10 20		150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	Γ	5.0 10 15	$I_{T} = (0.58 \ \mu A/kHz) f + I_{DD}$ $I_{T} = (1.20 \ \mu A/kHz) f + I_{DD}$ $I_{T} = (1.95 \ \mu A/kHz) f + I_{DD}$ $I_{T} = (1.95 \ \mu A/kHz) f + I_{DD}$						μAdc	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\* The formulas given are for the typical characteristics only at 25  $^\circ\text{C}.$ 

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where: I<sub>T</sub> is in  $\mu$ A (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

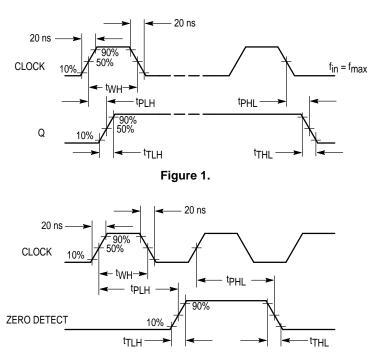
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

## SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = $25^{\circ}$ C)

		VDD		All Types		
Characteristic	Symbol	Vdc	Min	Тур #	Max	Unit
Output Rise Time	tτlh	5.0 10 15		100 50 40	200 100 80	ns
Output Fall Time	tthr	5.0 10 15		100 50 40	200 100 80	ns
Turn–On Delay Time Zero Detect Output	<sup>t</sup> PLH	5.0 10 15		420 175 125	700 300 250	ns
Q Output		5.0 10 15		675 285 200	1200 500 400	ns
Turn–Off Delay Time Zero Detect Output	<sup>t</sup> PHL	5.0 10 15		380 150 100	600 300 200	ns
Q Output		5.0 10 15		530 225 155	1000 400 300	ns
Clock Pulse Width	twh	5.0 10 15	300 150 115	100 45 30		ns
Clock Pulse Frequency	fcl	5.0 10 15		3.5 9.5 13.0	2.1 5.1 7.8	MHz
Clock Pulse Rise and Fall Time	tŢĹĦ, ťŢĦĹ	5.0 10 15		NO LIMIT		μs

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# SWITCHING WAVEFORMS





#### INPUTS

**P0**, **P1**, **P2**, **P3** (**Pins 3**, **4**, **5**, **6**) — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

**P4**, **P5**, **P6**, **P7** (**Pins 11**, **12**, **13**, **14**) — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

**Clock (Pin 9)** — Preset data is decremented by one on each positive transition of this signal.

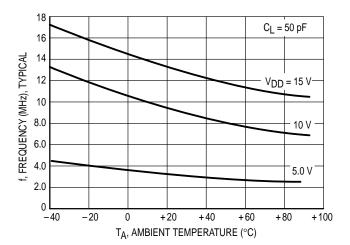
#### OUTPUTS

Zero Detect (Pin 1) — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

**Q** (Pin 15) — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

The MC14569B is a programmable divide–by–N dual 4–bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL<sub>1</sub> and CTL<sub>2</sub>.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles, one



## CONTROLS

**Cascade Feedback (Pin 7)** — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are "don't cares." Refer to Table 1 for output characteristics.

**CTL<sub>1</sub> (Pin 2)** — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

**CTL<sub>2</sub> (Pin 10)** — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

#### SUPPLY PINS

VSS (Pin 18) — Negative Supply Voltage. This pin is usually connected to ground.

**V<sub>DD</sub>** (Pin 16) — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

## **OPERATING CHARACTERISTICS**

pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14568B, MC14522B or the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to "0", Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to  $V_{DD}$ .

PIN	ASSIG	NME	ENT
ZERO DETECT	1•	16	□ v <sub>DD</sub>
CTL1	2	15	]Q
P0 [	3	14	] P7
P1 [	4	13	] P6
P2 [	5	12	] P5
P3 [	6	11	] P4
CASCADE FEEDBACK	7	10	
V <sub>SS</sub> [	8	9	сгоск

Table 1. Mode Controls (Cascade Feedback = Low)

Counter Co	ntrol Values	Divide Ratio				
CTL <sub>1</sub>	CTL <sub>2</sub>	Zero Detect	Q			
0	0	256	256			
0	1	160	160			
1	0	160	160			
1	1	100	100			

NOTE: Data Preset Inputs (P0–P7) are "Don't Cares" while Cascade Feedback is Low.

Table 2. Mode Controls ( $CTL_1 = Low, CTL_2 = Low, Cascade Feedback = High$ )

			Preset	Inputs				Divide	e Ratio	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	256	256	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•			•	•	•		X	
•	•	•	•		•	•	•	•	X	
•	•	•	•		•	•	•		x	
0	0	1	0	0	0	0	0	32	x	
•	•	•	•		•	•			x	
	.	•	.	.	.	•			x	
•	•	•				•		.	x	
0	1	0	0	0	0	0	0	64	x	
•	•	•				•		•	x	
•		•		.	.	•			x	
	.	•	.	.	.	•			x	
0	1	1	1	1	1	1	1	127	x	
1	0	0	0	Ó	0	0	0	128	128	Q Output Active
•									•	
•						•				
			.	.	.	•	•			
1	0	0	0		0	0	0	136	136	
	l .		l .		ľ.	•	ľ.	•		
•		•				•		.	.	
•		•				•				
1	1	1	1	1	1	1	1	255	255	¥
27	26	25	24	23	22	21	20		•	
128	64	32	16	8	4	2	1			Bit Value
Counter #2 Counter #1 Binary Binary										Counting Sequence

P7         P6         P3         P4         P3         P2         P1         P0         Zaro Detect         Q         Comments           0         0         0         0         0         0         0         160         Max Count           0         0         0         0         0         0         1         X         X           0         0         0         0         0         1         1         X         X           0         0         0         0         0         1         1         X         X           1         -         -         -         -         -         -         X         X           1         -         -         -         -         -         -         X         X           0         0         0         1         0         0         1         19         X           1         -         -         -         -         -         -         X         X           1         -         -         -         -         -         -         X         X           1         -         -					Inputs					Ratio	
0       0       0       0       0       1       X       X       X       Minequility         0       0       0       0       0       0       1       0       2       X       Minequility         0       0       0       0       0       1       1       3       X       Minequility         0       0       0       0       1       1       3       X       Minequility         1       -       -       -       -       -       -       -       X       X         1       -       -       -       -       -       -       -       X       X         0       0       0       1       0       0       0       10       X       X         1       -       -       -       -       -       -       X       X         0       0       1       1       0       0       0       1       19       X         1       -       -       -       -       -       -       X       X       X         0       1       1       0       0       0 <t< th=""><th>P7</th><th>P6</th><th>P5</th><th>P4</th><th>P3</th><th>P2</th><th>P1</th><th>P0</th><th></th><th>Q</th><th>Comments</th></t<>	P7	P6	P5	P4	P3	P2	P1	P0		Q	Comments
0       0       0       0       0       0       1       0       2       X       Min Count         0       0       0       0       0       0       1       1       3       X         1       1       1       3       X         1       1       1       3       X         1       1       1       1       3       X         1       1       1       1       1       1       X         1       1       1       1       1       1       X         0       0       0       1       0       0       1       9       X         1       1       0       0       1       19       X         1       1       0       0       1       19       X         1       1       0       0       1       19       X         1       1       0       0       0       1       19       X         1       1       0       0       0       0       1       1       1         1       1       0       0       0       0 <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>160</td> <td>160</td> <td>Max Count</td>	0	0	0	0	0	0	0	0	160	160	Max Count
0       0       0       0       1       1       3       X         1       1       1       1       3       X       X         1       1       1       1       1       1       X       X         1       1       1       1       1       1       1       X       X         1       1       1       1       1       1       1       1       1       X         0       0       0       1       0       0       0       1       1       X         1       1       1       1       1       1       1       1       1       1       1         0       0       1       1       0       0       1       1       1       1         1       1       0       0       0       0       20       X       X         1       1       1       0       0       0       30       X       X         1       1       1       0       0       0       0       30       X       X         1       1       1       0       0       0	0	0	0	0	0	0	0	1			
.       .	0	0	0	0	0	0	1	0			Min Count
.       .       .       .       .       .       .       .       .       .       .       .       .       X         0       0       0       1       0       0       0       1       9       X         0       0       0       1       0       0       0       10       X       X         1       -       -       -       -       -       -       X       X         0       0       0       1       1       0       0       1       X       X         0       0       1       1       0       0       1       19       X         0       0       1       1       0       0       1       19       X         1       -       -       -       -       -       X       X       X         0       1       1       0       0       0       0       30       X       X         1       -       -       -       -       -       X       X       X         1       -       -       -       -       -       X       X       X<	0	0	0	0	0	0	1	1	3		
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0       0       1       0       0       0       10       X         1       1       0       0       0       10       X         1       1       1       0       1       19       X         0       0       1       19       X         1       1       0       0       1       19       X         0       0       1       0       0       19       X         1       1       0       0       1       19       X         1       1       0       0       1       19       X         1       1       0       0       1       19       X         1       1       0       0       0       0       20       X         1       1       0       0       0       0       30       X         1       1       0       0       0       0       40       X         1       1       0       0       0       0       30       X         1       1       0       0       0       0       40       X         1	•	•	•	•	•	•	•	•	•		
·       ·	0	0	0	0	1	0	0	1	9	Х	
·       ·	0	0	0	1	0	0	0	0	10		
·         ·         ·         ·         ·         ·         ·         ·         ×	•	•	•	•	•	•	•	•	•		
0       0       0       1       1       0       0       0       1       19       X         0       0       1       0       0       0       0       0       10       20       X         1       1       0       0       0       0       0       0       20       X         1       1       1       0       0       0       0       0       30       X         0       0       1       1       0       0       0       0       30       X         1       1       0       0       0       0       0       30       X         1       1       0       0       0       0       0       0       30       X         1       1       0       0       0       0       0       40       X         1       1       0       0       0       0       0       40       X         1       1       0       0       0       0       0       0       0       10       10         1       1       0       0       0       0       0	•	•	•	•	•	•	•	•	•		
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0       1       0       0       0       0       40       X         i       i       i       i       i       i       X       X         i       i       i       i       i       i       X       X         i       i       i       i       i       i       i       i       i         1       0       1       0       0       0       0       50       X         i       i       i       i       i       i       i       i       i       i         1       0       1       0       0       0       0       50       X         i       i       i       i       i       i       i       i       i       i         1       1       0       0       0       0       i       i       i       i         1       1       1       0       0       0       i       i       i       i         1       1       1       0       0       0       i       i       i       i         1       1       1       1       i       i	•	•	•	•	•	•	•	•	•		
·       ·       ·       ·       ·       ·       ·       ×       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         ·       <	•	•	•	•	•	•	•	•	•		
·       ·       ·       ·       ·       ·       ·       ×       ×       ×         0       1       0       1       0       0       0       0       50       X         0       1       0       1       0       0       0       0       50       X         1       -       -       -       -       X       X       X         1       -       -       -       -       -       X       X         1       -       -       -       -       -       X       X         1       1       0       0       0       0       60       X         1       1       0       0       0       0       70       X         1       1       1       0       0       0       70       X         1       1       1       0       0       0       80       80       Q Output Active         1       0       0       0       0       0       80       80       Q Output Active         1       1       1       1       1       1       1       1       1	0	1	0	0	0	0	0	0	40		
·       ·       ·       ·       ·       ·       ·       X         0       1       0       0       0       0       50       X          ·       ·       ·       ·       ·       ·       ·       ·       X         ·       ·       ·       ·       ·       ·       ·       X       X         ·       ·       ·       ·       ·       ·       ·       ·       X         ·       ·       ·       ·       ·       ·       ·       ·       X       X         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·	•	•	•	•	•	•	•	•	•		
0       1       0       1       0       0       0       50       X         i       i       i       i       i       i       i       X         i       i       i       i       i       i       i       X         i       i       i       i       i       i       i       X         i       i       i       i       i       i       i       i       i         i       i       i       i       i       i       i       i       i       i         i       i       i       i       i       i       i       i       i       i       i         i       i       i       i       i       i       i       i       i       i       i       i         i	•	•	•	•	•	•	•	•	•		
·       ·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         0       1       1       0       ·       ·       ·       ·       ·       ×       ×         0       1       ·       ·       ·       ·       ·       ·       ·       ×       ×         0       · <t< td=""><td>•</td><td>•</td><td>•</td><td>•</td><td>•</td><td>•</td><td>•</td><td>•</td><td>•</td><td></td><td></td></t<>	•	•	•	•	•	•	•	•	•		
·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         0       1       1       0       0       0       0       0       60       ×       ×         0       1       1       0       0       0       0       60       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ·       ×       ·         ·	0	1	0	1	0	0	0	0	50		
·       ·       ·       ·       ·       ·       ·       ·       ×       ×         0       1       1       0       0       0       0       0       60       X         ·       ·       ·       ·       ·       ·       ·       ·       ·       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         0       1       1       0       0       0       0       70       X         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         1       1       1       0       0       0       0       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         ·       ·       ·       ·       ·       ·       ·       · <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td></td> <td></td>	•	•	•	•	•	•	•	•	•		
0       1       1       0       0       0       0       60       X         .             X         .            X       X         .           X       X         0       1       1       0       0       0       70       X         .           X       X         .           X       X         .           X       X         .           X       X              X       X              X       X               X	•	•	•	•	•	•	•	•	•		
·       ·       ·       ·       ·       ·       ·       ×       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         0       1       1       1       0       0       0       0       70       ×       ×         0       1       1       1       0       0       0       0       70       ×         ·       ·       ·       ·       ·       ·       ·       ·       ·       ×         1       1       1       0       0       0       0       0       70       ×         ·       ·       ·       ·       ·       ·       ·       ·       ·       ×         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         1       0       0       0       0       0       0       ·       ·       ·       ·       ·         1       0       0       0       0       0       0       0       0       ·       ·       ·       · <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td></td> <td></td> <td></td>	•	•	•	•	•	•	•	•			
.       .       .       .       .       .       .       .       .       .       .       X         0       1       1       1       0       0       0       0       70       X         .       .       .       .       .       .       .       .       X       X         .       .       .       .       .       .       .       X       X         .       .       .       .       .       .       .       .       X         .       .       .       .       .       .       .       .       X         1       0       0       0       0       0       0       0       0       0         .       .       .       .       .       .       .       .       .       .         1       0       0       0       0       0       .       .       .       .         1       0       0       0       0       0       .       .       .       .         1       1       1       0       0       0       150       150	0	1	1	0	0	0	0	0	60		
·       ·       ·       ·       ·       ·       ·       X         0       1       1       0       0       0       0       70       X         ·       ·       ·       ·       ·       ·       ·       ·       X         ·       ·       ·       ·       ·       ·       ·       ·       X         ·       ·       ·       ·       ·       ·       ·       ·       X         ·       ·       ·       ·       ·       ·       ·       ·       ·       X         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         1       0       0       0       0       0       0       ·       ·       ·         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         1       0       0       0       0       ·       ·       ·       ·       ·         1       1       1       0       0       0       ·       ·       ·       ·       ·       ·         1<	•	•	•	•	•	•	•	•	•		
0       1       1       1       0       0       0       70       X               X       X               X       X              X       X         1       0       0       0       0       0       80       80       Q Output Active                X         1       0       0       0       0       0       80       80       Q Output Active                   1       0       0       0       0       0       90       90                     1       1       1       0       0       0       150       150              <	•	•	•	•	•	•	•	•	•		
·       ·       ·       ·       ·       ·       ·       ×       ×         ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         1       0       0       0       0       0       0       0       0       80       80       Q Output Active         ·       ·       ·       ·       ·       ·       ·       ·       ·       ×       ×         1       0       0       0       0       0       0       80       80       Q Output Active         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         1       0       0       0       0       0       90       90       90         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         1       0       0       0       0       0       90       90       ·       ·       ·       ·         1       1       1       0       0       0       1       ·       ·       ·       ·       ·       · <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td></td> <td></td> <td></td>	•	•	•	•	•	•	•	•			
·       ·       ·       ·       ·       ·       ·       ·       X         1       0       0       0       0       0       0       80       80       Q Output Active         ·       ·       ·       ·       ·       ·       ·       ·       X         1       0       0       0       0       0       0       80       80       Q Output Active         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         1       0       0       1       ·       ·       ·       ·       ·       ·         1       0       0       1       ·       ·       ·       ·       ·       ·         1       0       0       0       0       ·       ·       ·       ·       ·       ·       ·         1       1       1       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·	0	1	1	1	0	0	0	0	70		
·       ·       ·       ·       ·       ·       ·       X       Q Output Active         1       0       0       0       0       0       0       0       80       80       Q Output Active         ·       ·       ·       ·       ·       ·       ·       ·       ·       ·       ·         ·	•	•	•	•	•	•	•	•	•		
1       0       0       0       0       0       80       80       Q Output Active         .                 .                 1       0       0       1       0       0       0       90       90                    1       0       0       1       0       0       0       90       90                              1       1       1       0       0       0       150       150                    1       1       1       1       0       0       1       159       159          80       40	•	•	•	•	•	•	•	•	•		
.       .	•	•									
.       .	1	0	0	0	0	0	0	0	80	80	Q Output Active
.       .	•	•	•	•	•	•	•	•	•	•	
1       0       0       1       0       0       0       90       90         .                 .                 .                 1       1       1       0       0       0       150       150          1       1       1       0       0       0       150       150  1       1       1       0       0       1       159       159          80       40       20       10       8       4       2       1        Bit Value	•	•	•	•	•	•	•	•	•	•	
.       .											
.       .	1	0	0	1	0	0	0	0	90	90	
.       .	•	•	•	•	•	•	•	•	•	•	
1       1       1       0       0       0       150       150         .       .       .       .       .       .       .       .       .         .       .       .       .       .       .       .       .       .         1       1       1       1       0       0       1       159       159       Image: state stat	•	•	•	•	•	•	•	•	•	•	
.       .											
•       •	1	1	1	1	0	0	0	0	150	150	
·       ·	•	•	•	•	•	•	•	•	•	· ·	
1       1       1       1       0       0       1       159       159       ♥         80       40       20       10       8       4       2       1       Bit Value         Counter #2	•	•	•	•	•	•	•	•	•	· ·	
80         40         20         10         8         4         2         1         Bit Value           Counter #2         Counter #1         Counting							-				
Counter #2 Counter #1 Counting						-			159	159	¥
	80	40	20	10	8			1			Bit Value
Binary BCD Sequence											
		Bin	ary			BC	D				Sequence

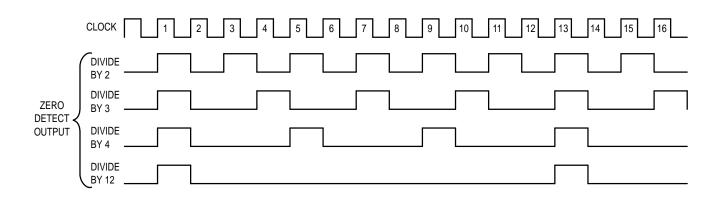
 $\label{eq:table_transform} \textbf{Table 3. Mode Controls} \; (\text{CTL}_1 = \text{High}, \; \text{CTL}_2 = \text{Low}, \; \text{Cascade Feedback} = \text{High})$ 

				Values				Divide	Ratio	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	Х	Х	Illegal State
0	0	0	0	0	0	1	0	2	Х	Min Count
0	0	0	0	0	0	1	1	3	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•			•	•	•	Х	
0	0	0	0		1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X X	
•	•	•	•	• 1	•	•	•	• 31	X	
0	0	1	0	0	0	0	0	32	X	
0						•	•		X	
								•	X	
								•	X	
0	0	1	1	0	0	0	0	48	X	
•	,	•		l .	l .	•	·	•	•	
•	•	•	•		•	•	•	•	•	
•	•	•	•		•	•	•	•	•	
0	1	0	0	0	0	0	0	64	х	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	1	0	0	0	0	80	Х	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	1	1	0	0	0	0	112	Х	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	0	0	0	0	128	128	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	· ·	•	•	•	•	•	•	•	•	
•	•	•		• 0	•	•	•	• 144	• 144	
									144	
								•		
1	0	0	1	1	1	1	1	159	159	↓
27	2 <sup>6</sup>	2 <sup>5</sup>	24	23	2 <sup>2</sup>	21	2 <sup>0</sup>			
128	64	32	16	8	4	2	1			Bit Value
		ter #2	1		Coun		1			Counting
BCD Binary									Sequence	
	A No Output (Always Low)									· ·

 Table 4. Mode Controls ( $CTL_1 = Low, CTL_2 = High, Cascade Feedback = High$ )

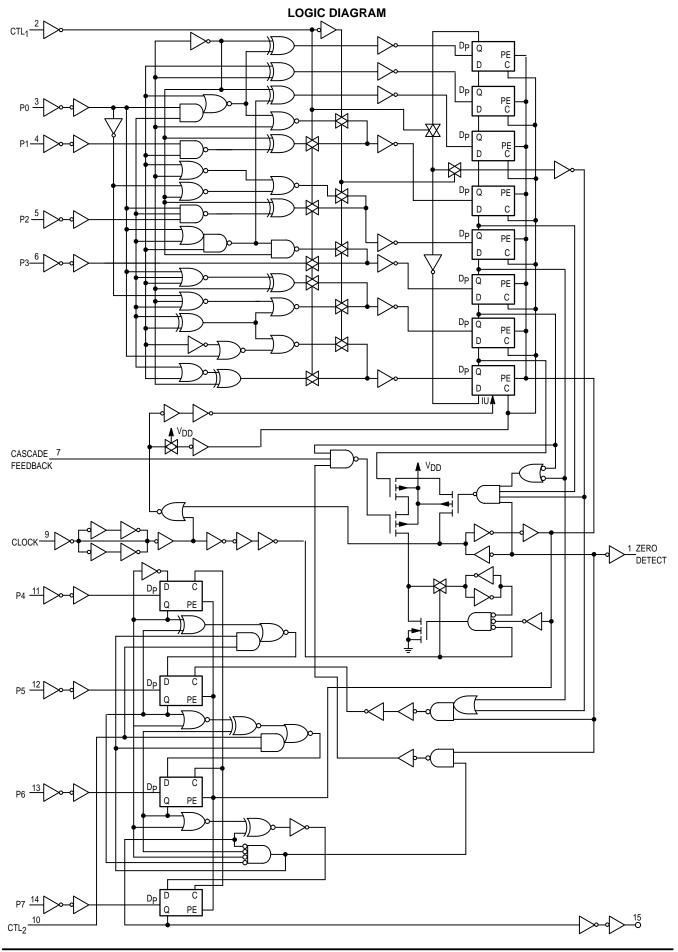
MC14569B

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## **TIMING DIAGRAM MC14569B**

				Values					Ratio	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	100	100	Max Count
0	0	0	0	0	0	0	1	Х	Х	illegal state
0	0	0	0	0	0	1	0	2	Х	Min Count
0	0	0	0	0	0	1	1	3	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•		•	Х	
0	0	0	0	1	0	0	1	9	Х	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X X	
•	•	•	•	•	•	•	•	• 30	X	
-		1					-		X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
• 0	•	•	•	•	•	•	•	• 40	X	
0		•		•	•	•		•	X	
								•	X	
					•	•		•	X	
0	1	0	1	0	0	0	0	50	X	
•		·		•	·	•	·	•	X	
	•	•			•	•		•	х	
	•	•			•	•		•	Х	
0	1	1	1	0	0	0	0	70	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
	•	•		•	•	•		•	•	
1	0	0	1	1	0	0	1	99	99	T
80	40	20	10	8	4	2	1			Bit Value
	Counter #2 Counter #1 BCD BCD									Counting Sequence



MOTOROLA CMOS LOGIC DATA

# **TYPICAL APPLICATIONS**

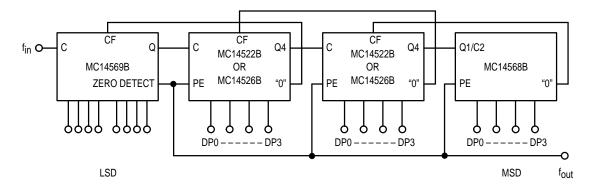


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B

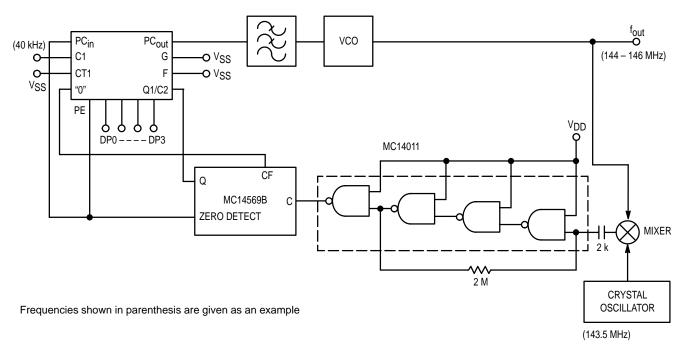
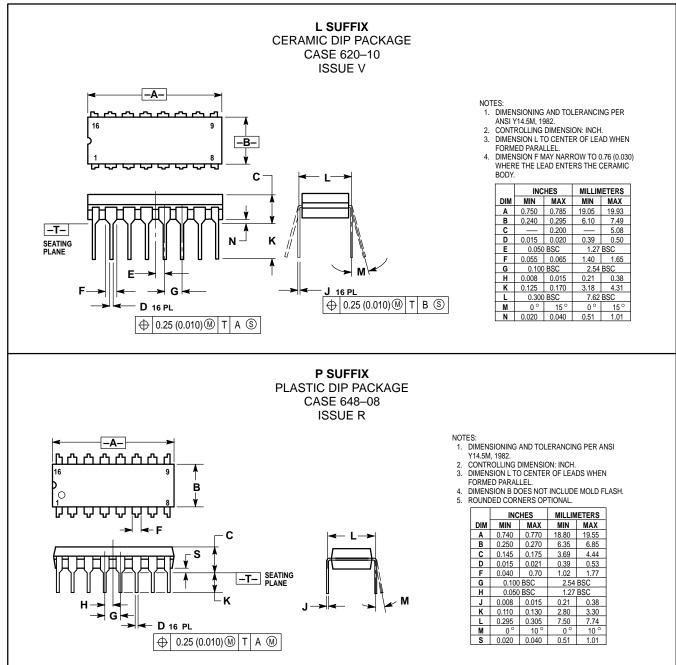


Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

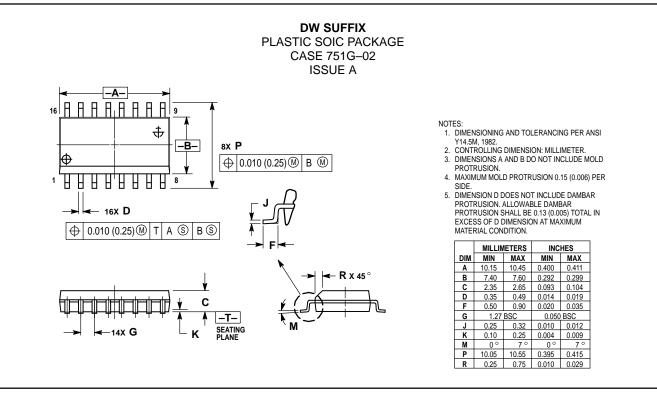
MC14569B

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## **OUTLINE DIMENSIONS**



## **OUTLINE DIMENSIONS**



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