

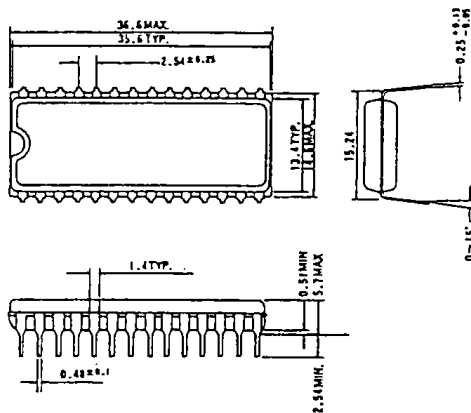
## SM5828B

8-bit Advanced Shift Register

variable-length 8-bit shift register fabricated using NPC's original molybdenum-gate technology. The external input pins of the IC allow 1 to 128-step shift register settings. The maximum frequency of 20 MHz ensures high-speed operation. When the shift register is not used, data is retained even when the shift clock is stopped.

### ■ PACKAGE DIMENSIONS (Unit: mm)

#### • Plastic (SM5828BP)

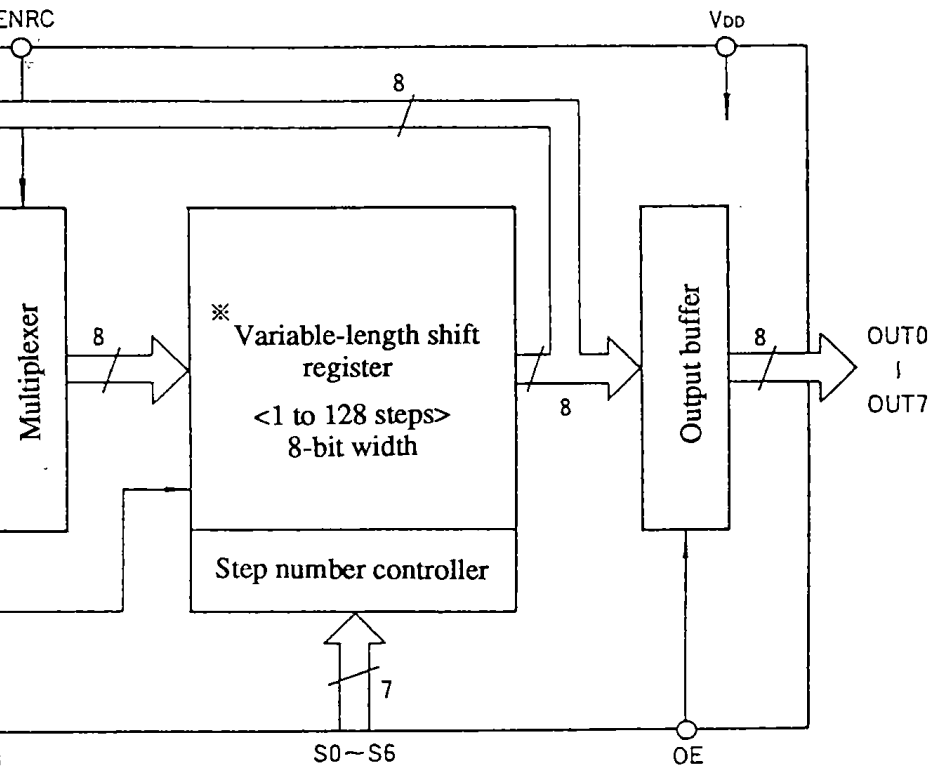


#### • Ceramic (SM5828BC)

|                    |
|--------------------|
| Package            |
| 28-pin plastic DIP |
| 28-pin ceramic DIP |

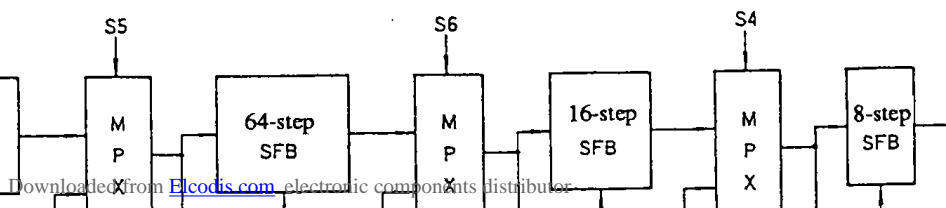
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AM



ation of the variable-length shift register

shows the configuration of the variable-length shift register. According to the S0~S6, the multiplexer selects the output of each shift register block, realizing 1 to 128-steps. The last 1-step register is always used.



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| Name            | Description                             |
|-----------------|---|
| N0              | Data input (0)                          |
| N1              | Data input (1)                          |
| N2              | Data input (2)                          |
| N3              | Data input (3)                          |
| N4              | Data input (4)                          |
| N5              | Data input (5)                          |
| N6              | Data input (6)                          |
| N7              | Data input (7)                          |
| S6              | Data length select (6)                  |
| S5              | Data length select (5)                  |
| S4              | Data length select (4)                  |
| S3              | Data length select (3)                  |
| CLK             | Clock input                             |
| V <sub>SS</sub> | Ground                                  |
| S2              | Register length select (2)              |
| S1              | Register length select (1)              |
| S0              | Register length select (0)              |
| OUT7            | Data output (7)                         |
| OUT6            | Data output (6)                         |
| OUT5            | Data output (5)                         |
| OUT4            | Data output (4)                         |
| OUT3            | Data output (3)                         |
| OUT2            | Data output (2)                         |
| OUT1            | Data output (1)                         |
| OUT0            | Data output (0)                         |
| OE              | Output enable                           |
| NRC             | Circulation and non-circulation control |
| V <sub>DD</sub> | Power supply (5 ± 0.5 V)                |

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**CHARACTERISTICS**

SM5828BP ... Ta = -20 to 70 °C, VDD = 4.5 to 5.5 V, Vss = 0 V  
 SM5828BC... Ta = -30 to 85 °C, VDD = 4.5 to 5.5 V, Vss = 0 V unless otherwise noted.)

| Pin | Symbol          | Condition                          | Rating |      |     | Unit | Remarks       |
|-----|-----------------|------------------------------------|--------|------|-----|------|---------------|
|     |                 |                                    | MIN    | TYP  | MAX |      |               |
| VDD | IST             | VDD = 5.5V                         |        | 0.01 | 100 | μA   |               |
| VDD | IDD             | Note                               |        |      | 100 | mA   | See Figure 2. |
| *1  | V <sub>IH</sub> |                                    | 2.4    |      |     | V    |               |
|     | V <sub>IL</sub> |                                    |        |      | 0.5 |      |               |
| *2  | V <sub>OH</sub> | I <sub>OH</sub> = -0.4mA           | 2.5    |      |     | V    |               |
|     | V <sub>OL</sub> | I <sub>OL</sub> = 1.6mA            |        |      | 0.4 |      |               |
| *1  | I <sub>IL</sub> | V <sub>IN</sub> = 0V               |        | 7    | 20  | μA   |               |
| *1  | I <sub>LH</sub> | V <sub>IN</sub> = V <sub>DD</sub>  |        |      | 1   | μA   |               |
| *2  | I <sub>ZH</sub> | V <sub>OUT</sub> = V <sub>DD</sub> |        |      | 5   | μA   |               |
|     | I <sub>ZL</sub> | V <sub>OUT</sub> = 0V              |        |      | 5   |      |               |

|                                     |
|-------------------------------------|
| ENRC, IN0 to IN7, S0 to S6, CLK, OE |
| OUT1 to OUT7                        |

clock frequency f<sub>CLK</sub> = 20 MHz, OE pin = 0 V  
 clock input voltage V<sub>IH</sub> = 2.4 V, V<sub>IL</sub> = 0.5 V

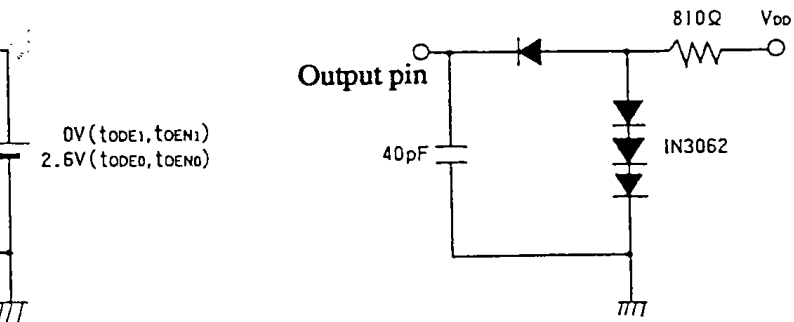
**CHARACTERISTICS**

(VDD = 4.5 to 5.5 V, Vss = 0 V unless otherwise noted)

| Pin     | Symbol           | Condition  | BP type (-20 to 70°C) |     |     | BC type (-30 to 70°C) |     |     | Unit | Remarks  |
|---------|------------------|--|-----------------------|-----|-----|-----------------------|-----|-----|------|----------|
|         |                  |  | BC type (-20 to 85°C) |     |     |                       |     |     |      |          |
|         |                  |  | MIN                   | TYP | MAX | MIN                   | TYP | MAX |      |          |
| CLK     | f <sub>CLK</sub> | V <sub>IH</sub> = 2.4V, V <sub>IL</sub> = 0.5V           |                       |     | 20  |                       |     | 20  | MHz  |          |
| CLK     | t <sub>cr</sub>  |  |                       |     | 100 |                       |     | 100 | nsec |          |
| CLK     | t <sub>cf</sub>  |  |                       |     | 100 |                       |     | 100 | nsec |          |
| CLK     | t <sub>WH</sub>  |  | 20                    |     |     | 20                    |     |     | nsec |          |
| IO to 7 | t <sub>s1</sub>  | Register length: LR<br>= 16 steps<br>Register length: LR | 60                    |     |     | 55                    |     |     | nsec | Figure 1 |

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(Note 2) Load condition 2



SETTING

steps by using the register length select pins S0 to S6.

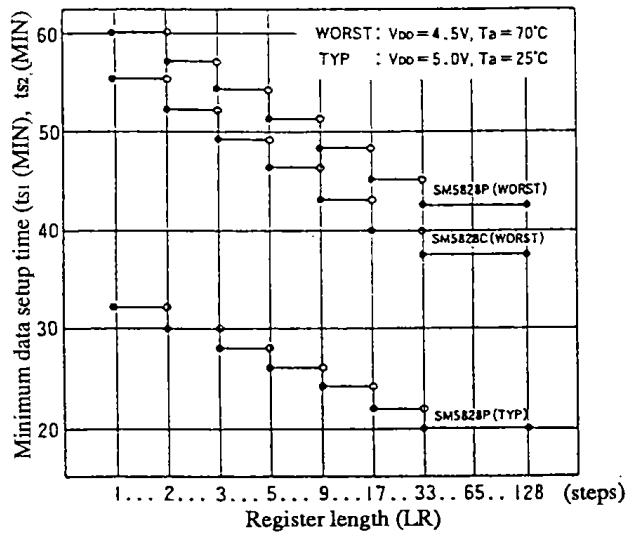
$$S4)+8(S3)+4(S2)+2(S1)+(S0)+1$$

| S4 | S3 | S2 | S1 | S0 |
|----|----|----|----|----|
| 1  | 1  | 1  | 1  | 1  |
| 1  | 1  | 1  | 1  | 0  |
| 1  | 1  | 1  | 0  | 1  |
| 1  | 1  | 1  | 0  | 0  |
| .  | .  | .  | .  | .  |
| 0  | 0  | 0  | 0  | 1  |
| 0  | 0  | 0  | 0  | 0  |
| .  | .  | .  | .  | .  |
| 0  | 0  | 0  | 1  | 0  |
| 0  | 0  | 0  | 0  | 1  |
| 0  | 0  | 0  | 0  | 0  |

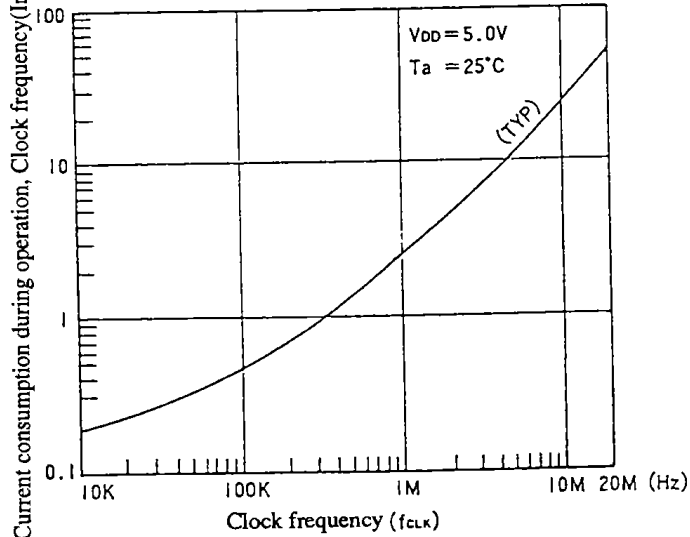
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CHARACTERISTICS

⊙  $t_{s1}, t_{s2}$  (MIN) - - LR characteristic (Figure 1)



⊙ -  $I_{DD-fCLK}$  characteristic (Figure 2)



⊙ -  $I_{DD-fCLK}$  vs  $T_a$  characteristic (Figure 3)

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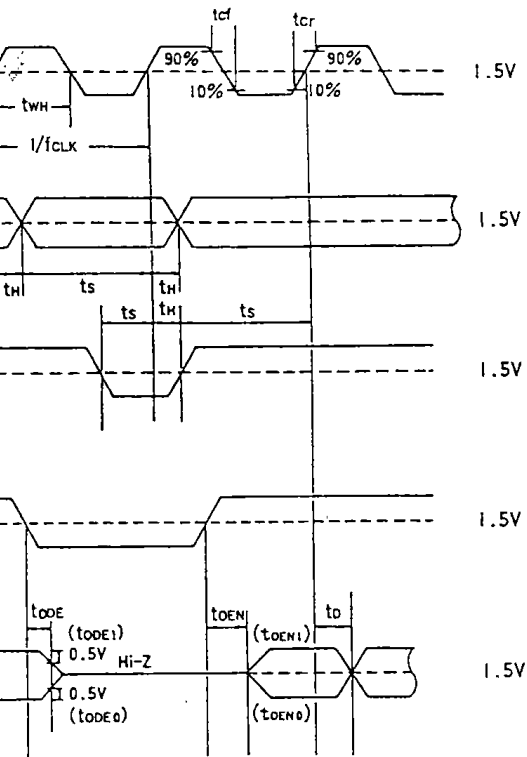


FIGURE 10. Block diagram of a 16-bit FIR digital filter using the SM5828B

