TDA9962

12-bit, 3.0 V, 30 Msps analog-to-digital interface for CCD cameras

Rev. 03 — 12 September 2002 **Preliminary data**

1. Description

The TDA9962 is a 12-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, PGA, clamp loops and a low-power 12-bit ADC together with its reference voltage regulator.

An internal CDS input buffer is incorporated in order to avoid using an external buffer that would consume more power and therefore optimizing the application for low noise, low power working.

The PGA gain and the ADC input clamp level are controlled via the serial interface.

An additional DAC is provided for additional system controls; its output voltage range is 1.0 V (p-p) which is available at pin OFDOUT.

2. Features

- Internal CDS input buffer, Correlated Double Sampling (CDS), Programmable Gain Amplifier (PGA), 12-bit Analog-to-Digital Converter (ADC) and reference regulator included
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 30 MHz
- PGA gain range of 36 dB (in steps of 0.1 dB)
- Low power consumption of only 115 mW at 2.7 V
- Power consumption in standby mode of 4.5 mW (typ.)
- 3.0 V operation and 2.2 to 3.6 V operation for the digital outputs
- All digital inputs accept 5 V signals
- Active control pulses polarity selectable via serial interface
- 8-bit DAC included for analog settings
- TTL compatible inputs, CMOS compatible outputs.

3. Applications

- Low-power, low-voltage CCD camera systems.

PHILIPS

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	digital outputs supply voltage		2.2	2.5	3.6	V
I_{CCA}	analog supply current	all clamps active	–	41	–	mA
I_{CCD}	digital supply current		–	2.0	–	mA
I_{CCO}	digital outputs supply current	f_{pix} = 30 MHz; C_L = 10 pF; input ramp of 800 µs duration	–	0.5	–	mA
ADC_{res}	ADC resolution		–	12	–	bits
$V_{i(CDS)(p-p)}$	maximum CDS input voltage (peak-to-peak value)	V_{CC} = 2.85 V	650	–	–	mV
		$V_{CC} \geq$ 3.0 V	800	–	–	mV
$f_{pix(max)}$	maximum pixel rate		25	–	–	MHz
$f_{pix(min)}$	minimum pixel rate	$O_{CCD(max)}$ = ±100 mV	–	–	1	MHz
		$O_{CCD(max)}$ = ±200 mV	–	–	2	MHz
DR_{PGA}	PGA dynamic range		–	24	–	dB
$N_{tot(rms)}$	total noise from CDS input to ADC output	PGA code = 00; see Figure 8	–	1.4	–	LSB
$E_{in(rms)}$	equivalent input noise (RMS value)	PGA code = 255	–	125	–	µV
P_{tot}	total power consumption	$V_{CCA} = V_{CCD}$ = 3 V; V_{CCO} = 2.5 V	–	130	–	mW
		$V_{CCA} = V_{CCD}$ = 2.7 V; V_{CCO} = 2.2 V	–	115	–	mW

5. Ordering information

Table 2: Ordering information

Type number	Package			
	Name	Description	Version	Pixel frequency
TDA9962HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2	30 MHz

6. Block diagram

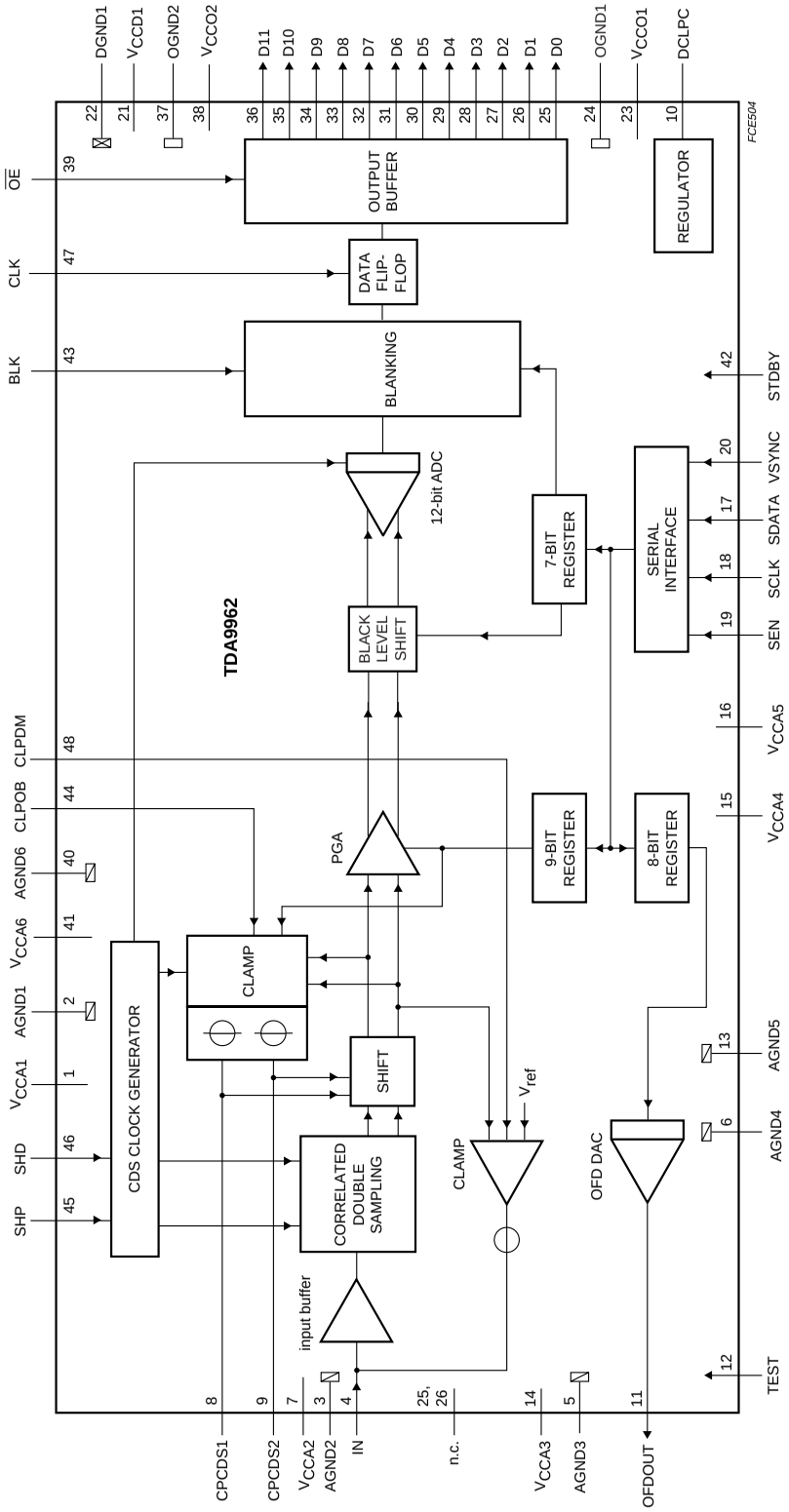


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

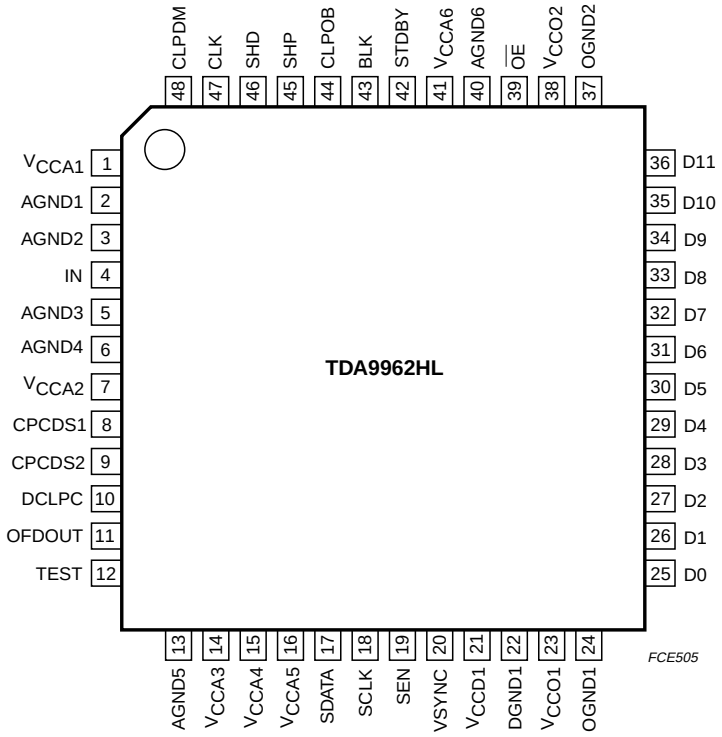


Fig 2. Pin configuration.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
V_{CCA1}	1	analog supply voltage 1
AGND1	2	analog ground 1
AGND2	3	analog ground 2
IN	4	input signal from CCD
AGND3	5	analog ground 3
AGND4	6	analog ground 4
V_{CCA2}	7	analog supply voltage 2
CPCDS1	8	clamp storage capacitor pin 1
CPCDS2	9	clamp storage capacitor pin 2
DCLPC	10	regulator decoupling pin
OFDOUT	11	analog output of the additional 8-bit control DAC
TEST	12	test mode input pin (should be connected to AGND5)
AGND5	13	analog ground 5
V_{CCA3}	14	analog supply voltage 3

Table 3: Pin description *...continued*

Symbol	Pin	Description
V_{CCA4}	15	analog supply voltage 4
V_{CCA5}	16	analog supply voltage 5
SDATA	17	serial data input for serial interface control
SCLK	18	serial clock input for serial interface
SEN	19	strobe pin for serial interface
VSYNC	20	vertical sync pulse input
V_{CCD1}	21	digital supply voltage 1
DGND1	22	digital ground 1
V_{CCO1}	23	digital outputs supply voltage 1
OGND1	24	digital output ground 1
D0	25	ADC digital output 0 (LSB)
D1	26	ADC digital output 1
D2	27	ADC digital output 2
D3	28	ADC digital output 3
D4	29	ADC digital output 4
D5	30	ADC digital output 5
D6	31	ADC digital output 6
D7	32	ADC digital output 7
D8	33	ADC digital output 8
D9	34	ADC digital output 9
D10	35	ADC digital output 10
D11	36	ADC digital output 11 (MSB)
OGND2	37	digital output ground 2
V_{CCO2}	38	digital outputs supply voltage 2
$\overline{OE}$	39	output enable control input (LOW = outputs active; HIGH = outputs in high-impedance)
AGND6	40	analog ground 6
V_{CCA6}	41	analog supply voltage 4
STDBY	42	standby mode control input (LOW = TDA9962 active; HIGH = TDA9962 standby)
BLK	43	blanking control input
CLPOB	44	clamp pulse input at optical black
SHP	45	preset sample-and-hold pulse input
SHD	46	data sample-and-hold pulse input
CLK	47	data clock input
CLPDM	48	clamp pulse input at dummy pixel

8. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage		[1]	–0.3	+4.5	V
V_{CCD}	digital supply voltage		[1]	–0.3	+4.5	V
V_{CCO}	digital outputs supply voltage		[1]	–0.3	+4.5	V
ΔV_{CC}	supply voltage difference					
	between V_{CCA} and V_{CCD}			–0.5	+0.5	V
	between V_{CCA} and V_{CCO}			–0.5	+1.2	V
	between V_{CCD} and V_{CCO}			–0.5	+1.2	V
V_i	input voltage	referenced to AGND		–0.3	+6.5	V
I_o	data output current			–	±10	mA
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–20	+75	°C
T_j	junction temperature			–	+150	°C

[1] All supplies are connected together.

9. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	76	K/W

10. Characteristics

Table 6: Characteristics

V_{CCA} = V_{CCD} = 3.0 V; V_{CCO} = 2.5 V; f_{pix} = 30 MHz; T_{amb} = −20 to +75 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	digital outputs supply voltage		2.2	2.5	3.6	V
I_{CCA}	analog supply current	all clamps active	–	41	–	mA
I_{CCD}	digital supply current		–	2.0	–	mA
I_{CCO}	digital outputs supply current	C_L = 10 pF on all data outputs; input ramp of 800 µs duration	–	0.5	–	mA
Digital inputs						
Pins SHP, SHD and CLK (referenced to DGND)						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
I_i	input current	$0 \leq V_i \leq 5.5$ V	–3	–	+3	µA
C_i	input capacitance		–	–	2	pF
Pins CLPDM, CLPOB, SEN, SCLK, SDATA, STBY, $\overline{OE}$, BLK and VSYNC						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
I_i	input current	$0 \leq V_i \leq 5.5$ V	–2	–	+2	µA
Clamps						
Global characteristics of the clamp loops						
$t_{W(clamp)}$	clamp active pulse width in number of pixels	PGA code = 255 for maximum 8 LSB error; C_{CPCDS} = 1 µF	15	–	–	pixels
Input clamp (driven by CLPDM)						
$g_{m(CDS)}$	CDS input clamp transconductance		–	15	–	mS
Correlated Double Sampling (CDS)						
$V_{i(CDS)(p-p)}$	maximum peak-to-peak CDS input amplitude (video signal)	V_{CC} = 2.85 V	650	–	–	mV
		$V_{CC} \geq$ 3.0 V	800	–	–	mV
$V_{reset(max)}$	maximum CDS input reset pulse amplitude		–	–	1.5	V
$I_{i(IN)}$	input current into pin IN	at floating gate level	–	–	3	µA
C_i	input capacitance		–	2	–	pF
$t_{CDS(min)}$	CDS control pulses minimum active time	$V_{i(CDS)(p-p)}$ = 800 mV black-to-white transition in 1 pixel with 98.5% V_i recovery	11	–	–	ns

Table 6: Characteristics *...continued*

V_{CCA} = V_{CCD} = 3.0 V; V_{CCO} = 2.5 V; f_{pix} = 30 MHz; T_{amb} = −20 to +75 °C; unless otherwise specified.

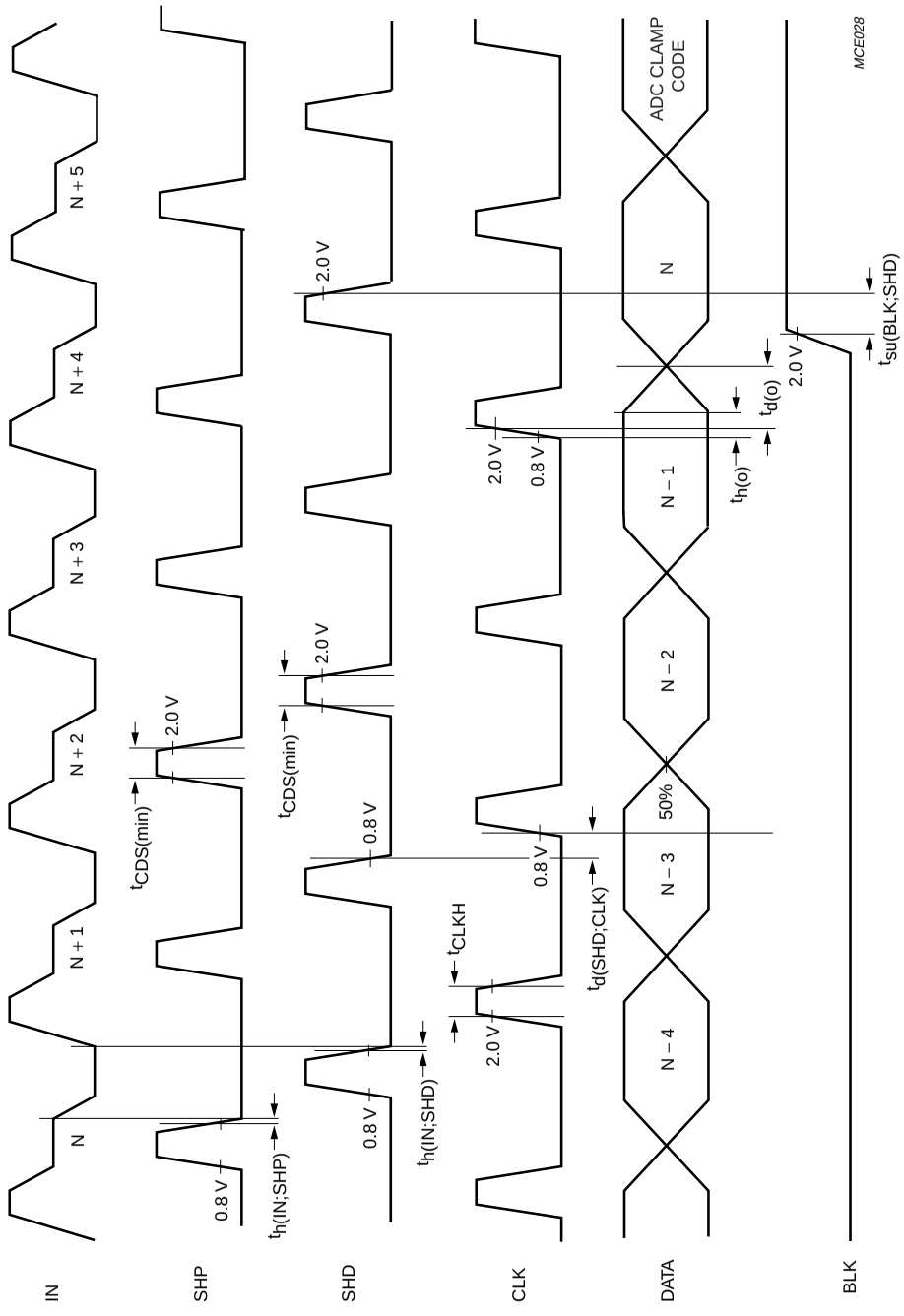
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(IN;SHP)}$	CDS input hold time (pin IN) compared to control pulse SHP	see Figure 3 and 4	3	–	–	ns
$t_{h(IN;SHD)}$	CDS input hold time (pin IN) compared to control pulse SHD	see Figure 3 and 4	3	–	–	ns
Amplifier						
DR_{PGA}	PGA dynamic range	see Figure 7 and Table 7	–	24	–	dB
ΔG_{PGA}	PGA gain step		0.08	0.10	0.12	dB
Analog-to-Digital Converter (ADC)						
DNL	differential non linearity	f_{pix} = 30 MHz; ramp input	–	±0.5	±0.9	LSB
Total chain characteristics (CDS + PGA + ADC)						
$f_{pix(max)}$	maximum pixel frequency		30	–	–	MHz
$f_{pix(min)}$	minimum pixel rate	$O_{CCD(max)}$ = ±100 mV	–	–	1	MHz
		$O_{CCD(max)}$ = ±200 mV	–	–	2	MHz
t_{CLKH}	CLK pulse width HIGH		15	–	–	ns
t_{CLKL}	CLK pulse width LOW		15	–	–	ns
$t_{d(SHD;CLK)}$	time delay between SHD and CLK	see Figure 3 and 4	–	10	–	ns
$t_{su(BLK;SHD)}$	set-up time of BLK compared to SHD	see Figure 3 and 4	5	–	–	ns
$V_{i(IN)(FS)}$	video input dynamic signal for ADC full-scale output	PGA code = 00	–	800	–	mV
		PGA code = 255	–	50	–	mV
$N_{tot(rms)}$	total noise from CDS input to ADC output (RMS value)	see Figure 8 [1]				
		PGA code = 00	–	1.4	–	LSB
		PGA code = 96	–	2.3	–	LSB
$E_{in(rms)}$	equivalent input noise voltage (RMS value)	PGA code = 255	–	125	–	μV
		PGA code = 96	–	150	–	μV
$O_{CCD(max)}$	maximum offset between CCD floating level and CCD dark pixel level		–200	–	+200	mV
Digital-to-analog converter (OFDOUT DAC)						
$V_{OFDOUT(p-p)}$	additional 8-bit control DAC (OFD) output voltage (peak-to-peak value)	R_i = 1 MΩ	–	1.0	–	V
$V_{OFDOUT(0)}$	DC output voltage for code 0		–	AGND	–	V
$V_{OFDOUT(255)}$	DC output voltage for code 255		–	AGND + 1.0	–	V
TC_{DAC}	DAC output range temperature coefficient		–	250	–	ppm/°C
Z_{OFDOUT}	DAC output impedance		–	2000	–	Ω
I_{OFDOUT}	DAC output current drive	static	–	–	100	μA

Table 6: Characteristics *...continued*

V_{CCA} = V_{CCD} = 3.0 V; V_{CCO} = 2.5 V; f_{pix} = 30 MHz; T_{amb} = −20 to +75 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital outputs (f_{pix} = 30 MHz; C_L = 10 pF); see Figure 3 and 4						
V_{OH}	HIGH-level output voltage	I_{OH} = −1 mA	V_{CCO} − 0.5	–	V_{CCO}	V
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.5	V
I_{OZ}	output current in 3-state mode	0.5 V < V_o < V_{CCO}	−20	–	+20	µA
$t_{h(o)}$	output hold time		5	–	–	ns
$t_{d(o)}$	output delay time	C_L = 10 pF; V_{CCO} = 3.6 V; V_{CCD} = 3.6 V	–	10	13	ns
		C_L = 10 pF; V_{CCO} = 2.5 V; V_{CCD} = 3 V	–	12	15	ns
		C_L = 10 pF; V_{CCO} = 2.2 V; V_{CCD} = 2.7 V	–	13	16	ns
C_L	output load capacitance		–	–	20	pF
Serial interface						
$f_{SCLK(max)}$	maximum frequency of serial clock interface		10	–	–	MHz

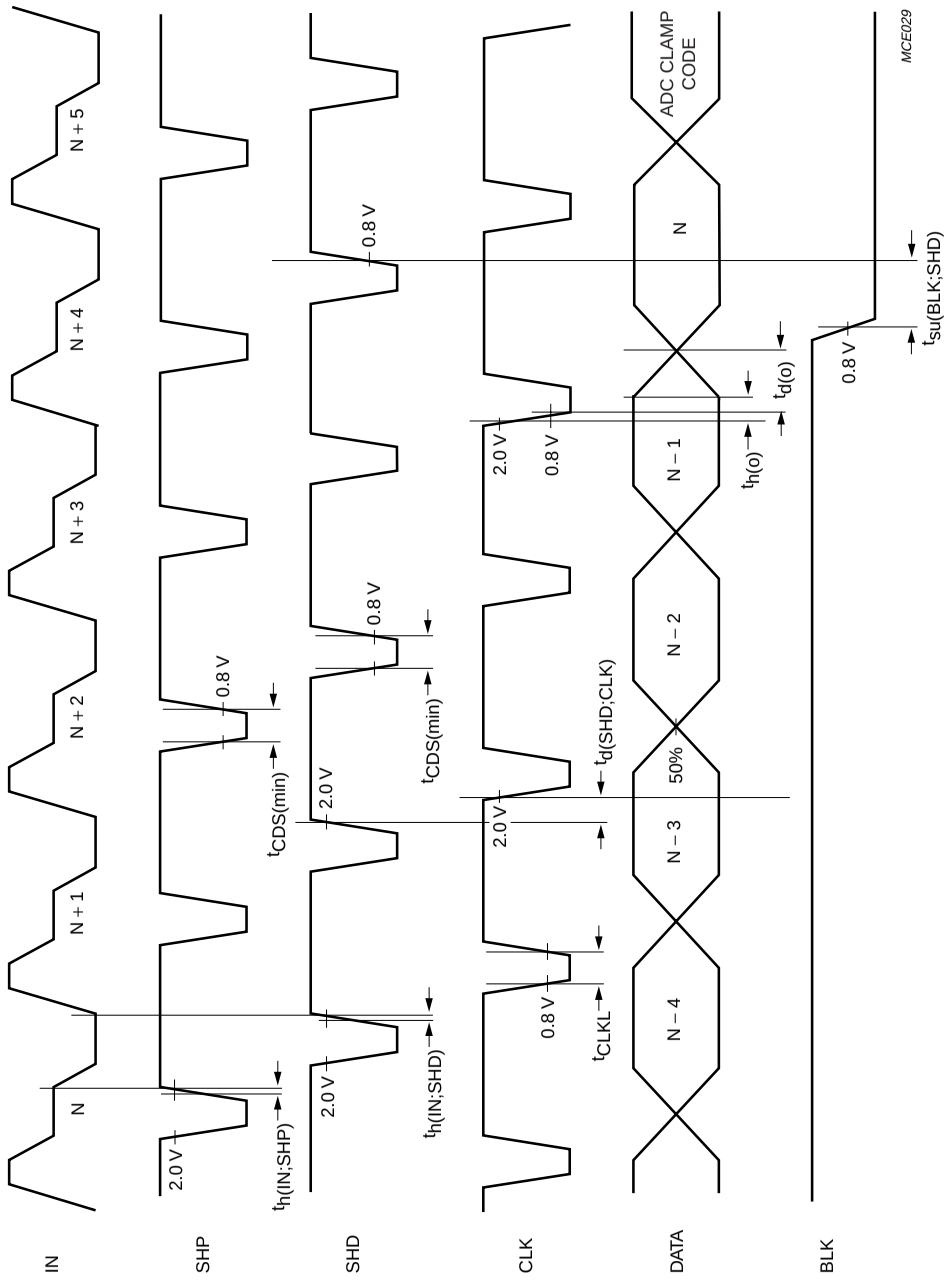
[1] Noise figure includes the internal input buffer circuit.



SHP and SHD should be aligned at optimum with the CCD signal. Samples are taken at the falling edge.

Recommended placement for CLK rising edge is between the falling edge of SHD and the rising edge of SHP.

Fig 3. Pixel frequency timing diagram; all polarities active HIGH.



SHP and SHD should be aligned at optimum with the CCD signal. Samples are taken at the rising edge.
Recommended placement for CLK falling edge is between the rising edge of SHD and the falling edge of SHP.

Fig 4. Pixel frequency timing diagram; all polarities active LOW.

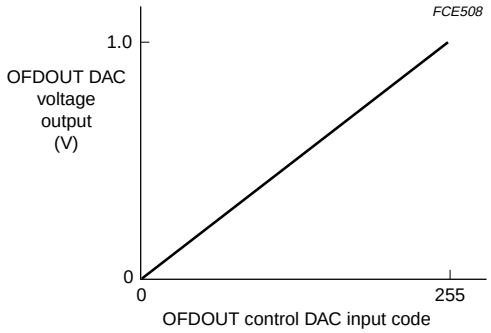


Fig 5. DAC voltage output as a function of DAC input code.

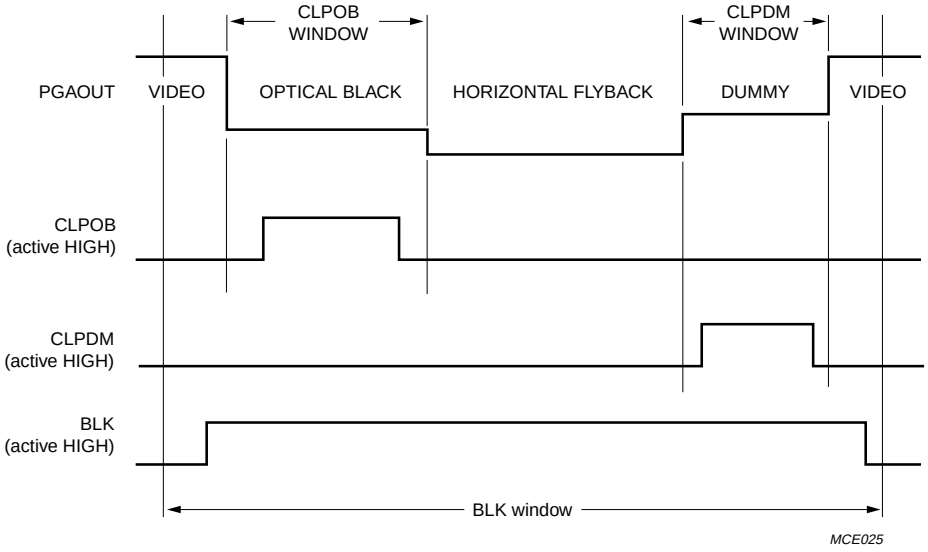
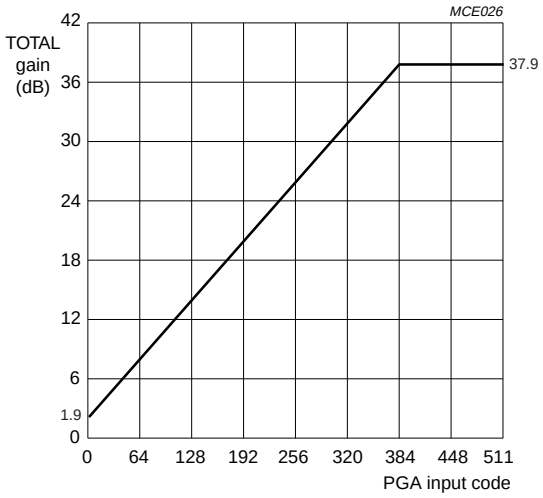


Fig 6. Line frequency timing diagram.

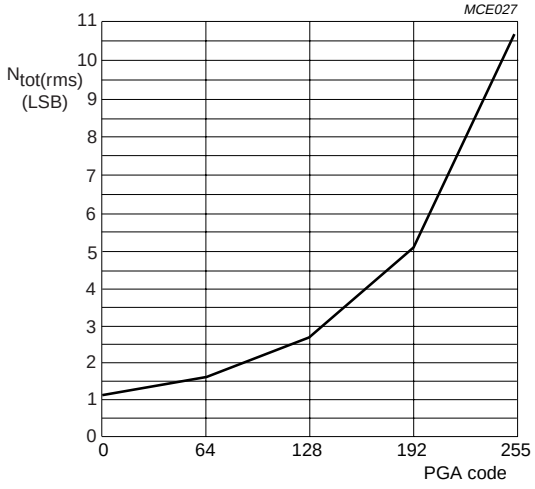


$$Gain(dB) = 1.9 + 36 \times \left(\frac{PGAcode}{383}\right)[dB]$$

Full-scale at the ADC input is reached at $V_{i(CDS)(p\text{-}p)}$ = 800 mV; PGA code 0.

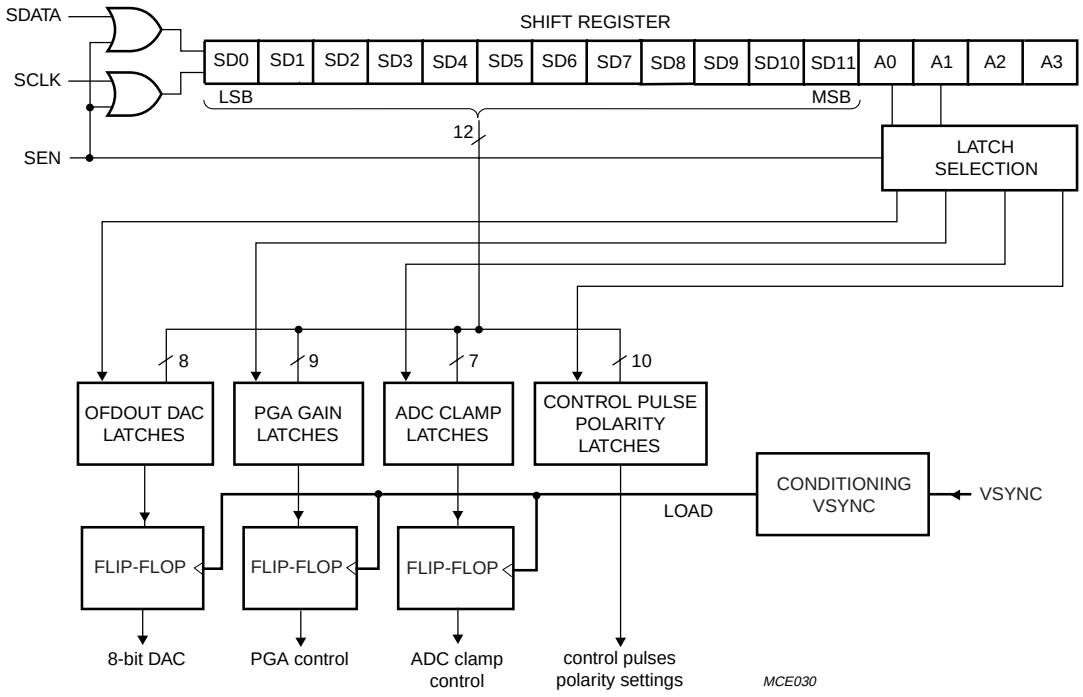
To use 36 dB gain range refer to Table 7, address 0100.

Fig 7. Total gain from CDS input to ADC input as a function of PGA control code.



Noise measurement at ADC outputs: Coupling capacitor at input is grounded, so only noise contribution of the front-end is evaluated. Front-end works at 30 Mpixels with line of 1024 pixels whose first 40 are used to run CLPOB and the last 40 for CLPDM. Data at the ADC outputs are measured during the other pixels. As a result of this, the standard deviation of the codes statistic is computed, resulting in the noise. No quantization noise is taken into account.

Fig 8. Typical total noise performance as a function of PGA gain.

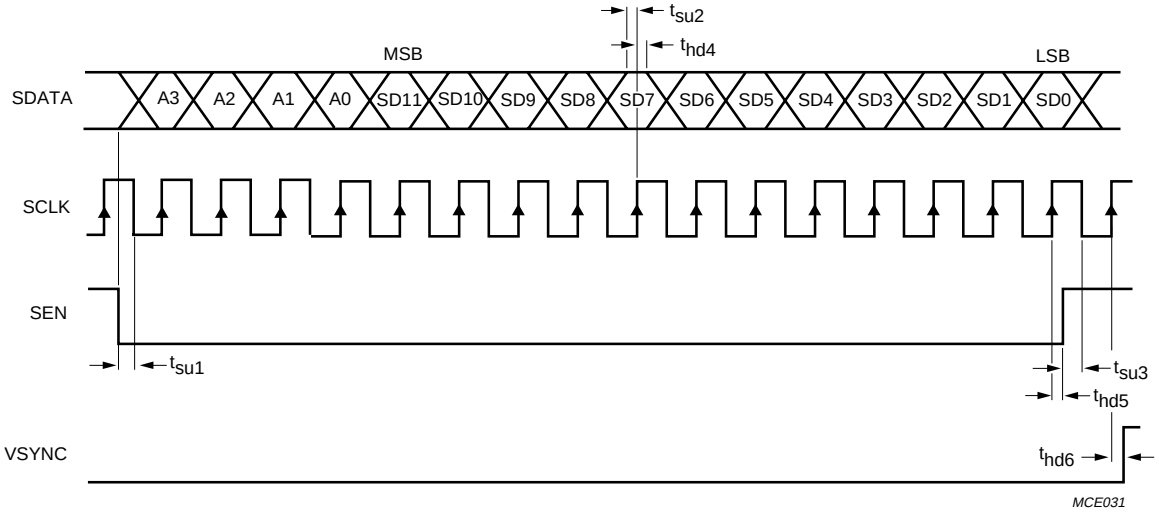


First logic layer (DFF) is clocked by the first falling SCLK edge after the rising SEN edge.

Second logic layer is clocked by the LOAD signal; this signal depends on the VSYNC signal.

If vertical sync is not available, VSYNC should be connected to SEN.

Fig 9. Serial interface block diagram.



$t_{su1} = t_{su2} = t_{su3} = 10$ ns (min.); $t_{hd4} = t_{hd5} = t_{hd6}$ 10 ns (min.).

Fig 10. Loading sequence of control input data via the serial interface.

Table 7: Serial interface programming

Address bits				Data bits SD11 to SD0
A3	A2	A1	A0	
0	0	0	0	PGA gain control (SD7 to SD0)
0	0	0	1	DAC OFDOUT output control (SD7 to SD0)
0	0	1	0	ADC clamp reference control (SD6 to SD0); from code 0 to 127
0	0	1	1	control pulses (pins SHP, SHD, CLPDM, CLPOB, BLK and CLK) polarity settings; SD2, SD6, SD7 and SD9 should be set to logic 1; for SD6 and SD7 see Table 9 and 10
0	1	0	0	SD7 = 0 by default; SD7 = 1 for 36 dB PGA gain range but noise and clamp behaviour are not guaranteed
other addresses				test modes (do not use in normal application)

Table 8: Polarity settings

Symbol	Pin	Serial control bit	Active edge or level
SHP and SHD	45 and 46	SD4	1 = HIGH; 0 = LOW
CLK	47	SD5	1 = rising; 0 = falling
CLPDM	48	SD0	1 = HIGH; 0 = LOW
CLPOB	44	SD1	1 = HIGH; 0 = LOW
BLK	43	SD3	1 = HIGH; 0 = LOW
VSYNC	20	SD8	0 = rising; 1 = falling

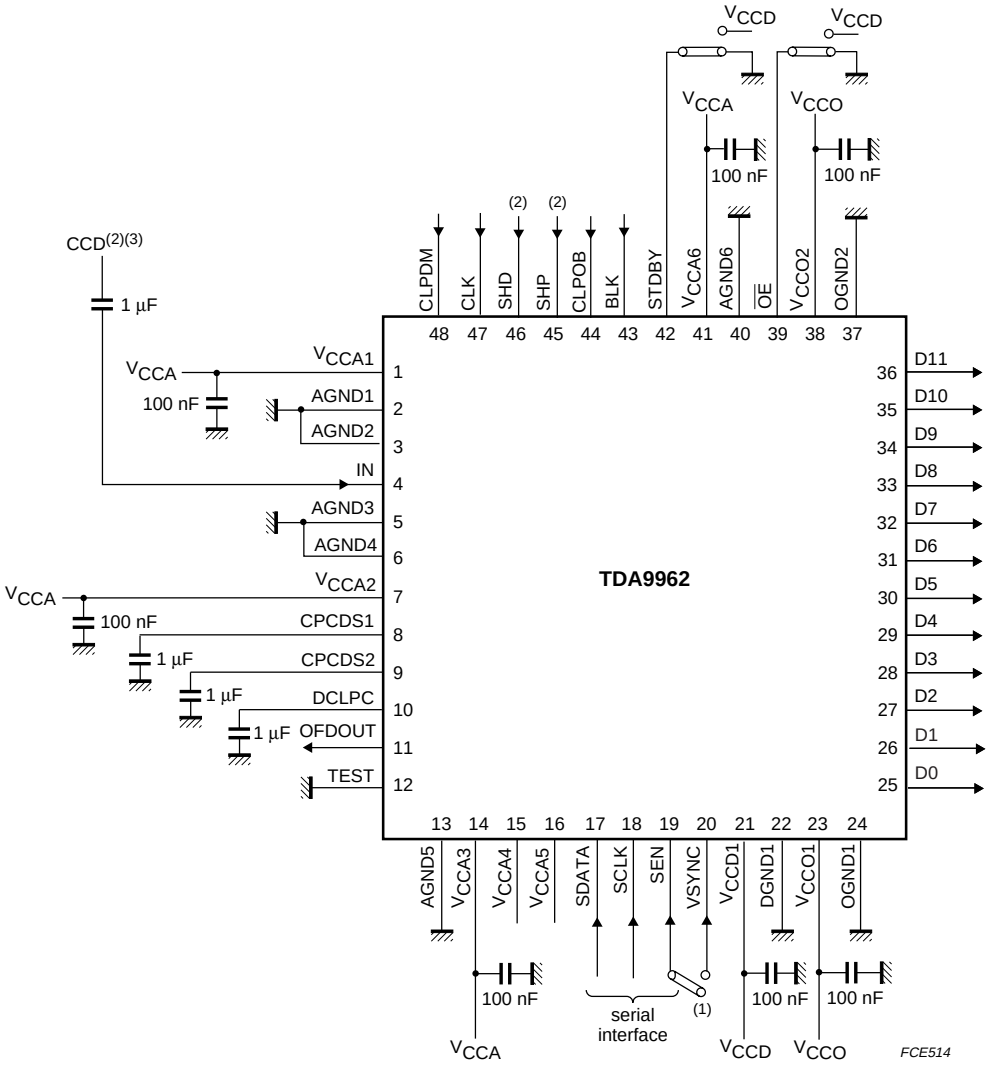
Table 9: Standby control using pin STDBY

Bit SD7 of register 0011	STDBY	ADC digital outputs SD11 to SD0	$I_{CCA} + I_{CCD}$ (typ.)
1	1	last logic state	1.5 mA
	0	active	43 mA
0	1	active	43 mA
	0	test logic state	1.5 mA

Table 10: Output enable selection using output enable pin ($\overline{OE}$)

Bit SD6 of register 0011	$\overline{OE}$	ADC digital outputs SD9 to SD0
1	0	active binary
	1	high-impedance
0	0	high-impedance
	1	active binary

11. Application information

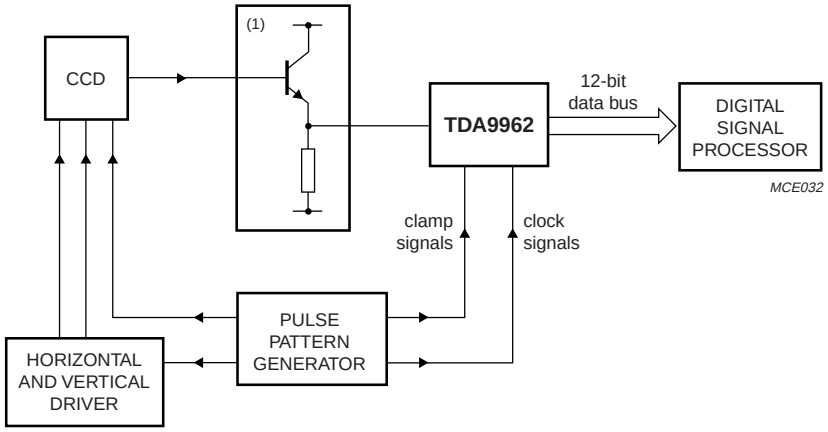


(1) Pins SEN and VSYNC should be interconnected when vertical sync signal is not available.

(2) Input signals IN, SHD and SHP must be adjusted to comply with timing signals $t_{h(IN;SHP)}$ and $t_{h(IN;SHD)}$ (see Section 10 "Characteristics").

(3) As an internal buffer is incorporated, depending on the CCD output impedance, an external input buffer may not be necessary and consequently power savings can be made.

Fig 11. Application diagram.



(1) The external input buffer can be omitted for CCDs with low output impedance, for CCDs with high output impedance, a small current (around 1 mA) is needed.

Fig 12. Typical imaging application.

11.1 Power and grounding recommendations

Care should be taken to minimize the noise when designing a printed-circuit board for applications such as PC cameras, surveillance cameras, camcorders and digital still cameras.

For the front-end integrated circuit, the basic rules of printed-circuit board design and implementation of analog components (such as classical operational amplifiers) must be taken into account, particularly with respect to power and ground connections.

The connections between the CCD interface and the CDS input should be as short as possible and a ground ring protection around these connections can be beneficial.

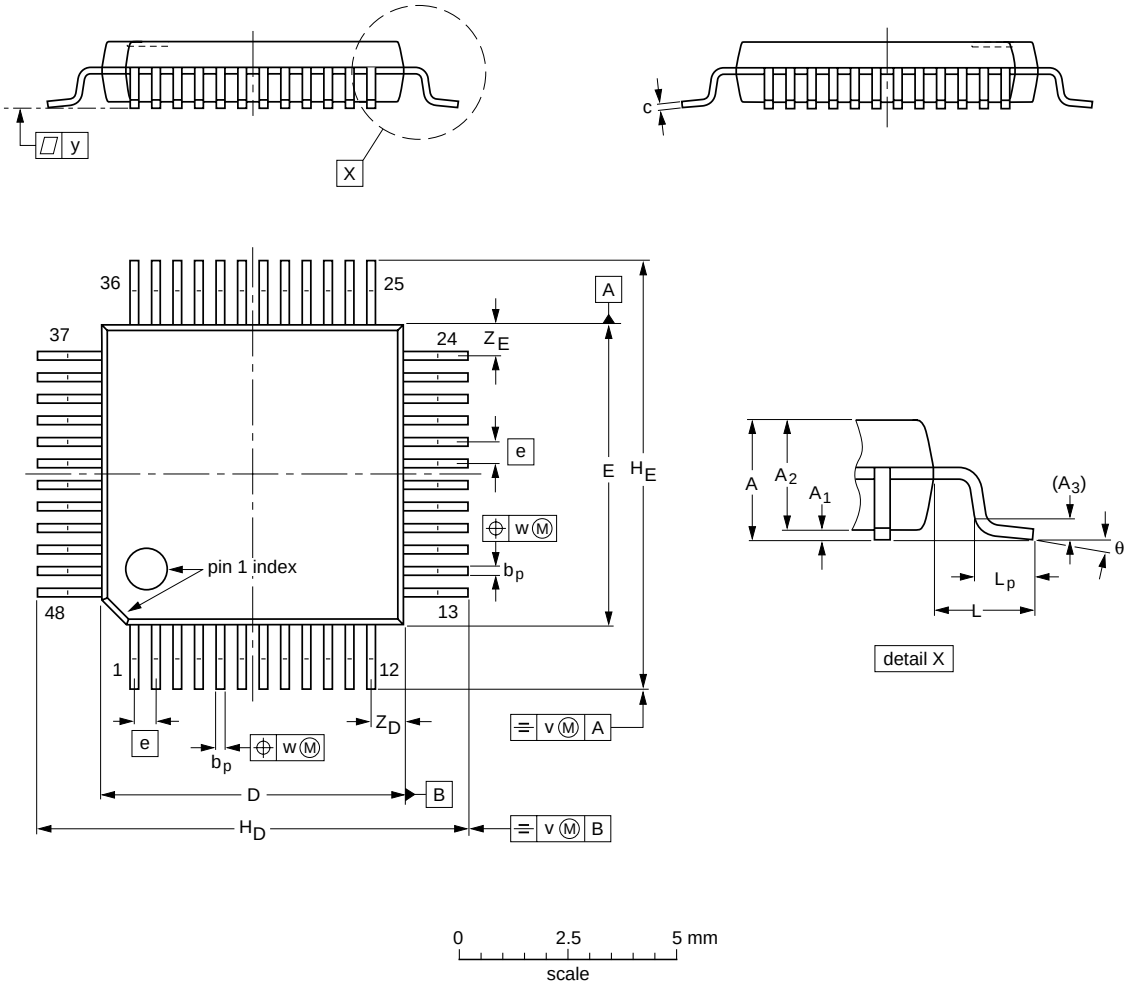
Separate analog and digital supplies provide the best performance. If it is not possible to do this on the board then the analog supply pins must be decoupled effectively from the digital supply pins. The decoupling capacitors must be placed as close as possible to the IC package.

In a two-ground system, in order to minimize the noise through package and die parasitics, the following recommendation must be implemented.

- The ground pin associated with the digital outputs must be connected to the digital ground plane and special care should be taken to avoid feedthrough in the analog ground plane. The analog and digital ground planes must be connected together with an inductor as closely as possible to the IC in order for them to have the same DC voltage.
- The digital output pins and their associated lines should be shielded by the digital ground plane which can then be used as a return path for digital signals.

12. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

Fig 13. SOT313-2.

13. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Package related soldering information

Table 11: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15. Revision history

Table 12: Revision history

Rev	Date	CPCN	Description
03	20020912	-	Preliminary specification; third version
02	20000804	-	Objective specification; second version
01	20000501	-	Objective specification; initial version

16. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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