TOSHIBA TC7W125FU

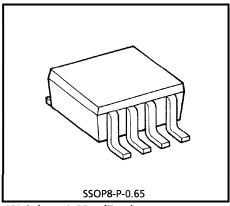
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T C 7 W 1 2 5 F U

DUAL BUS BUFFER

The TC7W125FU is a high speed C²MOS DUAL BUS BUFFERS fabricated with silicon gate C²MOS technology. It achieve the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation.

The require 3-state control input \overline{G} to be set high to place the output into the high impedance. All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight: 0.02g (Typ.)

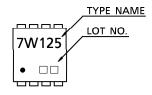
FEATURES

- High Speed $\cdots t_{pd} = 10$ ns (Typ.) at $V_{CC} = 5V$
- Low Power Dissipation $\cdots I_{CC} = 2\mu A$ (Max.) at $Ta = 25^{\circ}C$
- High Noise Immunity·········· V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- Output Drive Capability 15 LSTTL Loads
- Symmetrical Output Impedance $\cdots \cdot |I_{OH}| = I_{OL} = 6mA$ (Min.)
- Balanced Propagation Delays ······· t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ······ V_{CC} (opr) = 2~6V

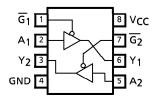
MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	Vcc	- 0.5~7	V
DC Input Voltage	VIN	-0.5~V _{CC} +0.5	V
DC Output Voltage	Vout	-0.5~V _{CC} +0.5	V
Input Diode Current	ΙΚ	± 20	mA
Output Diode Current	loк	± 20	mA
DC Output Current	IOUT	± 35	mA
DC V _{CC} /Ground Current	lcc	± 37.5	mΑ
Power Dissipation	PD	300	mW
Storage Temperature	T _{stg}	-65∼150	°C
Lead Temperature (10s)	TL	260	°C

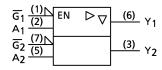
MARKING



PIN ASSIGNMENT (TOP VIEW)



LOGIC DIAGRAM



TRUTH TABLE

INP	UTS	OUTPUTS
G	Α	Υ
Н	Х	Z
┙	L	L
L	Н	Н

X : Don't Care Z : High Impedance

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	Vcc	2~6	V
Input Voltage	VIN	0~V _{CC}	<
Output Voltage	Vout	0~V _{CC}	\
Operating Temperature	T _{opr}	-40∼85	Ĵ
		$0\sim1000 \ (V_{CC}=2.0V)$	
Input Rise and Fall Time	t _r , t _f	$0 \sim 500 \ (V_{CC} = 4.5V)$	ns
		$0 \sim 400 \ (V_{CC} = 6.0V)$	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CIR-	TEST CONDITION r			Ta = 25°C			Ta = − 40~85°C		UNIT
	CUIT	TEST CONDITION		Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT	
High-Level Input				_		1.5	_	_	1.5	_	
Voltage	VIH	—				3.15	_	—	3.15	—	V
					6.0	4.2			4.2		
Low-Level Input			_		2.0	—	_	0.5	_	0.5	
Voltage	V _{IL}	—			4.5	—		1.35	-	1.35	V
					6.0	_	_	1.8		1.8	
	Voн		V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0	1.9	2.0	—	1.9		
High-Level					4.5	4.4	4.5	—	4.4	—	V
Output Voltage		_			6.0	5.9	6.0		5.9		
				$I_{OH} = -6mA$	4.5	4.18	4.31	—	4.13		
				$I_{OH} = -7.8 \text{mA}$	6.0	5.68	5.80		5.63	_	
	VOL		V _{IN} = V _{IL}	I _{OL} = 20μA	2.0	—	0.0	0.1	—	0.1	
Low-Level Output Voltage					4.5	_	0.0	0.1	_	0.1	
		 			6.0	_	0.0	0.1	_	0.1	V
Catput Voltage				$I_{OL} = 6mA$	4.5	—	0.17	0.26	-	0.33	
				$I_{OL} = 7.8 \text{mA}$	6.0	_	0.18	0.26		0.33	
3-State Output	loz	_	$V_{IN} = V_{IH}$		6.0	l		± 0.5	_	± 5.0	
Off-State Current	102		$V_{OUT} = V_{C}$	CC or GND	0.0			_ 0.5		_ 5.0	
Input Leakage	I _{IN}	l	V _{IN} = V _{CC} or GND		6.0	_	_	± 0.1	_	± 1.0	μ A
Current	'IIN				0.0			- 0.1			
Quiescent Supply Current	lcc	_	V _{IN} = V _{CC} or GND		6.0	—	_	2.0	_	20.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

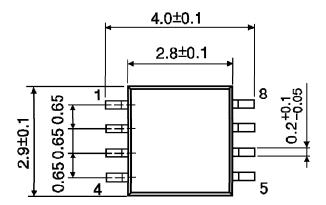
DADAMETED	CVMPOL	TEST	R-			Ta = 25°C			Ta = − 40~85°C		
PARAMETER	SYMBOL	CIR- CUIT		CL	Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Output Transition	+				2.0	_	20	60	_	75	
Time	t _{TLH}	_	_	50	4.5	—	6	12	-	15	
	TIFIL				6.0	_	5	10	_	13	
					2.0	—	30	90	-	115	
				50	4.5	—	11	18	_	23	
Propagation	tPLH	l	_		6.0	_	10	15	_	20	
Delay Time	^t pHL				2.0	—	42	130	—	165	
				150	4.5	—	14	26	 -	33	
					6.0	_	12	22	_	28	ns
	^t pZL ^t pZH		$ R_L = 1k\Omega$	50	2.0	—	30	90	—	115	-
Output Enable Time					4.5	_	11	18	—	23	
		l			6.0		10	15	_	20	
				150	2.0	—	42	130	-	165	
					4.5	—	14	26	—	33	
					6.0	_	12	22	_	28	
Output Disable	^t pLZ ^t pHZ	_	$ R_L = 1k\Omega$	50	2.0	—	24	100	—	125	
Time					4.5	—	12	20	—	25	
Time					6.0	_	10	17	_	21	
Input Capacitance	CIN	_	_	_		_	5	10	_	10	
Output Capacitance	COUT	_	_	_	_		10	_		_	рF
Power Dissipation Capacitance	C _{PD}	_	Note (1)	_	_	_	32	_	_	_	

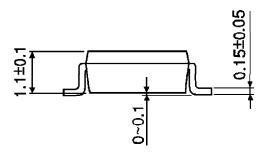
Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr) = C_{PD} · V_{CC} · f_{IN} + I_{CC} /2 (per Gate)

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PACKAGE DIMENSIONS SSOP8-P-0.65

Unit: mm





Weight: 0.02g (Typ.)

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000707EBA

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