

## TC74VHC138F, TC74VHC138FN, TC74VHC138FT, TC74VHC138FK

### 3-to-8 Line Decoder

The TC74VHC138 is an advanced high speed CMOS 3-to-8 DECODER fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ( $\bar{Y}0 - \bar{Y}7$ ) will go low.

When enable input G1 is held low or either  $\bar{G}2A$  or  $\bar{G}2B$  is held high, decoding function is inhibited and all outputs go high.

G1,  $\bar{G}2A$ , and  $\bar{G}2B$  inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

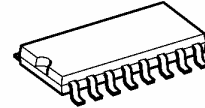
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

- High speed:  $t_{pd} = 5.7$  ns (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) at  $T_a = 25^\circ$ C
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} (opr) = 2$  V to 5.5 V
- Pin and function compatible with 74ALS138

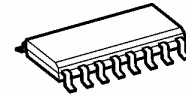
Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74VHC138F



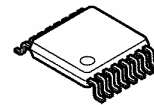
SOP16-P-300-1.27A

TC74VHC138FN



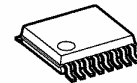
SOL16-P-150-1.27

TC74VHC138FT



TSSOP16-P-0044-0.65A

TC74VHC138FK

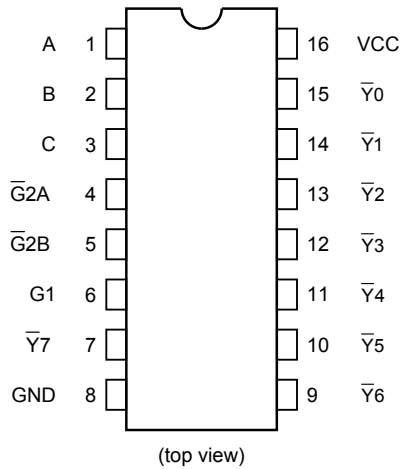


VSSOP16-P-0030-0.50

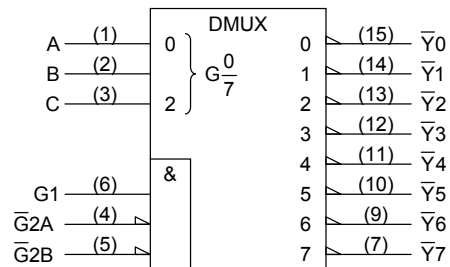
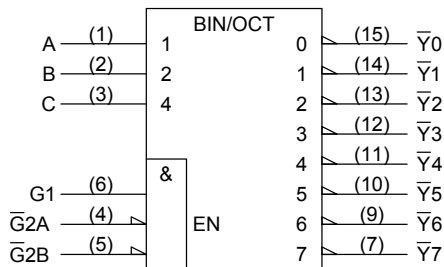
### Weight

SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)
TSSOP16-P-0044-0.65A	: 0.06 g (typ.)
VSSOP16-P-0030-0.50	: 0.02 g (typ.)

## Pin Assignment



## IEC Logic Symbol

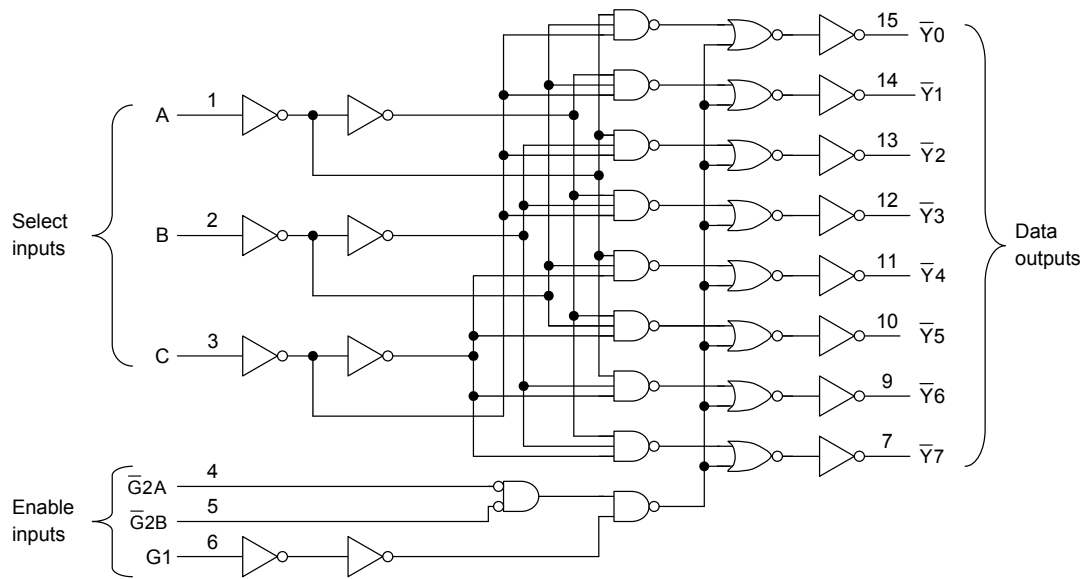


## Truth Table

Inputs						Outputs								Selected Output
Enable			Select			$\bar{Y}0$	$\bar{Y}1$	$\bar{Y}2$	$\bar{Y}3$	$\bar{Y}4$	$\bar{Y}5$	$\bar{Y}6$	$\bar{Y}7$	
G1	$\bar{G}2A$	$\bar{G}2B$	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	None
X	H	X	X	X	X	H	H	H	H	H	H	H	H	None
X	X	H	X	X	X	H	H	H	H	H	H	H	H	None
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\bar{Y}0$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\bar{Y}1$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\bar{Y}2$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\bar{Y}3$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\bar{Y}4$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\bar{Y}5$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\bar{Y}6$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\bar{Y}7$

X: Don't care

## Logic Diagram



## Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to 7.0	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC VCC/ground current	$I_{CC}$	$\pm 75$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dv	0 to 100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	— —	V
Low-level input voltage	V <sub>IL</sub>	—		2.0 3.0 to 5.5	— —	— —	— V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
			I <sub>OH</sub> = -8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I <sub>OL</sub> = 4 mA	3.0	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 8 mA	4.5	—	—	0.36	—	0.44	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	μA

## AC Characteristics (input: $t_r = t_f = 3$ ns)

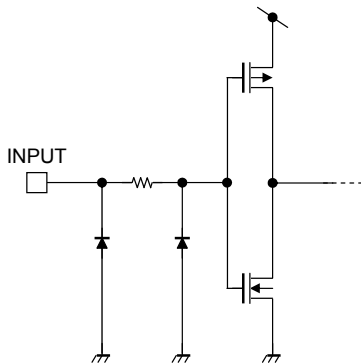
Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time (A, B, C- $\bar{Y}$ )	$t_{pLH}$	—	3.3 ± 0.3	15	—	8.2	11.4	1.0	13.5	ns
				50	—	10.0	15.8	1.0	18.0	
	$t_{pHL}$	5.0 ± 0.5	15	—	5.7	8.1	1.0	9.5		
			50	—	7.2	10.1	1.0	11.5		
Propagation delay time (G1- $\bar{Y}$ )	$t_{pLH}$	—	3.3 ± 0.3	15	—	8.1	12.8	1.0	15.0	ns
				50	—	10.6	16.3	1.0	18.5	
	$t_{pHL}$	5.0 ± 0.5	15	—	5.6	8.1	1.0	9.5		
			50	—	7.1	10.1	1.0	11.5		
Propagation delay time ( $\bar{G}2$ - $\bar{Y}$ )	$t_{pLH}$	—	3.3 ± 0.3	15	—	8.2	11.4	1.0	13.5	ns
				50	—	10.7	14.9	1.0	17.0	
	$t_{pHL}$	5.0 ± 0.5	15	—	5.8	8.1	1.0	9.5		
			50	—	7.3	10.1	1.0	11.5		
Input capacitance	C <sub>IN</sub>	—		—	4	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub>	—		(Note)	34	—	—	—	pF	

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

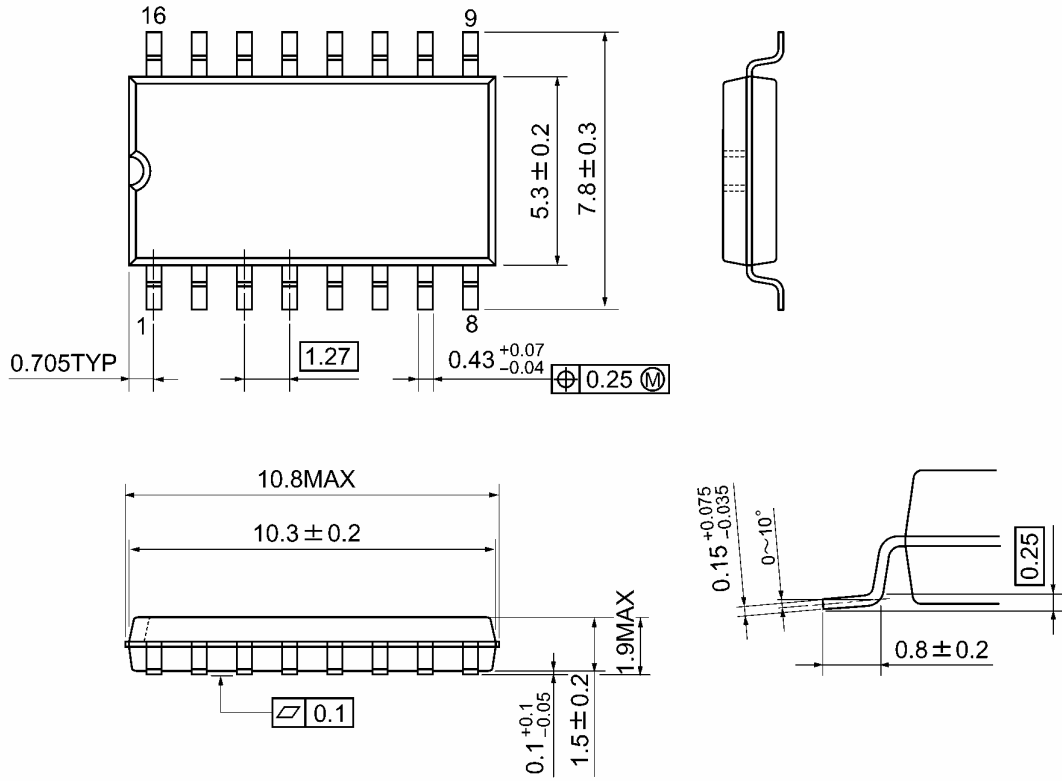
## Input Equivalent Circuit



## Package Dimensions

SOP16-P-300-1.27A

Unit: mm

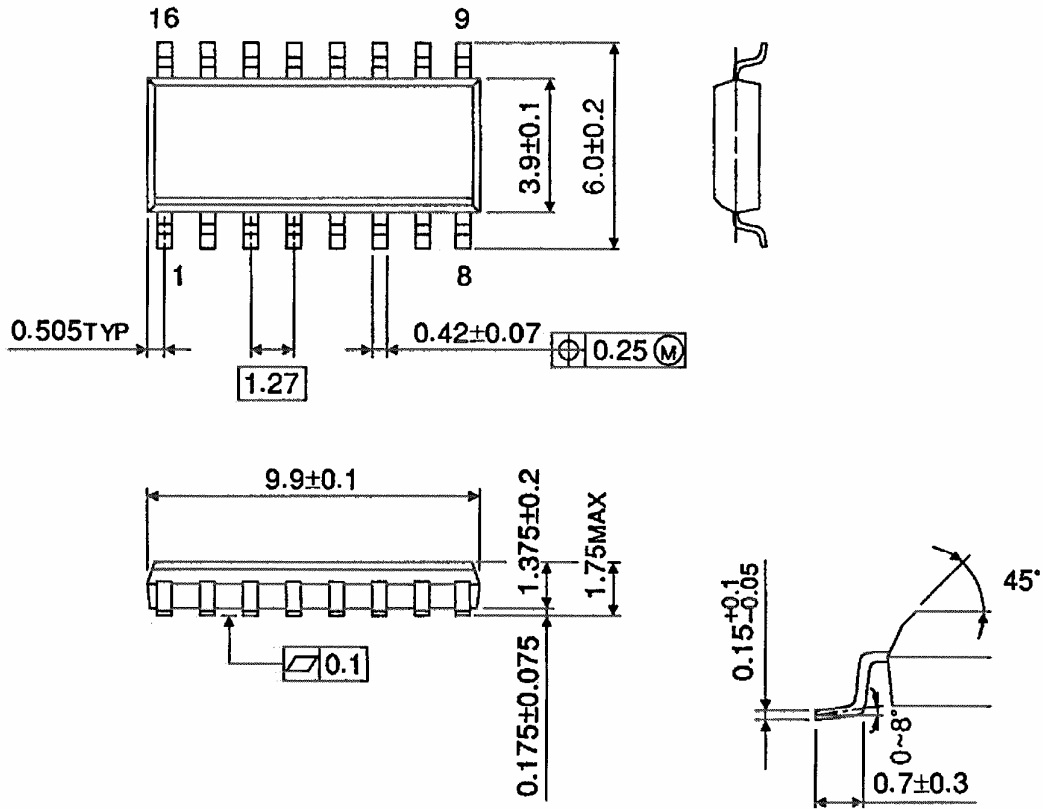


Weight: 0.18 g (typ.)

## Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



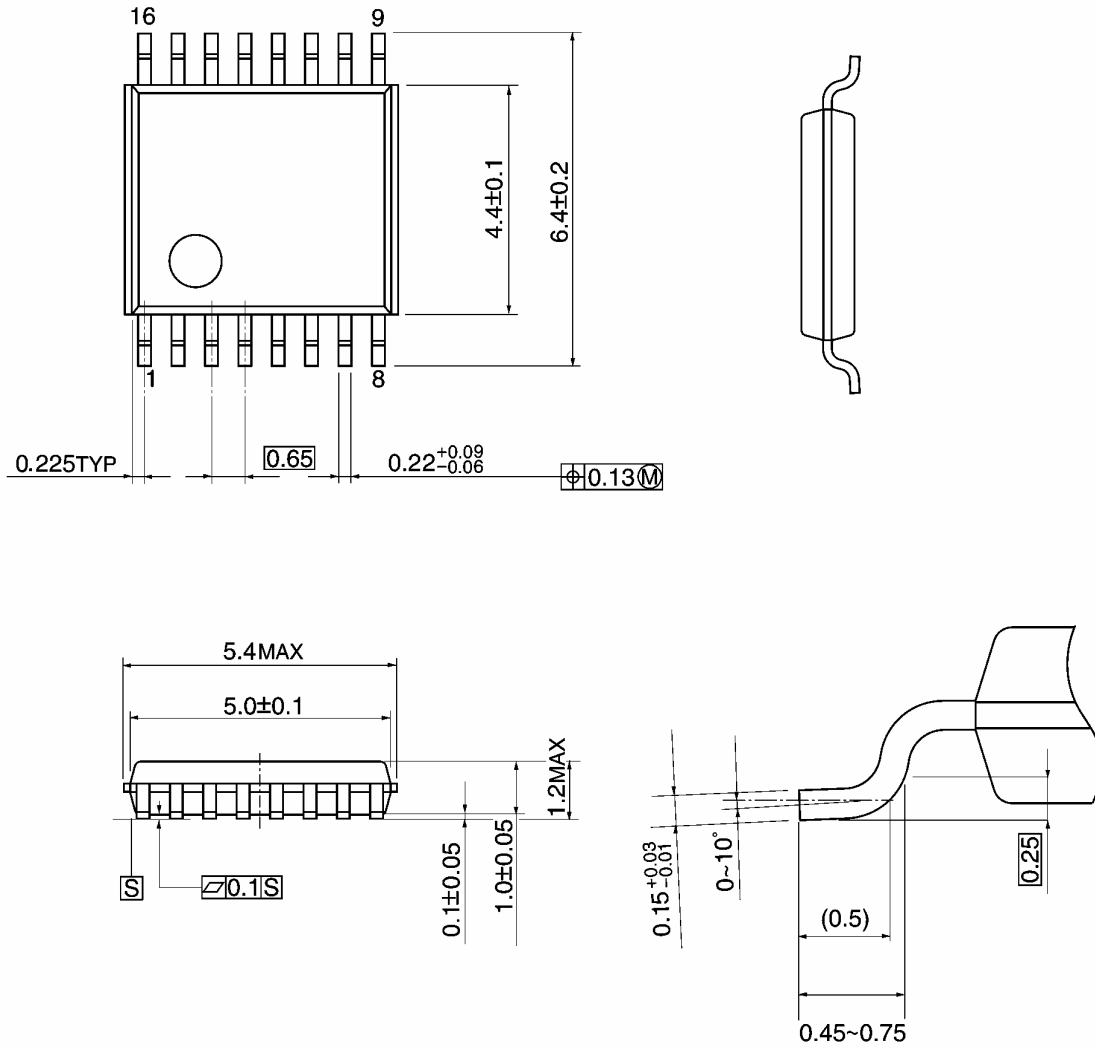
Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

## Package Dimensions

TSSOP16-P-0044-0.65A

Unit: mm



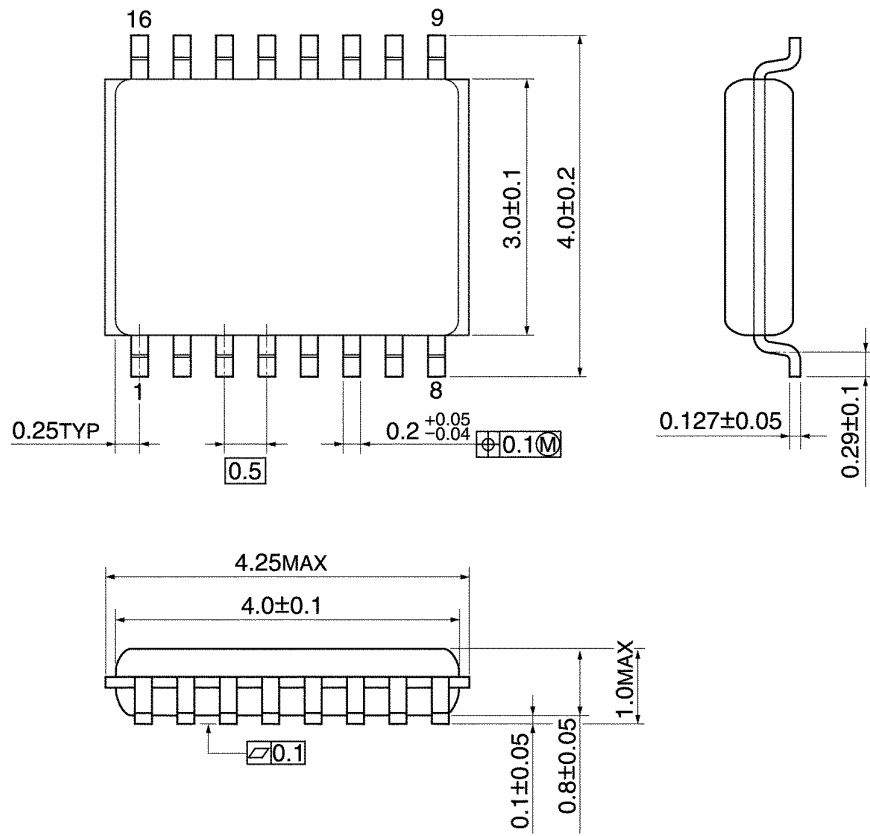
Weight: 0.06 g (typ.)



## Package Dimensions

VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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20070701-EN GENERAL

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