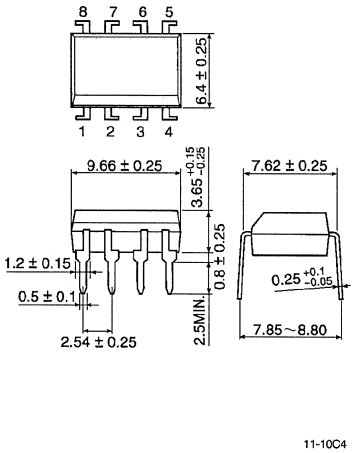
TOSHIBA Photocoupler GaAℓAs IRED & Photo IC

TLP552

Isolated Line Receiver
Simplex/Multiplex Data Transmission
Computer-Peripheral Interface
Microprocessor System Interface
Digital Isolation for A/D, D/A Conversion

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	11-10C4

Weight: 0.54 g (typ.)

The TOSHIBA TLP552 is a photocoupler which combines a GaAℓAs IRED as the emitter and an integrated high gain, high speed photodetector. This unit is 8-lead DIP.

The output of the detector circuit is an open collector, schottky clamped transistor.

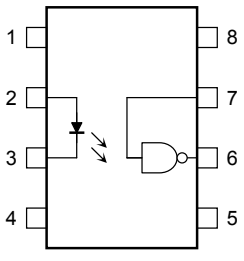
- TTL/LSTTL compatible: V_{CC} = 5 V
- Isolation voltage: 2500 Vrms (min)
- Switching speed: t_{pHL}, t_{pLH} = 60 ns (typ.) (@R_L = 350 Ω)
- Guaranteed performance over temp.: 0 to 70°C
- UL recognized: UL1577, file No. E67349

Truth Table (positive logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

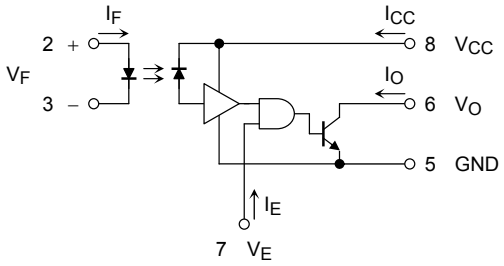
Note: A 0.1 μF bypass capacitor must be connected between pins 8 and 5 (see Note 1).

Pin Configurations (top view)



1: N.C.
2: Anode
3: Cathode
4: N.C.
5: GND
6: Output (open collector)
7: Enable
8: V_{CC}

Schematic



Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I_F	20	mA
	Pulse forward current (Note 1)	I_{FP}	40	mA
	Peak transient forward current (Note 2)	I_{FPT}	0.5	A
	Reverse voltage	V_R	5	V
	Diode power dissipation	P_D	40	mW
Detector	Output current	I_O	50	mA
	Output voltage	V_O	7	V
	Supply voltage (1 minute maximum)	V_{CC}	7	V
	Enable input voltage (Not to exceed V_{CC} by more than 500 mV)	V_E	5.5	V
	Output collector power dissipation	P_O	85	mW
Operating temperature range		T_{opr}	0 to 70	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Lead solder temperature (10 s) (Note 3)		T_{sol}	260	°C
Isolation voltage (AC, 1 min., R.H. ≤ 60%) (Note 4)		BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 50% duty cycle, 1 ms pulse width.

Note 2: Pulse width ≤ 1 μs, 300 pps.

Note 3: Soldering portion of lead: up to 2 mm from the body of the device.

Note 4: Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, low level	I_{FL}	0	—	250	μA
Input current, high level	I_{FH}	7	—	20	mA
Supply voltage, output*	V_{CC}	4.5	—	5.5	V
High level enable voltage	V_{EH}	2.0	—	V_{CC}	V
Low level enable voltage	V_{EL}	0	—	0.8	V
Fan out (TTL load)	N	—	—	8	—
Operating temperature	T_{opr}	0	—	70	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

*This item denotes operating ranges, not meaning of recommended operating conditions.

Electrical Characteristics (unless otherwise specified, for 0°C ≤ Ta ≤ 70°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V_F	I_F = 10 mA, Ta = 25°C	—	1.65	1.8	V
Input diode temperature coefficient	$\Delta V_F/\Delta Ta$	I_F = 10 mA	—	−2.0	—	mV/°C
Input reverse current	I_R	V_R = 5 V, Ta = 25°C	—	—	10	μA
Input capacitance	C_T	V_F = 0, f = 1 MHz	—	45	—	pF
High level output current	I_{OH}	V_{CC} = 5.5 V, V_O = 5.5 V I_F = 250 μA, V_E = 2.0 V	—	10	250	μA
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_F = 5 mA, V_{EH} = 2.0 V I_{OL} = (sinking) = 13 mA	—	0.4	0.6	V
Input current logic low output level	I_{FH}	I_{OL} = 13 mA (sinking), V_O = 0.6 V V_{CC} = 5.5 V, V_{EH} = 2.0 V	—	—	5	mA
High level enable current	I_{EH}	V_{CC} = 5.5 V, V_E = 2.0 V	—	−0.1	—	mA
Low level enable current	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V	—	−1.6	−2.0	mA
High level supply current	I_{CCH}	V_{CC} = 5.5 V, I_F = 0, V_E = 0.5 V	—	7	15	mA
Low level supply current	I_{CCL}	V_{CC} = 5.5 V, I_F = 10 mA, V_E = 0.5 V	—	12	18	mA
Current transfer ratio	CTR	I_F = 5.0 mA, R_L = 100 Ω V_{CC} = 5 V, Ta = 25°C	—	1000	—	%
Resistance (input-output)	R_S	V_S = 500 V, R.H. ≤ 60%, Ta = 25°C (Note 1)	5×10^{10}	10^{14}	—	Ω
Capacitance (input-output)	C_S	V_S = 0, f = 1 MHz, Ta = 25°C (Note 1)	—	0.6	—	pF

Note 1: Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 2: All typical values are at V_{CC} = 5 V, Ta = 25°C.

Switching Characteristics (Ta = 25°C, V_{CC} = 5 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to high output level (L → H)	t_{pLH}	1	R_L = 350 Ω, C_L = 15 pF I_F = 7.5 mA	—	60	120	ns
Propagation delay time to low output level (H → L)	t_{pHL}	1	R_L = 350 Ω, C_L = 15 pF I_F = 7.5 mA	—	60	120	ns
Output rise fall time (10 to 90%)	t_r, t_f	1	R_L = 350 Ω, C_L = 15 pF I_F = 7.5 mA	—	30	—	ns
Propagation delay time of enable from V_{EH} to V_{EL}	t_{ELH}	2	R_L = 350 Ω, C_L = 15 pF I_F = 7.5 mA, V_{EH} = 3.0 V	—	25	—	ns
Propagation delay time of enable from V_{EL} to V_{EH}	t_{EHL}	2	R_L = 350 Ω, C_L = 15 pF I_F = 7.5 mA, V_{EH} = 3.0 V	—	25	—	ns
Common mode transient immunity at logic high output level	CM_H	3	V_{CM} = 200 V, R_L = 350 Ω V_O (min) = 2 V, I_F = 0 mA (Note 4)	—	200	—	V/μs
Common mode transient immunity at logic low output level	CM_L	3	V_{CM} = 200 V, R_L = 350 Ω V_O (max) = 0.8 V, I_F = 5 mA (Note 4)	—	−500	—	V/μs

Note 1: A ceramic capacitor (0.1 μF) should be connected from pin 8 and pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 1 cm.

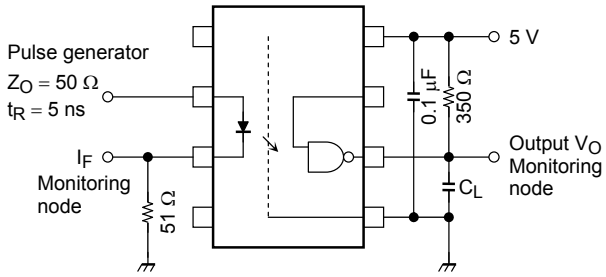
Note 2: Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 3: Enable input: No pull up resistor required as the device has an internal pull up resistor.

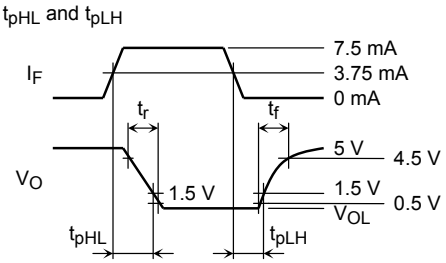
Note 4: CM_L: The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., V_{OUT} < 0.8 V).
CM_H: The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e., V_{OUT} > 2.0 V).
Measured in volts per microsecond (V/μs).

Note 5: Maximum electrostatic discharge voltage for any pins: 180 V (C = 200 pF, R = 0).

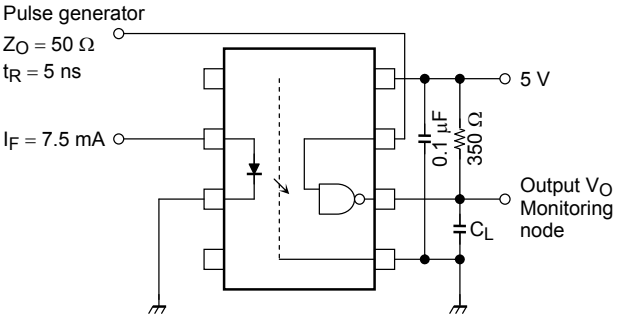
Test Circuit 1



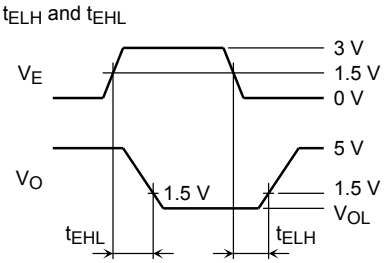
C_L is approximately 15 pF which includes probe and stray wiring capacitance.



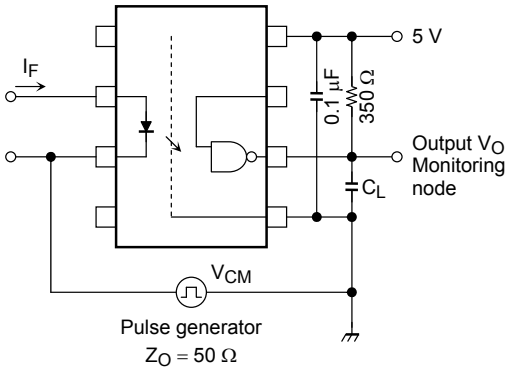
Test Circuit 2



C_L is approximately 15 pF which includes probe and stray wiring capacitance.

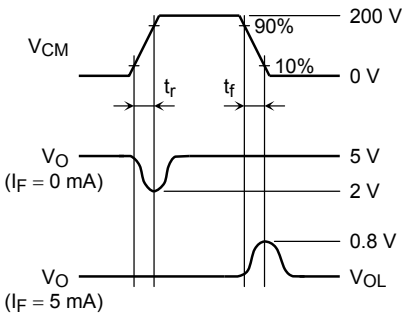


Test Circuit 3

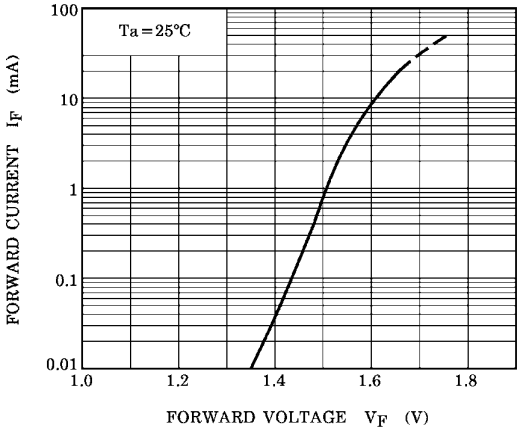


$$CM_H = \frac{160\ (V)}{t_r\ (\mu s)},\ CM_L = \frac{160\ (V)}{t_f\ (\mu s)}$$

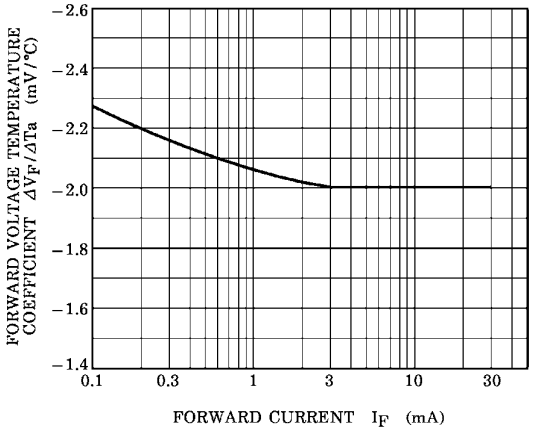
Transient immunity and typical waveform



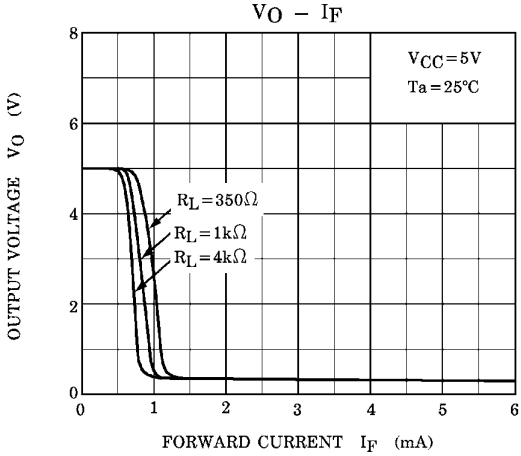
$I_F - V_F$



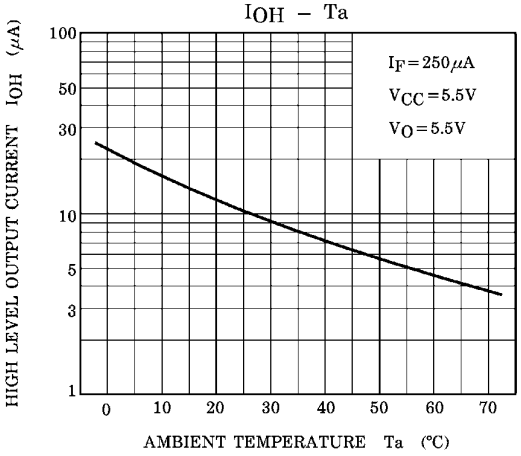
$\Delta V_F / \Delta Ta - I_F$



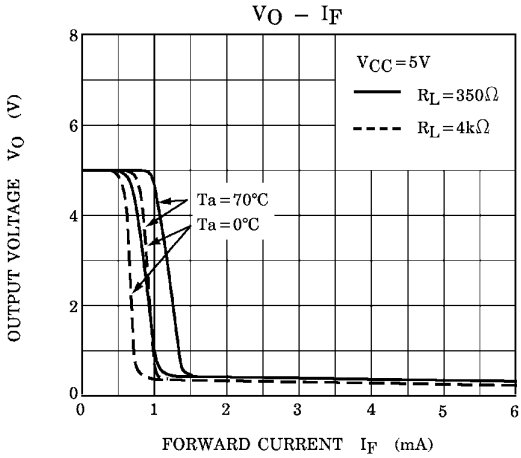
$V_O - I_F$



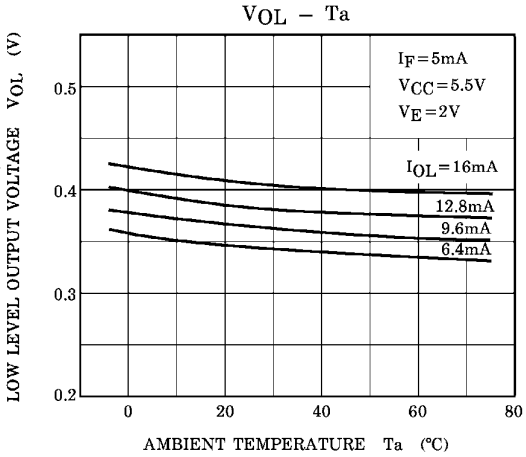
$I_{OH} - Ta$



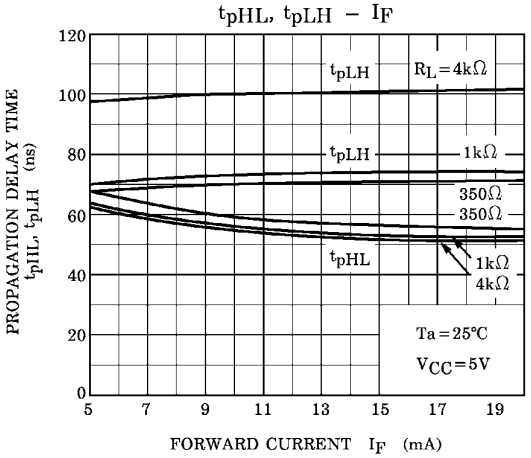
$V_O - I_F$



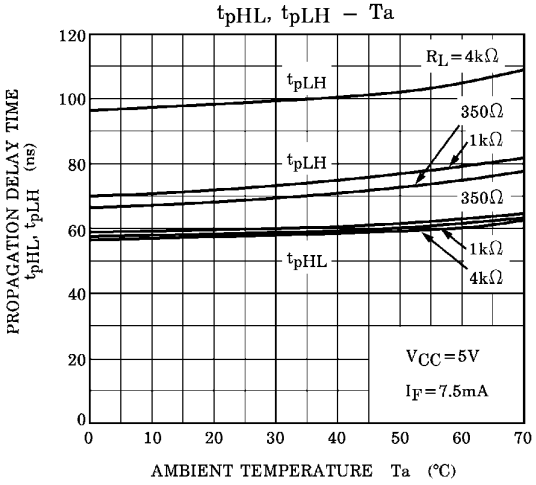
$V_{OL} - Ta$



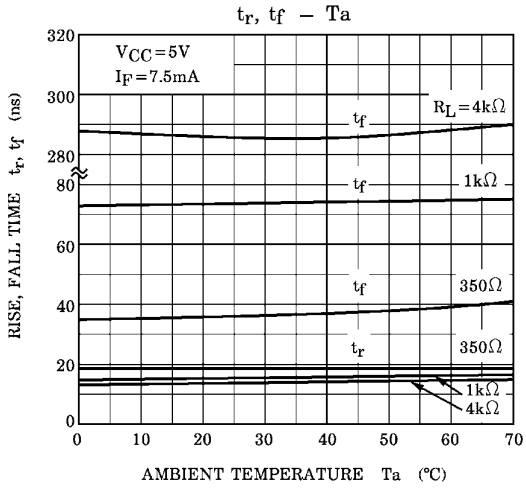
t_{pHL}, t_{pLH} – I_F



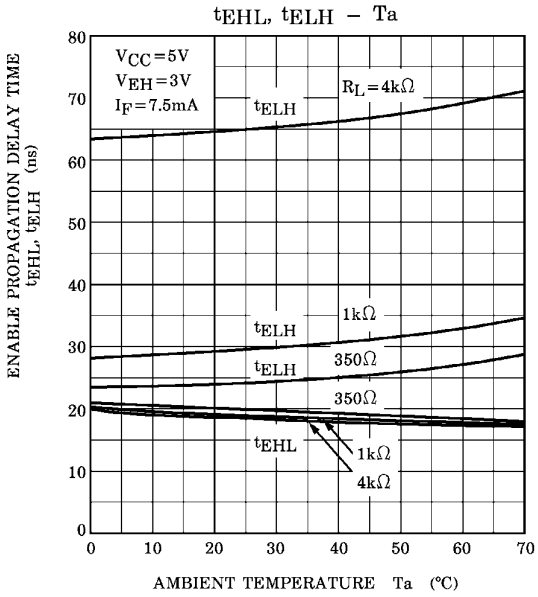
t_{pHL}, t_{pLH} – Ta



t_r, t_f – Ta



t_{EHL}, t_{ELH} – Ta



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