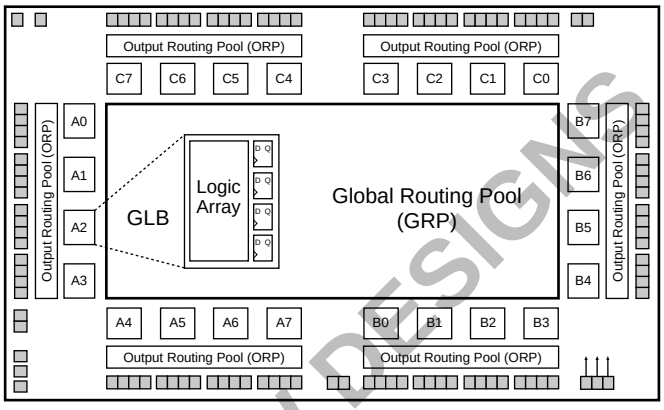
ispLSI® 2096V

3.3V High Density Programmable Logic

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **— 4000 PLD Gates**
  - **— 96 I/O Pins, Six Dedicated Inputs**
  - **— 96 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **3.3V LOW VOLTAGE 2096 ARCHITECTURE**
  - **— Interfaces with Standard 5V TTL Devices**
  - **— Fuse Map Compatible with 5V ispLSI 2096**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 80 MHz Maximum Operating Frequency**
  - **— t_{pd} = 10 ns Propagation Delay**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **— 3.3V In-System Programmability (ISP™) Using Boundary Scan Test Access Port (TAP)**
  - **— Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR or Bus Arbitration Logic**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAS**
  - **— Enhanced Pin Locking Capability**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispDesignEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **— Superior Quality of Results**
  - **— Tightly Integrated with Leading CAE Vendor Tools**
  - **— Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **— PC and UNIX Platforms**

Functional Block Diagram



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Description

The ispLSI 2096V is a High Density Programmable Logic Device containing 96 Registers, six Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2096V features in-system programmability through the Boundary Scan Test Access Port (TAP). The ispLSI 2096V offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2096V device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. C7 (see Figure 1). There are a total of 24 GLBs in the ispLSI 2096V device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output

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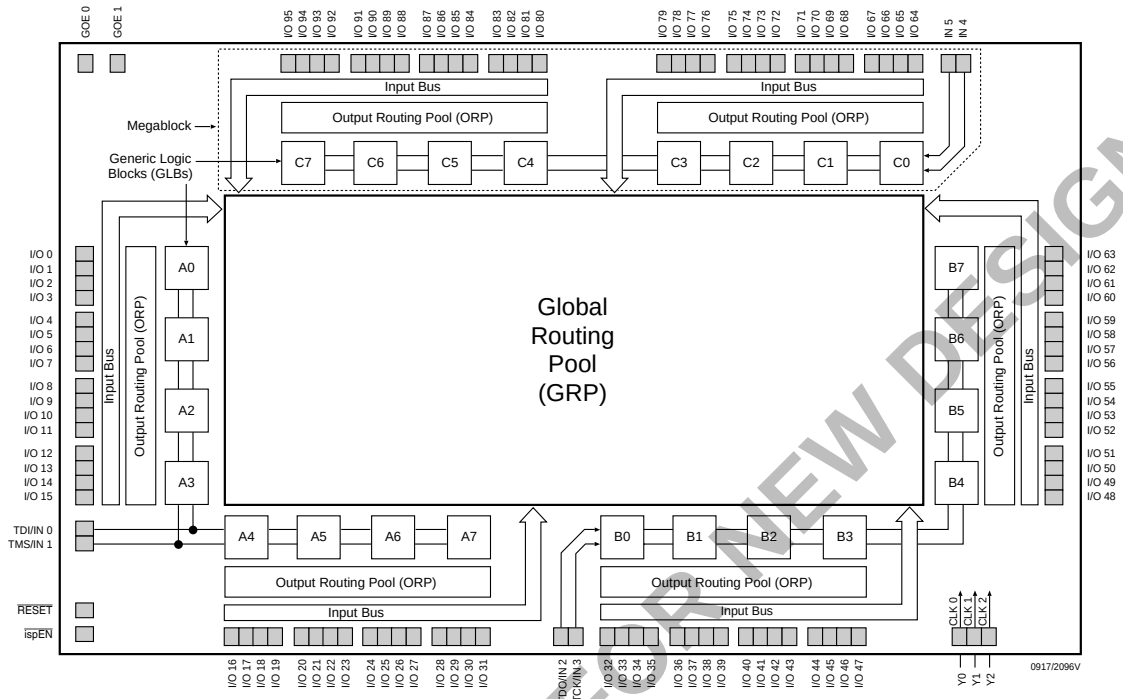
Functional Block Diagram

Figure 1. ispLSI 2096V Functional Block Diagram



slew rate to minimize overall output switching noise. Device pins can be safely driven to 5-volt signal levels to support mixed-voltage systems.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the two ORPs. Each ispLSI 2096V device contains three Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2096V device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 2096V are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. When this fuse is erased (JEDEC “1”), the output is configured as a totem-pole output. When this fuse is programmed (JEDEC “0”), the output is configured as an open-drain. The default configuration when the device is in bulk erased state is totem-pole configuration. The open-drain/totem-pole option is selectable through the ispDesignEXPERT software tools.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +5.6V

Input Voltage Applied ..... -0.5 to +5.6V

Off-State Output Voltage Applied ..... -0.5 to +5.6V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial T_A = 0°C to + 70°C	3.0	3.6	V
		Industrial T_A = -40°C to + 85°C	3.0	3.6	V
V_{IL}	Input Low Voltage		V_{SS} – 0.5	0.8	V
V_{IH}	Input High Voltage		2.0	5.25	V

Table 2-0005/2096V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	10	pf	V_{CC} = 3.3V, V_{IN} = 2.0V
C_2	I/O Capacitance	10	pf	V_{CC} = 3.3V, $V_{I/O}$ = 2.0V
C_3	Clock and Global Output Enable Capacitance	13	pf	V_{CC} = 3.3V, V_Y = 2.0V

Table 2-0006/2096V

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/2096V

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

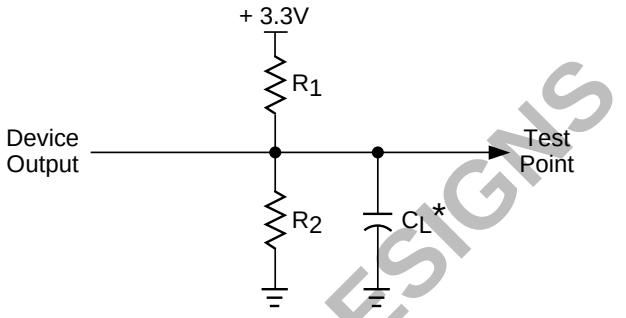
Table 2-0003/2096V

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		316Ω	348Ω	35pF
B	Active High	∞	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	348Ω	5pF
	Active Low to Z at V_{OL} +0.5V	316Ω	348Ω	5pF

Table 2-0004/2128V

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

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DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	(V_{CC} – 0.2)V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
		V_{CC} ≤ V_{IN} ≤ 5.25V	–	–	50	mA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V, V_{OUT} = 0.5V	–	–	-100	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{CLOCK} = 1 MHz	–	140	–	mA

Table 2-0007A/2096V

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using six 16-bit counters.
3. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-80		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	15.0	–	20.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	80.0	–	61.7	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	64.5	–	51.3	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	100	–	71.4	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	7.0	–	9.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	6.5	–	8.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	9.0	–	11.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	7.5	–	9.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	14.0	–	16.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	7.0	–	8.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	15.0	–	18.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	15.0	–	18.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	10.0	–	12.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	10.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	5.0	–	7.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	5.0	–	7.0	–	ns

Table 2-0030/2096V

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

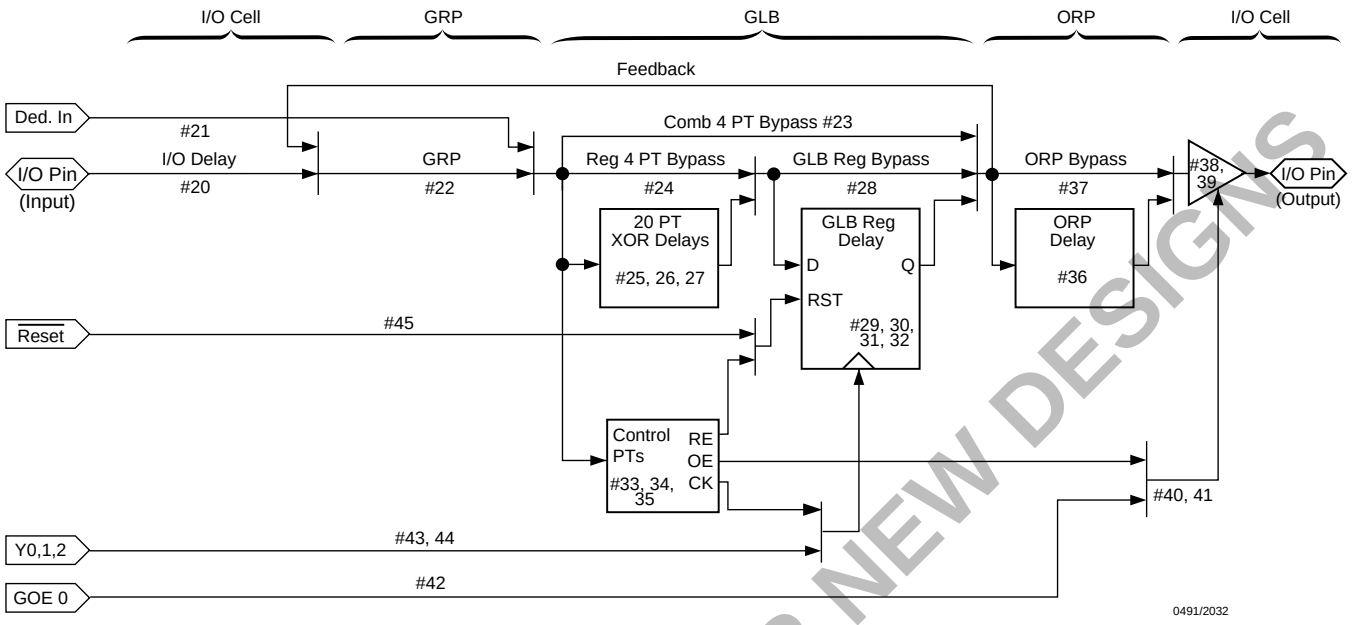
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	–	0.4	–	0.6	ns
t_{din}	21	Dedicated Input Delay	–	1.3	–	1.4	ns
GRP							
t_{grp}	22	GRP Delay	–	1.2	–	2.1	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	–	5.8	–	9.6	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	–	7.5	–	10.3	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	9.2	–	12.3	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	9.5	–	12.3	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	11.3	–	14.4	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.3	–	1.3	ns
t_{gsu}	29	GLB Register Setup Time befor Clock	0.2	–	0.2	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	5.4	–	8.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	1.6	–	1.6	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	2.5	–	2.8	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	5.6	–	9.3	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	8.5	–	10.4	ns
t_{ptck}	35	GLB Product Term Clock Delay	3.8	5.6	6.5	9.3	ns
ORP							
t_{orp}	36	ORP Delay	–	1.4	–	1.5	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.4	–	0.5	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	2.2	–	2.2	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	12.2	–	12.2	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	4.9	–	4.9	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	4.9	–	4.9	ns
t_{goe}	42	Global Output Enable	–	5.1	–	7.1	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.3	2.3	4.2	4.2	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.3	2.3	4.2	4.2	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	7.9	–	9.5	ns

Table 2-0036/2096V

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI 2096V Timing Model



Derivations of tsu, th and tco from the Product Term Clock

tsu = Logic + Reg su - Clock (min)
= (**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
= (#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
5.9 ns = (0.4 + 1.2 + 9.5) + (0.2) - (0.4 + 1.2 + 3.8)

th = Clock (max) + Reg h - Logic
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
= (#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
1.5 ns = (0.4 + 1.2 + 5.6) + (5.4) - (0.4 + 1.2 + 9.5)

tco = Clock (max) + Reg co + Output
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#20+ #22+ #35) + (#31) + (#36 + #38)
12.4 ns = (0.4 + 1.2 + 5.6) + (1.6) + (1.4 + 2.2)

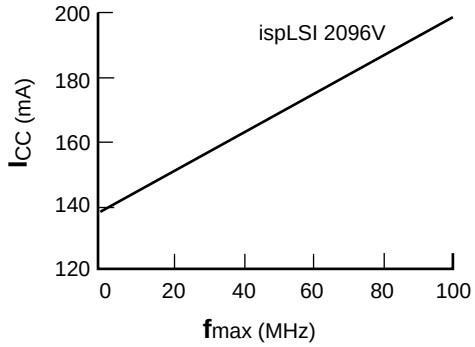
Note: Calculations are based upon timing specifications for the ispLSI 2096V-80L.

Table 2-0042/2096V

Power Consumption

Power consumption in the ispLSI 2096V device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of six 16-bit counters
Typical current at 3.3V, 25° C

I_{CC} can be estimated for the ispLSI 2096V using the following equation:

I_{CC} (mA) = 20.2 + (# of PTs * 0.611) + (# of nets * Max freq * 0.0063)

Where:

# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 3.3V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

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Power-up Considerations

When Lattice 3.3V 2000V devices are used in mixed 5V/3.3V applications, some consideration needs to be given to the power-up sequence. When the I/O pins on the 3.3V ispLSI devices are driven directly by 5V devices, a low impedance path can exist on the 3.3V device between its I/O and Vcc pins when the 3.3V supply is not present. This low impedance path can cause current to flow from the 5V device into the 3.3V ispLSI device. The maximum current occurs when the signals on the I/O pins are driven high by the 5V devices. If a large enough current flows through the 3.3V I/O pins, latch-up can occur and permanent device damage may result.

This latch-up condition occurs only during the power-up sequence when the 5V supply comes up before the 3.3V supply. The Lattice 3.3V ispLSI devices are guaranteed to withstand 5V interface signals within the device operating Vcc range of 3.0V to 3.6V.

The recommended power-up options are as follows:

Option 1: Ensure that the 3.3V supply is powered-up and stable before the 5V supply is powered up.

Option 2: Ensure that the 5V device outputs are driven to a high impedance or logic low state during power-up.

Pin Description

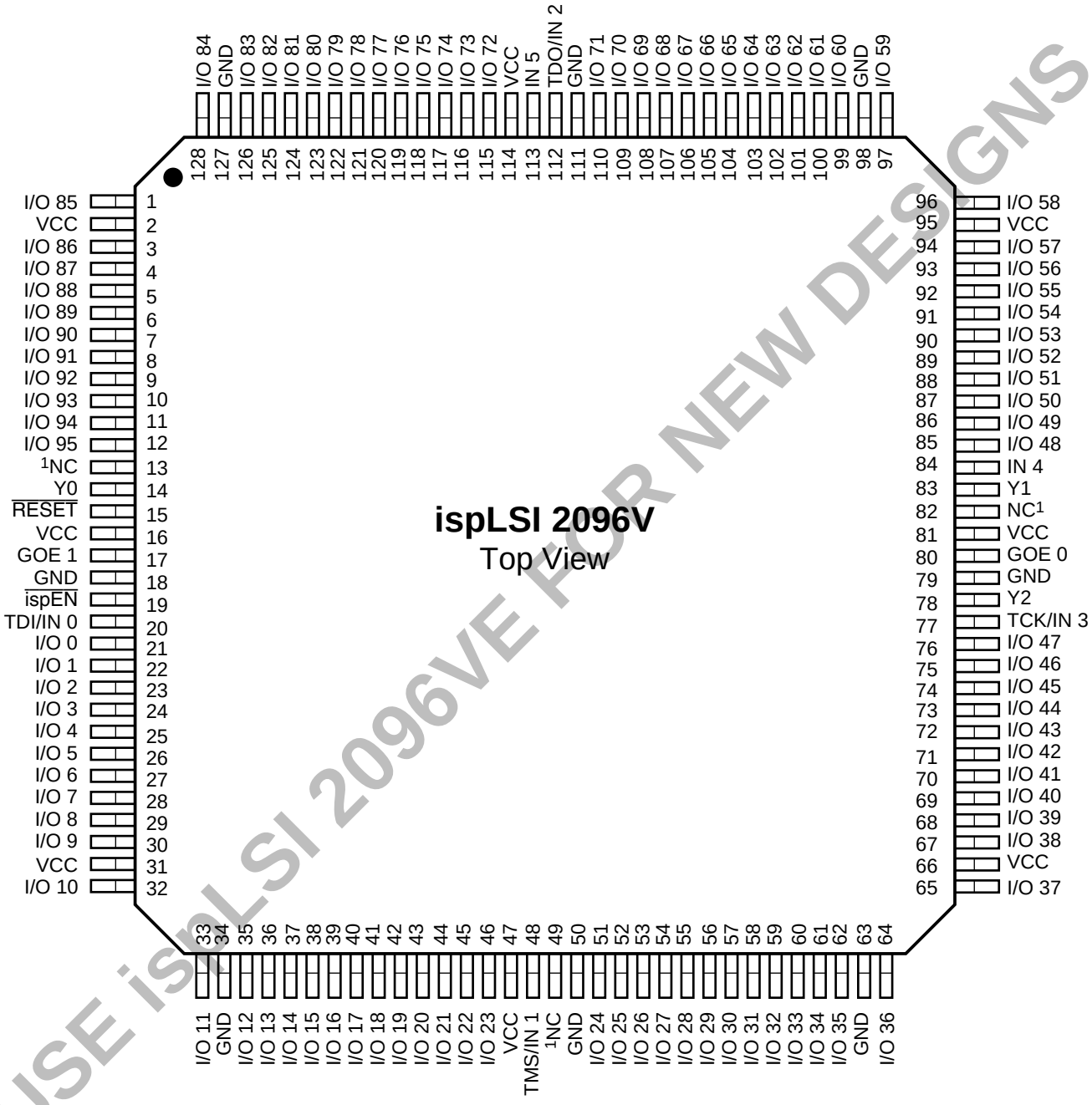
NAME	PQFP & TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	21, 22, 23, 24, 25, 26 27, 28, 29, 30, 32, 33 35, 36, 37, 38, 39, 40 41, 42, 43, 44, 45, 46 51, 52, 53, 54, 55, 56 57, 58, 59, 60, 61, 62 64, 65, 67, 68, 69, 70 71, 72, 73, 74, 75, 76 85, 86, 87, 88, 89, 90 91, 92, 93, 94, 96, 97 99, 100, 101, 102, 103, 104 105, 106, 107, 108, 109, 110 115, 116, 117, 118, 119, 120 121, 122, 123, 124, 125, 126 128, 1, 3, 4, 5, 6 7, 8, 9, 10, 11, 12	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0, GOE 1	80, 17	Global Output Enables input pins.
IN 4, IN 5	84, 113	Dedicated input pins to the device.
$\overline{\text{ispEN}}$	19	Input — Dedicated in-system programming Boundary Scan enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI/IN 0	20	Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a serial data input pin to load programming data into the device. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
TMS/IN 1	48	Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a mode control pin for the ISP/Boundary Scan state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
TDO/IN 2	112	Output/Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
TCK/IN 3	77	Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the ISP/Boundary Scan state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
$\overline{\text{RESET}}$	15	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0, Y1, Y2	14 83, 78	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
GND	18, 34, 50, 63, 79, 98, 111, 127	Ground (GND)
VCC	2, 16, 31, 47, 66, 81, 95, 114	V_{CC}
NC[1]	13, 49, 82	No Connect.

1. NC pins are not to be connected to any active signal, VCC or GND.

Table 2-0002-2096V

Pin Configuration

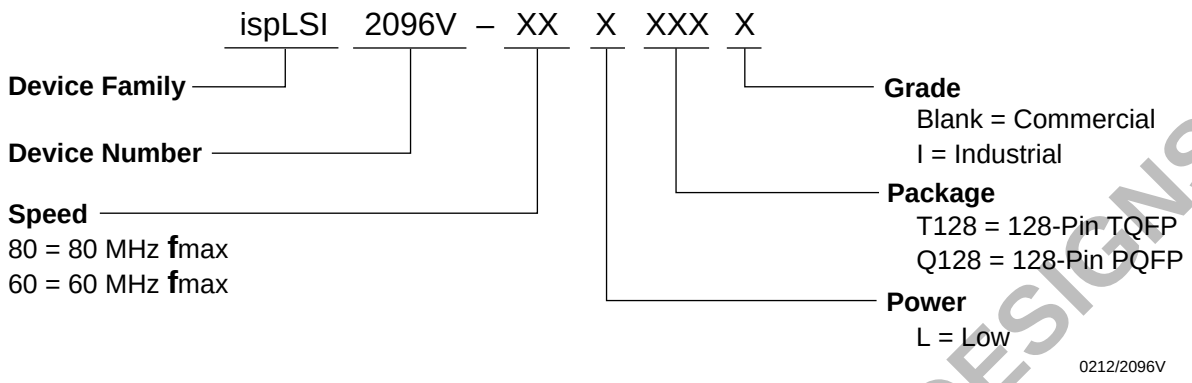
ispLSI 2096V 128-Pin PQFP and TQFP Pinout Diagram



1. NC pins are not to be connected to any active signals, VCC or GND.

0124-2096V

Part Number Description



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ispLSI 2096V Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	80	10	ispLSI 2096V-80LT128	128-Pin TQFP
	80	10	ispLSI 2096V-80LQ128	128-Pin PQFP
	60	15	ispLSI 2096V-60LT128	128-Pin TQFP
	60	15	ispLSI 2096V-60LQ128	128-Pin PQFP

Table 2-0041A/2096V

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	60	15	ispLSI 2096V-60LT128I	128-Pin TQFP

Table 2-0041B/2096V