# M62364FP

## 8-BIT 8-CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS

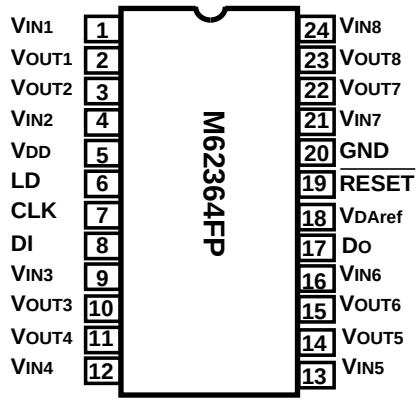
### GENERAL DESCRIPTION

The M62364FP is a CMOS 8-bit, 8-ch D/A converter having a multiplying function and output buffer amplifiers. It has a serial data input and can easily communicate with a microcontroller by the simple three-wiring method (DI, CLK, LD).
The output buffer amplifiers operating in AB-class has both sinking and driving capabilities of 1.0mA or more and can operate in a whole supply range from VDD to GND.
The IC is suitable for a use in automatic adjustment applications in conjunction with a MCU by utilizing the terminal DO for a cascading connection.

### FEATURES

- Three-wiring serial data transmission
- Doubled precision 8-ch D/A converter employing an R-2R with higher-order segment method
- 8 buffer amplifiers operating in a whole supply voltage range from VDD to GND
- 4-quadrant multiplication

### PIN CONFIGURATION (TOP VIEW)

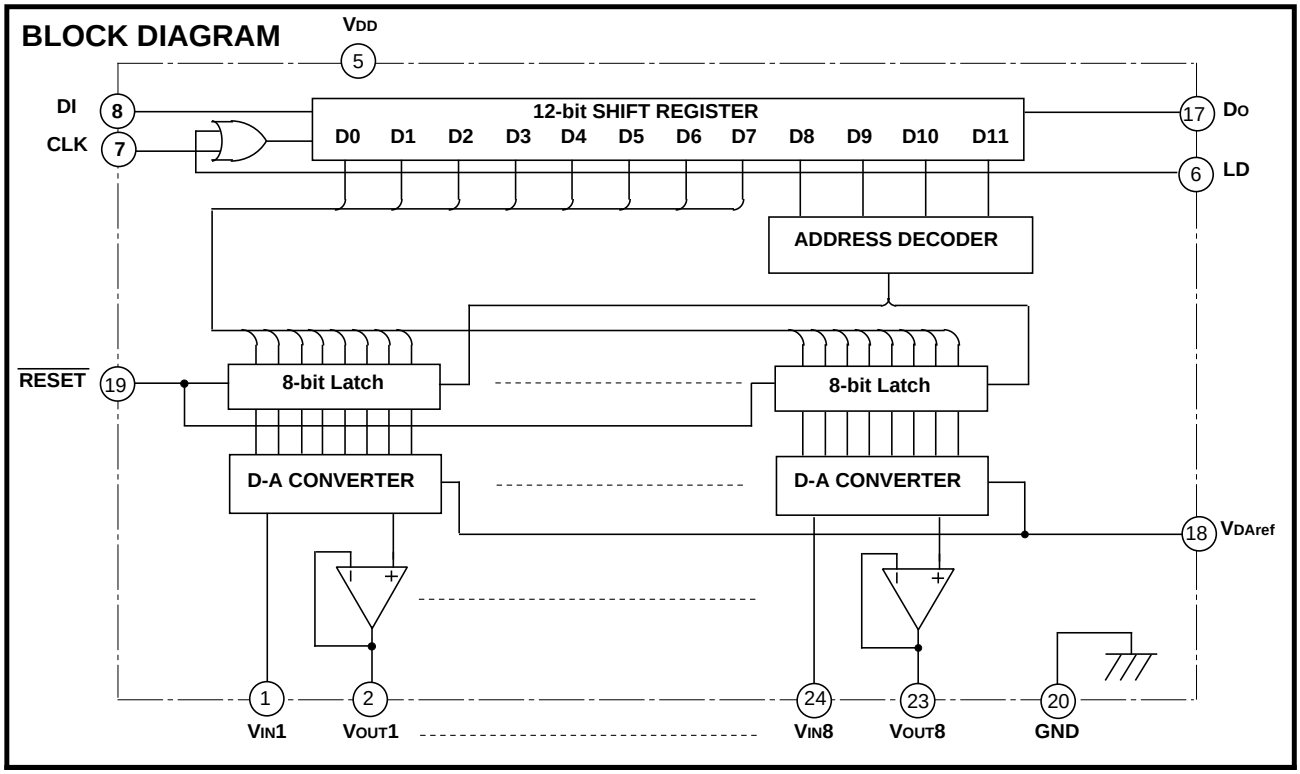



Outline 24P2Q (FP)

### APPLICATION

Digital to analog conversion for consumer and industrial equipment.
Gain setting and automatic adjustment of display-monitor and CTV.

### BLOCK DIAGRAM

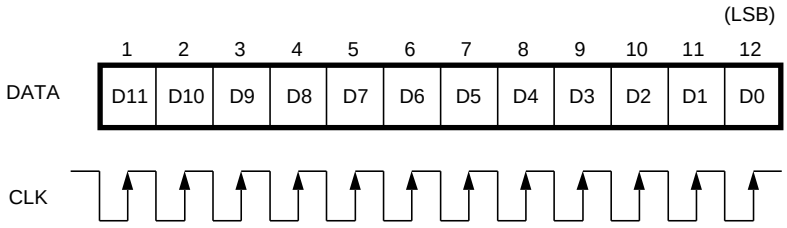


## EXPLANATION OF TERMINALS

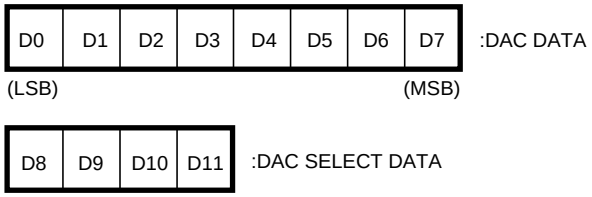
| PIN No. | Symbol | Function |
|---|---|---|
| 8 | D I | Serial data input |
| 17 | Do | Serial data output |
| 7 | CLK | Shift clock input. Input data of DI are taken into the 12-bit shift register on a rising edge of the clock. |
| 6 | L D | A low state enables data loading to the 12-bit shift register. During a rising edge of LD, the data will be loaded to the output register. |
| 19 | $\overline{\text{RESET}}$ | Reset 8-bit latches |
| 2 | $V_{OUT}1$ | D/A Converter Output with 8-bit resolution |
| 3 | $V_{OUT}2$ | |
| 10 | $V_{OUT}3$ | |
| 11 | $V_{OUT}4$ | |
| 14 | $V_{OUT}5$ | |
| 15 | $V_{OUT}6$ | |
| 22 | $V_{OUT}7$ | |
| 23 | $V_{OUT}8$ | |
| 5 | $V_{DD}$ | Power Supply |
| 20 | GND | Ground |
| 1 | $V_{IN}1$ | D/A Converter Input |
| 4 | $V_{IN}2$ | |
| 9 | $V_{IN}3$ | |
| 12 | $V_{IN}4$ | |
| 13 | $V_{IN}5$ | |
| 16 | $V_{IN}6$ | |
| 21 | $V_{IN}7$ | |
| 24 | $V_{IN}8$ | |
| 18 | $V_{DAref}$ | D-A Converter Reference Voltage Input |

## DIGITAL FORMAT

•12BIT SERIAL DATA




•DATA ASSIGNMENT



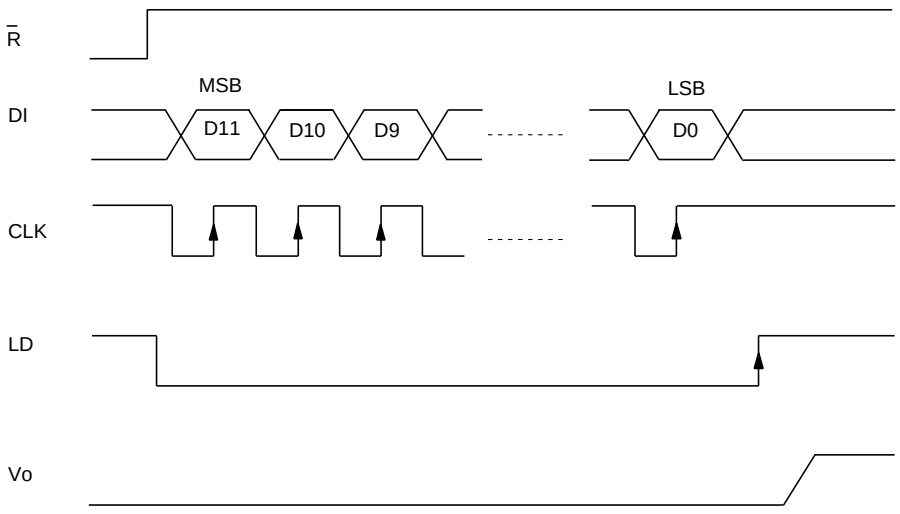

Dac Select Data

| D8 | D9 | D10 | D11 | **Dac Selection** |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Don't Care |
| 0 | 0 | 0 | 1 | VOUT1 Selection |
| 0 | 0 | 1 | 0 | VOUT2 Selection |
| 0 | 0 | 1 | 1 | VOUT3 Selection |
| 0 | 1 | 0 | 0 | VOUT4 Selection |
| 0 | 1 | 0 | 1 | VOUT5 Selection |
| 0 | 1 | 1 | 0 | VOUT6 Selection |
| 0 | 1 | 1 | 1 | VOUT7 Selection |
| 1 | 0 | 0 | 0 | VOUT8 Selection |
| 1 | 0 | 0 | 1 | Don't Care |
| 1 | 0 | 1 | 0 | Don't Care |
| 1 | 0 | 1 | 1 | Don't Care |
| 1 | 1 | 0 | 0 | Don't Care |
| 1 | 1 | 0 | 1 | Don't Care |
| 1 | 1 | 1 | 0 | Don't Care |
| 1 | 1 | 1 | 1 | Don't Care |

•Digital Data Format

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | DAC OUTPUT |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $V_{DAref}$ |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $(V_{IN}-V_{DAref})/256 \times 1+V_{DAref}$ |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | $(V_{IN}-V_{DAref})/256 \times 2+V_{DAref}$ |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | $(V_{IN}-V_{DAref})/256 \times 3+V_{DAref}$ |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $(V_{IN}-V_{DAref})/256 \times 255+V_{DAref}$ |

**TIMING CHART**




* Input data carried out LD signal Low besides CLK signal positive edge.
CLK,LD is keep generally HIGH level.

## ABSOLUTE MAXIMUM RATING

| SYMBOL | PARAMETER | MEASUREMENT CONDITION | RATINGS | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | -0.3 ~ +7.0 | V |
| $V_{IND}$ | Digital Input Voltage | | -0.3 ~ +7.0 | V |
| $V_{IN}$ | Analog Input Voltage | | -0.3 ~ VDD+0.3 | V |
| $V_{OUT}$ | Analog Output Voltage | | -0.3 ~ VDD+0.3 | V |
| $V_{DAref}$ | D-A Reference Voltage | | -0.3 ~ VDD+0.3 | V |
| $T_{opr}$ | Operating Temperature | | -20 ~ +75 | ℃ |
| $T_{stg}$ | Storage Temperature | | -40 ~ +125 | ℃ |

## ELECTRICAL CHARACTERISTICS

<Ana/Dig Common Part> ($V_{DD}$=5V±10%,$V_{DD}$≥$V_{IN}$,GND,$V_{DAref}$=0V,Ta=-20~85°C unless otherwise noted)

| SYMBOL | PARAMETER | MEASUREMENT CONDITION | LIMIT | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{DD}$ | Supply Voltage | | 2.7 | 3.0 | 3.6 | V |
| $I_{DD}$ | Supply Current | CLK=1MHz,$V_{CC}$=3V,IAO=0µA | | | 3.5 | mA |

<Digital Part> ($V_{DD}$=5V±10%,$V_{DD}$≥$V_{IN}$,GND,$V_{DAref}$=0V,Ta=-20~85°C unless otherwise noted)

| SYMBOL | PARAMETER | MEASUREMENT CONDITION | LIMIT | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $I_{ILK}$ | Input Leak Current | $V_{IN}$=0 ~ $V_{DD}$ | -10 | | 10 | µ A |
| $I_{IL}$ | Digital Input "Low" Voltage | | | | 0.2$V_{DD}$ | V |
| $I_{IH}$ | Digital Input "High" Voltage | | 0.8$V_{DD}$ | | | V |
| $V_{OL}$ | Do Terminal Output "Low" Voltage | $I_{OL}$=2.5mA | | | 0.4 | V |
| $V_{OH}$ | Do Terminal Output "High" Voltage | $I_{OH}$=-400µA | $V_{DD}$-0.4 | | | V |

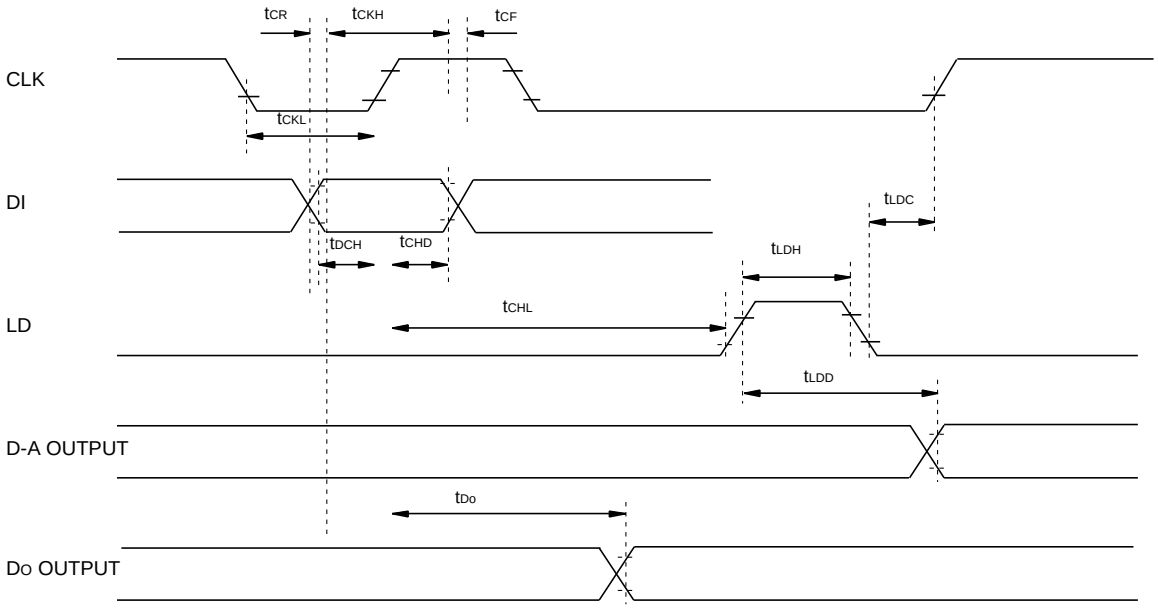
<Analog Part> ($V_{DD}$=5V±10%,$V_{DD}$≥$V_{IN}$,GND,$V_{DAref}$=0V,Ta=-20~85°C unless otherwise noted)

| SYMBOL | PARAMETER | MEASUREMENT CONDITION | LIMIT | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $I_{IN}$ | Input Current | $V_{IN}$=3V,$V_{DAref}$=0V,<br>*Proportional to max.<br>input current condition($V_{IN}$-$V_{DAref}$) and<br>digital data of each channels. | | | 0.18 | mA |
| $I_{DAref}$ | D-A Reference Input Current | $V_{IN}$=3V,$V_{DAref}$=0V,<br>*Proportional to max.<br>input current condition($V_{IN}$-$V_{DAref}$) and<br>digital data of each channels. | -1.44 | | | mA |
| RES | Resolution | $V_{DD}$=2.61V,$V_{DAref}$=0.050V(10mV/1LSB)<br>Without load(IAO=±0) | | 8 | | bit |
| DNL | Differential Nonlinearity | | -1 | | 1 | LSB |
| NL | Nonlinearity | | -1.5 | | 1.5 | LSB |
| $V_{AO}$ | Buffer Amplifier Output Voltage Range | $I_{AO}$=±100µA | 0.1 | | $V_{CC}$-0.1 | V |
| | | $I_{AO}$=±500µA | 0.2 | | $V_{CC}$-0.2 | |
| $I_{AO}$ | Buffer Amplifier Output Current Range | Upper Saturation Voltage=0.4V<br>Lower Saturation Voltage=0.4V | -1 | | 1 | mA |
| $C_O$ | Output Capacitative Load | | | | 0.1 | µ F |
| $R_O$ | Buffer Amplifier Output Impedance | | | 5 | | Ω |

<AC Characteristics> ($V_{DD}$=5V±10%,$V_{DD}$≥$V_{IN}$,GND,$V_{DAref}$=0V,Ta=-20~85°C, unless otherwise noted)

| SYMBOL | PARAMETER | MEASUREMENT CONDITION | LIMIT | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $t_{CKL}$ | Clock "L" Pulse Width | | 200 | | | nS |
| $t_{CKH}$ | Clock "H" Pulse Width | | 200 | | | nS |
| $t_{CR}$ | Clock Rise Time | | | | 200 | nS |
| $t_{CF}$ | Clock Fall Time | | | | | |
| $t_{DCH}$ | Data Set Up Time | | 60 | | | nS |
| $t_{CHD}$ | Data Hold Time | | 100 | | | nS |
| $t_{CHL}$ | LD Set Up Time | | 200 | | | nS |
| $t_{LDC}$ | LD Hold Time | | 100 | | | nS |
| $t_{LDH}$ | LD "H" Pulse Duration Time | | 100 | | | nS |
| $t_{Do}$ | Data Output Delay Time | $C_L$=100pF | 70 | | 350 | nS |
| $t_{LDD}$ | D-A Output Setting Time | $C_L$≤100pF,$V_{AO}$:0.1<=>2.6V This Time Until The Output Becomes The final Value Of 1/2 LSB | | | 300 | µS |

## TIMING CHART




⚠ Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable,but there is always the possibility that trouble may occur with them.Trouble with semiconductors may lead to personal injury, fire or property damage.Remember to give due consideration to safety when making your circuit design,in order to prevent fires from spreading,redundancy,malfunction or other mishap.