# PROGRAMMABLE SYNCHRONOUS DC/DC HYSTERETIC CONTROLLER FOR ADVANCED PROCESSORS



PRELIMINARY - March 1, 2000

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## DESCRIPTION

The SC1154 is a synchronous-buck switch-mode controller designed for use in single ended power supply applications where efficiency is the primary concern. The controller is a hysteretic type, with a user selectable hysteresis. The SC1154 is ideal for implementing DC/DC converters needed to power advanced microprocessors such as Pentium® II, in both single and multiple processor configurations. Inhibit, undervoltage lockout and soft-start functions are included for controlled power-up.

SC1154 features include an integrated 5 bit D/A converter, temperature compensated voltage reference, current limit comparator, over-current protection, and an adaptive deadtime circuit to prevent shoot-through of the power MOSFET during switching transitions. Power good signaling, logic compatible shutdown, and over-voltage protection are also provided. The integrated D/A converter provides programmability of output voltage from 2.0V to 3.5V in 100mV increments and 1.3V to 2.05V in 50mV increments with no external components.

The SC1154 high side driver can be configured as either a grounded reference or as a floating bootstrap driver. High and low side drivers have a peak current rating of 2 amps.

## FEATURES

- Programmable hysteresis
- 5 bit DAC programmable output (1.3V-3.5V)
- On-chip power good and OVP functions
- Designed to meet latest Intel specifications
- Up to 95% efficiency
- ±1% tolerance over temperature

## APPLICATIONS

- Server Systems and Workstations
- Pentium® II Core Supply
- Multiple Microprocessor Supplies
- Voltage Regulator Modules

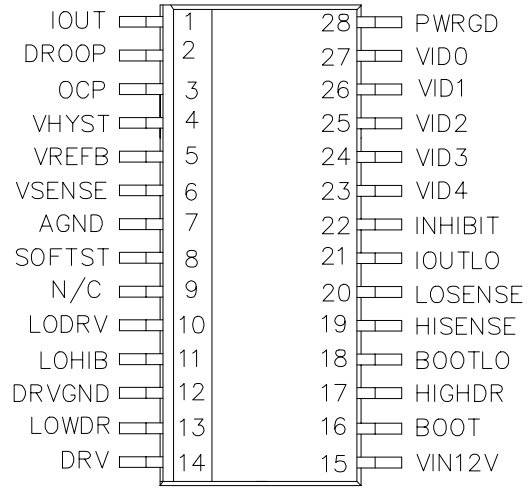
## ORDERING INFORMATION

| DEVICE(1) | PACKAGE | TEMP. RANGE ($T_J$) |
|---|---|---|
| SC1154CSW | SO-28 | 0 - 125°C |

Note:
(1) Add suffix 'TR' for tape and reel.

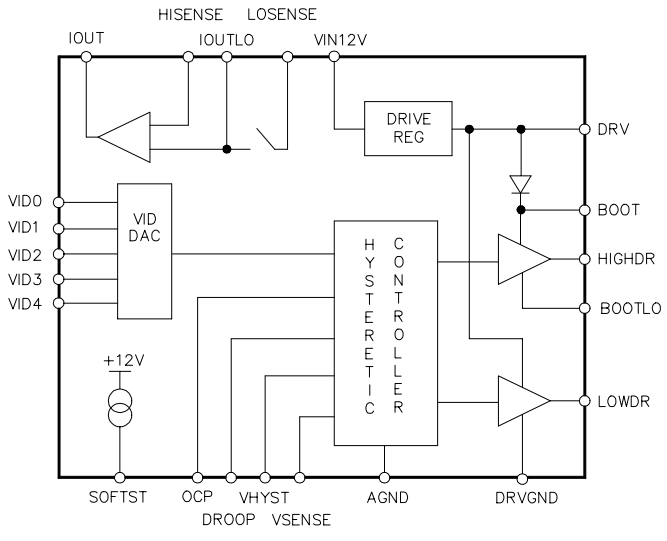
## PIN CONFIGURATION

Top View




(28-Pin SOIC)

## SIMPLIFIED BLOCK DIAGRAM







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## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Maximum | Units |
|---|---|---|---|
| VIN12V | $VIN_{MAX}$ | 14 | V |
| BOOT to DRVGND | | 25 | V |
| BOOT to BOOTLO | | 15 | V |
| Digital Inputs | | -0.3 to +7.3 | V |
| AGND to DRVGND | | ±0.5V | V |
| LOHIB to AGND | | 14 | V |
| LOSENSE to AGND | | 14 | V |
| IOUTLO to AGND | | 14 | V |
| HISENSE to AGND | | 14 | V |
| VSENSE to AGND | | 5 | V |
| Continuous Power Dissipation, $T_A = 25°C$ | $P_D$ | 1.2 | W |
| Continuous Power Dissipation, $T_C = 25°C$ | $P_D$ | 6.25 | W |
| Operating Junction Temperature | $T_J$ | 0 to +125 | ℃ |
| Lead Temperature (Soldering) 10 seconds | $T_L$ | 300 | ℃ |
| Storage Temperature | $T_{STG}$ | -65 to 150 | ℃ |

## PIN DESCRIPTION

| Pin | Pin Name | Pin Function |
|---|---|---|
| 1 | IOUT | Current Out. The output voltage on this pin is proportional to the load current as measured across the high side MOSFET, and is approximately equal to 2 x $R_{DS(ON)}$ x $I_{LOAD}$. |
| 2 | DROOP | Droop Voltage. This pin is used to set the amount of output voltage set-point droop as a function of load current. The voltage is set by a resistor divider between IOUT and AGND. |
| 3 | OCP | Over Current Protection. This pin is used to set the trip point for over current protection by a resistor divider between IOUT and AGND. |
| 4 | VHYST | Hysteresis Set Pin. This pin is used to set the amount of hysteresis required by a resistor divider between VREFB and AGND. |
| 5 | VREFB | Buffered Reference Voltage (from VID circuitry). |
| 6 | VSENSE | Output Voltage Sense. |
| 7 | AGND | Small Signal Analog and Digital Ground. |
| 8 | SOFTST | Soft Start. Connecting a capacitor from this pin to AGND sets the time delay. |
| 9 | NC | Not connected |
| 10 | LODRV | Low Drive Control. Connecting this pin to +5V enables normal operation. When LOHIB is grounded, this pin can be used to control LOWDR. |
| 11 | LOHIB | Low Side Inhibit. This pin is used to eliminate shoot-thru current. |
| 12 | DRVGND | Power Ground. |
| 13 | LOWDR | Low Side Driver Output. |
| 14 | DRV | Drive Regulator for the MOSFET Drivers. |
| 15 | VIN12V | 12V Supply. |
| 16 | BOOT | Bootstrap. This pin is used to generate a floating drive for the high side FET driver. |
| 17 | HIGHDR | High Side Driver Output. |
| 18 | BOOTLO | Bootstrap Low. In desktop applications, this pin connects to DRVGND. |
| 19 | HISENSE | High Current Sense. Connected to the drain of the high side FET, or the input side of a current sense resistor between the input and the high side FET. |
| 20 | LOSENSE | Low Current Sense. Connected to the source of the high side FET, or the FET side of a current sense resistor between the input and the high side FET. |
| 21 | IOUTLO | This is the sampling capacitors bottom leg. Voltage on this pin is voltage on the LOSENSE pin when the high side FET is on. |
| 22 | INHIBIT | Inhibit. If this pin is grounded, the MOSFET drivers are disabled. Usually connected to +5V through a pull-up resistor. |
| 23 | VID4(1) | Programming Input (MSB). |
| 24 | VID3(1) | Programming Input. |
| 25 | VID2(1) | Programming Input. |
| 26 | VID1(1) | Programming Input. |
| 27 | VID0(1) | Programming Input (LSB). |
| 28 | PWRGD(1) | Power Good. This open collector logic output is high if the output voltage is within 5% of the set point. |

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## ELECTRICAL CHARACTERISTICS

Unless specified: 0 < $T_J$ < 125°C, VIN = 12V

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage Range | VIN12V | | 11.4 | 12 | 13 | V |
| Supply Current (Quiescent) | $I_{IN}q$ | INH = 5V, VID not 11111, VIN above UVLO threshold during start-up, $f_{SW}$ = 200kHz, BOOTLO = 0V, $C_{DH}$ = $C_{DL}$ = 50pF | | 15 | | mA |
| High Side Driver Supply Current (Quiescent) | $I_{BOOT}q$ | INH = 0V or VID = 11111 or VIN below UVLO threshold during start-up, BOOT = 13V, BOOTLO = 0V | | | 10 | µA |
| | | INH = 5V, VID not 11111, VIN above UVLO threshold during start-up, $f_{SW}$ = 200kHz, BOOT = 13V, BOOTLO = 0V, $C_{DH}$ = 50pF | | 5 | | mA |
| **REFERENCE/VOLTAGE IDENTIFICATION** | | | | | | |
| Reference Voltage Accuracy | $V_{REF}$ | 11.4V < VIN12V < 12.6V, over full VID range (see Output Voltage Table) | -1 | | 1 | % |
| VID0 - VID4 High Threshold Voltage | $V_{TH(H)}$ | | 2.25 | | | V |
| VID0 - VID4 Low Threshold Voltage | $V_{TH(L)}$ | | | | 1 | V |
| **POWER GOOD** | | | | | | |
| Undervoltage Threshold | $V_{TH(PWRGD)}$ | | 90 | | 95 | % $V_{REF}$ |
| Output Saturation Voltage | $V_{SAT}$ | $I_O$ = 5mA | | 0.5 | | V |
| Hysteresis | $V_{HYS(PWRGD)}$ | | | 10 | | mV |
| **OVER VOLTAGE PROTECTION** | | | | | | |
| OVP Trip Point | $V_{OVP}$ | | 12 | 15 | 20 | %$V_{REF}$ |
| Hysteresis(1) | $V_{HYS(OVP)}$ | | | 10 | | mV |

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## ELECTRICAL CHARACTERISTICS (cont.)

Unless specified: 0 < $T_J$ < 125°C, VIN = 12V

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SOFT START** | | | | | | |
| Charge Current | $I_{CHG}$ | $V_{SS}$ = 0.5V, resistance from VREFB pin to AGND = 20kΩ, $V_{REFB}$ = 1.3V<br>Note: $I_{CHG}$ = ($I_{VREFB}$ / 5) | 10.4 | 13 | 15.6 | µA |
| Discharge Current | Idischg | $V_{(S/S)}$ = 1V | | 1 | | mA |
| **INHIBIT COMPARATOR** | | | | | | |
| Start Threshold | $Vstart_{INH}$ | | 1 | 2.0 | 2.4 | V |
| **VIN12V UVLO** | | | | | | |
| Start Threshold | $Vstart_{UVLO}$ | | 9.25 | 10 | 10.75 | V |
| Hysteresis | $Vhys_{UVLO}$ | | 1.8 | 2 | 2.2 | V |
| **HYSTERETIC COMPARATOR** | | | | | | |
| Input Offset Voltage | $Vos_{HYSCMP}$ | $V_{DROOP}$ pin grounded | | | 5 | mV |
| Input Bias Current | $Ibias_{HYSCMP}$ | | | | 1 | µA |
| Hysteresis Accuracy | $V_{HYS\_ACC}$ | | | | 7 | mV |
| Hysteresis Setting | $V_{HYS\_SET}$ | | | | 60 | mV |
| **DROOP COMPENSATION** | | | | | | |
| Initial Accuracy | $V_{DROOP\_ACC}$ | $V_{DROOP}$ = 50mV | | | 5 | mV |
| **OVERCURRENT PROTECTION** | | | | | | |
| OCP Trip Point | $V_{OCP}$ | | 0.09 | 0.1 | 0.11 | V |
| Input Bias Current | $Ibias_{OCP}$ | | | | 100 | nA |
| **HIGH-SIDE VDS SENSING** | | | | | | |
| Gain | | | | 2 | | V/V |
| Initial Accuracy | $V_{IOUT\_ACC}$ | $V_{HISENSE}$ = 12V, $V_{IOUTLO}$ = 11.9V | | | 6 | mV |
| IOUT Source | $Isource_{IOUT}$ | $V_{IOUT}$ = 0.5V, $V_{HISENSE}$ = 12V, $V_{IOUTLO}$ = 11.5V | 500 | | | µA |
| IOUT Sink Current | $Isink_{IOUT}$ | $V_{IOUT}$ = 0.05V, $V_{HISENSE}$ = 12V, $V_{IOUTLO}$ = 12V | 40 | 50 | | µA |
| Output Voltage Swing | | $V_{HISENSE}$ = 11V, $R_{IOUT}$ = 10k0hm | 0 | | 3.75 | V |

## ELECTRICAL CHARACTERISTICS (cont.)

Unless specified: 0 < $T_J$ < 125°C, VIN12V = 12V

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **HIGH-SIDE VDS SENSING (cont.)** | | | | | | |
| | | $V_{HISENSE}$ = 4.5V, $R_{IOUT}$ = 10kOhm | 0 | | 2.0 | V |
| | | $V_{HISENSE}$ = 3V, $R_{IOUT}$ = 10kOhm | 0 | | 1.0 | V |
| LOSENSE High Level Input Voltage | $Vih_{LOSENSE}$ | $V_{HISENSE}$ = 4.5V (Note 1) | 2.85 | | | V |
| LOSENSE Low Level Input Voltage | $Vil_{LOSENSE}$ | $V_{HISENSE}$ = 4.5V (Note 1) | | | 1.8 | V |
| Sample/Hold Resistance | $R_{S/H}$ | 4.5V < = 13V | 50 | 65 | 80 | Ω |
| **BUFFERED REFERENCE** | | | | | | |
| VREFB Load Regulation | $Vldreg_{REFB}$ | 10µA < $I_{REFB}$ < 500µA | | 2 | | mV |
| **DEADTIME CIRCUIT** | | | | | | |
| LOHIB High Level Voltage | $Vih_{LOHIB}$ | | 2 | | | V |
| LOHIB Low Level Input Voltage | $Vil_{LOHIB}$ | | | | 1.0 | V |
| LOWDR High Level Input Voltage | $Vih_{LOWDR}$ | (Note 1) | 2 | | | V |
| LOWDR Low Level Input Voltage | $Vil_{LOWDR}$ | (Note 1) | | | 1.0 | V |
| **DRIVE REGULATOR** | | | | | | |
| Output Voltage | $V_{DRV}$ | 11.4 < VIN12V < 12.6V, $I_{DRV}$ = 50mA | 7 | | 9 | V |
| Load Regulation | $Vldreg_{DRV}$ | 1mA < $I_{DRV}$ < 50mA | | 100 | | mV |
| Short Circuit Current | $Ishort_{DRV}$ | | 100 | | | mA |
| **HIGH-SIDE OUTPUT DRIVER** | | | | | | |
| Peak Output Current | $Isrc_{HIGHDR}$, $Isink_{HIGHDR}$ | duty cycle < 2%, tpw < 100us, $T_J$ = 125°C $V_{BOOT}$ - $V_{BOOTLO}$ = 6.5V, $V_{HIGHDR}$ = 1.5V (src), or $V_{HIGHDR}$ = 5V (sink) (Note 1) | 2 | | | A |

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## ELECTRICAL CHARACTERISTICS (cont.)

Unless specified: 0 < $T_J$ < 125°C, VIN12V = 12V

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **HIGH-SIDE OUTPUT DRIVER (cont.)** | | | | | | |
| Output Resistance | $Rsrc_{HIGHDR'}$ | $T_J$ = 125°C<br>$V_{BOOT}$ - $V_{BOOTLO}$ = 6.5V,<br>$V_{HIGHDR}$ = 6V | | | 45 | Ω |
| | $Rsink_{HIGHDR}$ | $T_J$ = 125°C<br>$V_{BOOT}$ - $V_{BOOTLO}$ = 6.5V,<br>$V_{HIGHDR}$ = 0.5V | | | 5 | |
| **LOW-SIDE OUTPUT DRIVER** | | | | | | |
| Peak Outout Current | $Isrc_{LOWDR'}$<br>$Isink_{LOWDR}$ | duty cycle < 2%, tpw < 100us,<br>$T_J$ = 125°C<br>$V_{DRV}$ = 6.5V, $V_{LOWDR}$ = 1.5V (src), or $V_{LOWDR}$ = 5V (sink)<br>(Note 1) | 2 | | | A |
| Output Resistance | $Rsrc_{LOWDR'}$ | $T_J$ = 125°C<br>$V_{DRV}$ = 6.5V, $V_{LOWDR}$ = 6V | | | 45 | Ω |
| | $Rsink_{LOWDR}$ | $T_J$ = 125°C<br>$V_{DRV}$ = 6.5V, $V_{LOWDR}$ = 0.5V | | | 5 | |
| **HYSTERETIC COMPARATORS**(1) | | | | | | |
| Propagation Delay Time from VSENSE to HIGHDR or LOWDR (excluding deadtime) | $t_{HCPROP}$ | 10mV overdrive,<br>1.3V ≤ Vref ≤ 3.5V | | 150 | 250 | ns |
| **OUTPUT DRIVERS** | | | | | | |
| HIGHDR rise/fall time | $tr_{HIGHDR}$<br>$tf_{HIGHDR}$ | Cl = 9nF, $V_{BOOT}$ = 6.5v,<br>$V_{BOOTLO}$ = grounded,<br>$T_J$ = 125 °C | | | 60 | ns |
| LOWDR rise/fall time | $tr_{LOWDR}$ ,<br>$tf_{LOWDR}$ | Cl = 9nF, $V_{DRV}$ = 6.5v,<br>$T_J$ = 125 °C | | | 60 | ns |
| **OVERCURRENT PROTECTION**(1) | | | | | | |
| Comparator Propagation Delay Time | $t_{OCPROP}$ | | | 1 | | µs |
| Deglitch Time | $t_{OCDGL}$ | | 1 | | 3 | µs |
| **OVERVOLTAGE PROTECTION** | | | | | | |
| Comparator Propagation Delay Time | $t_{OVPROP}$ | | | 1 | | µs |
| Deglitch Time | $t_{OVDGL}$ | | 1 | | 3 | µs |

## ELECTRICAL CHARACTERISTICS (cont.)

Unless specified: 0 < $T_J$ < 125° C, VIN12V = 12V

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **HIGH-SIDE Vds SENSING(1)** | | | | | | |
| Response Time | $t_{VDSRESP}$ | $V_{HISENSE}$ = 12v, $V_{IOUTLO}$ pulsed from 12v to 11.9v, 100ns rise and fall times | | | 2 | µs |
| | | $V_{HISENSE}$ = 4.5v, $V_{IOUTLO}$ pulsed from 4.5v to 4.4v, 100ns rise and fall times | | | 3 | µs |
| | | $V_{HISENSE}$ = 3v, $V_{IOUTLO}$ pulsed from 3.0v to 2.9v, 100ns rise and fall times | | | 3 | µs |
| Short Circuit Protection Rising Edge Delay | $t_{VDSRED}$ | LOSENSE grounded | 300 | | 500 | ns |
| Sample/Hold Switch turn-on/turn-off Delay | $t_{SWXDLY}$ | 3v < $V_{HISENSE}$ < 11v<br>$V_{LOSENSE}$ = $V_{HISENSE}$ | 30 | | 100 | ns |
| **POWER GOOD** | | | | | | |
| Comparator Propagation Delay | $t_{PWRGD}$ | | | 1 | | µs |
| **SOFTSTART** | | | | | | |
| Comparator Propagation Delay | $t_{SLST}$ | overdrive = 10mv | | 560 | 900 | ns |
| **DEADTIME** | | | | | | |
| Driver Nonoverlap Time | $t_{NUL}$ | | 30 | | 100 | ns |

Note 1: Guaranteed, but not tested

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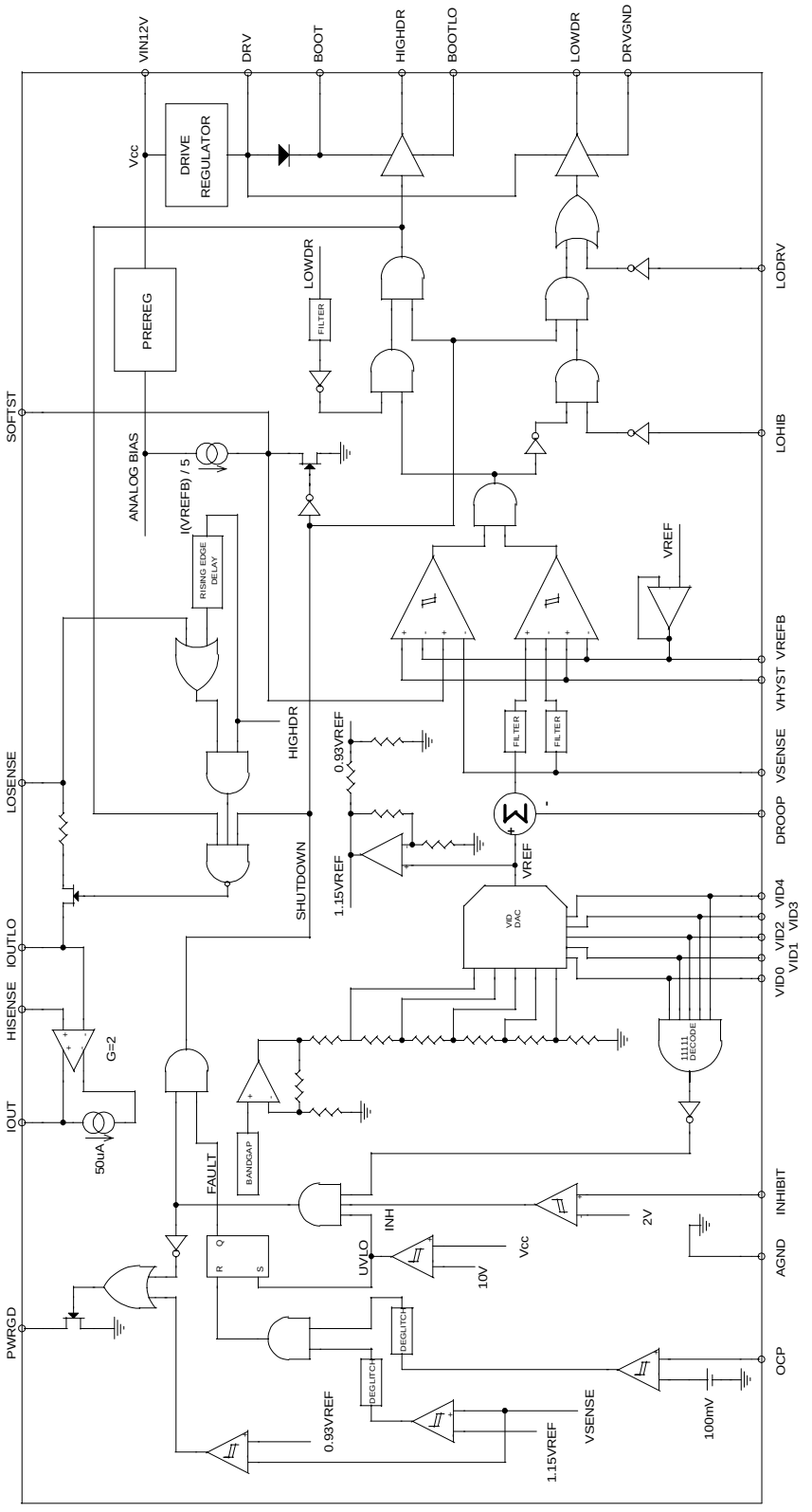
## BLOCK DIAGRAM



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## OUTPUT VOLTAGE TABLE

0 = GND; 1 = Floating or +5V pull-up

| VID4 | VID3 | VID2 | VID1 | VID0 | VDC (V) |
|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1.30 |
| 0 | 1 | 1 | 1 | 0 | 1.35 |
| 0 | 1 | 1 | 0 | 1 | 1.40 |
| 0 | 1 | 1 | 0 | 0 | 1.45 |
| 0 | 1 | 0 | 1 | 1 | 1.50 |
| 0 | 1 | 0 | 1 | 0 | 1.55 |
| 0 | 1 | 0 | 0 | 1 | 1.60 |
| 0 | 1 | 0 | 0 | 0 | 1.65 |
| 0 | 0 | 1 | 1 | 1 | 1.70 |
| 0 | 0 | 1 | 1 | 0 | 1.75 |
| 0 | 0 | 1 | 0 | 1 | 1.80 |
| 0 | 0 | 1 | 0 | 0 | 1.85 |
| 0 | 0 | 0 | 1 | 1 | 1.90 |
| 0 | 0 | 0 | 1 | 0 | 1.95 |
| 0 | 0 | 0 | 0 | 1 | 2.00 |
| 0 | 0 | 0 | 0 | 0 | 2.05 |
| 1 | 1 | 1 | 1 | 1 | NO CPU |
| 1 | 1 | 1 | 1 | 0 | 2.10 |
| 1 | 1 | 1 | 0 | 1 | 2.20 |
| 1 | 1 | 1 | 0 | 0 | 2.30 |
| 1 | 1 | 0 | 1 | 1 | 2.40 |
| 1 | 1 | 0 | 1 | 0 | 2.50 |
| 1 | 1 | 0 | 0 | 1 | 2.60 |
| 1 | 1 | 0 | 0 | 0 | 2.70 |
| 1 | 0 | 1 | 1 | 1 | 2.80 |
| 1 | 0 | 1 | 1 | 0 | 2.90 |
| 1 | 0 | 1 | 0 | 1 | 3.00 |
| 1 | 0 | 1 | 0 | 0 | 3.10 |
| 1 | 0 | 0 | 1 | 1 | 3.20 |
| 1 | 0 | 0 | 1 | 0 | 3.30 |
| 1 | 0 | 0 | 0 | 1 | 3.40 |
| 1 | 0 | 0 | 0 | 0 | 3.50 |

**NOTE:**
(1) If the VID bits are set to 11111, then the high-side and the low-side driver outputs will be set low, and the controller will be set to a low-Iq state.

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## FUNCTIONAL DESCRIPTION

### Reference/Voltage Identification

The reference/voltage identification (VID) section consists of a temperature compensated bandgap reference and a 5-bit voltage selection network. The 5 VID pins are TTL compatable inputs to the VID selection network. They are internally pulled up to +5V generated from the +12V supply by a resistor divider, and provide programmability of output voltage from 2.0V to 3.5V in 100mV increments and 1.3V to 2.05V in 50mV increments.
Refer to the Output Voltage Table for the VID code settings. The output voltage of the VID network, VREF is within 1% of the nominal setting over the full input and output voltage range and junction temperature range. The output of the reference/VID network is indirectly brought out through a buffer to the REFB pin. The voltage on this pin will be within 3mV of VREF. It is not recommended to drive loads with REFB other than setting the hysteresis of the hysteretic comparator, because the current drawn from REFB sets the charging current for the soft start capacitor. Refer to the soft start section for additional information.

### Hysteretic Comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by connecting the center point of a resistor divider from REFB to AGND to the HYST pin. The hysteresis of the comparator will be equal to twice the voltage difference between REFB and HYST, and has a maximum value of 60mV. The maximum propagation delay from the comparator inputs to the driver outputs is 250ns.

### Low Side Driver

The low side driver is designed to drive a low $R_{DS(ON)}$ N-channel MOSFET, and is rated for 2 amps source and sink. The bias for the low side driver is provided internally from VDRV.

### High Side Driver

The high side driver is designed to drive a low $R_{DS(ON)}$ N-channel MOSFET, and is rated for 2 amps source and sink. It can be configured either as a ground referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from the DRV regulator. The internal bootstrap diode, connected between the DRV and BOOT pins, is a Schottky for improved drive efficiency. The maximum voltage that can be applied between the BOOT pin and ground is 25V. The driver can be referenced to ground by connecting BOOTLO to PGND, and connecting +12V to the BOOT pin.

### Deadtime Control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turn-on times of the FET drivers. The high side driver is not allowed to turn on until the gate drive voltage to the low-side FET is below 2 volts, and the low side driver is not allowed to turn on until the voltage at the junction of the 2 FETs (VPHASE) is below 2 volts. An internal low-pass filter with an 11MHz pole is located between the output of the low-side driver (DL) and the input of the deadtime circuit that controls the high-side driver, to filter out noise that could appear on DL when the high-side driver turns on.

### Current Sensing

Current sensing is achieved by sampling and holding the voltage across the high side FET while it is turned on. The sampling network consists of an internal 50Ω switch and an external 0.1µF hold capacitor. Internal logic controls the turn-on and turn-off of the sample/hold switch such that the switch does not turn on until VPHASE transitions high and turns off when the input to the high side driver goes low. Thus sampling will occur only when the high side FET is conducting current. The voltage at the IO pin equals 2 times the sensed voltage. In applications where a higher accuracy in current sensing is required, a sense resistor can be placed in series with the high side FET and the voltage across the sense resistor can be sampled by the current sensing circuit.

### Droop Compensation

The droop compensation network reduces the load transient overshoot/undershoot at VOUT, relative to VREF. VOUT is programmed to a voltage greater than VREF (equal to VREF x (1+R5/R6)) by an external resistor divider from VOUT to the VSENSE pin to reduce the undershoot on VOUT during a low to high load current transient. The overshoot during a high to low load current transient is reduced by subtracting the voltage that is on the DROOP pin from VREF. The voltage on the IO pin is divided down with an external

## FUNCTIONAL DESCRIPTION (cont.)

resistor divider, and connected to the DROOP pin. Thus, under loaded conditions, VOUT is regulated to Vout = Vref • (1+R7/R8) - IOUT • R2/(R1+R2).

### Inhibit

The inhibit pin is a TTL compatible digital pin that is used to enable the controller. When INH is low, the output drivers are low, the soft start capacitor is discharged, the soft start current source is disabled, and the controller is in a low $I_Q$ state. When INH goes high, the short across the soft start capacitor is removed, the soft start current source is enabled, and normal converter operation begins. When the system logic supply is connected to INH, it controls power sequencing by locking out controller operation until the system logic supply exceeds the input threshold voltage of the INH circuit; thus the +12V supply and the system logic supply (either +5V or 3.3V) must be above UVLO thresholds before the controller is allowed to start up.

### VIN

The VIN undervoltage lockout circuit disables the controller while the +12V supply is below the 10V start threshold during power-up. While the controller is disabled, the output drivers will be low, the soft start capacitor will be shorted and the soft start current is disabled and the controller will be in a low $I_Q$ state. When VIN exceeds the start threshold, the short across the soft start capacitor is removed, the soft start current source is enabled and normal converter operation begins. There is a 2V hysteresis in the undervoltage lockout circuit for noise immunity.

### Soft Start

The soft start circuit controls the rate at which VOUT powers up. A capacitor is connected between SS and AGND and is charged by an internal current source. The value of the current source is proportional to the reference voltage so the charging rate of $C_{SS}$ is also proportional to the reference voltage. By making the charging current proportional to VREF, the power-up time for VOUT will be independent of VREF. Thus, $C_{SS}$ can remain the same value for all VID settings. The soft start charging current is determined by the following equation: $I_{SS} = I_{REFB}/5$. Where $I_{REFB}$ is the current flowing out of the REFB pin. It is recommended that no additional loads be connected to REFB, other than the resistor divider for setting the hysteresis voltage. Thus these resistor values will determine the soft start charging current. The maximum current that can be sourced by REFB is 500µA.

### Power Good

The power good circuit monitors for an undervoltage condition on VOUT. If VSENSE is 7% (nominal) below VREF, then the power good pin is pulled low. The PWRGD pin is an open drain output.

### Overvoltage Protection

The overvoltage protection circuit monitors VOUT for an overvoltage condition. If VSENSE is 15% above VREF, than a fault latch is set and both output drivers are turned off. The latch will remain set until VIN goes below the undervoltage lockout value. A 1ms deglitch timer is included for noise immunity.

### Overcurrent Protection

The overcurrent protection circuit monitors the current through the high side FET. The overcurrent threshold is adjustable with an external resistor divider between IO and AGND, with the divider voltage connected to the OCP pin. If the voltage on the OCP pin exceeds 100mV, then a fault latch is set and the output drivers are turned off. The latch will remain set until VIN goes below the undervoltage lockout value. A 1ms deglitch timer is included for noise immunity. The OCP circuit is also designed to protect the high side FET against a short-to-ground fault on the terminal common to both power FETs (VPHASE).

### Drive Regulator

The drive regulator provides drive voltage to the low side driver, and to the high side driver when the high side driver is configured as a floating driver. The minimum drive voltage is 7V. The minimum short circuit current is 100mA.

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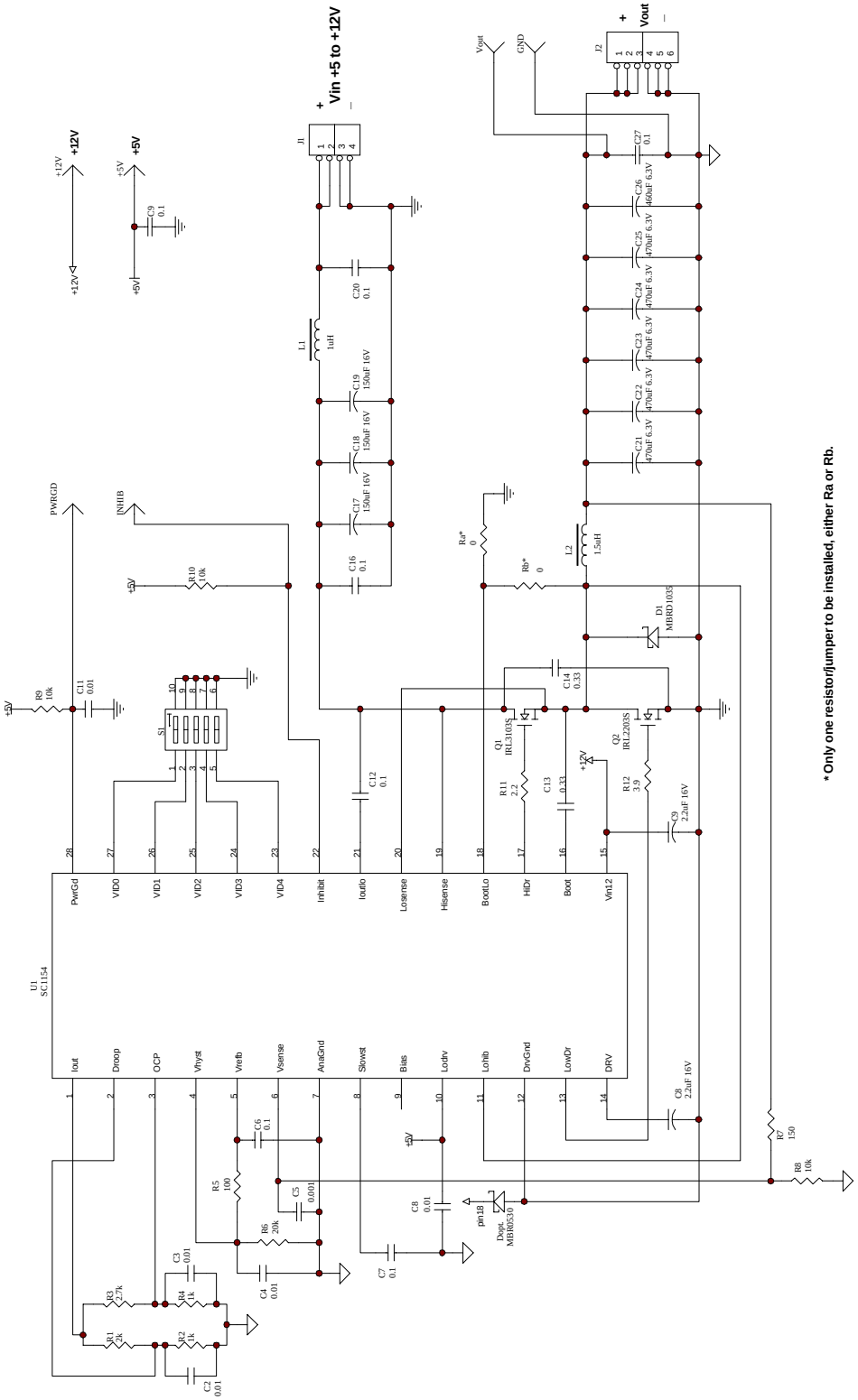
## APPLICATION CIRCUIT



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**MATERIALS LIST**

| Quantity | Reference | Part/Description | Vendor | Notes |
|---|---|---|---|---|
| 1 | C5 | 0.001µF | | |
| 6 | C1-C4, C8, C11 | 0.01µF | | |
| 3 | C17-C19 | 150µF, 16V (TPS) | AVX | |
| 7 | C6,C7,C9,C12,C16,C20, C27 | 0.1µF | | |
| 2 | C13,C14 | 0.33µF | | |
| 6 | C21-C26 | 470µF, 6.3V (TPS) | AVX | |
| 2 | C10,C15 | 2.2µF, 16V | | |
| 1 | D1 | MBRD1035 | MOT | |
| 1 | L1 | 1µH, DO5022P-102 | Coilcraft | |
| 1 | L2 | 1.5µH, DO5022P-152HC | Coilcraft | |
| 1 | Q1 | IRL3103NS, D2PAK | Int. Rect. | |
| 1 | Q2 | IRL2203NS, D2PAK | Int. Rect. | |
| 2 | RA,RB | 0Ω | | |
| 1 | R1 | 2K | | |
| 2 | R2,R4 | 1K | | |
| 1 | R3 | 2.7K | | |
| 1 | R5 | 100 | | |
| 1 | R6 | 20K | | |
| 1 | R7 | 150 | | |
| 3 | R8,R9,R10 | 10K | | |
| 1 | R11 | 2.2 | | |
| 1 | R12 | 3.9 | | |
| 1 | U1 | SC1154, SO-28 | SEMTECH | |

**Layout guidelines**

1. Locate R8 and C5 close to pins 6 and 7.
2. Locate C6 close to pins 5 and 7.
3. Components connected to IOUT, DROOP, OCP, VHYST, VREFB, VSENSE, and SOFTST should be referenced to AGND.
4. The bypass capacitors C10 and C15 should be placed close to the IC and referenced to DRVGND.
5. Locate bootstrap capacitor C13 close to the IC.
6. Place bypass capacitor C14 close to Drain of the top FET and Source of the bottom FET to be effective.
7. Route HISENSE and LOSENSE close to each other to minimize induced differential mode noise.
8. Bypass a high frequency disturbance with ceramic capacitor at the point where HISENSE is connected to Vin.
9. Input bulk capacitors should placed as close as possible to the power FETs because of the very high ripple current flow in this pass.
10. If Schottky diode used in parallel with a synchronous (bottom) FET, to achieve a greater efficiency at lower Vout settings, it needs to be placed next to the aforementioned FET in very close proximity.
11. Since the feedback path relies on the accurate sampling of the output ripple voltage, the best results can be achieved by connecting the AGND to the ground side of the bulk output capacitors.
12. DRVGND pin should be tight to the main ground plane utilizing very low impedance connection, e.g., multiple vias.
13. In order to prevent substrate glitching, a small (0.5A) Schottky diode should be placed in close proximity to the chip with the cathode connected to BOOTLO and anode connected to DRVGND.

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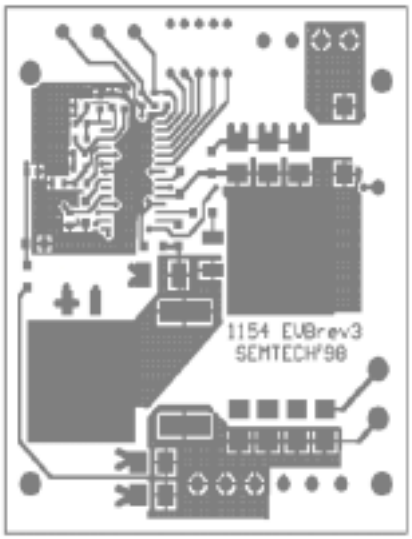
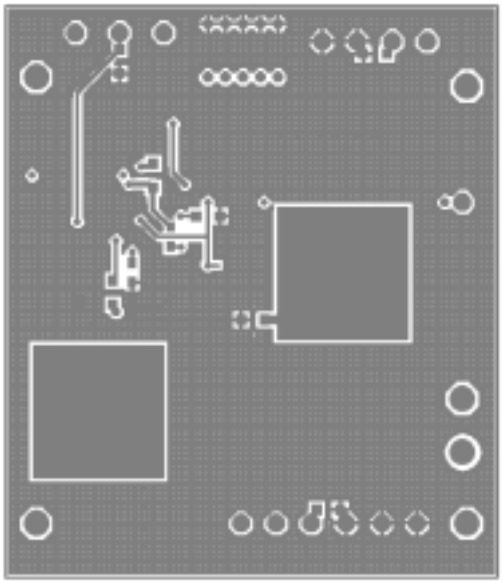
## EVALUATION BOARD ARTWORK




**TOP LAYER**



**BOTTOM LAYER**

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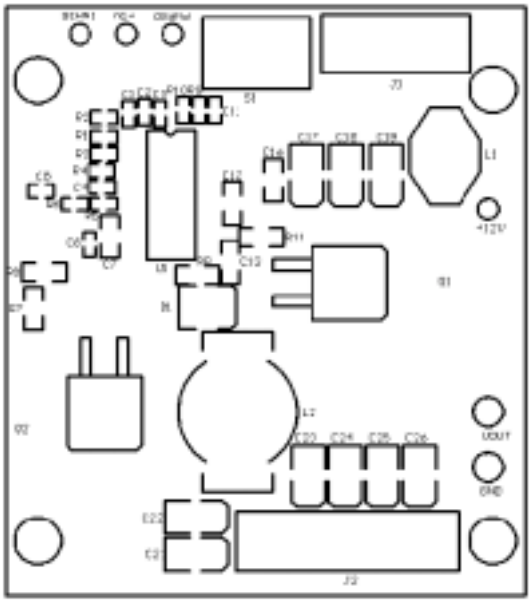
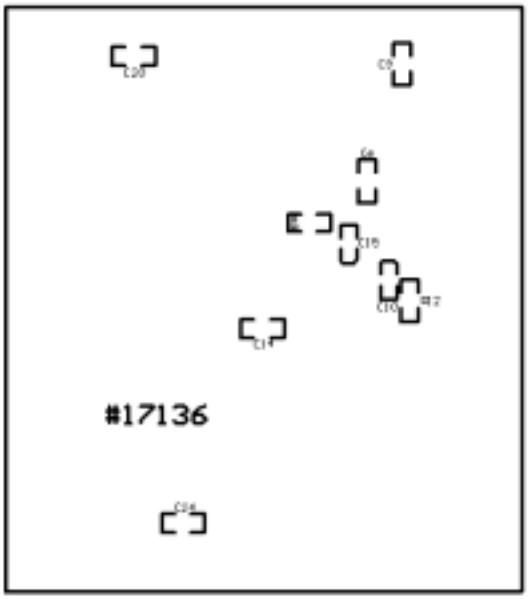
## EVALUATION BOARD LAYOUT



**TOP VIEW**




**BOTTOM VIEW**

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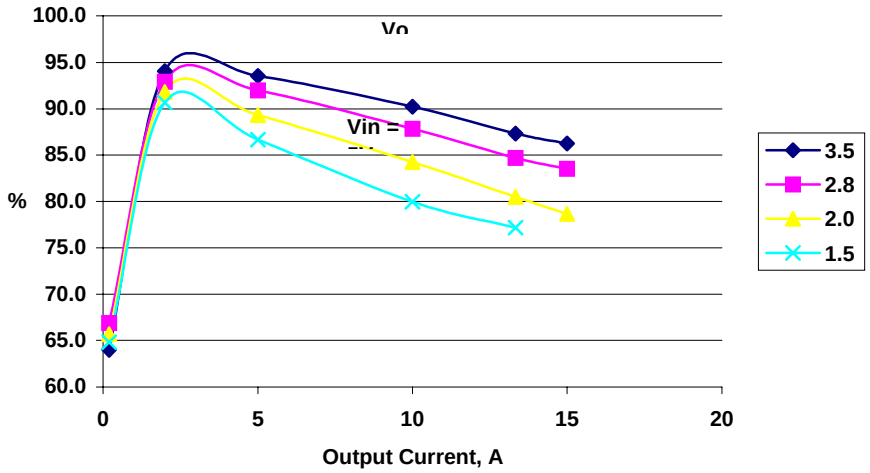
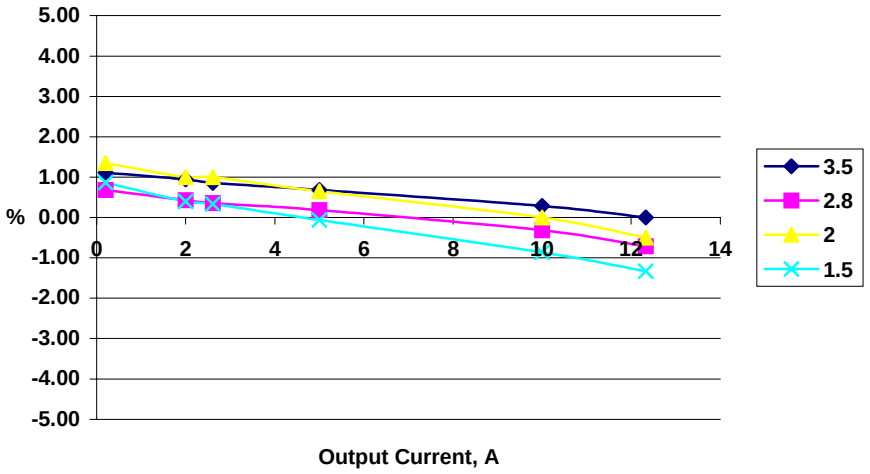
## TEST DATA

### SC1154 Efficiency




### SC1154 Voltage Regulation



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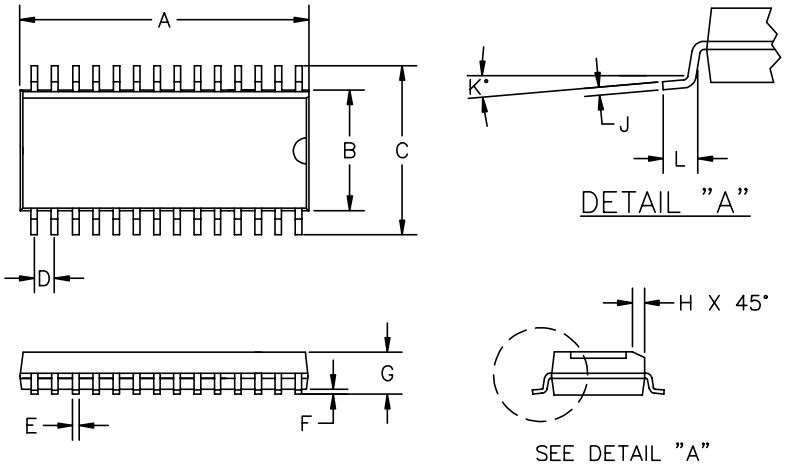
## OUTLINE - SO-28




| DIMENSIONS [1] | | | | | |
|---|---|---|---|---|---|
| DIM | INCHES | | MM | | NOTE |
| | MIN | MAX | MIN | MAX | |
| A | .6985 | .7141 | 17.73 | 18.13 | [2] |
| B | .2914 | .2992 | 7.40 | 7.60 | [2] |
| C | .394 | .419 | 10.00 | 10.64 | – |
| D | .050 | BSC | 1.27 | BSC | – |
| E | .013 | .020 | .33 | .51 | – |
| F | .004 | 0.118 | .10 | .30 | – |
| G | .0926 | .1043 | 2.35 | 2.64 | – |
| H | .010 | .029 | .25 | .74 | – |
| J | .0091 | .0125 | .23 | .32 | – |
| K | 0° | 8° | 0° | 8° | – |
| L | .016 | .050 | .41 | 1.27 | – |

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS
[1] CONTROLLING DIMENSION : MILLIMETERS.

ECN00-904