SAA7131E

Global standard low-IF demodulator and PCI audio and video decoder for analog TV

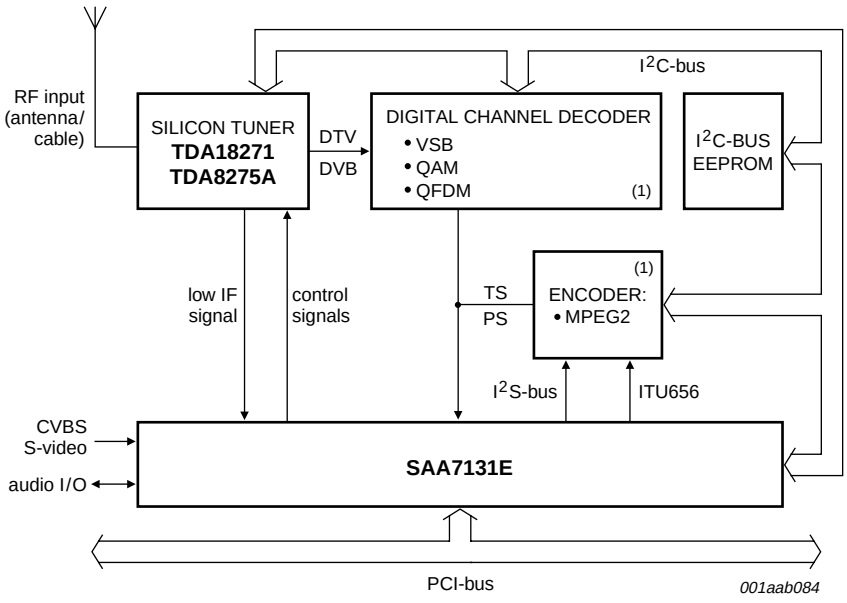
Rev. 03 — 19 May 2008 **Product data sheet**

1. General description

The SAA7131E combines a digital global standard low-IF demodulator for analog TV with a PCI audio and video decoder.

The IF demodulator is an alignment-free digital multistandard vision and sound low-IF signal PLL demodulator for positive and negative video modulation. It can be used worldwide for M/N, B/G/H, I, D/K and L/L' standards. The IF demodulator is especially suited for the application with the TV Silicon Tuner TDA18271, TDA8275A or equivalent IC.

The PCI audio and video broadcast decoder is a highly integrated, low-cost and solid foundation for TV capture in the PC, for analog TV and digital video broadcast (DTV and DVB). The various multimedia data types are transported over the PCI-bus by bus master-write, to best exploit the streaming capabilities of a modern host based system; see Figure 1.



(1) Alternative.

Fig 1. Application diagram for capturing live TV video and audio streams in the PC

2. Features

2.1 Generic properties

- Package: LBGA256
- Power supply: 3.3 V/1.8 V
- Power consumption of typical application: 1.35 W
- Meets requirements of *PC Design Guides 98/99 and 2001*
- Is compliant with *PCI Specification 2.2* and Advanced Configuration
- *PCI-bus Power Management Interface Specification, rev. 1.1*, compliant (supported states: D0, D1, D2 and D3-hot)
- Reference designs available

2.2 Digital global standard low-IF demodulator for analog TV

- Digital IF demodulation for all analog TV standards worldwide (M/N, B/G/H, D/K, I and L/L' standards)
- Multistandard true synchronous demodulation with active carrier regeneration
- Gated IF AGC acting on black level by using H/V PLL
- Composite Video Blanking Sync (CVBS) gain levelling stage to provide nearly constant signal amplitude
- Precise AFC/lock detector
- 16 MHz reference frequency input (from low-IF tuner) or operating as crystal oscillator
- High selectivity video low-pass filter for all standards
- Sound performance comparable to or better than QSS single reference concepts
- Alignment free
- Nyquist filter in video baseband
- Switchable IF PLL and IF AGC loop bandwidth
- Accurate group delay equalization for all standards
- Mostly digital FIR filter implementation (NSC notches, video low-pass filters)
- No SAW filter needed
- Especially suited for the Silicon Tuner TDA18271
- Low application effort and external component count in combination with the TDA18271
- Very robust IF demodulator coping with adverse field conditions
- High pull-in range
- CVBS and SSIF (Second Sound IF)/audio output with simple post filter (capacitor only)
- Excellent FM sound
- Acceptable AM sound
- High FM deviation mode for China
- Low video into sound crosstalk
- Auto or forced mute for sound
- Auto or forced blank for video
- One 10-bit IF ADC on-chip
- Two 10-bit DACs on-chip for CVBS and SSIF/audio
- Internal PLL synthesizer which permits to use a low-cost crystal (typically 16 MHz)

- Easy programming for I^2C-bus
- High flexibility through expert mode
- I^2C-bus interface and I^2C-bus switch
- Four I^2C-bus addresses selectable through 2 external pins
- Three general purpose input/output pins
- Separate Standby mode.

2.3 TV video decoder and video scaling

- All standards TV decoder: NTSC, PAL and SECAM
- Five analog video inputs: CVBS and S-video
- Video digitizing by two 9-bit ADCs at 27 MHz
- Sampling according ITU-R *BT.601* with 720 pixel/line
- Adaptive comb filter for NTSC and PAL, also operates for non-standard signals
- Automatic TV standard detection
- Three-level Macrovision copy protection detection according to *Macrovision detect specification Rev.1*
- Control of brightness, contrast, saturation and hue
- Versatile filter bandwidth selection
- Horizontal and vertical downscaling or zoom
- Adaptive anti-alias filtering
- Capture of raw VBI samples
- Two alternating settings for active video scaling, e.g. for independent capturing and preview definition
- Output in YUV or RGB
- Gamma compensation and black stretching.

2.4 TV sound decoder and TV audio I/O

- All standards TV sound decoder: BTSC, EIAJ, NICAM, FM A2 and AM
- dbx-TV noise reduction decoding for BTSC systems
- FM radio stereo decoding
- Input of analog SIF signal and 8-bit ADC at 24.576 MHz
- Automatic sound standard detection
- Automatic dematrixing (stereo and dual)
- Volume, balance, bass and treble control
- Automatic Volume Levelling (AVL)
- Incredible Mono and Incredible Stereo
- Audio sampling clock can be locked to video frame rate (no drift of audio stream against video stream)
- Four analog audio baseband inputs (two stereo pairs) and on-chip stereo ADCs
- Supported audio sampling rates: 32 kHz, 44.1 kHz and 48 kHz
- Input of external audio reference clock, e.g. 24.576 MHz
- Output of audio master clock ($768 \times f_s$, $512 \times f_s$, $384 \times f_s$ or $256 \times f_s$ selectable).

2.5 PCI and DMA bus mastering

- PCI 2.2 compliant including full Advanced Configuration and Power Interface (ACPI)
- 3.3 V and 5 V compliant
- System vendor ID, etc. through I^2C-bus EEPROM
- DMA bus master-write for video, audio, VBI and TS or PS
- Configurable PCI FIFOs, graceful overflow recovery
- Packed and planar video formats, overlay clipping
- Hardware support for virtual addressing by Memory Management Unit (MMU).

2.6 Peripheral interface

- I^2C-bus master interface: 3.3 V and 5 V compatible, 100 kHz and 400 kHz mode
- The device can operate without the PCI-bus (using I^2C-bus) for stand-alone applications, application note available
- Digital video output: ITU, VIP, VMI and ZV formats
- Two digital audio outputs: I^2S-bus for up to 4 channels
- Analog stereo audio output
- Integrated analog audio pass-through
- Support for analog audio loopback cable to sound card
- TS input: serial or parallel
- MPEG elementary or program stream input, parallel
- General purpose I/O, e.g. for strapping and interrupt
- Propagate reset and ACPI state D3.

3. Applications

- Desktop and portable PCs
- Hybrid cable, terrestrial and satellite set-top boxes
- PCTV
- Digital television
- Personal Video Recorders (PVR)
- Digital Video Recorders (DVR)
- DVD players and recorders
- VCRs
- PCI satellite modem
- PCI cable modem
- Video conferencing
- Analog and digital video editing
- Data broadcast receiver
- Media hub for home server.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SAA7131E	LBGA256	plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2

5. Block diagram

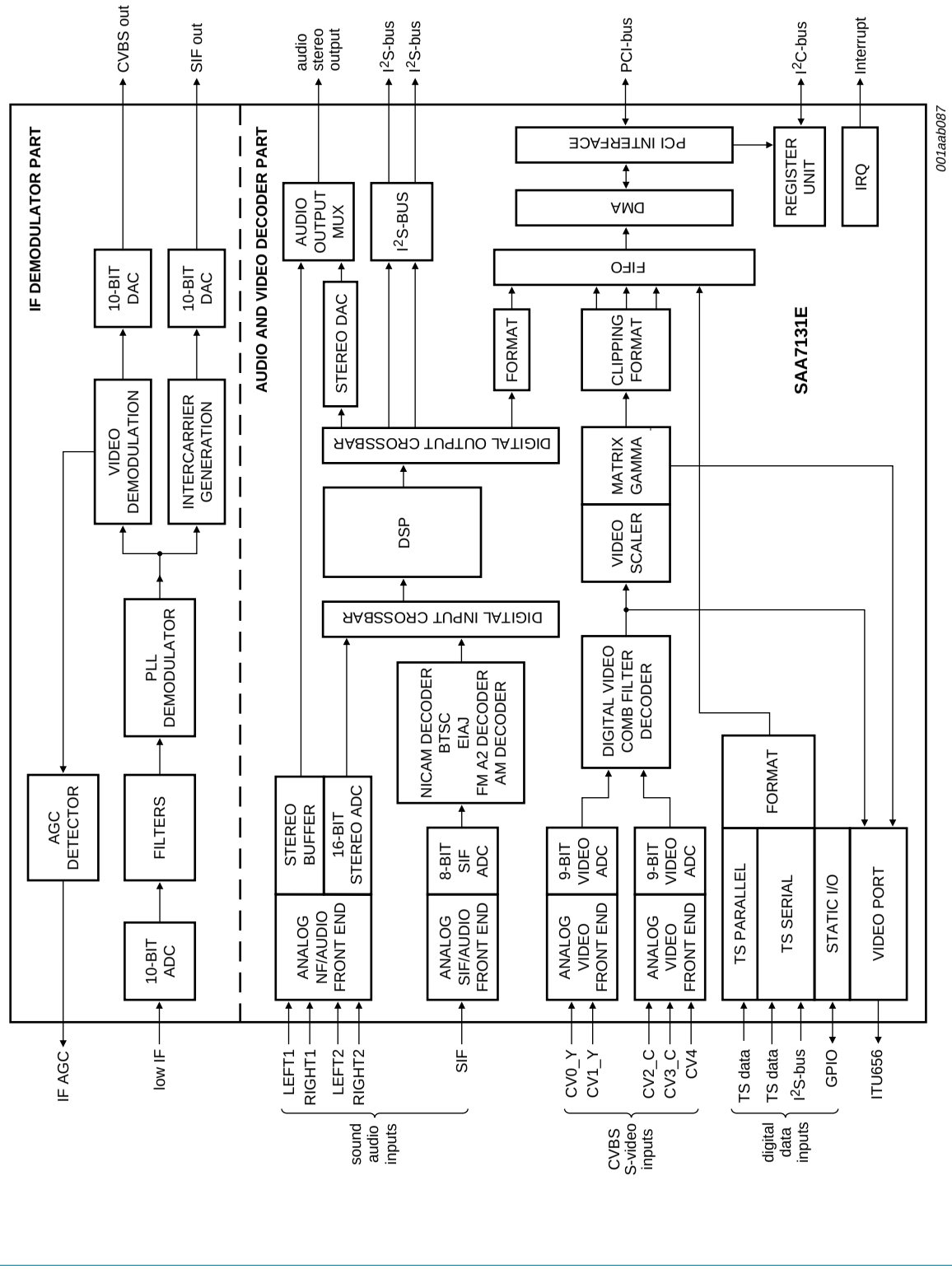


Fig 2. Block diagram

6. Pinning information

6.1 Pinning

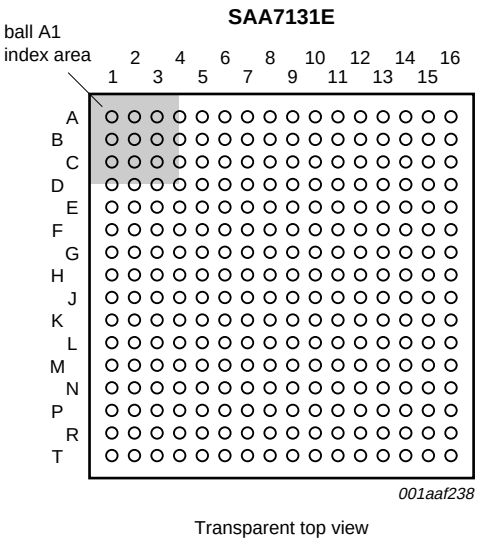


Fig 3. Pin configuration LBGA256 (SOT740-2)

Table 2. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	TESTMODE	2	V_{SSA1}	3	XTALII	4	XTALOI
5	V_{SSA1}	6	RST_N	7	IF_AGC	8	V_SYNC
9	SCL_O	10	SDA_O	11	SCLI	12	GPIO25
13	GPIO26	14	GPIO27	15	GPIO0	16	GPIO1
Row B							
1	V_{SSA2}	2	V_{SSA2}	3	V_{DDA1}	4	V_{DDD2}
5	V_{DDD2}	6	TDII	7	TDOI	8	TMSI
9	TCKI	10	TRSTI_N	11	SDAI	12	SCLD
13	GPIO2	14	GPIO3	15	GPIO4	16	GPIO5
Row C							
1	IF_POS	2	V_{DDA2}	3	V_{DDD2}	4	V_{DDD1}
5	V_{SSD1}	6	V_{SSD1}	7	TDID	8	TDOD
9	TMSD	10	TCKD	11	TRSTD_N	12	SDAD
13	GPIO6	14	GPIO7	15	GPIO8	16	GPIO9
Row D							
1	IF_NEG	2	V_{DDA2}	3	V_{DDA1}	4	V_{SSD1}
5	V_{SSD2}	6	V_{SSD2}	7	V_{SSA3}	8	RIGHT2
9	LEFT2	10	RIGHT1	11	LEFT1	12	V_{SSA3}
13	GPIO10	14	GPIO11	15	GPIO12	16	GPIO13

Table 2. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row E							
1	V_{SSA2}	2	V_{SSA2}	3	V_{SSD1}	4	V_{SSD1}
5	V_{SSD1}	6	V_{DDD1}	7	V_{SSA3}	8	V_{REF2A}
9	V_{REF2}	10	V_{REF1}	11	V_{REF0}	12	V_{SSA3}
13	GPIO14	14	GPIO15	15	GPIO16	16	GPIO17
Row F							
1	V_{SSA2}	2	RSET	3	V_{DDA2}	4	V_{DDA1}
5	V_{DDA1}	6	V_{REF3}	7	V_{SSA3}	8	V_{DDA3}
9	V_{DDA3}	10	V_{DDA3}	11	V_{DDA3}	12	V_{SSA3}
13	GPIO18	14	GPIO19	15	GPIO20	16	GPIO21
Row G							
1	V_IOUTP	2	V_IOUTN	3	V_{DDA2}	4	SADDR[0]
5	SADDR[1]	6	OUT_LEFT	7	V_{DDA3}	8	V_{DDA3}
9	V_{DDD3}	10	V_{DDD3}	11	V_{DDD3}	12	V_{DDD3}
13	V_{DDD3}	14	V_CLK	15	GPIO22	16	GPIO23
Row H							
1	V_{SSA2}	2	V_{SSA2}	3	V_{DDA2}	4	PROP_RST_N
5	V_{SSA3}	6	OUT_RIGHT	7	V_{DDA3}	8	V_{SSA3}
9	V_{SSD3}	10	V_{SSD3}	11	V_{SSD3}	12	V_{SSD3}
13	V_{SSD3}	14	V_{DDD3}	15	V_{DDD3}	16	V_{SSD3}
Row J							
1	S_IOUTP	2	S_IOUTN	3	V_{DDA2}	4	AOUT
5	V_{SSA3}	6	V_{DDA3}	7	V_{DDA3}	8	V_{SSA3}
9	V_{SSD3}	10	V_{SSD3}	11	V_{SSD3}	12	V_{SSD3}
13	V_{SSD3}	14	V_{DDD3}	15	XTALID	16	XTALOD
Row K							
1	SIF	2	V_{REF4}	3	V_{SSA3}	4	V_{SSA3}
5	V_{SSA3}	6	V_{SSA3}	7	V_{DDA3}	8	V_{SSA3}
9	V_{SSD3}	10	V_{SSD3}	11	V_{SSD3}	12	V_{SSD3}
13	V_{SSD3}	14	V_{DDD3}	15	V_{DDD3}	16	V_{SSD3}
Row L							
1	V_{SSA3}	2	V_{SSA3}	3	V_{SSA3}	4	V_{SSA3}
5	V_{SSA3}	6	V_{SSA3}	7	V_{DDA3}	8	V_{SSA3}
9	V_{SSD3}	10	V_{SSD3}	11	V_{SSD3}	12	V_{SSD3}
13	V_{SSD3}	14	AD[2]	15	AD[1]	16	AD[0]
Row M							
1	CV2_C	2	CV4	3	V_{SSA3}	4	V_{SSA3}
5	V_{SSA3}	6	V_{SSA3}	7	V_{DDA3}	8	V_{SSD3}
9	V_{SSD3}	10	V_{SSD3}	11	V_{SSD3}	12	V_{SSD3}
13	V_{SSD3}	14	AD[5]	15	AD[4]	16	AD[3]

Table 2. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row N							
1	CV3_C	2	DRCV_C	3	V_{SSA3}	4	INT_A
5	PCI_RST#	6	GNT#	7	V_{DDD3}	8	V_{DDD3}
9	V_{DDD3}	10	V_{DDD3}	11	V_{DDD3}	12	V_{DDD3}
13	V_{DDD3}	14	C/BE[0]#	15	AD[7]	16	AD[6]
Row P							
1	V_{SSA3}	2	V_{SSA3}	3	V_{SSA3}	4	REQ#
5	AD[29]	6	AD[26]	7	C/BE[3]#	8	AD[22]
9	AD[19]	10	AD[16]	11	IRDY#	12	STOP#
13	PAR	14	AD[14]	15	PCI_CLK	16	AD[9]
Row R							
1	CV1_Y	2	CV0_Y	3	V_{SSA3}	4	AD[31]
5	AD[28]	6	AD[25]	7	IDSEL	8	AD[21]
9	AD[18]	10	C/BE[2]#	11	TRDY#	12	PERR#
13	C/BE[1]#	14	AD[13]	15	AD[11]	16	AD[8]
Row T							
1	DRCV_Y	2	V_{SSA3}	3	V_{SSA3}	4	AD[30]
5	AD[27]	6	AD[24]	7	AD[23]	8	AD[20]
9	AD[17]	10	FRAME#	11	DEVSEL#	12	SERR#
13	AD[15]	14	AD[12]	15	AD[10]	16	i.c.[1]

[1] i.c.: internally connected; leave open.

6.2 Pin description

The SAA7131E is packaged in a rectangular plastic ball grid array package with 256 pins (LBGA256); see Figure 3.

Table 3. Pin description overview

Pin category	Table number
Power supply pins	Table 4
JTAG test interface pins (for boundary scan test)	Table 5
Digital control pins	Table 6
I^2C-bus slave interface pins	Table 7
PCI interface pins	Table 8
GPIO pins and functions, audio and video decoder part	Table 9
Analog interface pins	Table 10
Crystal oscillator pins	Table 11
Pins for test purposes	Table 12

Table 4. Power supply pins

Symbol	Pin	Type[1]	Description
V_{SSA1}	A2 and A5	AG	analog ground 1, for integrated analog signal processing
V_{DDA1}	B3, D3, F4 and F5	AS	analog supply voltage 1 (1.8 V), for integrated analog signal processing of IF demodulator part
V_{SSA2}	B1, B2, E1, E2, F1, H1 and H2	AG	analog ground 2, for integrated analog signal processing
V_{DDA2}	C2, D2, F3, G3, H3 and J3	AS	analog supply voltage 2 (3.3 V), for integrated analog signal processing of IF demodulator part
V_{SSA3}	D7, D12, E7, E12, F7, F12, H5, H8, J5, J8, K3 to K6, K8, L1 to L6, L8, M3 to M6, N3, P1 to P3, R3, T2 and T3	AG	analog ground 3, for integrated analog signal processing
V_{DDA3}	F8 to F11, G7, G8, H7, J6, J7, K7, L7 and M7	AS	analog supply voltage 3 (3.3 V), for integrated analog signal processing of audio-video decoder part
V_{SSD1}	C5, C6, D4 and E3 to E5	VG	digital ground 1, for digital circuit, core and I/Os
V_{DDD1}	C4 and E6	VS	digital supply voltage 1 (1.8 V), for digital circuits, core and I/Os of IF demodulator part
V_{SSD2}	D5 and D6	VG	digital ground 2, for digital circuits, core and I/Os
V_{DDD2}	B4, B5 and C3	VS	digital supply voltage 2 (3.3 V), for digital circuits, core and I/Os of IF demodulator part
V_{SSD3}	H9 to H13, H16, J9 to J13, K9 to K13, K16, L9 to L13 and M8 to M13	VG	digital ground 3, for digital circuit, core and I/Os
V_{DDD3}	G9 to G13, H14, H15, J14, K14, K15 and N7 to N13	VS	digital supply voltage 3 (3.3 V), for digital circuits, core and I/Os of audio and video decoder part

[1] The pin types are defined in Table 13.

Table 5. JTAG test interface pins (for boundary scan test)

Symbol	Pin	Type[1]	Description
Audio and video decoder			
TDID	C7	I	test serial data input: tie HIGH or let float for normal operation
TDOD	C8	O	test serial data output: 3-state
TMSD	C9	I	test mode select input: tie HIGH or let float for normal operation
TCKD	C10	I	test clock input: drive LOW for normal operation
TRSTD_N	C11	I	test reset input: drive LOW for normal operation
IF demodulator			
TDII	B6	I	test serial data input: tie HIGH or let float for normal operation
TDOI	B7	O	test serial data output: 3-state
TMSI	B8	I	test mode select input: tie HIGH or let float for normal operation
TCKI	B9	I	test clock input: drive LOW for normal operation
TRSTI_N	B10	I	test reset input: drive LOW for normal operation

[1] The pin types are defined in Table 13.

Table 6. Digital control pins

Symbol	Pin	Type[1]	Description
IF demodulator			
RST_N	A6	I	asynchronous reset for IF demodulator
IF_AGC	A7	OD2	IF AGC output to control tuner AGC (RC filter needed)
V_SYNC	A8	O	vertical synchronization pulse to TDA18271
SCL_O	A9	IO2	for TDA18271 control; equivalent to SCL; can be set to 3-state by software
SDA_O	A10	IO2	for TDA18271 control; equivalent to SDA; can be set to 3-state by software

[1] The pin types are defined in Table 13.

Table 7. I^2C-bus slave interface

Symbol	Pin	Type[1]	Description
Audio and video decoder (multi-master)			
SCLD	B12	IO2	serial clock input (slave mode) or output (multi-master mode)
SDAD	C12	IO2	serial data input and output; always available
PROP_RST_N	H4	GO	propagate reset and D3-hot output; to peripheral board circuitry (active LOW)
IF demodulator (slave)			
SCLI	A11	IO2	serial clock input (slave mode)
SDAI	B11	IO2	serial data input and output
SADDR[1:0]	G5 and G4	IO2	serial data input and output

[1] The pin types are defined in Table 13.

Table 8. PCI interface pins

Symbol	Pin	Type[1]	Description
AD[31:0]	L14 to L16, M14 to M16, N15 and N16, P5 and P6, P8 to P10, P14, P16, R4 to R6, R8 and R9, R14 to R16, T4 to T9, T13 to T15[2]	PIO and TS	multiplexed address and data input or output: bidirectional, 3-state
INT_A	N4	PO and OD	interrupt A output: this pin is an open-drain interrupt output, conditions assigned by the interrupt register
PCI_RST#	N5	PI	PCI reset input: will 3-state all PCI pins (active LOW)
GNT#	N6	PI	PCI grant input: the SAA7131E is granted to master access PCI-bus (active LOW)
REQ#	P4	PO	PCI request output: the SAA7131E requests master access to PCI-bus (active LOW)
C/BE[3:0]#	P7, R10, R13 and N14	PIO and TS	command code input or output: indicates type of requested transaction and byte enable, for byte aligned transactions (active LOW)
IRDY#	P11	PIO and STS	initiator ready input or output: driven by the initiator, to indicate readiness to continue transaction (active LOW)
STOP#	P12	PIO and STS	stop input or output: target is requesting the master to stop the current transaction (active LOW)
PAR	P13	PIO and TS	parity input or output: driven by the data source, even parity over all pins AD and C/BE[3:0]#

Table 8. PCI interface pins *…continued*

Symbol	Pin	Type[1]	Description
PCI_CLK	P15	PI	PCI clock input: reference for all bus transactions, up to 33.33 MHz
IDSEL	R7	PI	initialization device select input: this input is used to select the SAA7131E during configuration read and write transactions
TRDY#	R11	PIO and STS	target ready input or output: driven by the addressed target, to indicate readiness for requested transaction (active LOW)
PERR#	R12	PIO and STS	parity error input or output: the receiving device detects data parity error (active LOW)
FRAME#	T10	PIO and STS	frame input or output: driven by the current bus master (owner), to indicate the beginning and duration of a bus transaction (active LOW)
DEVSEL#	T11	PIO and STS	device select input or output: driven by the target device, to acknowledge address decoding (active LOW)
SERR#	T12	PO and OD	system error output: reports address parity error (active LOW)

[1] The pin types are defined in Table 13.

[2] See Table 2 for details.

Table 9. GPIO pins and functions, audio and video decoder part [1]

Symbol	Pin	Type[2]	Function			
			Audio and video port outputs	TS and PS capture outputs	Raw DTV/DVB outputs	GPIO
GPIO27	A14	GIO	A_SDO (I^2S-bus 1 data)	-	-	R/W
GPIO26	A13	GIO	A_WS (I^2S-bus word select)	-	-	R/W
GPIO25	A12	GIO	A_SCK (I^2S-bus clock)	-	-	R/W
GPIO23	G16	GIO	HSYNC	-	ADC_C[0] (LSB)	R/W and INT
GPIO22	G15	GIO	VSYNC	TS_LOCK (channel decoder locked)	-	R/W and INT
GPIO21	F16	GIO	-	TS_S_D (bit-serial data)	-	R/W
GPIO20	F15	GIO	-	TS_CLK (< 33 MHz)	-	R/W
GPIO19	F14	GIO	-	TS_SOP (packet start)	-	R/W
GPIO18	F13	GIO	VAUX2; A_CLK_MASTER, A_REF_CLK	-	X_CLK_IN	R/W and INT
GPIO17	E16	GIO	VAUX1 (e.g. VACTIVE); A_SDO_AUX, I^2S-bus 2 data	-	ADC_Y[0] (LSB)	R/W
GPIO16	E15	GIO	-	TS_VAL (valid flag)	-	R/W and INT

Table 9. GPIO pins and functions, audio and video decoder part *...continued*[1]

Symbol	Pin	Type[2]	Function			
			Audio and video port outputs	TS and PS capture outputs	Raw DTV/DVB outputs	GPIO
GPIO15 to GPIO8	E14, E13, D16, D15, D14, D13, C16 and C15	GIO	VP[7:0] for formats: ITU-R *BT.656*, VMI, VIP (1.1, 2.0), etc.	-	ADC_Y[8:1]	R/W
GPIO7 to GPIO0	C14, C13, B16, B15, B14, B13, A16 and A15	GIO	VP extension for 16-bit formats: ZV, VIP-2, DMSD etc.	TS_P_D[7:0] (transport stream or program stream, byte-parallel data)	ADC_C[8:1]	R/W
V_CLK	G14	GO	V_CLK (also gated)	-	ADC_CLK (out)	-

[1] The SAA7131E offers a peripheral interface with General Purpose Input/Output (GPIO) pins. Dedicated functions can be selected:

a) Digital video port (VP[7:0]): output only; in 8-bit and 16-bit formats, such as VMI, DMSD (ITU-R *BT.601*); zoom-video, with discrete sync signals; ITU-R *BT.656*; VIP (1.1 and 2.0), with sync encoded in SAV and EAV codes.

b) Transport Stream (TS) capture input: from the peripheral DTV/DVB channel decoder; synchronized by Start Of Packet (SOP); in byte-parallel or bit-serial protocol.

c) Digitized raw DTV/DVB samples stream output: from internal ADCs; to feed the peripheral DTV/DVB channel decoder.

d) Program Stream (PS) capture input, e.g. from an external MPEG encoder chip.

e) GPIO: as default (no other function selected); static (no clock); read and write from or to individually selectable pins; latching 'strap' information at system reset time.

f) Peripheral interrupt (INT) input: enabled by interrupt enable register; routed to PCI interrupt (pin INT_A).

[2] The pin types are defined in Table 13.

Table 10. Analog interface pins

Symbol	Pin	Type[1]	Description
Audio and video decoder; the related analog supply pins are included			
CV0_Y	R2	AI	composite video input (mode 0) or Y input (modes 6 and 8)[2]
CV1_Y	R1	AI	composite video input (mode 1) or Y input (modes 7 and 9)[2]
CV2_C	M1	AI	composite video input (mode 2) or C input (modes 6 and 8)[2]
CV3_C	N1	AI	composite video input (mode 3) or C input (modes 7 and 9)[2]
CV4	M2	AI	composite video input (mode 4)[2]
DRCV_Y	T1	AR	differential reference connection (for CV0 and CV1); to be supported with a capacitor of 47 nF connected to V_{SSA}
DRCV_C	N2	AR	differential reference connection (for CV2, CV3 and CV4); to be supported with a capacitor of 47 nF connected to V_{SSA}
LEFT2	D9	AI	analog audio stereo left 2 input or mono input
LEFT1	D11	AI	analog audio stereo left 1 input or mono input; default analog pass-through to pin OUT_LEFT after reset
RIGHT1	D10	AI	analog audio stereo right 1 input or mono input; default analog pass-through to pin OUT_RIGHT after reset
RIGHT2	D8	AI	analog audio stereo right 2 input or mono input
V_{REF0}	E11	AR	analog reference ground for audio sigma-delta ADC; to be connected V_{SSA}
V_{REF1}	E10	AR	analog reference voltage for audio sigma-delta ADC; to be connected to V_{DDA} and through a 220 nF capacitor connected to pin V_{REF0}

Table 10. Analog interface pins *...continued*

Symbol	Pin	Type[1]	Description
V_{REF2}	E9	AR	analog reference voltage for audio sigma-delta ADC; to be supported with two parallel capacitors of 47 µF and 0.1 µF connected to V_{SSA}; connect pin E8 with pin E9
V_{REF2A}	E8	AR	
V_{REF3}	F6	AR	analog reference voltage for audio FIR-DAC and SCART audio input buffer; to be supported with two parallel capacitors of 47 µF and 0.1 µF connected to V_{SSA}
V_{REF4}	K2	AR	analog reference voltage; to be supported with a capacitor of 220 nF connected to V_{SSA}
OUT_RIGHT	H6	AO	analog audio stereo right channel output; 1 V (RMS) line-out; coupling capacitor of 2.2 µF
OUT_LEFT	G6	AO	analog audio stereo left channel output; 1 V (RMS) line-out, coupling capacitor of 2.2 µF
SIF	K1	AI	sound IF input from TV tuner (4.5 MHz to 9.2 MHz); coupling capacitor of 47 pF[3]
IF demodulator			
ADC			
IF_POS	C1	AI	positive analog input for internal IF ADC
IF_NEG	D1	AI	negative analog input for internal IF ADC
DAC			
V_IOUTP	G1	AO	positive analog current output of the video output
V_IOUTN	G2	AO	negative analog current output of the video output
S_IOUTP	J1	AO	positive analog current output of the SSIF audio output
S_IOUTN	J2	AO	negative analog current output of the SSIF audio output
RSET	F2	AR	external bias setting of the DACs

[1] The pin types are defined in Table 13.

[2] To operate in Silicon Tuner mode the video DAC output signal V_IOUT of the IF demodulator part must be looped back to one of the composite video inputs.

[3] To operate in Silicon Tuner mode the sound DAC output signal S_IOUT of the IF demodulator part must be looped back to the SIF input.

Table 11. Crystal oscillator pins

Symbol	Pin	Type[1]	Description
Audio and video decoder			
XTALID	J15	CI	quartz oscillator input or input for external clock signal
XTALOD	J16	CO	quartz oscillator output
IF demodulator			
XTALII	A3	CI	quartz oscillator input or input for external clock signal from TDA18271
XTALOI	A4	CO	quartz oscillator output

[1] The pin types are defined in Table 13.

Table 12. Pins for test purposes [1]

Symbol	Pin	Type	Description
TESTMODE	A1	I	test mode pin; connect to digital ground
AOUT	J4	AO	analog video output for test and debug purposes

[1] The pin types are defined in Table 13.

Table 13. Pin type description

Type	Description
AG	analog ground
AI	analog input; video, audio and sound
AO	analog output
AR	analog reference support pin
AS	analog supply voltage
CI	CMOS input; 3.3 V signal level (not 5 V tolerant)
CO	CMOS output; 3.3 V signal level (not 5 V tolerant)
GI	digital input (GPIO); 3.3 V signal level (5 V tolerant)
GIO	digital input/output (GPIO); 3.3 V signal level (5 V tolerant)
GO	digital output (GPIO); 3.3 V signal level (5 V tolerant)
I	digital input; 3.3 V signal level
IO2	digital input and output of the I^2C-bus interface; 3.3 V and 5 V compatible; auto-adapting
O	digital output; 3.3 V level
OD	open-drain output; multiple clients can drive LOW at the same time (wired OR)
OD2	open-drain output; for bitstream DAC with external filter circuit
PI	input according to PCI requirements
PIO	input and output according to PCI requirements
PO	output according to PCI requirements
STS	sustained 3-state (for certain PCI pins); previous owner drives HIGH for one clock cycle before leaving to 3-state
TS	3-state I/O according to PCI requirements; bidirectional
VG	ground for digital supply
VS	supply voltage

7. Functional description

7.1 General description

The SAA7131E combines the demodulation functionality of the specific low-IF with audio and video decoding functionality; see Figure 4. The low-IF is delivered from a Silicon Tuner, such as the TDA18271.

The SAA7131E is functionally compatible with the SAA7135 audio and video broadcast decoder device and the stand-alone low-IF device TDA8295.

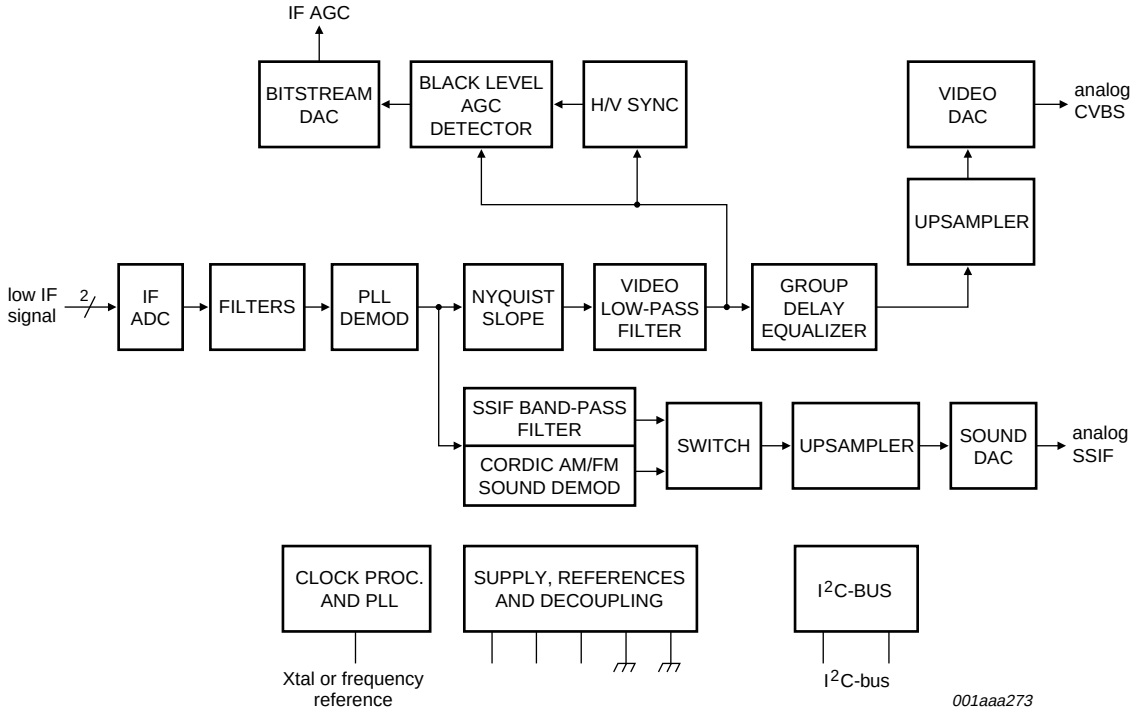


Fig 4. Functional diagram of the low-IF part

7.2 Internal functions of the low-IF demodulator

7.2.1 Filters

The low-IF spectrum (1 MHz to 10 MHz) from the Silicon Tuner (TDA18271) is fed symmetrically to the 10-bit IF ADC of the SAA7131E, where it is sampled at 54 MHz. All anti-aliasing filtering is done previously in the Silicon Tuner.

The filter forms a baseband complex signal and enables a sampling rate to 13.5 MHz. Moreover, the neighboring sound carriers are removed, so that no malfunctioning of the picture carrier PLL happens and no moire becomes visible.

7.2.2 Carrier synchronization

The second-order PLL is the heart of the IF demodulator part. It has been made very robust against adverse field conditions, such as excessive overmodulation, no residual carrier presence or unwanted phase/frequency modulation of the picture carrier. Therefore, a lot of effort in the form of various protection algorithms has been spent to achieve that goal. The AFC data is available through the I^{2}C-bus.

7.2.3 Nyquist filter

The down-mixed complex signal (see Section 7.2.1) already consists of the demodulated content of the picture carrier together with the sound carriers (the so-called intercarriers); this signal is applied to the Nyquist filter to obtain a flat video response and is made real.

The video low-pass filter eliminates the sound carriers and other disturbances.

The equalizer circuit removes the transmitter group delay pre-distortion.

A video levelling stage follows, which brings the output within the SCART specification (±3 dB overall), despite heavy overmodulation.

7.2.4 Video output

The so filtered and compensated CVBS signal is connected to the heavily oversampled 10-bit video DAC (f_s = 108 MHz) through an interpolation stage. The reason is to save the former very complicated LCR filtering. As consequence, only a first-order simple RC low-pass filter is needed acting as a sufficient post filter. This holds also for the sound DAC, described below.

7.2.5 SSIF output

In addition, the complex signal is routed through a band-pass and interpolation filter to the 10-bit sound DAC for the recovery of the second sound carriers (SSIF).

7.2.6 IF AGC

The IF AGC detector is a gated one with a very robust and well proven H/V sync PLL block. Gating occurs on the black level (most of the time on the back porch) of the video signal and the control is delivered to the Silicon Tuner through a bitstream DAC (PWM signal at 13.5 MHz) and an external and uncritical first-order RC low-pass filter.

The correlated or small-band AGC loop, closed through the continuous IF AGC amplifier in the TDA18271, is of first-order integral action and settles at a constant IF ADC input level with a permanent headroom of 6 dB to 9 dB, depending on the standard chosen. This headroom is needed for the sound carriers and the leaking neighbor (N – 1) spectrum, more than sufficient even under strong video overmodulation.

7.3 Internal functions of the PCI audio and video decoder

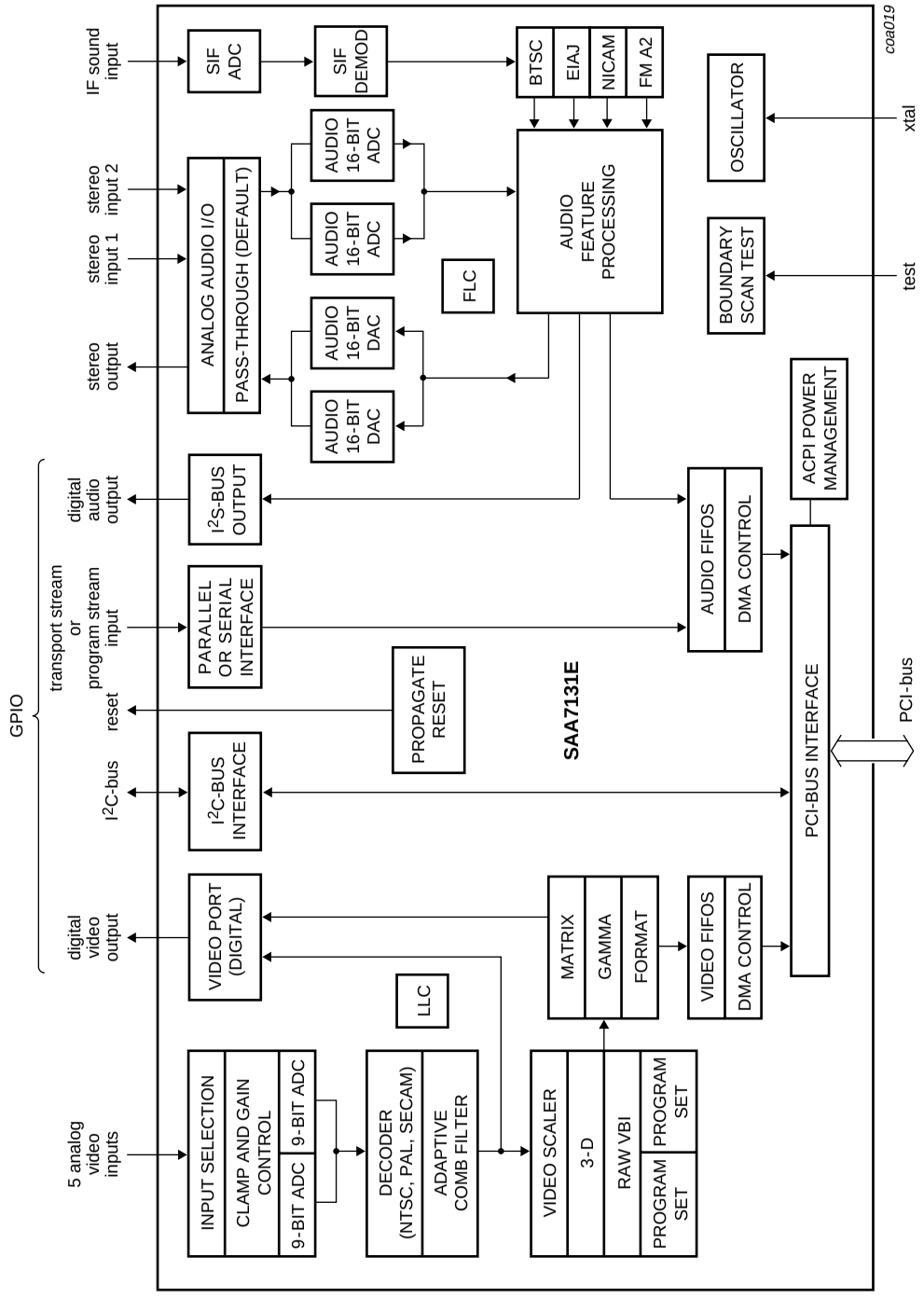


Fig 5. Functional diagram of the PCI audio and video decoder

The SAA7131E is able to capture TV signals over the PCI-bus in personal computers; see Figure 5.

The SAA7131E incorporates two 9-bit video ADCs and the entire decoding circuitry of any analog TV signal: NTSC, PAL and SECAM, including non-standard signals, such as playback from a VCR. The adaptive multi-line comb filter provides superb picture quality, component separation, sharpness and high bandwidth. The video stream can be cropped and scaled to the needs of the application. Downscaling and upscaling is supported in the horizontal and vertical direction, and an adaptive filter algorithm prevents aliasing artifacts. With the acquisition unit of the scaler two different 'tasks' can be defined, e.g. to capture video to the CPU for compression, and write video to the screen from the same video source but with different resolution, color format and frame rate.

The SAA7131E contains TV sound stereo decoding from Sound IF (SIF), for all known sound standards and also non-standard signals. Baseband stereo audio sampling is also implemented, e.g. for capturing from a camcorder or other external devices. The audio sampling rate can be locked to the video frame rate to ensure synchronization (lip sync) between the video and audio data flow, e.g. for storage, compression or time shift viewing applications.

The SAA7131E incorporates analog audio pass-through and support for the analog audio loopback cable to the sound card function.

The decoded video streams are fed to the PCI-bus, and are also applied to a peripheral streaming interface, in ITU, VIP or VMI format. A possible application extension is on-board hardware MPEG compression, or other feature processing. The compressed data as PS or TS is fed back through the peripheral interface, in parallel or serial format, to be captured by the system memory through the PCI-bus. The Transport Stream (TS) from a DTV/DVB channel decoder can be captured through the peripheral interface in the same way.

Audio, video and transport streams are collected in a configurable FIFO with a total capacity of 1 kB. The DMA controller monitors the FIFO filling degree and writes the audio and video streams to the associated DMA channels. The virtual memory address space (from OS) is translated into physical (bus) addresses by the on-chip hardware Memory Management Unit (MMU).

The application of the SAA7131E is supported by reference designs and a set of drivers for the Windows operating system (Windows driver model compliant).

7.4 PCI interface

7.4.1 PCI configuration registers

The PCI interface of the SAA7131E complies with the *PCI Specification 2.2* and supports power management and Advanced Configuration and Power Interface (ACPI) as required by the *PC Design Guide 2001*.

The PCI specification defines a structure of the PCI configuration space that is investigated during the boot-up of the system. The configuration registers (see Table 14) hold information essential for plug-and-play, to allow system enumeration and basic device setup without depending on the device driver, and support association of the proper software driver. Some of the configuration information is hard-wired in the device; some information is loaded during the system start-up.

The device vendor ID is hard coded to 1131h, which is the code for NXP as registered with PCI-SIG.

The device ID is hard coded to 7133h.

During power-up, initiated by a PCI reset, the SAA7131E fetches additional system information through the I^2C-bus from the on-board EEPROM, to load actual board type specific codes for the system vendor ID, sub-system ID (board version) and ACPI related parameters into the configuration registers.

Table 14. PCI configuration space registers

Function	Register address	Value	Remark
Device vendor ID	00h and 01h	1131h	for NXP
Device ID	02h and 03h	7133h	for SAA7131E
Revision ID	08h	D1h	for SAA7131E
Class code	09h to 0Bh	04 8000h	multimedia
Memory address space required	10h to 13h	XXXX XXXX XXXX XXXXb XXXX X000 0000 0000b	2 kB [1]
System (board) vendor ID	2Ch and 2Dh	loaded from EEPROM	
Sub-system (board version) ID	2Eh and 2Fh	loaded from EEPROM	

[1] X = don't care.

7.4.2 ACPI and power states

The *PCI specification 2.2* requires support of *Advanced Configuration and Power Interface specification 1.0* (ACPI); more details are defined in the *PCI Power Management Specification 1.1*.

The power management capabilities and power states are reported in the extended configuration space. The main purpose of ACPI and PCI power management is to tailor the power consumption of the device to the actual needs.

The SAA7131E supports all four ACPI device power states; see Table 15.

The pin PROP_RST_N of the peripheral interface is switched active LOW during the PCI reset procedure, and for the duration of the D3-hot state. Peripheral devices on board of the add-on card should use the level of this signal PROP_RST_N to switch themselves in any Power-save mode (e.g. disable device) and reset to the default settings on the rising edge of signal PROP_RST_N. The length of signal PROP_RST_N is programmable.

7.4.3 DMA and configurable FIFO

The SAA7131E supports seven DMA channels to master-write captured active video, audio, raw VBI and DTV/DVB Transport Streams (TS) and MPEG streams (PS and TS) into the PCI memory. Each DMA channel contains inherently the definition of two buffers in the system address space, e.g. for odd and even fields in case of interlaced video, or two alternating buffers to capture a continuous audio stream.

The DMA channels share in time and space one common FIFO pool of 256 Dwords (1024 bytes) total. It is freely configurable how much FIFO capacity is associated with which DMA channel. Furthermore, a preferred minimum burst length can be programmed, i.e. the amount of data to be collected before the request for the PCI-bus is issued. This means that latency behavior per DMA channel can be tailored and optimized for a given application.

In the event that the FIFO of a certain channel overflows due to latency conflict on the bus, graceful overflow recovery is applied. The amount of data that gets lost because it could not be transmitted, is monitored (counted) and the PCI-bus address pointer is incremented accordingly. Thus new data will be written to the correct memory place after the latency conflict is resolved.

Table 15. Power management

Power state	Description
D0	Normal operation: all functions accessible and programmable. The default setting after reset and before driver interaction (D0 un-initialized) switches most of the circuitry of the SAA7131E into the Power-down mode, effectively such as D3-hot.
D1	First step of reduced power consumption: no functional operation; program registers are not accessible, but content is maintained. Most of the circuitry of the SAA7131E is disabled with the exception of the crystal and real time clock oscillators, so that a quick recovery from D1 to D0 is possible.
D2	Second step of reduced power consumption: no functional operation; program registers are not accessible, but content is maintained. All functional circuitry of the SAA7131E is disabled, including the crystal and clock oscillators.
D3-hot	Lowest power consumption: no functional operation. The content of the programming registers gets lost and is set to default values when returning to D0.

Table 16. FIFO configuration; typical example

DMA	Data stream	Data rate	FIFO size programmable to	Tolerant to latency of
1	Y	13.5 MB/s	384 B	28.4 µs
2	U	6.75 MB/s	256 B	37.9 µs
3	V	6.75 MB/s	256 B	37.9 µs
4	audio	160 kB/s	128 B	800 µs

Table 17. FIFO configuration; fastidious example

DMA	Data stream	Data rate	FIFO size programmable to	Tolerant to latency of
1	raw VBI	27 MB/s	640 B	22.5 µs
	active video, unscaled YUV 4 : 2 : 2			
2	-	-	-	-
3	MPEG stream	9.5 MB/s	256 B	202.1 µs
4	audio	192 kB/s	128 B	583.3 µs

7.4.4 Virtual and physical addressing

Most operating systems allocate memory to requesting applications for DMA as continuous ranges in virtual address space. The data flow over the PCI-bus points to physical addresses, usually not continuous and split in pages of 4 kB (Intel architecture, most UNIX systems, PowerPC).

The association between the virtual (logic) address space and the fragmented physical address space is defined in page tables (system files); see Figure 6. The SAA7131E incorporates hardware support (MMU) to translate virtual to physical addresses on the fly, by investigating the related page table information. This hardware support reduces the demand for real time software interaction and interrupt requests, and therefore saves system resources.

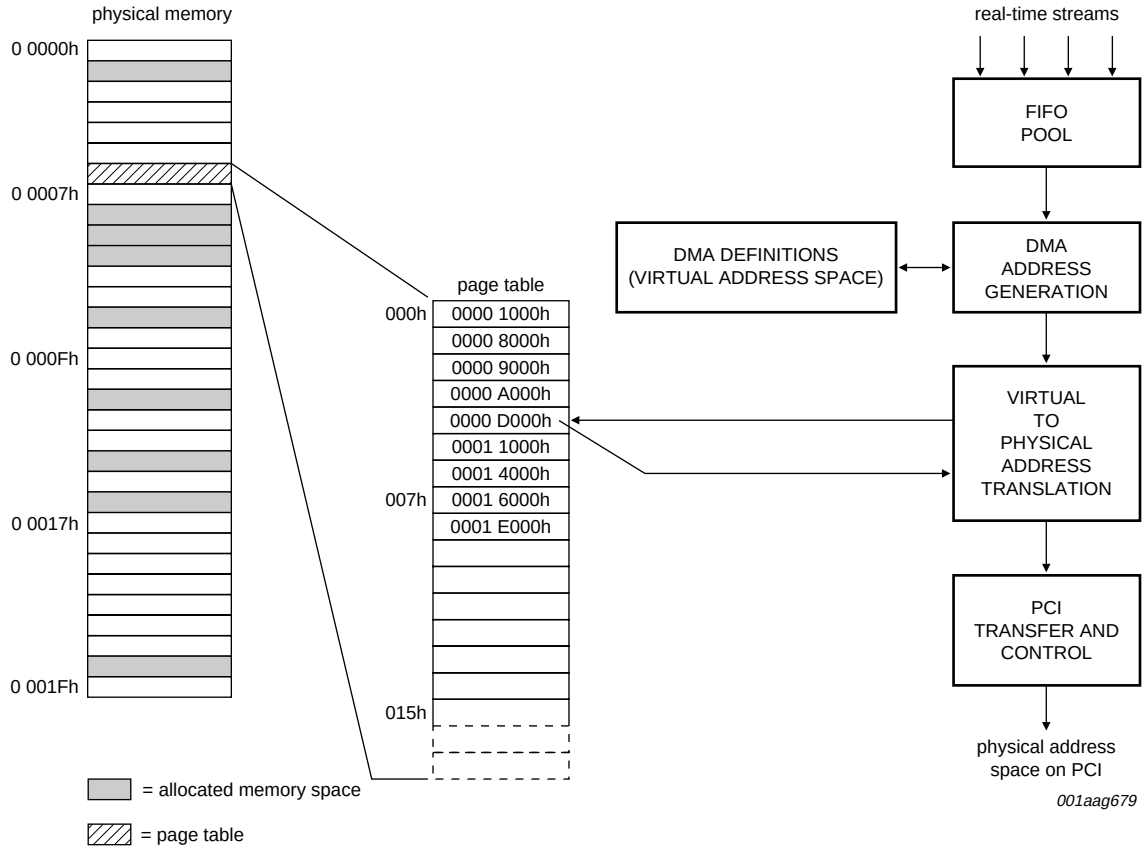


Fig 6. MMU implementation (shown bit width indication is valid for 4 kB mode)

7.4.5 Status and interrupts on PCI-bus

The SAA7131E provides a set of status information about internal signal processing, video and audio standard detection, peripheral inputs and outputs (pins GPIO) and behavior on the PCI-bus. This status information can be conditionally enabled to raise an interrupt on the PCI-bus, e.g. completion of a certain DMA channel or buffer, or change in a detected TV standard or the state of peripheral devices.

The cause of an issued interrupt is reported in a dedicated register, even if the original condition has changed before the system was able to investigate the interrupt.

7.5 Analog TV standards

Analog TV signals are described in three categories of standards:

- Basic TV systems: defining frame rate, number of lines per field, levels of synchronization signals, level of video signals, blanking, black and white, signal bandwidth and the RF modulation scheme
- Color transmission: defining color coding and modulation method
- Sound and stereo: defining coding for transmission.

TV signals that are broadcast usually conform fairly accurately to the standards. Transmission over the air or through a cable can distort the signal with noise, echoes, crosstalk or other disturbances.

Video signals from local consumer equipment, e.g. VCR, camcorder, camera, game console, or even DVD player, often do not follow the standard specification very accurately.

Playback from video tape cannot be expected to maintain correct timing, especially not during feature mode (fast forward, etc.).

Table 18, Table 19 and Table 20 list some characteristics of the various TV standards.

The SAA7131E decodes all color TV standards and non-standard signals as generated by video tape recorders e.g. automatic video standard detection can be applied, with preference options for certain standards, or the decoder can be forced to a dedicated standard.

The SAA7131E incorporates BTSC and EIAJ stereo decoding and TV mono sound decoding on-chip. Baseband stereo audio can be fed into the device as analog signal.

Table 18. Overview of basic TV standards

Main parameter	Standard							Unit
	M	N	B	G/H	I	D/K	L	
RF channel width	6	6	7	8	8	7	8	MHz
Video bandwidth	4.2	4.2	5	5	5.5	6	6	MHz
1st sound carrier[1]	4.5	4.5	5.5	5.5	6.0	6.5	6.5	MHz
Field rate f_v	59.94006	50	50	50	50	50	50	Hz
Lines per frame	525	625	625	625	625	625	625	-
Line frequency f_h	15.734	15.625	15.625	15.625	15.625	15.625	15.625	kHz
ITU clocks per line	1716	1728	1728	1728	1728	1728	1728	-
Sync (setup level)[2]	–40 (7.5)	–40 (7.5)	–43 (0)	–43 (0)	–43 (0)	–43 (0)	–43 (0)	-
Gamma correction	2.2	2.2	2.8	2.8	2.8	2.8	2.8	-
Associated color TV standard	NTSC, PAL	PAL	PAL	PAL	PAL	SECAM, PAL	SECAM	-
Associated stereo TV sound system	BTSC, EIAJ, FM A2	BTSC	NICAM, FM A2	NICAM, FM A2	NICAM	NICAM, FM A2	NICAM, AM	-
Country examples	USA, Brazil, Korea, Japan	Argentina	part of Europe, Australia	Spain, Malaysia, Singapore	UK, Northern Europe	China, Eastern Europe	France, Eastern Europe	-

[1] AM for standard L, FM for all other standards listed

[2] In IRE units

Table 19. TV system color standards

Main parameter	NTSC	PAL			SECAM		PAL 4.4 (60 Hz)	Unit
	M	M	N	B, G, H, I, D	L, D, G, H, K			
Field rate f_v	59.94	59.94	50	50	50		≈60	Hz
Lines per frame	525	525	625	625	625		525	-
Chrominance subcarrier f_{sub}	3.580	3.576	3.582	4.434	4.406	4.250	4.434	MHz
f_{sub} to f_h ratio	227.5	227.25	229.25	283.75	282	272	n.a.	-
f_{sub} offset (PAL)	-	n.a.	50	50	-	-	n.a.	Hz
Alternating phase	no	yes	yes	yes	-	-	yes	-
Country examples	USA, Japan, Asia-Pacific	Brazil	Middle and South America	Europe, China, Common-wealth,	Africa, France, Eastern Europe, Middle East		transcoding VCR tapes from NTSC to PAL	-

Table 20. TV stereo sound standards

Main parameter	Analog systems				Digital coding	Unit
	Mono	BTSC	EIAJ	FM A2	NICAM	
Stereo coding scheme	-	internal carrier (MPX)	internal carrier (MPX)	2-Carrier Systems	2-Carrier Systems	-
		AM	FM	2nd FM carrier	DQPSK on 2nd carrier	-
2nd language	-	mono SAP, internal FM	alternative to stereo	alternative to stereo	mono on 1st carrier	-
De-emphasis	75	75[1]	50	50 to 75	50 to 75	µs
Audio bandwidth	15	15	15	15	15	kHz
Country examples	worldwide	USA, South America	Japan	part of Europe, Korea	part of Europe, China	-

[1] dbx-TV noise reduction system

7.6 Video processing

7.6.1 Analog video inputs

The SAA7131E provides five analog video input pins:

- Composite video signal (CVBS), from looped back video-DAC output of the IF demodulator core
- Composite video signals (CVBS), from conventional tuner or external source
- S-video signals (pairs of Y-C), e.g. from camcorder
- DTV/DVB low-IF signal, from an appropriate DTV or combi-tuner.

Analog anti-alias filters are integrated on-chip and therefore, no external filters are required. The device also contains automatic clamp and gain control for the video input signals, to ensure optimum utilization of the ADC conversion range. The nominal video signal amplitude is 1 V (p-p) and the gain control can adapt deviating signal levels in the range of +3 dB to −6 dB. The video inputs are digitized by two ADCs of 9-bit resolution, with a sampling rate of nominal 27 MHz (the line-locked clock) for analog video signals.

7.6.2 Video synchronization and line-locked clock

The SAA7131E recovers horizontal and vertical synchronization signals from the selected video input signal, even under extremely adverse conditions and signal distortions. Such distortions are noise, static or dynamic echoes from broadcast over air, crosstalk from neighboring channels or power lines (hum), cable reflections, time base errors from video tape play-back and non-standard signal levels from consumer type video equipment (e.g. cameras or DVD).

The heart of this TV synchronization system is the generation of the Line-Locked Clock (LLC) of nominal 27 MHz, as defined by ITU-R *BT.601*. The LLC ensures orthogonal sampling, and always provides a regular pattern of synchronization signals, that is a fixed and well defined number of clock pulses per line. This is important for further video processing devices connected to the peripheral video port (pins GPIO). It is very effective to run under the LLC of 27 MHz, especially for on-board hardware MPEG encoding devices, since MPEG is defined on this clock and sampling frequency.

7.6.3 Video decoding and automatic standard detection

The SAA7131E incorporates color decoding for any analog TV signal. All color TV standards and flavours of NTSC, PAL, SECAM and non-standard signals (VCR) are automatically recognized and decoded into luminance and chrominance components, i.e. Y-C_B-C_R (also known as YUV).

The video decoder of the SAA7131E incorporates an automatic standard detector, that not only distinguishes between 50 Hz and 60 Hz systems, but also determines the color standard of the video input signal. Various preferences (‘look first’) for automatic standard detection can be selected, or a selected standard can be forced directly.

7.6.4 Adaptive comb filter

The SAA7131E applies adaptive comb filter techniques to improve the separation of luminance and chrominance components in comparison to the separation by a chroma notch filter, as used in traditional TV color decoder technology. The comb filter compares the signals of neighboring lines, taking into account the phase shift of the chroma subcarrier from line to line. For NTSC the signals of three adjacent lines are investigated, and in the event of PAL the comb filter taps are spread over four lines.

Comb filtering achieves higher luminance bandwidth, resulting in a sharper picture and detailed resolution. Comb filtering further minimizes color crosstalk artifacts, which would otherwise produce erroneous colors on detailed luminance structures.

The comb filter as implemented in the SAA7131E is adaptive in two ways:

- Adaptive to transitions in the picture content
- Adaptive to non-standard signals (e.g. VCR).

The integrated digital delay lines are always exactly correct, due to the applied unique line-locked sampling scheme (LLC). Therefore the comb filter does not need to be switched off for non-standard signals and remains operating continuously.

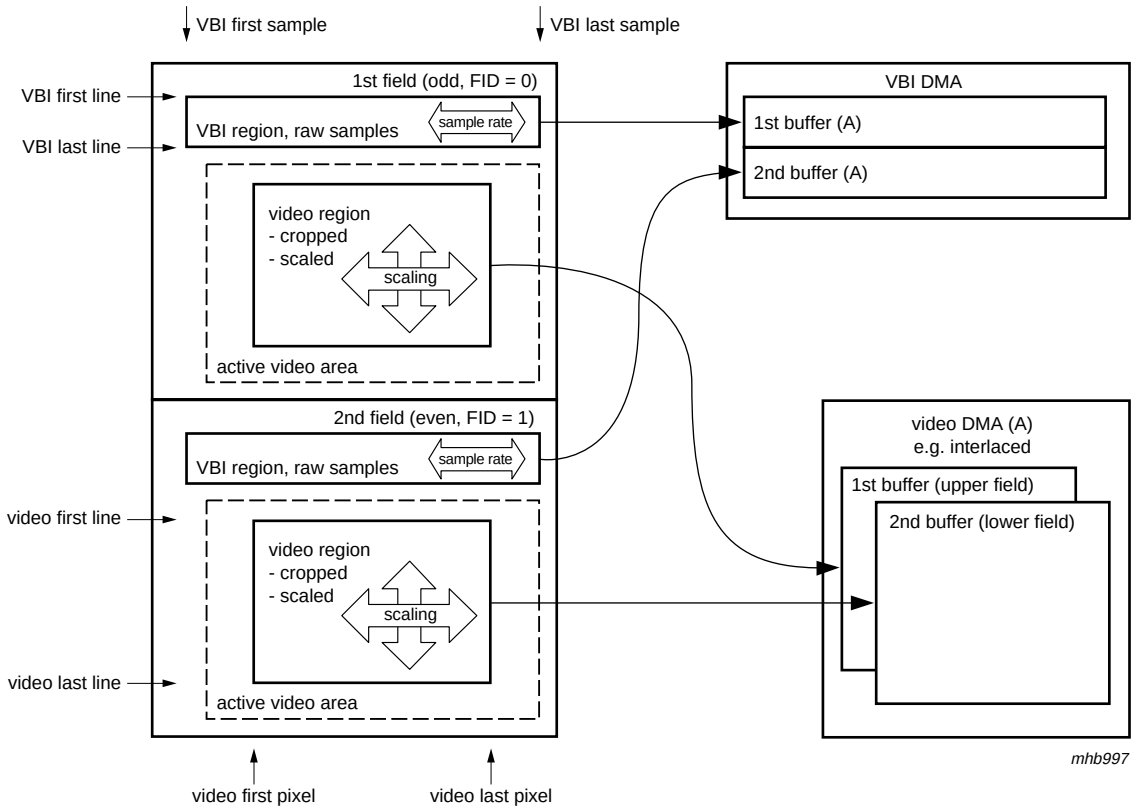
7.6.5 Macrovision detection

The SAA7131E detects if the decoded video signal is copy protected by the Macrovision system. The detection logic distinguishes the three levels of the copy protection as defined in rev. 7.01, and are reported as status information. The Macrovision detection also works for copy protected video signals, which contain inverted bursts but no AGC pulses and no pseudo syncs. Those signals come from some so-called Macrovision-killer boxes. The decoded video stream is not effected directly, but application software and Operation System (OS) has to ensure that this video stream remains tagged as ‘copy protected’, and such video signals would only leave the system with the reinforced copy protection. The multi-level Macrovision detection on the video capture side supports proper TV re-encoding on the output point, e.g. by NXP TV encoders SAA7120 or SAA7104.

7.6.6 Video scaling

The SAA7131E incorporates a filter and processing unit to downscale or upscale the video picture in the horizontal and vertical dimension, and in frame rate; see Figure 7 and Figure 8. The phase accuracy of the resampling process is $1/64$ of the original sample distance. This is equivalent to a clock jitter of less than 1 ns. The filter depth of the anti-alias filter adapts to the scaling ratio, from 10 taps horizontally for scaling ratios close to 1 : 1, to up to 74 taps for an icon sized video picture.

Most video capture applications typically require downscaling. However, some zooming is required for the conversion of ITU sampling to square pixel, or to convert the 240 lines of an NTSC field to 288 lines to comply with ITU-T video phone formats.

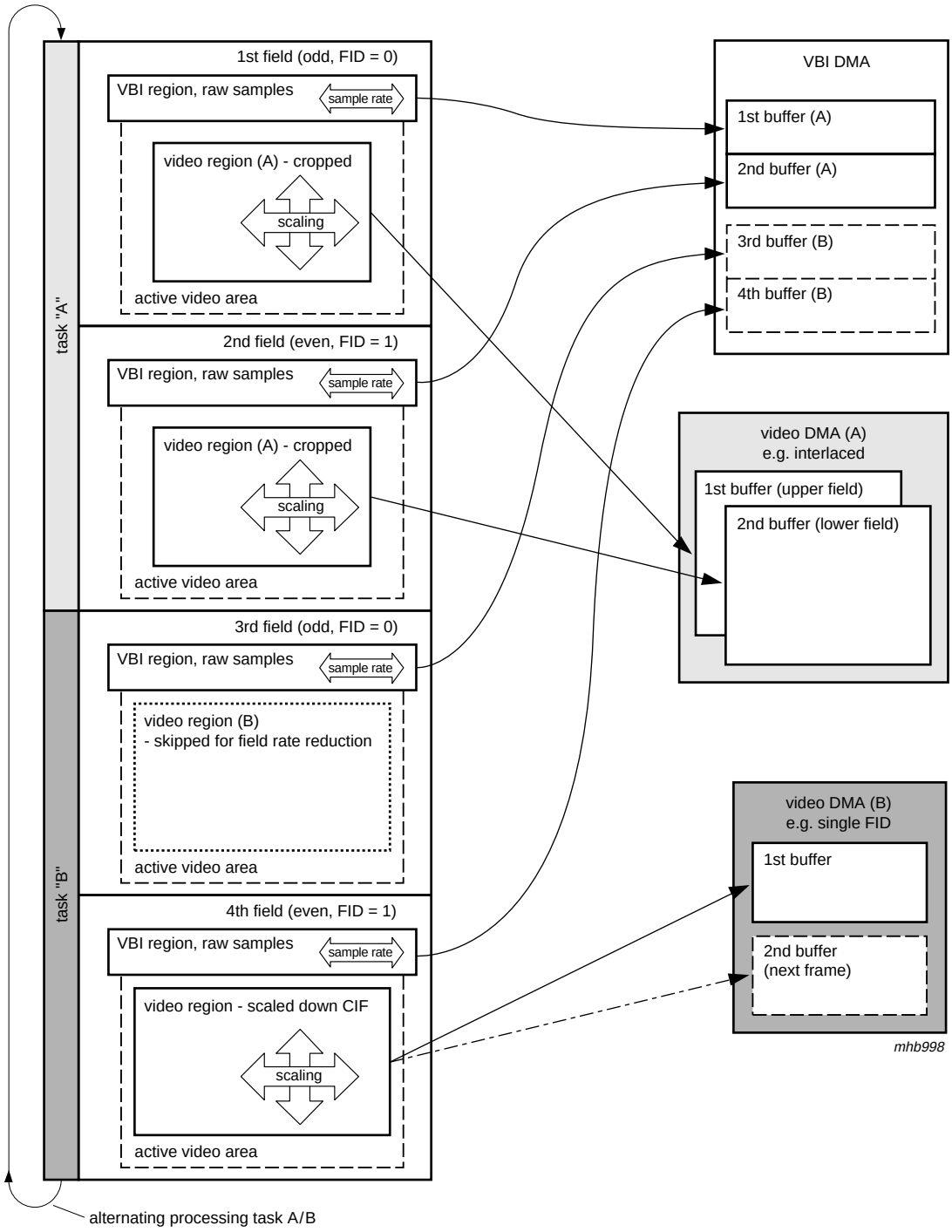


The capture acquisition for scaling and DMA has separate programming parameters for VBI and video region and associated DMA channels.

Fig 7. Scaler processing with DMA interfacing

The scaling acquisition definition also includes cropping, frame rate reduction, and defines the amount of pixel and lines to be transported through DMA over the PCI-bus.

Two programming pages are available to enable re-programming of the scaler in the 'shadow' of the running processing, without holding or disturbing the flow of the video stream. Alternatively, the two programming pages can be applied to support two video destinations or applications with different scaler settings, e.g. firstly to capture video to CPU for compression (storage, video phone), and secondly to preview the picture on the monitor screen. A separate scaling region is dedicated to capture raw VBI samples, with a specific sampling rate, which is written into its own DMA channel.



Two video capture tasks can be processed in an alternating manner, without need to reprogram any scaling parameter or DMA definition.

Fig 8. Example of scaler task processing with DMA interfacing

7.6.7 VBI data

The Vertical Blanking Interval (VBI) is often utilized to transport data over analog video broadcast. Such data can closely relate to the actual video stream, or just be general data (e.g. news). Some examples for VBI data types are given below:

- Closed Caption (CC) for the hearing impaired (CC, on line 21 of first field)
- Intercast data [in USA coded in North American Broadcast Text System (NABTS) format, in Europe in World System Teletext (WST)], to transmit internet related services, optionally associated with actual video program content
- Teletext, transporting news services and broadcast related information, Electronic Program Guide (EPG), widely used in Europe (coded in WST format)
- EPG, broadcaster specific program and schedule information, sometimes with proprietary coding scheme (pay service), usually carried on NABTS, WST, Video Programming System (VPS), or proprietary data coding format
- Vertical Interval Time Codes (VITC) as inserted in camcorders e.g. use for video editing
- Copy Guard Management System (CGMS) codes, to indicate copy protected video material, sometimes combined with format information [Wide Screen Signalling (WSS)].

This information is coded in the unused lines of the vertical blanking interval, between the vertical sync pulse and the active visible video picture. So-called full-field data transmission is also possible, utilizing all video lines for data coding.

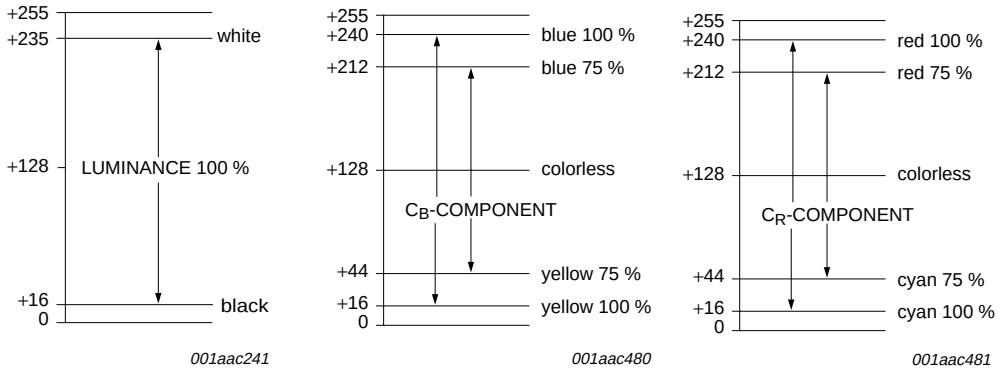
The SAA7131E supports the capture of VBI data, by the definition of a VBI region, which is captured as raw VBI samples. These samples are sliced and decoded by software on the host CPU. The raw sample stream is taken directly from the ADC and is not processed or filtered by the video decoder. The sampling rate of raw VBI data can be adjusted to the needs of the data slicing software.

7.6.8 Signal levels and color space

Analog TV video signals are decoded into their various components, luminance and color difference signals (YUV) or its digital form Y-C_B-C_R. ITU-R *BT.601* defines 720 pixel/line (corresponding to a sampling rate of 27 MHz divided by two), and a certain relationship from level to number range; see Figure 9.

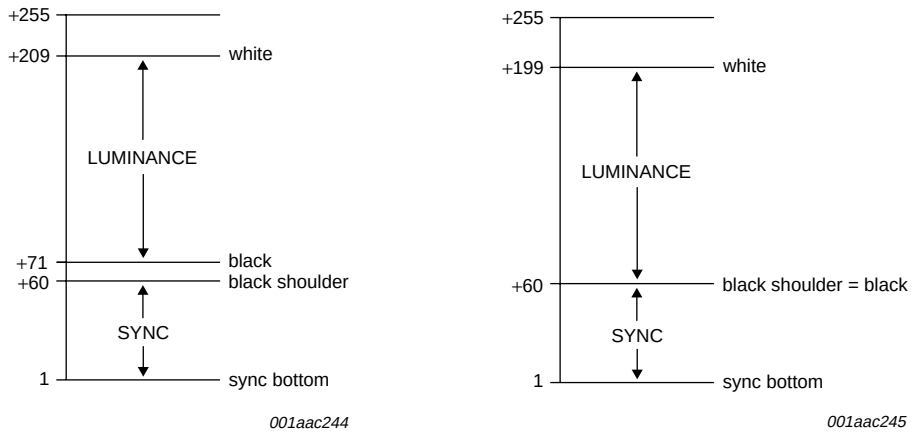
The video components do not use the entire number range, but leave some margin for overshoots and intermediate values during processing. For the raw VBI samples there is no official specification how to code, but it is common practice to reserve the lower quarter of the number range for the sync, and to leave some room for overmodulation beyond the nominal white amplitude; see Figure 10.

The automatic clamp and gain control at the video input, together with the automatic chroma gain control of the SAA7131E, ensures that the video component stream at the output complies to the standard levels. Additional brightness, contrast, saturation and hue control can also be applied to satisfy special needs of a given application. The raw VBI samples can be adjusted independent of the active video.



a. Y output range b. C_B output range c. C_R output range

Fig 9. Nominal digital levels for YUV (Y, C_B and C_R) in accordance with ITU-R *BT.601*



a. For sources containing 7.5 IRE black-level offset (e.g. NTSC M)

b. For sources not containing black-level offset

Fig 10. Nominal digital levels for CVBS and raw VBI samples

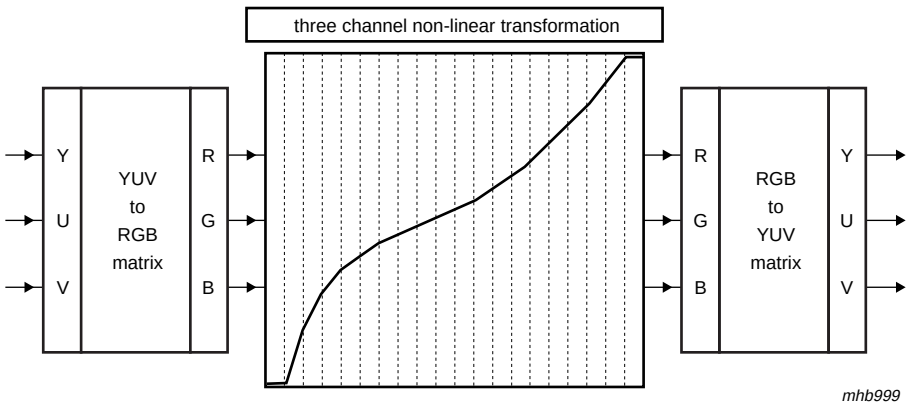


Fig 11. Color space conversion and look-up table

The SAA7131E incorporates the YUV-to-RGB matrix (optional), the RGB-to-YUV matrix and a three channel look-up table in between; see Figure 11. Under nominal settings, the RGB space will use the same number range as defined by the ITU (see Figure 9) for luminance, between 16 and 235. As graphic related applications are based on full-scale RGB, i.e. 0 to 255, the range can be stretched by applying appropriate brightness, contrast and saturation values. The look-up table supports gamma correction (freely definable), and allows other non-linear signal transformation such as black stretching.

The analog TV signal applies a quite strong gamma pre-compensation (2.2 for NTSC and 2.8 for PAL). As computer monitors exhibit a gamma (around 2.5), the difference between gamma pre-compensation and actual screen gamma has to be corrected, to achieve best contrast and color impression.

The SAA7131E offers a multitude of formats to write video streams over the PCI-bus: YUV and RGB color space, 15-bit, 16-bit, 24-bit and 32-bit representation in a packed or in a planar format. For legacy requirements a clipping procedure is implemented, that allows the definition of 8 overlay rectangles. This process can be used alternatively to associate alpha values with the video pixel.

7.6.9 Video port, ITU and VIP codes

The SAA7131E can capture a decoded and scaled video stream or a scaled video stream from the video side port VP[7:0] through PCI-DMA to the system memory. Additionally the decoded and scaled video stream can be made available through the video side port by using the GPIO pins (see Table 9). This functionality can also be used without PCI.

Two types of applications are intended:

- Streaming real time video to a video side port at the VGA card, e.g. through ribbon cable over the top
- Feeding the video stream to a local MPEG compression device on the same PCI board, e.g. for a time shift viewing application.

The video port of the SAA7131E supports the following 8-bit and 16-bit wide YUV video signalling standards; see Table 9:

- VMI: 8-bit wide data stream, clocked by LLC at 27 MHz, with discrete sync signals HSYNC, VSYNC and VACTIVE
- ITU-R *BT.656*, parallel: 8-bit wide data stream, clocked by LLC at 27 MHz, synchronization coded in SAV and EAV codes
- VIP 1.1 and 2.0: 8-bit or 16-bit wide data stream, clocked by LLC at 27 MHz, synchronization coded in SAV and EAV codes (with VIP extensions)
- Zoom Video (ZV): 16-bit wide pixel stream, clocked by LLC/2 at 13.5 MHz, with discrete sync signals HSYNC and VSYNC
- ITU-R *BT.601* direct (DMSD): 16-bit wide pixel stream, clocked by LLC at 27 MHz, with discrete sync signals HSYNC, VSYNC/FID and CREF
- Raw DTV/DVB sample stream: 9-bit wide data, clocked with a copy of signal X_CLK_IN.

The VIP standard is designed to transport scaled video and discontinuous data stream by allowing the insertion of the value 0h as a marker for empty clock cycles. For the other video port standards, a data valid flag or gated clock can be applied.

7.7 Sound processing

7.7.1 TV sound stereo decoding

The SAA7131E incorporates TV sound decoding from the Second Sound Intermediate Frequency (SSIF) signal. The analog SIF signal is taken from the tuner, digitized and digitally FM or AM demodulated. If one of the supported TV sound standards is found (BTSC, EIAJ, NICAM, FM A2 or mono), the pilot tone is investigated (mono, stereo and dual) and stereo or dual decoded.

The SAA7131E supports the stereo audio standards BTSC (including SAP), EIAJ, NICAM, FM A2 and all mono standards on-chip. dbx-TV noise reduction and de-emphasis filters are also integrated; see Table 21.

Table 21. TV sound decoding, supported feature processing and sampling rate

Supported function	Input and sound standard							
	SIF from tuner						Baseband audio	
	BTSC	EIAJ	NICAM	FM A2	FM radio	Other AM/FM	L or R	L and R
Decoding	mono or stereo and SAP[1]	mono or stereo or dual	mono or stereo or dual	mono or stereo or dual	mono or stereo	mono	mono or 2 × mono	stereo
Analog audio output to loopback cable	mono or stereo or SAP	mono or stereo or dual	mono or stereo or dual	mono or stereo or dual	mono or stereo	mono	mono or 2 × mono	stereo[2]
I²S-bus output								
Signal	mono or stereo or SAP	mono or stereo or dual	mono or stereo or dual	mono or stereo or dual	mono or stereo	mono	mono or 2 × mono	stereo
Sample rate	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz, 44.1 kHz or 48 kHz	32 kHz, 44.1 kHz or 48 kHz
PCI (audio streaming)								
Signal	mono or stereo and/or SAP	mono, stereo or dual	mono, stereo or dual	mono, stereo or dual	mono or stereo	mono	mono or 2 × mono	stereo
Sample rate	32 kHz	32 kHz or 48 kHz	32 kHz or 48 kHz	32 kHz or 48 kHz	32 kHz or 48 kHz	32 kHz or 48 kHz	32 kHz, 44.1 kHz or 48 kHz	32 kHz, 44.1 kHz or 48 kHz
Feature processing								
Volume and balance	X	X	X	X	X	X	X	X
Bass and treble	X	X	X	X	X	X	X	X
Incredible Stereo	X	X	X	X	X	-	-	X
Incredible Mono	if SAP	either or dual	either or dual	either or dual	-	X	X	-

[1] Simultaneous decoding of stereo and SAP. dbx-TV noise reduction either on stereo or SAP.

[2] Default pass-through of L1 and R1.

The digital FM demodulation maintains stable phase accuracy, which results in improved channel separation, compared to traditional analog demodulation. TV sound decoding operates at a sample rate of 32 kHz, which results in an audio bandwidth of up to 15 kHz.

The SAA7131E incorporates baseband stereo audio ADCs, to capture sound signals associated with external video sources, e.g. camera, camcorder or VCR.

For concurrent capture of audio and video signals, it is important to maintain synchronization between the two streams. The spoken word and other sound should match the displayed picture within a video frame ($\frac{1}{30}$ s respectively $\frac{1}{25}$ s 'lip-sync'). The SAA7131E uses a special technique to lock the audio sampling clock to the video frame frequency through the Frame-Locked Clock (FLC), so that a programmable but constant number of audio samples is associated with each video frame. This is especially important for video editing, compression and recording, e.g. time shift viewing. There is no drift between the audio and video streams, not even for longer recording times.

7.7.2 Additional audio features

The SAA7131E provides several audio control and enhancement features, such as the following:

- Bass, treble, balance and volume control
- Automatic volume levelling (this algorithm lowers louder parts, e.g. commercials)
- Incredible Mono (this algorithm adds stereo-like sound impression to monaural audio signals)
- Incredible Stereo (this algorithm makes stereo sound impression wider: the distance between the two loudspeakers seems to become greater)
- FM radio stereo decoding.

7.7.3 Audio interfaces

The SIF input can handle the sound subcarrier signal from the tuner. Baseband audio signals can be captured through the stereo line-in inputs LEFT1, RIGHT1, LEFT2 and RIGHT2 or the I^2S-bus input.

The decoded and possibly enhanced digital audio stream can be captured through dedicated DMA into the PCI memory space, or to the output in I^2S-bus format, e.g. to a peripheral digital sound amplifier. The third way is to reconvert the audio signal to analog through the integrated audio stereo DACs and feed it directly through the loopback cable to the sound card or to headphones for local monitoring.

A master clock output (register A_CLK_MASTER) for synchronous clocking of external devices is available through a GPIO output. The audio block is also able to work synchronously to an external audio reference clock (register A_REF_CLK).

7.7.4 Default analog audio pass-through and loopback cable

Most operating systems accept the audio input at only one single entry point, namely at the sound card function. Therefore the sound associated with video has to be routed through the sound card.

The SAA7131E supports analog audio pass-through and the loopback cable on-chip. No external components are required. The audio signal, that was otherwise connected to the sound card line-in, e.g. analog sound from a CD-ROM drive, has to be connected to one

of the inputs of the SAA7131E. By default, after a system reset and without involvement of any driver, this audio signal is passed through to the analog audio output pins that will feed the loopback cable to the sound card line-in connector. The A/V capture driver has to open the default audio pass-through and switch in the TV sound signal.

7.7.5 FM radio

In Silicon Tuner mode the SAA7131E supports FM radio reception and decoding. The SIF input must be connected to the Silicon Tuner device (TDA18271) through additional cheap external circuitry; see *Application Notes SAA7131E*.

7.8 DTV/DVB channel decoding and MPEG TS or PS capture

The SAA7131E also supports application extensions to cover the reception of digital TV broadcast (ATSC, DTV, DVB-T, DVB-C or DVB-S). The low-IF signal from a hybrid tuner is fed to a peripheral channel decoder to decode it into the transport stream. This TS, accompanied by a clock and handshake signals [Start Of Packet (SOP), etc.] can be captured by the SAA7131E, in serial or parallel format. The TS packets are written in a structured way in dedicated DMA definition into the PCI memory space. Toggling between two DMA buffers is supported automatically.

The SAA7131E supports the capturing of MPEG elementary and program streams. This expands the connectivity to MPEG encoders.

7.9 Control of peripheral devices

7.9.1 I^2C-bus master

The SAA7131E incorporates an I^2C-bus master to setup and control peripheral devices such as a tuner, DTV/DVB channel decoder, audio DSP co-processors, etc. The I^2C-bus interface itself is controlled from the PCI-bus on a command level, reading and writing byte by byte. The actual I^2C-bus status is reported (status register) and, as an option, can raise error interrupts on the PCI-bus.

At PCI reset time, the I^2C-bus master receives board specific information from the on-board EEPROM to update the PCI configuration registers.

The I^2C-bus interface is multi-master capable and can assume slave operation too. This allows an application of the device in the stand-alone mode, i.e. with the PCI-bus not connected. Under the Slave mode, all internal programming registers can be reached through the I^2C-bus with the exception of the PCI configuration space.

7.9.2 Propagate reset

The PCI system reset and ACPI power management state D3 is propagated to peripheral devices by the dedicated pin PROP_RST_N. This signal is switched to active LOW by reset and D3, and is only switched HIGH under control of the device driver ‘by will’. The intention is that peripheral devices will use the PROP_RST_N signal as Chip-Enable (CE). The peripheral devices should enter a low power consumption state if pin PROP_RST_N = LOW, and reset into the default setting at the rising edge.

When connecting PROP_RST_N (audio and video decoder part) and RST_N (IF demodulator) the driver must set PROP_RST_N to HIGH, as described above.

7.9.3 GPIO

The SAA7131E offers a set of General Purpose Input/Output (GPIO) pins, to interface to on-board peripheral circuits; see Table 9. These GPIOs are intended to manage dedicated functions:

- Digital video port output: 8-bit or 16-bit wide (including raw DTV)
- Digital audio serial output: i.e. I^2S-bus output
- Transport stream input:
  - parallel (also applicable for program stream and elementary stream)
  - serial (also applicable as I^2S-bus input)
- Peripheral interrupt input: four GPIO pins of the SAA7131E can be enabled to raise an interrupt on the PCI-bus. By this means, peripheral devices can directly intercept with the device driver on changed status or error conditions.

Any GPIO pin that is not used for a dedicated function is available for direct read and write access through the PCI-bus. Any GPIO pin can be selected individually as input or output (masked write). By these means, very tailored interfacing to peripheral devices can be created through the SAA7131E capture driver operating on a Windows operating system.

At system reset (PCI reset) all GPIO pins will be set to 3-state and input, and the logic level present on the GPIO pins at that moment will be saved into a special ‘strap’ register. All GPIO pins have an internal pull-down resistor (LOW level), but can be strapped externally with a 4.7 kΩ resistor to the supply voltage (HIGH level). The device driver can investigate the strap register for information concerning the hardware configuration of a given board.

8. Limiting values

Table 22. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All ground pins connected together and grounded (0 V); all supply pins connected together.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDD1}	digital supply voltage 1	for IF demodulator		–0.5	+2.0	V
V_{DDD2}	digital supply voltage 2	for IF demodulator		–0.5	+3.6	V
V_{DDD3}	digital supply voltage 3	for decoder		–0.5	+3.6	V
V_{DDA1}	analog supply voltage 1	for IF demodulator		–0.5	+2.0	V
V_{DDA2}	analog supply voltage 2	for IF demodulator		–0.5	+3.6	V
V_{DDA3}	analog supply voltage 3	for decoder		–0.5	+3.6	V
ΔV_{SS}	ground supply voltage difference	between pins V_{SSA} and V_{SSD}		-	100	mV
$V_{I(a)}$	analog input voltage	at analog inputs		–0.5	+3.6	V
V_I	input voltage	at pin XTALII		–0.5	V_{DDD1} + 0.5	V
		at pins SCLI and SDAI		–0.5	V_{DDD2} + 0.5	V
		at pins XTALID, SDAD and SCLD		–0.5	V_{DDD3} + 0.5	V
$V_{I(D)}$	digital input voltage	at digital I/O stages, outputs in 3-state				
		$-0.5\ V < V_{DDD2} < +3.0\ V$		–0.5	+4.6	V
		$3.0\ V < V_{DDD2} < 3.6\ V$		–0.5	+5.5	V
		$-0.5\ V < V_{DDD3} < +3.0\ V$		–0.5	+4.6	V
		$3.0\ V < V_{DDD3} < 3.6\ V$		–0.5	+5.5	V
T_{stg}	storage temperature			–40	+150	°C
T_{amb}	ambient temperature		[1]	0	70	°C
V_{esd}	electrostatic discharge voltage	human body model	[2]	-	±2000	V
		machine model	[3]	-	±150	V

[1] The device has to be programmed according to the register settings described in the *User Manual SAA7131E*, in order not to exceed 1.55 W.

[2] Class 2 according to *EIA/JESD22-114-B*.

[3] Class A according to *EIA/JESD22-115-A*.

9. Thermal characteristics

Table 23. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	35	K/W

[1] The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. An ample copper area direct under the SAA7131E with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Please do not use any solder-stop varnish under the chip. In addition the usage of soldering glue with a high thermal conductance after curing is recommended.

10. Characteristics

Operating conditions for minimum and maximum values in Table 24 to Table 26: V_{DDD1} = 1.7 V to 1.9 V; V_{DDD2} = V_{DDD3} = 3.15 V to 3.45 V; V_{DDA1} = 1.7 V to 1.9 V; V_{DDA2} = V_{DDA3} = 3.15 V to 3.45 V; T_{amb} = 0 °C to 70 °C; unless otherwise specified.

Operating conditions for typical values in Table 24 to Table 26: V_{DDD1} = 1.8 V; V_{DDD2} = V_{DDD3} = 3.3 V; V_{DDA1} = 1.8 V; V_{DDA2} = V_{DDA3} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

10.1 Supplies

Table 24. Supply characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDD1}	digital supply voltage 1	for IF demodulator		1.7	1.8	1.9	V
V_{DDD2}	digital supply voltage 2	for IF demodulator		3.15	3.3	3.45	V
V_{DDD3}	digital supply voltage 3	for decoder		3.15	3.3	3.45	V
V_{DDA1}	analog supply voltage 1	for IF demodulator		1.7	1.8	1.9	V
V_{DDA2}	analog supply voltage 2	for IF demodulator		3.15	3.3	3.45	V
V_{DDA3}	analog supply voltage 3	for decoder		3.15	3.3	3.45	V
I_{DDD1}	digital supply current 1		[1]	26	32	40	mA
I_{DDD2}	digital supply current 2		[1]	210	225	250	mA
I_{DDD3}	digital supply current 3		[1]	210	225	250	mA
I_{DDA1}	analog supply current 1		[1]	1.1	1.25	1.5	mA
I_{DDA2}	analog supply current 2		[1]	240	247	260	mA
I_{DDA3}	analog supply current 3		[1]	240	247	260	mA
P	power dissipation	power state (see Table 15)					
		D0 in Silicon Tuner mode	[2]	1.1	1.35	1.55	W
		D0 in non-Silicon Tuner mode	[3]	1.1	1.35	1.55	W
		D1		-	0.55	-	W
		D2		-	0.50	-	W
		D3-hot	[4]	-	-	0.45	W
		D3-hot	[5]	-	-	0.05	W

[1] All features are enabled.

[2] CVBS operation in Silicon Tuner mode with first video decoder analog front end; second video decoder front end is disabled through PCI-bus or I^2C-bus; see *User Manual SAA7131E*.

[3] CVBS or Y/C operation through external sources e.g. VCR; IF demodulator is set in Standby mode through PCI-bus or I^2C-bus; see *User Manual SAA7131E*.

[4] If pins PROP_RST_N and RST_N are connected.

[5] If IF demodulator is set in Standby mode and pins PROP_RST_N and RST_N are not connected; RST_N must be inactive; see *User Manual SAA7131E*.

10.2 IF demodulator

Table 25. IF demodulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital pins (pins RST_N, TESTMODE, SADDR0, SADDR1, V_SYNC, SCL_O, SDA_O, TRSTI_N, TCKI, TMSI, TDOI and TDII)						
V_{IH}	HIGH-level input voltage	all inputs except XTALII	2	-	5.5	V
V_{IL}	LOW-level input voltage	all inputs except XTALII	-	-	0.8	V
V_{OH}	HIGH-level output voltage	source current 4 mA	2.4	-	V_{DDD2} + 0.5	V
V_{OL}	LOW-level output voltage	sink current 4 mA	-	-	0.4	V
C_i	input capacitance		-	-	5	pF
IF demodulator master clock						
f_{clk}	clock frequency	see *User Manual SAA7131E* for PLL settings	-	54	-	MHz
$\Delta f/f_{clk}$	relative frequency deviation from clock frequency		-	-	±200	ppm
Reference frequency in slave mode (square wave signal on pin XTALII)						
$f_{clk(ext)}$	external clock frequency		4	16	50	MHz
$V_{i(clk)(p-p)}$	peak-to-peak clock input voltage		400	-	900	mV
C_i	input capacitance		-	-	2	pF
Reference fundamental frequency in oscillator mode (with crystal)						
f_{xtal}	crystal frequency		8	16	30	MHz
$\Delta f_{xtal(T)}/f_{xtal}$	relative crystal frequency variation with temperature		-	-	±50	ppm
$\Delta f_{xtal(t)}/f_{xtal}$	relative crystal frequency variation with time		-	-	±10	ppm
$T_{amb(xtal)}$	crystal ambient temperature		–20	-	+70	°C
IF input (pins IF_POS and IF_NEG)						
$V_{i(p-p)}$	peak-to-peak input voltage	for 0 dB	1.8	2.0	2.2	V
$R_{i(dif)}$	differential input resistance		10	-	-	kΩ
$C_{i(dif)}$	differential input capacitance		-	-	2	pF
V_i	input voltage	operational voltage from AGC feedback loop				
		all standards except L/L’	–6	–6	–6	dB
		L/L’	–9	–9	–9	dB

Table 25. IF demodulator characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency	Picture Carrier (PC)					
		M/N		-	-	5.75	MHz
		B		-	-	6.75	MHz
		G/H		-	-	7.75	MHz
		I		-	-	7.75	MHz
		D/K, L		-	-	7.75	MHz
		L’		-	-	1.25	MHz
		first Sound Carrier (SC1)					
		M/N		-	-	1.25	MHz
		B		-	-	1.25	MHz
		G/H		-	-	2.25	MHz
		I		-	-	1.75	MHz
		D/K, L		-	-	1.25	MHz
		L’		-	-	7.75	MHz
IF selectivity							
$\alpha_{sup(stpb)}$	stop-band suppression	Hilbert filter		–60	-	-	dB
		decimation filter		–60	-	-	dB
		notch filter for NSC (NPC for L’), all standards	[1]	–40	-	-	dB
Carrier recovery PLL							
$B_{-3dB(cl)}$	closed-loop –3 dB bandwidth	super wide		150	-	-	kHz
		wide		70	-	-	kHz
		medium		30	-	-	kHz
		small		15	-	-	kHz
$\Delta f_{lock\text{-}in}$	lock-in frequency range			800	830	-	kHz
$m_{over(PC)}$	picture carrier overmodulation index	black for L/L’, flat field white else		115	117	-	%
$f_{step(AFC)}$	AFC step frequency	128 steps		13	-	-	kHz
IF demodulation							
$B_{T(tot)}$	total transition bandwidth	Nyquist filter, all standards		1	-	-	MHz
$\alpha_{sup(stpb)}$	stop-band suppression	Nyquist filter, all standards		–60	-	-	dB
		video low-pass filter (M/N, B/G/H, I, D/K and L/L’)		–60	-	-	dB
$B_{video(-1dB)}$	–1 dB video bandwidth	M/N		3.9	-	-	MHz
		B/G/H, I, D/K, L/L’		4.9	-	-	MHz
$t_{ripple(GDE)}$	group delay equalizer ripple time	peak value	[2]	-	30	50	ns
$B_{-3dB(cl)}$	closed-loop –3 dB bandwidth	closed-loop through IF AGC and TDA18271		0.15	0.2	0.25	kHz
$f_{-3dB(lpf)}$	low-pass filter –3 dB frequency	IF AGC post filter		0.9	1.0	1.1	kHz

Table 25. IF demodulator characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
CVBS output							
$V_{o(p-p)}$	peak-to-peak output voltage	75 Ω DC load; sync-white modulation					
		negative PC modulation (except L/L')					
		65 %		0.8	0.9	1.2	V
		90 % (nominal)		0.8	1.0	1.2	V
		115 %		0.8	1.1	1.2	V
		positive PC modulation (L/L')					
		65 % PC		0.8	0.9	1.2	V
		97 % PC (nominal)		0.8	1.1	1.2	V
		115 %		0.8	1.0	1.2	V
f_{video}	video frequency	overall video response (–3 dB)					
		all standards except M/N		4.8	4.85	-	MHz
		M/N		4.0	4.05	-	MHz
G_{dif}	differential gain			-	< 2.0	5	%
φ_{dif}	differential phase			-	< 1.5	4	deg
$V_{stlt}/V_{CVBS(p-p)}$	synchronization tilt voltage to peak-to-peak CVBS voltage ratio			-	1	2	%
$V_{ftlt}/V_{CVBS(p-p)}$	frame tilt voltage to peak-to-peak CVBS voltage ratio			-	1.5	3	%
$\Delta V_{tro}/V_{tro}$	relative transient response overshoot voltage variation	2T pulse	[3]	-	3	5	%
$\alpha_{IM(blue)}$	intermodulation suppression (blue)	carrier levels related to PC sync: PC = –3.2 dB; CC = –19.2 dB; SC = –13 dB					
		at 1.1 MHz (related to black/white in RMS, equals CC + 3.6 dB)		63	67	-	dB
		at 3.3 MHz (related to CC)		64	68	-	dB
$\alpha_{IM(yellow)}$	intermodulation suppression (yellow)	carrier levels related to PC sync: PC = –10.0 dB; CC = –19.2 dB; SC = –13 dB					
		at 1.1 MHz (related to black/white in RMS, equals CC + 3.6 dB)		55	58	-	dB
		at 3.3 MHz (related to CC)		63	67	-	dB
$(S/N)_w$	weighted signal-to-noise ratio	all standards except L/L'	[4]	55	57	-	dB
		L/L'		53	55	-	dB

Table 25. IF demodulator characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PSRR	power supply rejection ratio	f_{ripple} = 70 Hz; 100 mV (p-p); video signal: grey, level: 50 %; input level: 60 dB µV (RMS) PC				
		SAA7131E stand-alone				
		positive video modulation, standard L, 1.8 V	55	58	-	dB
		positive video modulation, standard L, 3.3 V	32	34	-	dB
		negative video modulation, standard B, 1.8 V	55	58	-	dB
		negative video modulation, standard B, 3.3 V	32	34	-	dB
		SAA7131E together with TDA18271				
		positive video modulation, standard L, 1.8 V	40	41	-	dB
		positive video modulation, standard L, 3.3 V	14	16	-	dB
		negative video modulation, standard B, 1.8 V	40	42	-	dB
		negative video modulation, standard B, 3.3 V	14	16	-	dB
$\alpha_{sup(f)L(unw)}$	unwanted leakage frequency suppression	4.8 MHz video modulation; related to black-to-white in 10 MHz to 200 MHz band	55	60	-	dB
SSIF audio output						
$V_{o(RMS)}$	RMS output voltage	1 kΩ DC or AC load; no modulation; PC/SC1 = 13 dB; scaled linearly for all other ratios				
		all standards except L/L'	40	56	-	mV
		standard L/L'	40	45	-	mV

Table 25. IF demodulator characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$(S/N)_{aud(w)}$	weighted audio signal-to-noise ratio	**FM**: through SSIF sound demodulator in dual mode; *CCIR468-4*, FM mode related to 27 kHz deviation before pre-emphasis; 10 % residual PC				
		1st Sound Carrier (SC1)				
		black picture	60	63	-	dB
		flat field white picture	55	58	-	dB
		6 kHz sine wave picture	50	51	-	dB
		250 kHz square wave picture	50	53	-	dB
		crosshatch picture	50	53	-	dB
		color bar picture	59	62	-	dB
		2nd Sound Carrier (SC2)				
		black picture	54	59	-	dB
		flat field white picture	51	55	-	dB
		6 kHz sine wave picture	50	51	-	dB
		250 kHz square wave picture	40	44	-	dB
		crosshatch picture	50	52	-	dB
		color bar picture	51	55	-	dB
		AM: through SSIF sound demodulator in dual mode; *CCIR468-4*, AM mode related to 54 % modulation degree; 3 % residual PC; 1st Sound Carrier (SC1)				
		black picture	38	41	-	dB
		flat field white picture	36	38	-	dB
		color bar picture	38	41	-	dB
PSRR	power supply rejection ratio	f_{ripple} = 70 Hz; 100 mV (p-p); video signal: grey, level: 50 %; input level: 60 dB µV (RMS) PC				
		SAA7131E stand-alone				
		FM sound, standard B, 1.8 V	55	60	-	dB
		FM sound, standard B, 3.3 V	45	49	-	dB
		AM sound, standard L, 1.8 V	55	59	-	dB
		AM sound, standard L, 3.3 V	45	49	-	dB
		SAA7131E together with TDA18271				
		FM sound, standard B, 1.8 V	50	52	-	dB
		FM sound, standard B, 3.3 V	46	50	-	dB
		AM sound, standard L, 1.8 V	44	47	-	dB
		AM sound, standard L, 3.3 V	22	24	-	dB
$\alpha_{sup(f)L(unw)}$	unwanted leakage frequency suppression	related to SSIF (SC1) in 10 MHz to 200 MHz band	40	42	-	dB

[1] Standard dependent located at 7.25 MHz, 8.25 MHz, 9.25 MHz and 10.25 MHz.

[2] For standards B/G/H half, D/K half, I flat, M (FCC) full and L/L' full.

[3] Half-Amplitude Duration (HAD): 250 ns for M and 200 ns for all other standards.

[4] According to *ITU-T J.61 (CCIR567)*.

10.3 Audio and video decoder

Table 26. Audio and video decoder characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Crystal oscillator						
V_{IH}	HIGH-level input voltage	at pin XTALID	2	-	V_{DDD3} + 0.3	V
V_{IL}	LOW-level input voltage	at pin XTALID	–0.3	-	+0.8	V
P_{drive}	drive power	at pin XTALID or XTALOD	-	0.5	-	mW
$f_{xtal(nom)}$	nominal crystal frequency	see Table 27	24	24.576	33	MHz
$\Delta f/f_{xtal(nom)}$	nominal crystal frequency deviation		-	-	±70	ppm
I²C-bus interface, compatible to 3.3 V and 5 V signalling (pins SDAD and SCLD)						
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD3}$	-	V_{DDD3} + 0.5	V
V_{IL}	LOW-level input voltage		–0.5	-	$+0.3 \times V_{DDD3}$	V
V_{OL}	LOW-level output voltage	$I_{o(sink)}$ = 3 mA	-	-	0.4	V
f_{bit}	bit rate		0	-	400	kbit/s
Analog video inputs						
Inputs (pins CV0_Y, CV1_Y, CV2_C, CV3_C and CV4)						
I_{CL}	clamping current	DC input voltage V_I = 0.9 V	-	±8	-	µA
$V_{i(p-p)}$	peak-to-peak input voltage	[1]	0.375	0.75	1.07	V
C_i	input capacitance		-	-	10	pF
9-bit analog-to-digital converters						
$\alpha_{ct(ch)}$	channel crosstalk	f_i < 5 MHz	-	-	–50	dB
$B_{video(-3dB)}$	–3 dB video bandwidth	ADC only	-	7	-	MHz
φ_{dif}	differential phase	amplifier plus anti-alias filter bypassed	-	2	-	deg
G_{dif}	differential gain	amplifier plus anti-alias filter bypassed	-	2	-	%
DLE_{DC}	DC differential linearity error		-	1.4	-	LSB
ILE_{DC}	DC integral linearity error		-	2	-	LSB
S/N	signal-to-noise ratio	f_i = 4 MHz; anti-alias filter bypassed; AGC = 0 dB	-	50	-	dB
ENOB	effective number of bits	f_i = 4 MHz; anti-alias filter bypassed; AGC = 0 dB	-	8	-	bit

Table 26. Audio and video decoder characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Analog sound input (pin SIF)							
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	input level adjustment					
		0 dB		-	941	-	mV
		−10 dB		-	2976	-	mV
$V_{i(min)(p-p)}$	minimum input voltage (peak-to-peak value)	input level adjustment	[2]				
		0 dB		-	59	-	mV
		−10 dB		-	188	-	mV
$V_{i(AGC)}$	AGC input voltage	in addition to 0 dB and −10 dB switch		-	24	-	dB
f_i	input frequency			3	-	12	MHz
R_i	input resistance	default pre-gain selection for pin SIF (0 dB)		10	-	-	kΩ
C_i	input capacitance			-	7.5	11	pF
Analog audio inputs (pins LEFT1, RIGHT1, LEFT2 and RIGHT2) and outputs (pins OUT_LEFT and OUT_RIGHT)							
$V_{i(nom)(rms)}$	nominal input voltage (RMS value)		[3]	-	200	-	mV
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	THD < 3 %	[4]	-	1	2	V
$V_{o(nom)(rms)}$	nominal output voltage (RMS value)		[3]	-	180	-	mV
$V_{o(max)(rms)}$	maximum output voltage (RMS value)	THD < 3 %		-	1	-	V
R_i	input resistance	$V_{i(max)}$ = 1 V (RMS)		-	145	-	kΩ
		$V_{i(max)}$ = 2 V (RMS)		-	48	-	kΩ
R_o	output resistance			150	250	375	Ω
$R_{L(AC)}$	AC load resistance			10	-	-	kΩ
$C_{o(L)}$	output load capacitance			-	-	12	nF
$V_{offset(DC)}$	DC offset voltage			-	10	30	mV
S/N	signal-to-noise ratio	reference voltage V_o = 1 V (RMS); f_i = 1 kHz; *ITU-R BS.468* weighted; quasi peak		70	75	-	dB
THD+N	total harmonic distortion-plus-noise	$V_i = V_o$ = 1 V (RMS); f_i = 1 kHz; bandwidth = 20 Hz to 20 kHz		-	0.1	0.3	%
α_{ct}	crosstalk attenuation	between any analog input pairs; f_i = 1 kHz		60	-	-	dB
α_{cs}	channel separation	between left and right of each input pair		60	-	-	dB

Table 26. Audio and video decoder characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Sound demodulator performance[5]							
Audio AM mono characteristics (DDEP standard code = 10, driven with external SSIF)							
S/N	signal-to-noise ratio	AM carrier 6.5 MHz; 54 % AM; f_i = 1 kHz; second SIF AGC off; *ITU-R BS.468* weighted; quasi peak	[6]	-	47	-	dB
THD+N	total harmonic distortion-plus-noise	AM carrier 6.5 MHz; 54 % AM; f_i = 1 kHz; second SIF AGC off; *ITU-R BS.468* weighted; quasi peak	[6]	-	0.43	-	%
ΔG_f	frequency gain variation	from 20 Hz to 15 kHz; f_{ref} = 1 kHz; no clipping		-	–0.5 to +0.1	-	dB
Audio M standard BTSC characteristics (DDEP standard code = 13, driven with external SSIF)							
S/N	signal-to-noise ratio	**BTSC stereo** with L or R only; 100 % modulation; f_i = 1 kHz; unweighted RMS	[6]	-	77	-	dB
THD+N	total harmonic distortion-plus-noise	**BTSC stereo** with L or R only; 100 % modulation; f_i = 1 kHz; unweighted RMS	[6]	-	0.23	-	%
$\alpha_{cs(stereo)}$	stereo channel separation	L or R only; 50 Hz to 10 kHz					
		10 % EIM	[7]	-	≥ 32	-	dB
		1 % to 66 % EIM	[7]	-	≥ 27	-	dB
ΔG_f	frequency gain variation	30 % modulation; f_{ref} = 1 kHz					
		stereo; L or R only		-	–0.4 to +1.5	-	dB
		mono; L = R		-	–0.2 to +0.04	-	dB
Audio M standard SAP characteristics (DDEP standard code = 13, driven with external SSIF)							
S/N	signal-to-noise ratio	100 % modulation; f_i = 1 kHz; compromise de-emphasis (register SAPDBX = 0b); bandwidth = 0 kHz to 15 kHz; unweighted RMS	[6]	-	59	-	dB
THD+N	total harmonic distortion-plus-noise	100 % modulation; f_i = 1 kHz; compromise de-emphasis (register SAPDBX = 0b); bandwidth = 0 kHz to 15 kHz; unweighted RMS	[6]	-	0.27	-	%

Table 26. Audio and video decoder characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Audio M standard EIAJ characteristics (DDEP standard code = 14, driven with external SSIF)							
S/N	signal-to-noise ratio	100 % modulation; f_i = 1 kHz; unweighted RMS					
		EIAJ stereo with L or R; at EIAJ decoder output	[6]	-	61	-	dB
		EIAJ dual; at EIAJ sub-channel decoder output	[8]	-	59	-	dB
THD+N	total harmonic distortion-plus-noise	100 % modulation; f_i = 1 kHz; unweighted RMS					
		EIAJ stereo with L or R; at EIAJ decoder output	[6]	-	0.17	-	%
		EIAJ dual; at EIAJ sub-channel decoder output	[8]	-	0.8	-	%
$\alpha_{ct(dual)}$	dual crosstalk attenuation	100 % modulation; f_i = 1 kHz					
		main to sub-channel		-	80	-	dB
		sub to main channel		-	80	-	dB
$\alpha_{cs(stereo)}$	stereo channel separation	50 % modulation; selective RMS; L or R					
		100 Hz to 5 kHz		-	38	-	dB
		50 Hz to 8 kHz		-	28	-	dB
ΔG_f	frequency gain variation	**EIAJ stereo**; from 20 Hz to 12 kHz; 15 % modulation; f_{ref} = 1 kHz		-	–0.9 to +0.1	-	dB
Audio FM radio characteristics (DDEP standard code = 15 to 18, driven with external SSIF)							
S/N	signal-to-noise ratio	**FM radio stereo** with L or R only; 10.7 MHz carrier; 100 % modulation; f_i = 1 kHz; 75 µs de-emphasis; unweighted RMS	[6]	-	55	-	dB
THD+N	total harmonic distortion-plus-noise	**FM radio stereo** with L or R only; 10.7 MHz carrier; 100 % modulation; f_i = 1 kHz; 75 µs de-emphasis; unweighted RMS	[6]	-	0.2	-	%
$\alpha_{cs(stereo)}$	stereo channel separation	60 % modulation; selective RMS; pre-emphasis off; 100 Hz to 14 kHz		-	45 to 55	-	dB

Table 26. Audio and video decoder characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔG_f	frequency gain variation	**FM radio stereo**; from 20 Hz to 15 kHz; 10.7 MHz carrier; 75 µs de-emphasis; 30 % modulation; f_{ref} = 1 kHz	-	–0.2 to +0.4	-	dB
Audio identification of EIAJ mono/stereo (Japanese) standards, driven with external SSIF						
m_{pilot}	modulation degree of pilot tone	nominal pilot level and identification frequency; no overmodulation				
		European system	-	10	-	%
		Japanese system	-	21	-	%
Δf_{ident}	identification frequency window	M standard (EIAJ)				
		stereo; slow mode	-	981.9 to 983.0	-	Hz
		stereo; fast mode	-	979.7 to 985.1	-	Hz
		slow mode	-	921.8 to 923.0	-	Hz
		fast mode	-	919.3 to 925.8	-	Hz
$t_{d(on)(ident)}$	identification on delay time	slow mode	-	2	-	s
		fast mode	-	0.5	-	s
$t_{d(off)(ident)}$	identification off delay time	slow mode	-	2	-	s
		fast mode	-	0.5	-	s
Audio Automatic Standard Detection (ASD) timing; STDSEL = 1Dh						
$t_{asd(mono)}$	mono automatic standard detection time	default threshold settings	-	65	-	ms
$t_{asd(stereo)}$	stereo automatic standard detection time	BTSC stereo [9]	-	0.25	-	s
		BTSC SAP [9]	-	0.3	-	s
		EIAJ [9]	-	0.5	-	s
All digital I/Os: GPIO pins and BST test pins (5 V tolerant)						
Pins GPIO0 to GPIO23, V_CLK, GPIO25 to GPIO27, TDID, TDOD, TMSD, TCKD and TRSTD_N						
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V
V_{IL}	LOW-level input voltage		–0.3	-	+0.8	V
I_{LI}	input leakage current		-	-	1	µA
$I_{L(I/O)}$	leakage current (I/O)	3.3 V signal levels at $V_{DDD} \geq 3.3$ V	-	-	10	µA
C_i	input capacitance	I/O at high-impedance	-	-	8	pF
V_{OH}	HIGH-level output voltage	I_O = –2 mA	2.4	-	V_{DDD} + 0.5	V
V_{OL}	LOW-level output voltage	I_O = 2 mA	0	-	0.4	V

Table 26. Audio and video decoder characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{pd}	pull-down resistance	$V_I = V_{DDD}$		-	50	-	kΩ
R_{pu}	pull-up resistance	$V_I = 0$ V		-	50	-	kΩ
Audio-video port outputs (digital video stream from comb filter decoder or scaler, digital audio from sound decoder or baseband audio inputs through I²S-bus)							
LLC and LLC2 clock output on pin V_CLK; see Figure 13							
$C_{o(L)}$	output load capacitance			15	-	50	pF
T_{cy}	cycle time	LLC active		35	-	39	ns
		LLC2 active		70	-	78	ns
δ	duty cycle	C_L = 40 pF	[10]				
		LLC active		35	-	65	%
		LLC2 active		35	-	65	%
t_r	rise time	0.4 V to 2.4 V		-	-	5	ns
t_f	fall time	2.4 V to 0.4 V		-	-	5	ns
Video data output with respect to signal V_CLK on pins GPIO0 to GPIO17, GPIO22 and GPIO23; see Figure 13							
$C_{o(L)}$	output load capacitance			15	-	50	pF
$t_{h(o)}$	output hold time	LLC active	[11][12]	5	-	-	ns
		LLC2 active		15	-	-	ns
t_{PD}	propagation delay	from positive edge of signal V_CLK	[11][12]				
		LLC active		-	-	28	ns
		LLC2 active		-	-	55	ns

[1] Nominal analog video input signal is to be terminated by 75 Ω that results in 1 V (p-p) amplitude. This termination resistor should be split into 18 Ω and 56 Ω, and the dividing tap should feed the video input pin, through a coupling capacitor of 47 nF, to achieve a control range from −3 dB (attenuation) to +6 dB (amplification) for the internal automatic gain control.

[2] Lower limit of AGC

[3] Definition of levels and level setting:

a) The full-scale level for analog audio signals V_{FS} = 0.8 V (RMS). The nominal level at the digital crossbar switch is defined at −15 dB (FS).

b) Nominal audio input levels: external, mono, V_i = 180 mV (RMS); −15 dB (FS).

[4] The analog audio inputs (pins LEFT1, RIGHT1, LEFT2 and RIGHT2) are supported by two input levels: 1 V (RMS) and 2 V (RMS), selectable independently per stereo input pair, LEFT1, RIGHT1 and LEFT2, RIGHT2.

[5] V_{DDA} = 3.3 V; $V_{i(SIF)}$ = 196 mV (RMS); level and gain settings according to Table note [3]; for external components see the application diagram in the *Application Notes SAA7131E*; unless otherwise specified.

[6] Characterizing AM demodulator or measured at BTSC, SAP, EIAJ or FM decoder output, respectively.

[7] Effective Input Modulation (EIM) means 75 µs de-emphasis applied to audio input signals of the BTSC stereo encoder.

[8] Characterizing EIAJ sub-channel decoder output.

[9] Detection times are the same for multi-channel sound standard detection.

[10] The definition of the duty factor: $\delta = t_{clk(H)} / T_{cy}$

[11] The output timing must be measured with the load of a 30 pF capacitor to ground and a 500 Ω resistor to 1.4 V.

[12] Signal V_CLK inverted; not delayed (default setup).

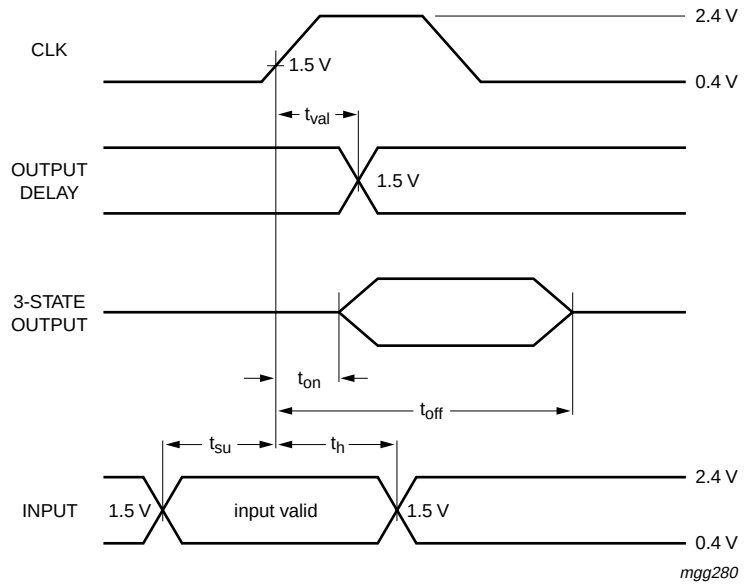


Fig 12. PCI I/O timing

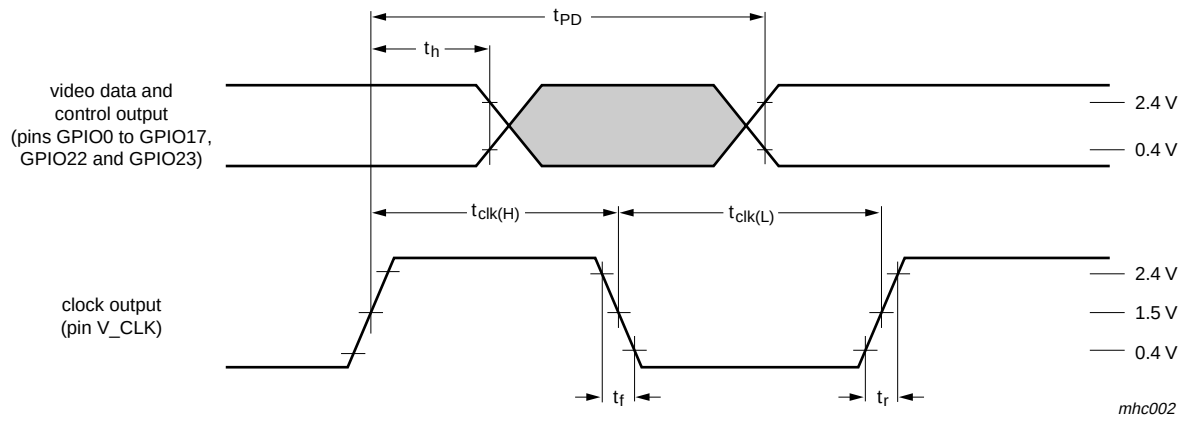


Fig 13. Data output timing (video data, control outputs and raw DTV/DVB)

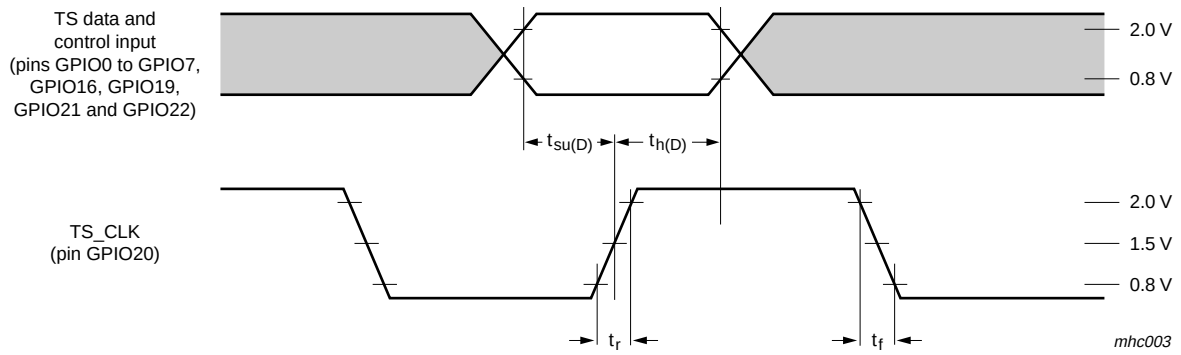


Fig 14. Data input timing (TS data and control inputs)

Table 27. Specification of crystal and related applications (examples)[1]

Standard	Crystal frequency 24.576 MHz			Unit
	Fundamental		3rd harmonic	
	2B	2C	2A	
Crystal specification				
Typical load capacitance	20	8	10	pF
Maximum series resonance resistance	30	60	80	Ω
Typical motional capacitance	20	1	1.5	fF
Maximum parallel capacitance	7	3.3	3.5	pF
Maximum permissible deviation	±30	±30	±50	ppm
Maximum temperature deviation	±30	±30	±20	ppm
External components				
Typical load capacitance at pin XTALII	27	5.6	18	pF
Typical load capacitance at pin XTALOI	27	5.6	18	pF
Typical capacitance of LC filter	-	-	1	nF
Typical inductance of LC filter	-	-	4.7	µH

[1] For oscillator application, see the *Application Notes SAA7131E*.

11. Support information

11.1 Related documents

This document describes the functionality and characteristics of the SAA7131E. Other documents related to the SAA7131E are as follows:

- *User Manual SAA7131E*, describing the programming aspects
- *Application Notes SAA7131E*, focusing on recommendations for system implementation

12. Test information

12.1 Boundary scan test

The SAA7131E has built-in logic and five dedicated pins to support boundary scan testing which allows board testing without special hardware (nails) according to *IEEE 1149.1* of the Joint Test Action Group (JTAG) as chaired by NXP.

The 5 special pins are: Test Mode Select (TMS), Test Clock (TCK), Test Reset (TRST_N), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, SAMPLE, CLAMP and IDCODE are all supported; see Table 29. Details about the JTAG BST test can be found in the specification *IEEE 1149.1*. A file containing the detailed Boundary Scan Description Language (BSDL) description of the SAA7131E is available on request.

12.1.1 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in the functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state if pin TRST_N is at LOW level.

Table 28. Boundary scan test naming conventions

Pin		Boundary scan test signals
IF part	Decoder part	
TMSI	TMSD	test mode select input
TCKI	TCKD	test clock input
TRSTI_N	TRSTD_N	test reset input
TDII	TDID	test data input
TDOI	TDOD	test data output

Table 29. BST instructions supported by the SAA7131E

Instruction	Description
BYPASS	This mandatory instruction provides a minimum length serial path (1 bit) between pins TDI and TDO when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.

12.1.2 Device identification codes

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected internally between pins TDI and TDO of the IC. The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller and this code can subsequently be shifted out. At board level, this code can be used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDI) and bit 0 is the least significant bit (nearest to TDO); see Figure 15 and Figure 16.

A device identification register as specified in *IEEE 1149.1*, is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and determination of the version number of ICs during field service.

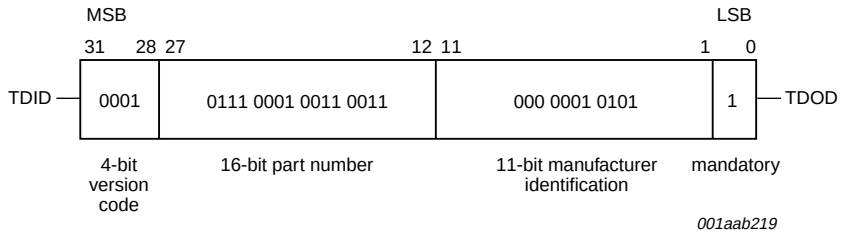


Fig 15. 32 bits of identification code, decoder part

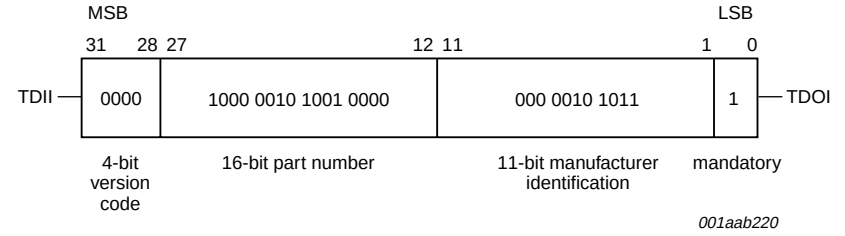
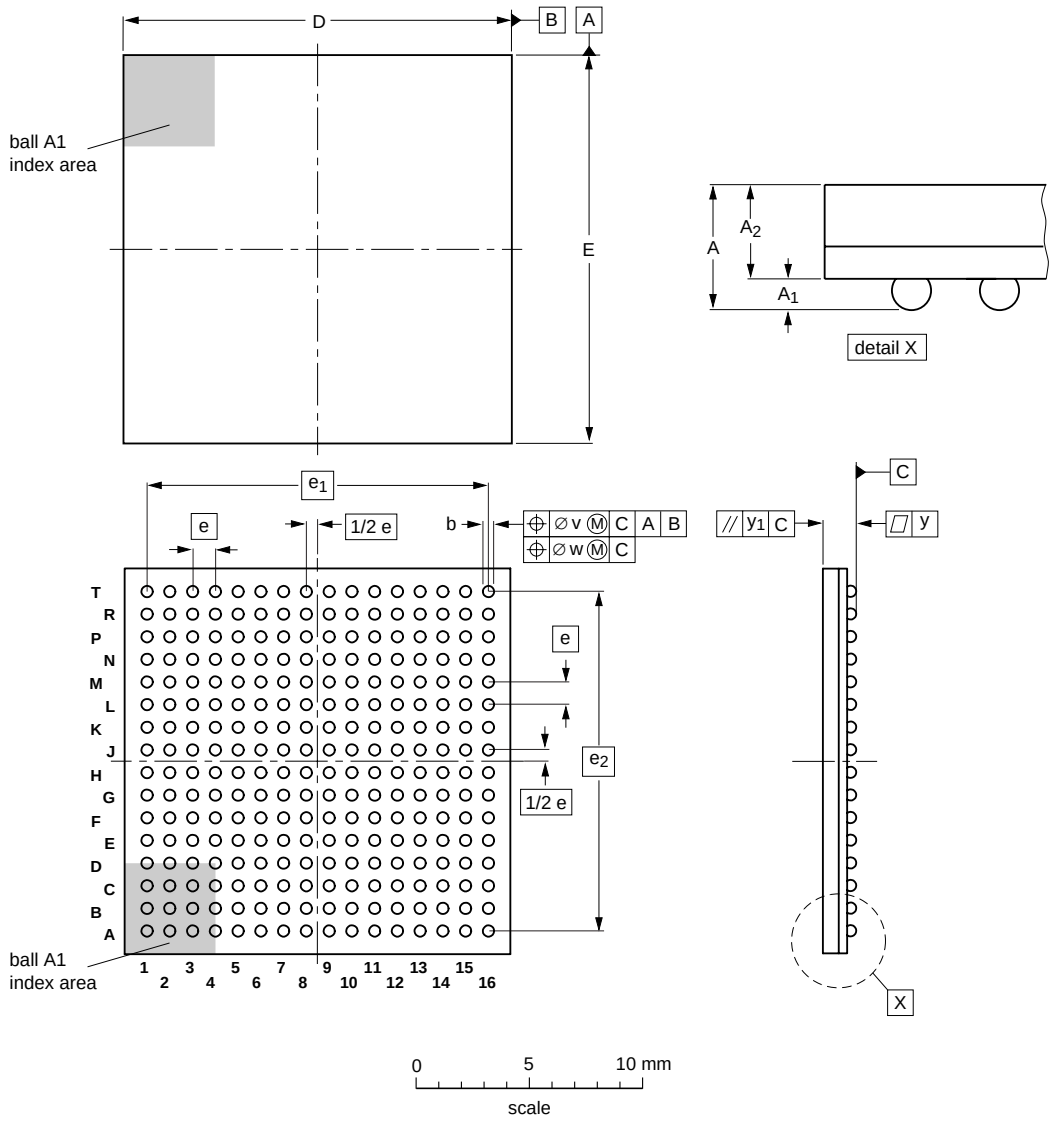


Fig 16. 32 bits of identification code, IF demodulator part

13. Package outline

LBGA256: plastic low profile ball grid array package; 256 balls; body 17 x 17 x 1 mm **SOT740-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.55	0.45 0.35	1.1 0.9	0.55 0.45	17.2 16.8	17.2 16.8	1	15	15	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT740-2	- - -	MO-192	- - -			~~05-06-16~~ 05-08-04

Fig 17. Package outline SOT740-2 (LBGA256)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 30 and 31

Table 30. SnPb eutectic process (from J-STD-020C)

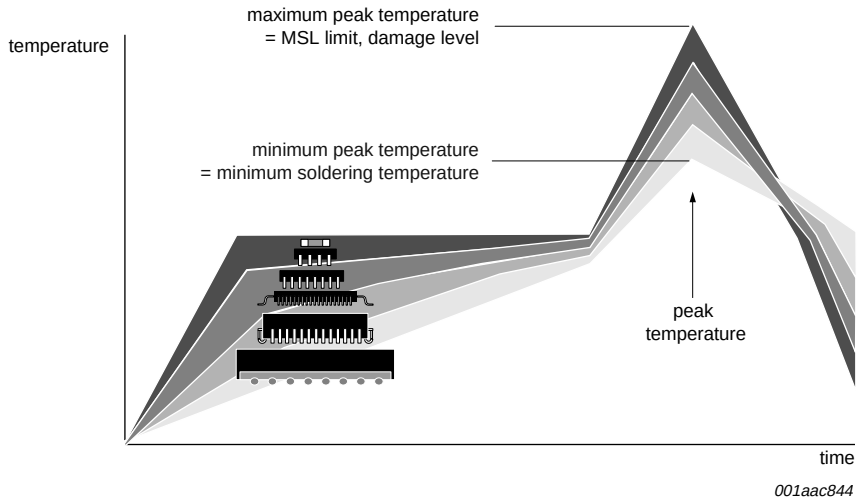
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 31. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 32. Abbreviations

Acronym	Description
2CS	2-Carrier System
A/V	Audio and Video
AC-3	Audio Code 3 (Dolby Digital)
ACPI	Advanced Configuration Power Interface
ADC	Analog-to-Digital Converter
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AM	Amplitude Modulation
ATSC	Advanced Television Systems Committee
AVL	Automatic Volume Levelling
BSDL	Boundary Scan Description Language
BST	Boundary Scan Test
BTSC	Broadcast Television Systems Committee
CC	Closed Captioning (in running text)
	Color Carrier (in Characteristics)
CD-ROM	Compact Disk Read Only Memory
CGMS	Copy Guard Management System
CIF	Common Intermediate Format[1]
CMOS	Complementary MOS

Table 32. Abbreviations *...continued*

Acronym	Description
CPU	Central Processing Unit
CVBS	Composite Video Blanking Sync[2]
DAC	Digital-to-Analog Converter
DDEP	Demodulator and Decoder Easy Programming
DMA	Direct Memory Access
DMSD	Digital MultiStandard Decoder
DQPSK	Differential Quadrature Phase Shift Keying
DSP	Digital Signal Processor
DTV	Digital TeleVision
DVB	Digital Video Broadcasting
DVB-C	DVB-Cable
DVB-S	DVB-Satellite
DVB-T	DVB-Terrestrial
DVD	Digital Video Disc
DVR	Digital Video Recorder
EAV	End of Active Video
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
EIAJ	Electronic Industries Association of Japan
EIM	Effective Input Modulation
EPG	Electronic Program Guide
FCC	Federal Communications Commission
FID	Field-ID
FIFO	First-in First-Out
FIR	Finite-Impulse Response
FLC	Frame-Locked Clock
FM	Frequency Modulation
FS	Full-Scale
GDE	Group Delay Equalizer
GPIO	General Purpose Input/Output
H/V	Horizontal/Vertical
HAD	Half-Amplitude Duration
I^2C	Inter-IC-Connection
I^2S	Inter-IC Sound
I/O	Input/Output
IC	Integrated Circuit
ID	IDentifier
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
INT	INTerrupt

Table 32. Abbreviations *…continued*

Acronym	Description
IRE	Institute of Radio Engineers
IRQ	Interrupt ReQuest
ITU	International Telecommunication Union
ITU-R	ITU-Radiocommunication sector
ITU-T	ITU-Telecommunication standardization sector
JTAG	Joint Test Action Group
JEDEC	Joint Electron Device Engineering Council
JEITA	Japan Electronics and Information Technology industrial Association
LLC	Line-Locked Clock
MMU	Memory Management Unit
MOS	Metal-Oxide-Semiconductor
MPEG	Motion Picture Experts Group
MPX	MultiPleX
MUX	MUltipleXer
NABTS	North American Broadcast Text System
NICAM	Near-Instantaneously Companded Audio Multiplex
NPC	Neighbor Picture Carrier
NSC	Neighbor Sound Carrier
NTSC	National Television Systems Committee
OS	Operating System
PAL	Phase Alternating Line
PC	Personal Computer (in running text)
	Picture Carrier (in Characteristics)
PCI	Peripheral Component Interconnect
PLL	Phase-Locked Loop
PS	Program Stream
PVR	Personal Video Recorder
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation
QFDM	Quadrature Frequency Division Modulation
QSS	Quasi Split Sound
RC	Resistor Capacitor (electrical filter network)
RF	Radio Frequency
RGB	Red-Green-Blue (additive color space)
RISC	Reduced Instruction Set Computing
RMS	Root Mean Square
SAP	Secondary Audio Program
SAV	Start of Active Video
SAW	Surface Acoustic Wave
SC	Sound Carrier
SCART	Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs

Table 32. Abbreviations *...continued*

Acronym	Description
SECAM	Systeme Electronique Couleur Avec Mémoire (French color TV standard)
SIF	Sound IF
SIG	Special Interest Group
SMD	Surface Mounted Device
SOP	Start Of Packet
SSIF	Second SIF
TAP	Test Access Port
THD	Total Harmonic Distortion
TS	Transport Stream
TV	TeleVision
UK	United Kingdom
UNIX	UNIpleXed information and computing system
USA	United States of America
VESA	Video Electronics Standards Association
VBI	Vertical Blanking Interval
VCR	Video Cassette Recorder
VGA	Video Graphic Adapter
VIP	VESA video Interface Port
VITC	Vertical Interval Time Codes
VMI	Video Module Interface
VPS	Video Programming System
VSB	Vestigial SideBand modulation
VITC	Vertical Interval Time Codes
WSS	Wide Screen Signaling
WST	World System Teletext
XTAL	CrystTAL[3]
ZV	Zoom Video

[1] CIF is a video resolution of 352 × 240 pixel (NTSC) and 352 × 288 pixel (PAL).

[2] CVBS is also known as “composite video signal”.

[3] X became a synonym for Crys.

16. Glossary

dbx — American company, which has invented the dbx-TV noise reduction system used within BTSC as based on dynamic compression.

FM A2 — FM modulated sound system based on 2 analog carriers, transporting either the signals (L + R) / 2 and 2R or the dual signals A and B.

Hilbert, David — German mathematician; so-called Hilbert transformation is a special way to filter signals.

Incredible Mono — An algorithm which adds stereo-like sound impression to monaural audio signals.

Incredible Stereo — An algorithm which makes stereo sound impression wider. The distance between the two loudspeakers seems to become greater.

IRE — A unit of an arbitrary scale dividing the 1 V (p-p) video signal from the bottom of sync (−40 IRE) to the peak white level (+100 IRE) into 140 equal units. The active video range lasts from 0 IRE to 100 IRE.

LCR — Electrical filter network which uses inductors (L), capacitors (C) and resistors (R).

MPEG-2 — Standard for A/V coding and data compression; successor of MPEG-1.

Nyquist, Harry — American physicist, who developed modern sampling theory.

PCTV — An application which allows to watch TV on a PC.

PowerPC — Performance optimization with enhanced RISC Performance Chip

S-video — Separated video (signals for luminance Y and modulated chrominance C)

YUV — Component video (signals for luminance Y and chrominance vectors U,V)

17. References

[1] **BS.468 —** ITU-R Recommendation concerning Broadcasting (Sound): “Measurement of audio-frequency noise voltage level in sound broadcasting”

[2] **BT.601 —** ITU-R Recommendation concerning Broadcasting (Television): “Studio encoding parameters of digital television for standard 4 : 3 and wide-screen 16 : 9 aspect ratios”

[3] **BT.656 —** ITU-R Recommendation concerning Broadcasting service (Television): “Interfaces for digital component video signals in 525-line and 625-line television systems operating at the 4 : 2 : 2 level of ITU-R BT.601 (Part A)”

[4] **JESD22-114-D —** JEDEC Standard 22, Test Method A114-D (preferably used): “Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)”

[5] **JESD22-115-A —** JEDEC Standard 22, Test Method A115-A (currently not used): “Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)”

[6] **J.61 —** ITU-T Recommendation for cable networks and transmission of television, sound programme and other multimedia signals: “Transmission performance of television circuits designed for use in international connections”

[7] **IEEE 1149.1 —** IEEE “Standard Test Access Port and Boundary Scan Architecture” according to JTAG, issued in 1990, 1993, 1994 and 2001.

18. Revision history

Table 33. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAA7131E_3	20080519	Product data sheet	CPCN200606027	SAA7131E_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors • Legal texts have been adapted to the new company name where appropriate • Selective improvements in style or wording • Update of other ICs mentioned • Update due to package change (Section 2.1, Table 1, Figure 3 and Figure 17) • Harmonized content of Table 3 with table title captions from Section 6.2 • Update of hexadecimal notation (Figure 6) • Corrected error in Revision ID, see Table 14 • Adjusted Symbols and Parameters to latest standards (Section 8 to Section 10) • Rearranged data to improve clarity (Section 8 and Section 10) • Changed table title captions to improve readability (Table 24 to Table 26) • Update of symbols (Figure 13) • Update of binary notation (Figure 15 and Figure 16) • Moved former chapter “Related documents” to Section 11 • New: Abbreviations, Glossary and References (Section 15 to Section 17)			
SAA7131E_2	20050610	Product data sheet	-	SAA7131E_1
SAA7131E_1	20041209	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

19.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

19.4 Licenses

ICs with Macrovision copyright protection technology

This product incorporates copyright protection technology that is protected by method claims of certain U.S. patents and other intellectual property rights owned by Macrovision Corporation and other rights owners. Use of this copyright protection technology must be authorized by Macrovision Corporation and is intended for home and other limited viewing uses only, unless otherwise authorized by Macrovision Corporation. Reverse engineering or disassembly is prohibited.

Purchase of NXP ICs with digital dbx-TV noise reduction functionality

Licensed Chips — Purchase of NXP Semiconductors ICs with digital dbx-TV noise reduction functionality for which on top of the IC price, the related THAT Corporation royalty payment is paid to NXP Semiconductors, includes a license from THAT Corporation to use the ICs in a BTSC decoding application.

Unlicensed Chips — Purchase of NXP Semiconductors ICs with digital dbx-TV noise reduction functionality for which on top of the IC price, no related THAT Corporation royalty payment is paid to NXP Semiconductors, is only permitted to parties who according to information supplied to NXP Semiconductors by THAT Corporation, have a BTSC set-maker license from THAT Corporation,
45 Summer street, Milford, Massachusetts 01757-1656, USA.

19.5 Patents

Notice is herewith given that the subject device uses one or more of the following patents and that each of these patents may have corresponding patents in other jurisdictions.

US 4907093 — owned by Macrovision Corporation

19.6 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

Silicon Tuner — is a trademark of NXP B.V.

20. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

21. Tables

22. Figures

23. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 19 May 2008
Document identifier: SAA7131E_3