SONY

CXD1199AQ

CD-ROM DECODER

For the availability of this product, please contact the sales office.

Description

The CXD1199AQ is a CD-ROM decoder LSI with a built-in ADPCM decoder.

Features

- Supports CD-ROM, CD-I and CD-ROM XA formats
- Real-time error correction
- Supports double speed playback
- Connectable with standard SRAM of up to 1 M-bits (128 K-byte)
- All audio output sampling frequencies : 132.3 kHz (built-in oversampling filter)
- De-emphasis digital filter
- Digital attenuator
- Intel CPU 80 series host interface
- Operates on 3.5 V

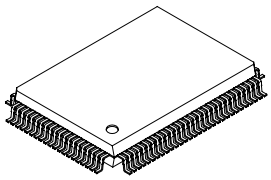
Applications

CD-ROM drives

Structure

Silicon gate CMOS IC

100 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

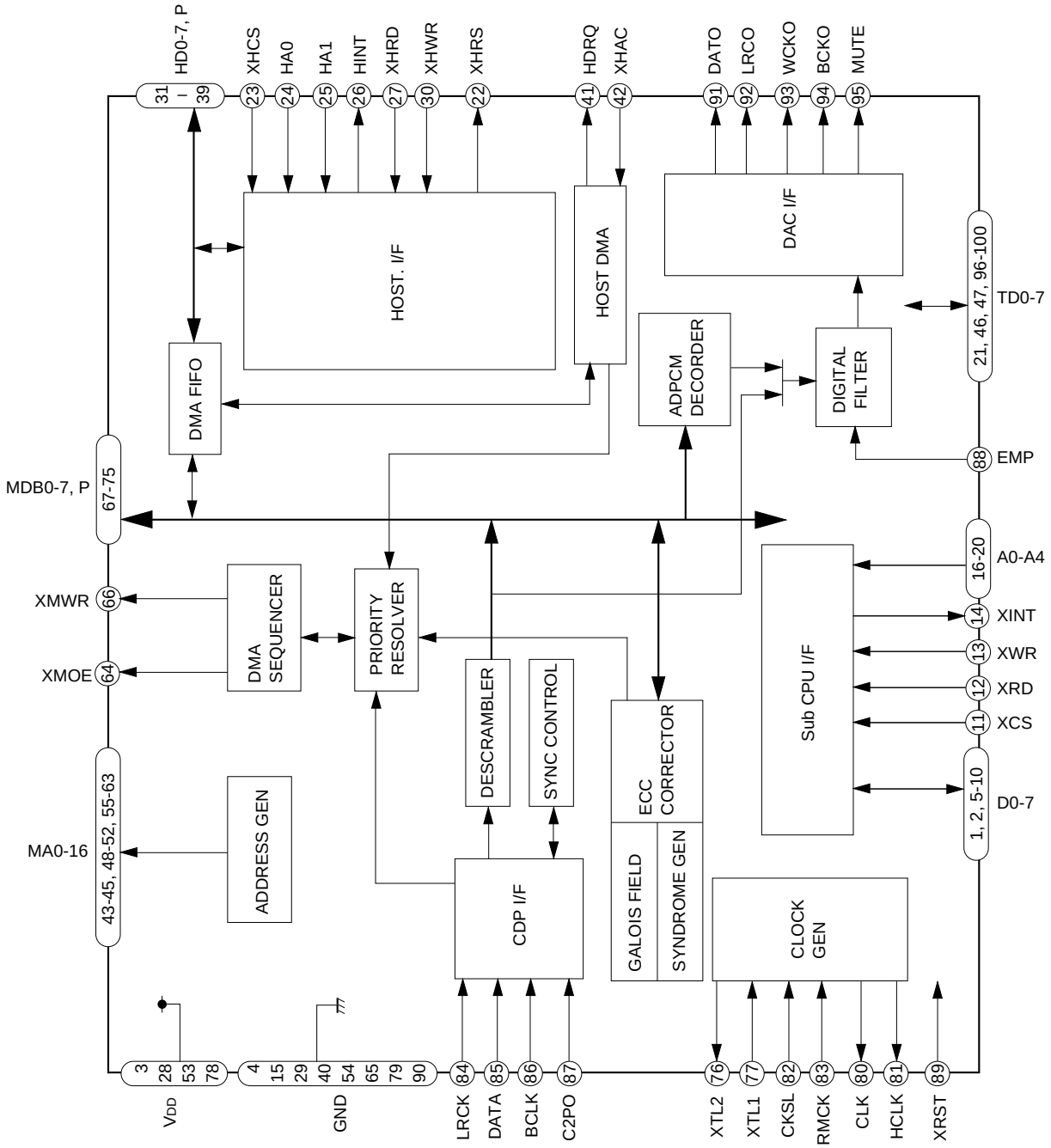
• Supply voltage	V_{DD}	–0.5 to +7.0	V
• Input voltage	V_I	–0.5 to V_{DD} +0.5	V
• Output voltage	V_O	–0.5 to V_{DD} +0.5	V
• Operating temperature	Topr	–20 to +75	℃
• Storage temperature	Tstg	–55 to +150	℃

Recommended Operating Conditions

• Supply voltage	V_{DD}	+3.5 to +5.5 (+5.0 typ.)	V
• Operating temperature	Topr	–20 to +75	℃

E93Z06A78-TE

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	D0	I/O	Sub CPU data bus
2	D1	I/O	Sub CPU data bus
3	V_{DD}	—	Power supply (+5 V)
4	GND	—	GND
5	D2	I/O	Sub CPU data bus
6	D3	I/O	Sub CPU data bus
7	D4	I/O	Sub CPU data bus
8	D5	I/O	Sub CPU data bus
9	D6	I/O	Sub CPU data bus
10	D7	I/O	Sub CPU data bus
11	XCS	I	IC select negative logic signal from sub CPU
12	XRD	I	Sub CPU strobe negative logic signal to read this IC internal register
13	XWR	I	Sub CPU strobe negative logic signal to write this IC internal register
14	XINT	O	Interrupt request negative logic signal from IC to sub CPU
15	GND	—	GND
16	A0	I	Sub CPU address
17	A1	I	Sub CPU address
18	A2	I	Sub CPU address
19	A3	I	Sub CPU address
20	A4	I	Sub CPU address
21	TD0	I/O	Test I/O
22	XHRS	O	Negative logic signal indicating that IC has been reset from host; open drain output
23	XHCS	I	IC select negative logic signal from host
24	HA0	I	Host address signal
25	HA1	I	Host address signal
26	HINT	O	Interrupt request negative logic signal to host; open drain output
27	XHRD	I	Host strobe negative logic signal to read this IC internal register
28	V_{DD}	—	Power supply (+5 V)
29	GND	—	GND
30	XHWR	I	Host strobe negative logic signal to read this IC internal register
31	HD0	I/O	Host data bus
32	HD1	I/O	Host data bus
33	HD2	I/O	Host data bus
34	HD3	I/O	Host data bus
35	HD4	I/O	Host data bus

Pin No.	Symbol	I/O	Description
36	HD5	I/O	Host data bus
37	HD6	I/O	Host data bus
38	HD7	I/O	Host data bus
39	HDP	I/O	Host data bus
40	GND	—	GND
41	HDRQ	O	Host DMA request positive logic signal
42	XHAC	I	Host DMA acknowledge negative logic signal
43	MA0	O	Buffer memory address (LSB)
44	MA1	O	Buffer memory address
45	MA2	O	Buffer memory address
46	TD1	I/O	Test I/O
47	TD2	I/O	Test I/O
48	MA3	O	Buffer memory address
49	MA4	O	Buffer memory address
50	MA5	O	Buffer memory address
51	MA6	O	Buffer memory address
52	MA7	O	Buffer memory address
53	V_{DD}	—	Power supply (+5 V)
54	GND	—	GND
55	MA8	O	Buffer memory address
56	MA9	O	Buffer memory address
57	MA10	O	Buffer memory address
58	MA11	O	Buffer memory address
59	MA12	O	Buffer memory address
60	MA13	O	Buffer memory address
61	MA14	O	Buffer memory address
62	MA15	O	Buffer memory address
63	MA16	O	Buffer memory address
64	XMOE	O	Buffer memory output enable negative logic signal
65	GND	—	GND
66	XMWR	O	Buffer memory write enable negative logic signal
67	MDB0	I/O	Buffer memory data bus
68	MDB1	I/O	Buffer memory data bus
69	MDB2	I/O	Buffer memory data bus
70	MDB3	I/O	Buffer memory data bus

Pin No.	Symbol	I/O	Description
71	MDB4	I/O	Buffer memory data bus
72	MDB5	I/O	Buffer memory data bus
73	MDB6	I/O	Buffer memory data bus
74	MDB7	I/O	Buffer memory data bus
75	MDBP	I/O	Buffer memory data bus (for error flag)
76	XTL2	O	Crystal oscillation circuit output
77	XTL1	I	Crystal oscillation circuit output (16.9344 MHz)
78	V_{DD}	—	Power supply (+5 V)
79	GND	—	GND
80	CLK	O	16.9344 MHz clock output
81	HCLK	O	8.4672 MHz clock output
82	CKSL	I	Clock select signal for CD-ROM decoder
83	RMCK	I	Clock signal for CD-ROM decoder
84	LRCK	I	LR clock signal from CD DSP (for discriminating L, R channels)
85	DATA	I	Data signal from CD DSP
86	BCLK	I	DATA pin strobe clock signal (bit clock)
87	C2PO	I	Error flag (C2 pointer) positive logic signal from CD DSP
88	EMP	I	Emphasis ON positive logic signal from CD DSP
89	XRST	I	Reset negative logic signal
90	GND	—	GND
91	DATO	O	Data signal to DAC (D/A converter)
92	LRCO	O	LR clock signal to DAC
93	WCKO	O	Word clock signal to DAC
94	BCKO	O	Bit clock signal to DAC
95	MUTE	O	Mute positive logic signal
96	TD7	I/O	Test I/O
97	TD6	I/O	Test I/O
98	TD5	I/O	Test I/O
99	TD4	I/O	Test I/O
100	TD3	I/O	Test I/O

Electrical Characteristics

DC characteristics

(V_{DD}=5 V±10 %, V_{SS}=0 V, Topr=–20 to 75 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
TTL input level pin *1 High level input voltage	V_{IH1}		2.2			V
TTL input level pin *1 Low level input voltage	V_{IL1}				0.8	V
CMOS input level pin *2 High level input voltage	V_{IH2}		0.7 V_{DD}			V
CMOS input level pin *2 Low level input voltage	V_{IL2}				0.3 V_{DD}	V
CMOS Schmitt input level pin *3 High level input voltage	V_{IH4}		0.8 V_{DD}			V
CMOS Schmitt input level pin *3 Low level input voltage	V_{IL4}				0.2 V_{DD}	V
CMOS Schmitt input level pin *3 Input voltage hysteresis	V_{IH4}–V_{IL4}			0.6		V
TTL Schmitt input level pin *4 High level input voltage	V_{IH5}		2.2 V			V
TTL Schmitt input level pin *4 Low level input voltage	V_{IL5}				0.8 V	V
TTL Schmitt input level pin *4 Input voltage hysteresis	V_{IH5}–V_{IL4}			0.4		V
Bidirectional pin with pull-up resistance *5 Input current	I_{IL3}	V_{IN}=0 V	–90	–200	–440	µA
Input pin with pull-up resistance *6 Input current	I_{IL4}	V_{IN}=0 V	–40	–100	–240	µA
High level output voltage *7	V_{OH1}	I_{OH}=–2 mA	V_{DD}–0.8			V
Low level output voltage *7	V_{OL1}	I_{OL}=4 mA			0.4	V
Input leakage current *8	Iη	V_{IN}=V_{SS} or V_{DD}	–10		10	µA
Output leakage current *9	I_{OZ}	High-impedance state	–40		40	µA
Oscillation cell *10 High level input voltage	V_{IH4}		0.7 V_{DD}			V
Oscillation cell Low level input voltage	V_{IL4}				0.3 V_{DD}	V
Oscillation cell Logic threshold value	LV_{TH}			0.5 V_{DD}		V
Oscillation cell Feedback resistance value	R_{FB}	V_{IN}=V_{SS} or V_{DD}	250 K	1 M	2.5 M	Ω
Oscillation cell High level output voltage	V_{OH2}	I_{OH}=–3 mA	0.5 V_{DD}			V
Oscillation cell Low level output voltage	V_{OL2}	I_{OL}=3 mA			0.5 V_{DD}	V

AC characteristics (V_{DD}=3.5 V, V_{SS}=0 V, Topr=–20 to 75 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
TTL input level pin *1 High level input voltage	V_{IH1}		2.2			V
TTL input level pin *1 Low level input voltage	V_{IL1}				0.6	V
CMOS input level pin *2 High level input voltage	V_{IH2}		0.7 V_{DD}			V
CMOS input level pin *2 Low level input voltage	V_{IL2}				0.3 V_{DD}	V
CMOS Schmitt input level pin *3 High level input voltage	V_{IH4}		0.8 V_{DD}			V
CMOS Schmitt input level pin *3 Low level input voltage	V_{IL4}				0.2 V_{DD}	V
CMOS Schmitt input level pin *3 Input voltage hysteresis	V_{IH4}–V_{IL4}			0.5		V
TTL Schmitt input level pin *4 High level input voltage	V_{IH5}		2.2 V			V
TTL Schmitt input level pin *4 Low level input voltage	V_{IL5}				0.6 V	V
TTL Schmitt input level pin *4 Input voltage hysteresis	V_{IH5}–V_{IL4}			0.3		V
Bidirectional pin with pull-up resistance *5 Input current	I_{IL3}	V_{IN}=0 V	–20	–50	–110	µA
Input pin with pull-up resistance *6 Input current	I_{IL4}	V_{IN}=0 V	–10	–25	–60	µA
High level output voltage *7	V_{OH1}	I_{OH}=–1.6 mA	V_{DD}–0.8			V
Low level output voltage *7	V_{OL1}	I_{OL}=3.2 mA			0.4	V
Input leakage current *8	Iη	V_{IN}=V_{SS} or V_{DD}	–10		10	µA
Output leakage current *9	I_{OZ}	High-impedance state	–40		40	µA
Oscillation cell *10 High level input voltage	V_{IH4}		0.7 V_{DD}			V
Oscillation cell Low level input voltage	V_{IL4}				0.3 V_{DD}	V
Oscillation cell Logic threshold value	LV_{TH}			0.5 V_{DD}		V
Oscillation cell Feedback resistance value	R_{FB}	V_{IN}=V_{SS} or V_{DD}	1.2 M	2.5 M	5 M	Ω
Oscillation cell High level output voltage	V_{OH2}	I_{OH}=–1.3 mA	0.5 V_{DD}			V
Oscillation cell Low level output voltage	V_{OL2}	I_{OL}=1.3 mA			0.5 V_{DD}	V

*1. D7 to 0, A4 to 0, XWR, XRD, XCS, MDB7 to 0, MDBP, HD7 to 0, HDP, TD7 to 0
*2. DATA, LRCK, C2PO, EMP, CKSL, RMCK
*3. BCKL, XRST, CKSL
*4. A4 to 0, XWR, XRD, XCS, HA1, HA0, XHWR, XHRD, XHCS, XHAC
*5. D7 to 0, MDB7 to 0, MDBP, HD7 to 0, HDP, TD7 to 0
*6. HA1, HA0, XHWR, XHRD, XHCS, XHAC
*7. All output pins except XTL2.
*8. All input pins except *5, *6 and XTL1.
*9. HINT
*10. input : XTL1; output : XTL2

I/O capacitance (V_{DD}=V_I=0 V, f=1 MHz)

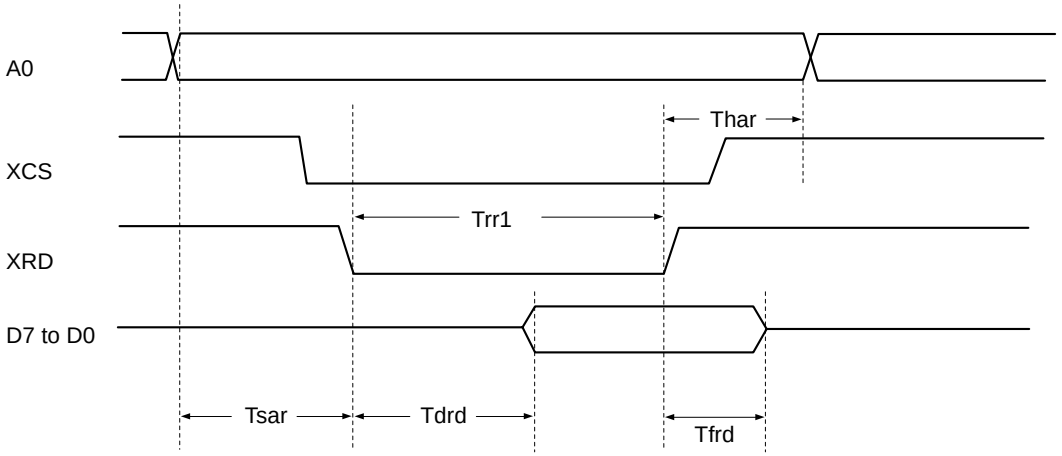
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			11	pF
I/O pin	C_{OUT}			11	pF

AC Characteristics (V_{DD}=5 V±10 %, V_{SS}=0 V, Topr=–20 to 75 °C, output load=50 pF)

Value in parentheses in the tables for V_{DD}=3.5 V, V_{SS}=0 V, Topr=–20 to +75 °C and output load=50 pF. Others for V_{DD}=5 V±10 % and V_{DD}=3.5 V.

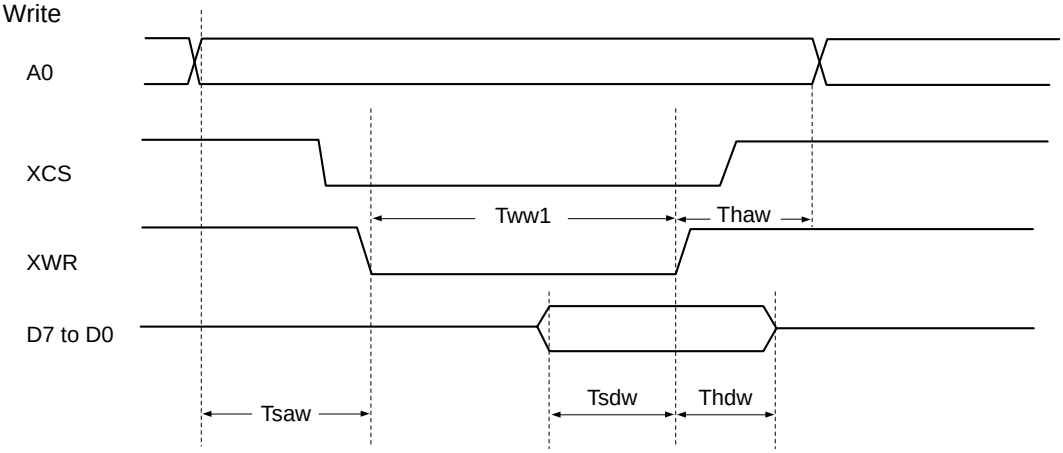
1. Sub CPU interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XCS & XRD ↓)	Tsar	30 (70)			ns
Address hold time (for XCS & XRD ↑)	Thar	20 (50)			ns
Data delay time (for XCS & XRD ↓)	Tdrd			60 (100)	ns
Data float time (for XCS & XRD ↑)	Tfrd	0		15 (25)	ns
Low level XRD pulse width	Trr1	100 (150)			ns

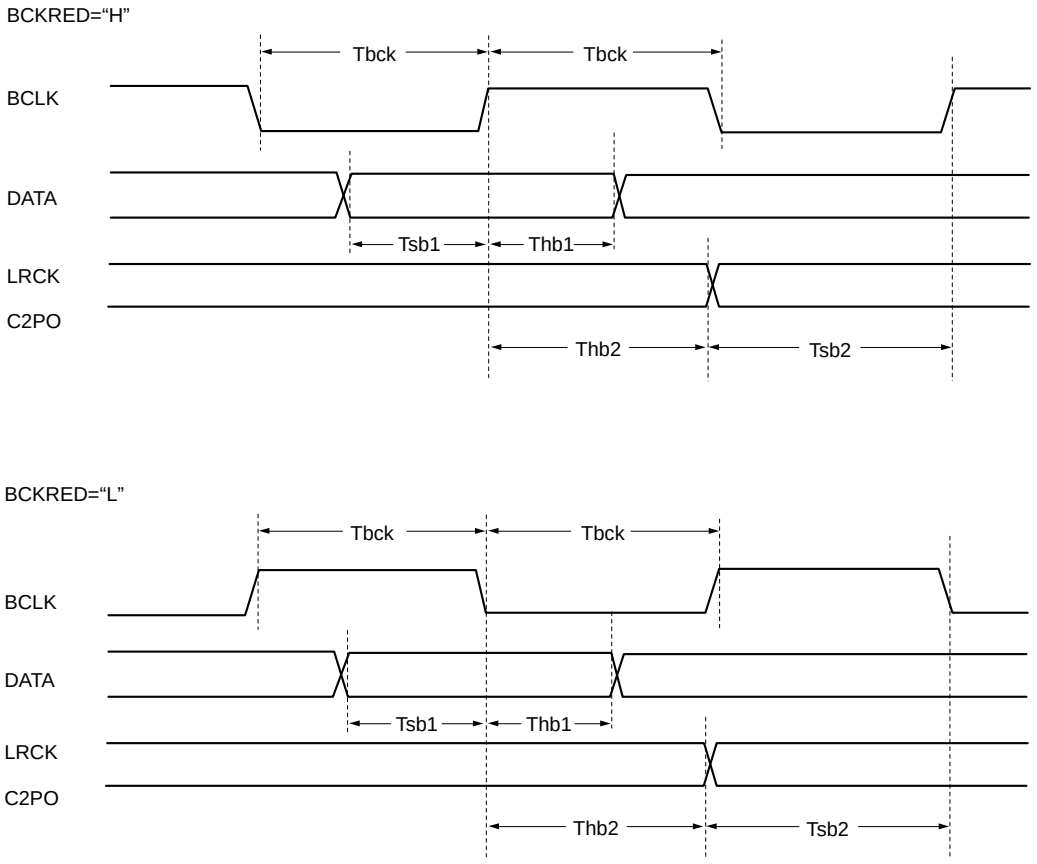
(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XCS & XWR ↓)	Tsaw	30 (70)			ns
Address hold time (for XCS & XWR ↑)	Thaw	20 (50)			ns
Data setup time (for XCS & XWR ↑)	Tsdw	40 (70)			ns
Data hold time (for XCS & XWR ↑)	Thdw	10 (30)			ns
Low level XWR pulse width	Tww1	50 (80)			ns

2. CD DSP Interface

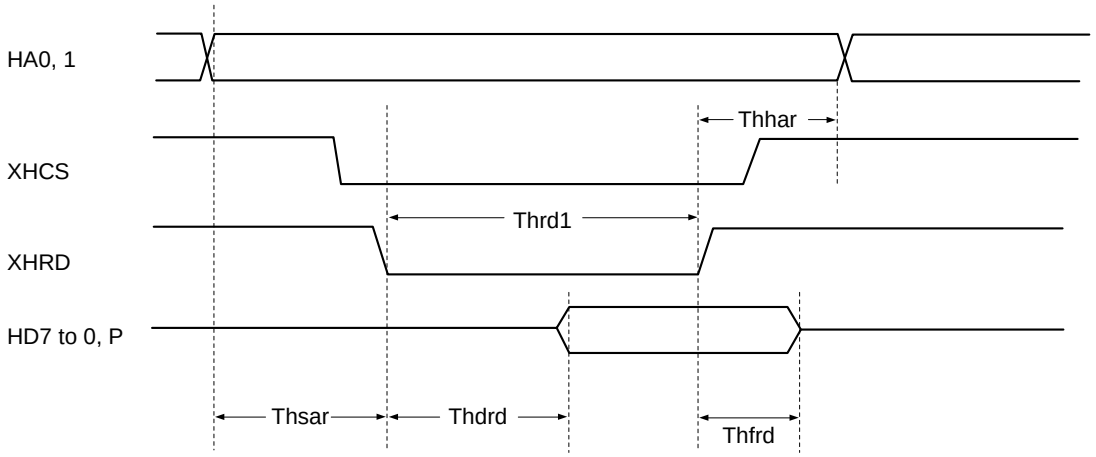
(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
BCLK frequency	Fbck			11.3	MHz
BCLK pulse width	Tbck	88			ns
Data setup time (for BCLK)	Tsb1	20			ns
Data hold time (for BCLK)	Thb1	20			ns
LRCK, C2PO setup time (for BCLK)	Tsb2	20			ns
LRCK, C2PO hold time (for BCLK)	Thb2	20			ns

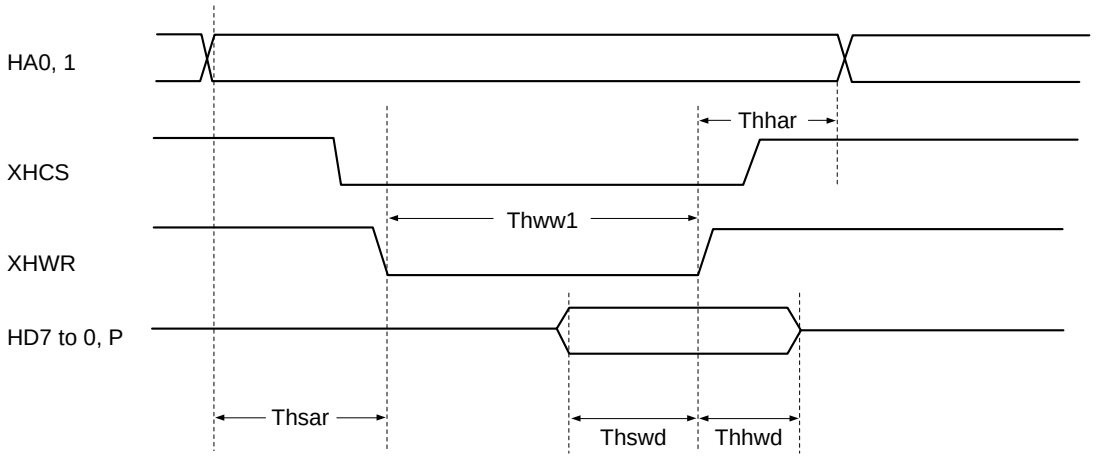
3. Host interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XHCS & XHRD ↓)	Thsar	30 (70)			ns
Address hold time (for XHCS & XHRD ↑)	Thhar	20 (50)			ns
Data delay time (for XHCS & XHRD ↓)	Thdrd			60 (100)	ns
Data float time (for XHCS & XHRD ↑)	Thfrd	0		15 (25)	ns
Low level XHRD pulse width	Thrd1	100 (150)			ns

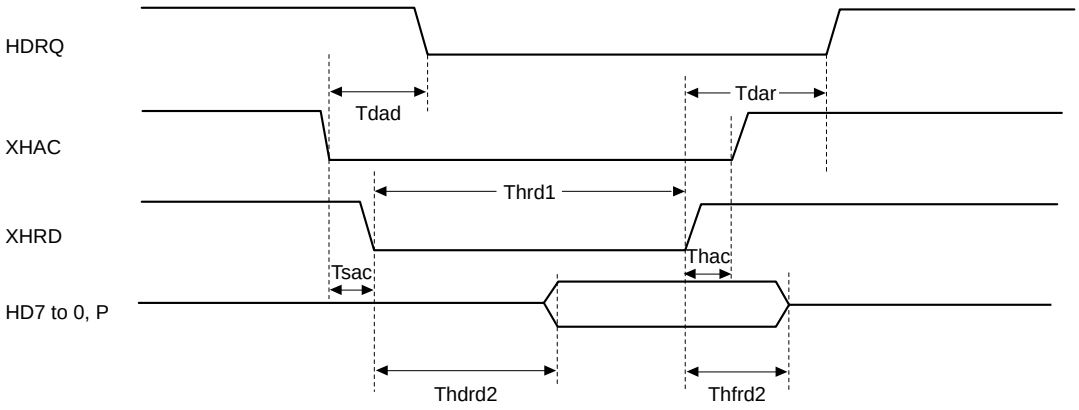
(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XHCS & XHWR ↓)	Thsar	30 (70)			ns
Address hold time (for XHCS & XHWR ↑)	Thhar	20 (50)			ns
Data setup time (for XHCS & XHWR ↑)	Thswd	40 (70)			ns
Data hold time (for XHCS & XHWR ↑)	Thhwd	10 (30)			ns
Low level XHWR pulse width	Thww1	60 (100)			ns

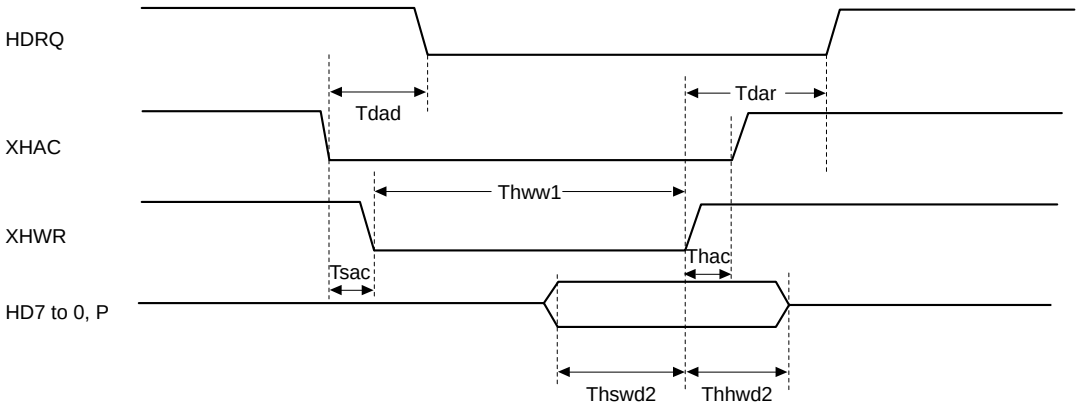
4. Host DMA cycle

(1) Read



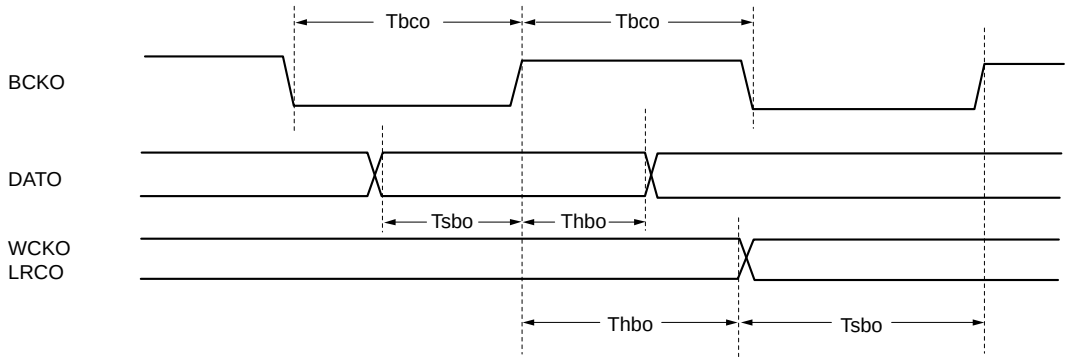
Item	Symbol	Min.	Typ.	Max.	Unit
HDRQ fall time (for XHAC ↓)	Tdad			45 (70)	ns
HDRQ rise time (for XHAC ↑)	Tdar			45 (70)	ns
XHAC setup time (for XHRD ↓)	Tsac	5 (20)			ns
XHAC hold time (for XHRD ↑)	Thac	0 (20)			ns
Data delay time (for XHRD ↓)	Thdrd2			60 (100)	ns
Data float time (for XHRD ↑)	Thfrd2	0		15 (25)	ns
Low level XHRD pulse width	Thrd1	100 (150)			ns

(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
HDRQ fall time (for XHAC ↓)	Tdad			45 (70)	ns
HDRQ rise time (for XHAC ↑)	Tdar			45 (70)	ns
XHAC setup time (for XHWR ↓)	Tsac	5 (20)			ns
XHAC hold time (for XHWR ↑)	Thac	0 (20)			ns
Data setup time (for XHWR ↓)	Thswd2	40 (70)			ns
Data hold time (for XHWR ↑)	Thhwd2	10 (30)			ns
Low level XHWR pulse width	Thww1	60 (100)			ns

5. DAC interface



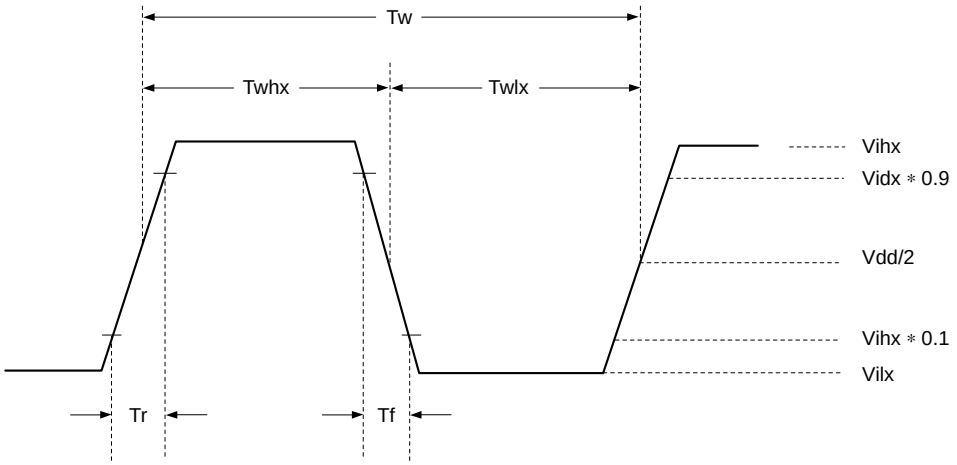
Item	Symbol	Min.	Typ.	Max.	Unit
BCKO frequency	Fbco		8.4672		MHz
BCKO pulse width	Tbco	50			ns
DATO, WCO1, WCO2, LRCO setup time (for BCKO ↑)	Tsbo	30			ns
DATO, WCO1, WCO2, LRCO hold time (for BCKO ↑)	Thbo	30			ns

6. XTL1 and XTL2 pins

(1) For self oscillation

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	Fmax		16.9344		MHz

(2) When a pulse is input to XTL1



Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	Twhx	20			ns
Low level pulse width	Twhx	20			ns
Pulse period	Tw		59		ns
Input high level	Vihx	V_{DD}–1.0			ns
Input low level	Vihx			0.8	ns
Rise time	Tr			15	ns
Fall time	Tf			15	ns

Note) Synchronize the XTL1 clock signal with that of the CD DSP.
(use the clock signal from the same oscillator)

7. RMCK pin

Item	Symbol	Min.	Typ.	Max.	Unit
Frequency	Fmck			33.3 (23.4 with 3.5 V)	MHz

Note) The maximum RMCK frequency is 35.0 MHz when V_{DD} is 5 V±5 %.
Playback at quadruple normal speed can be accommodated when a clock signal with a frequency double 16.9344 MHz or more is input to RMCK.

Description of Functions

1. Pin Description

The pin description by function is given below.

1-1. CD player interface (5 pins)

This enables direct connection with the digital signal processor LSI for Sony's CD players. Digital signal processor LSI for CD applications is hereafter called "CD DSP". See 2-1-1 for the data formats.

(1) DATA (DATA : input)
Serial data stream from CD DSP.

(2) BCLK (bit clock : input)
Bit clock signal ; DATA signal strobe.

(3) LRCK (LR clock : input)
LR clock signal ; indicates left and right channels of DATA signals.

(4) C2PO (C2 pointer : input)
C2 pointer signal ; indicates that an error is contained in the DATA input.

(5) EMP (emphasis : input)
Emphasis positive logic signal ; indicates that emphasis has been applied to the data from CD DSP.

1-2. Buffer memory interface (28 pins)

This is connected to a 32 K-byte (256 K-bit) or 128 K-byte (1 M-bit) standard SRAM.

(1) XMWR (buffer memory write : output)
Data write strobe negative logic output signal to buffer memory.

(2) XMOE (buffer memory output enable : output)
Data read strobe negative logic output signal to buffer memory.

(3) MA0 to 16 (buffer memory address : output)
Address signals to buffer memory.

(4) MDB0 to 7, P (buffer memory data bus : bus)
Data bus signals of buffer memory ; pulled up by standard 25 kΩ resistance ; MDBP pin is left open when connected to an 8-bit/word SRAM.

1-3. Sub CPU interface (17 pins)

(1) XWR (sub CPU write : input)
Strobe negative logic input signal for writing IC internal register.

(2) XRD (sub CPU read : input)
Strobe negative logic input signal for reading IC internal register status.

(3) D0 to 7 (sub CPU data bus : input/output)
8-bit data bus.

(4) A0 to 4 (sub CPU address : input)
Address signal for selecting IC internal register from sub CPU.

(5) XINT (sub CPU interrupt : output)
Interrupt request negative logic signal to sub CPU.

(6) XCS (chip select : input)
IC select negative logic signal from sub CPU.

1-4. Host interface (17 pins)

(1) HDRQ (host data request : output)
DMA data request positive logic signal to host.
(2) XHAC (host DMA acknowledge : input)
DMA acknowledge negative logic signal from host.
(3) XHWR (host write : input)
Data write strobe input from host.
(4) XHRD (host read : input)
Data read strobe input from host.
(5) XHCS (host chip select : input)
Chip select negative logic signal from host.
(6) HA0, 1 (host address : input)
Address signals for selecting IC internal register from host.
(7) HD0 to 7 (host data bus : input/output)
Host data bus signals.
(8) HDP (host data bus pointer : input/output)
Host data bus positive logic signal for error pointer.
(9) HINT (host interrupt : output)
Interrupt request negative logic output signal to host ; open drain output.

1-5. DAC interface (4 pins)

The output format to DAC is shown in Fig.1-1.

(1) BCKO (bit clock output : output)
Bit clock output signal to D/A converter.
(2) WCKO (word clock output : output)
Word clock output signal to D/A converter.
(3) LRCO (LR clock output : output)
LR clock output signal to D/A converter.
(4) DATO (data output : output)
Data output signal to D/A converter.

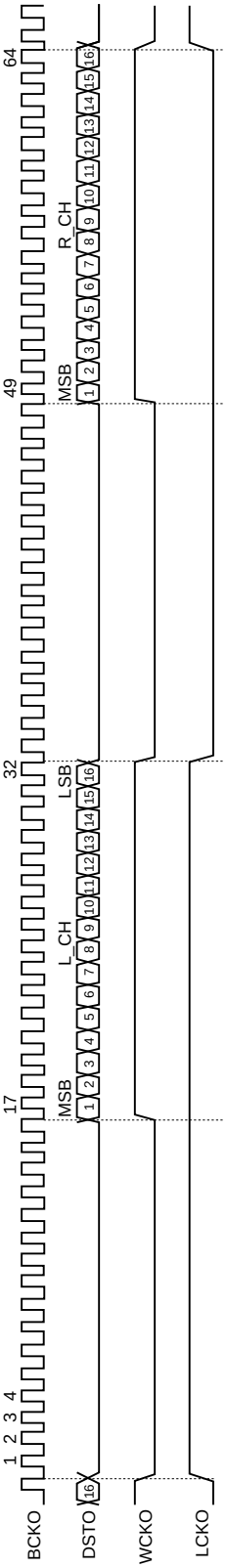


Fig. 1-1. D/A Converter Interface

1-6. Others (16 pins)

(1) MUTE (mute : output)
Outputs high when the DA data (DATO) is muted.
(2) XRST (reset : input)
Chip reset negative logic input signal.
(3) XTL1 (crystal1 : input)
(4) XTL2 (crystal2 : output)
A 16.9344 MHz crystal oscillator is connected between XTL1 and XTL2. (The capacitor value depends on the crystal oscillator.)
Alternatively, a 16.9344 MHz clock signal is input to the XTL1 pin.
(5) CLK (clock : output)
Outputs a 16.9344 MHz clock signal. The output can be fixed low when this signal is not used.
(6) HCLK (half clock : output)
Outputs an 8.4672 MHz clock signal. The output can be fixed low when this signal is not used.
(7) CKSL (clock select : input)
High or open : The IC is operated by the XTL1 clock.
Low : The audio block (ADPCM decoder and digital filter) is operated by the XTL1 clock, and the CD-ROM decoder unit is operated by the RMCK clock. In this case, the slow mode described later is prohibited.
This pin is pulled up by a 50 kΩ standard resistor in the IC.
(8) RMCK (ROM clock : input)
When the CKSL pin is set low, the clock of the CD-ROM decoder unit is input. When it is high or open, fix the RMCK pin high or low.
(9) XHRS (host reset : output)
This pin is low when the IC has been reset by the host. It is an open drain output.
(10) TD0 to 7 (test data 0 to 7 : input/output)
The data pins for testing the IC. They are pulled up by a 25 kΩ standard resistor and are normally left open.

1-7. Power supply pins (12 pins)

V_{DD} : 4 pins ; GND: 8 pins

2. Sub CPU Registers

2-1. Write registers

2-1-1. DRVIF (drive interface) register

This register controls the connection mode with the CD DSP. After the IC has been reset, the sub CPU sets this register according to the CD DSP to be connected.

bit 7 : C2PL1ST (C2PO lower byte 1st)
- High : When two bytes of data are input, C2PO inputs the lower byte first followed by the upper byte.
- Low : When two bytes of data are input, C2PO inputs the upper byte first followed by the lower byte. Here, “upper byte” means the upper 8 bits including MSB from the CD DSP and “lower byte” means the lower 8 bits including LSB from the CD DSP. For instance, the header minute byte is the lower byte and the second byte, the upper byte.

bit 6 : LCHLOW (Lch low)
- High : When LRCK is low, determined to be the left channel data.
- Low : When LRCK is high, determined to be the left channel data.

bit 5 : BCKRED (rising edge of BCLK)
- High : The DATA is strobed at the rising edge of BCLK.
- Low : The DATA is strobed at the falling edge of BCLK.

bits 4, 3 : BCKMD1, 0 (BCLK mode 1, 0)

These bits are set according to the number of clocks output for BCLK during one WCLK cycle by the CD digital signal processor LSI (CD DSP).

BCKMD1	BCKMD0	
“L”	“L”	16 BCLKs/WCLK
“L”	“H”	24 BCLKs/WCLK
“H”	“X”	32 BCLKs/WCLK

bit 2 : LSB1ST (LSB first)
- High : Connected with the CD DSP which outputs DATA with LSB first.
- Low : Connected with the CD DSP which outputs DATA with MSB first.

bits 1, 0 : Reserved

Normally set below.

Any change of each bit value in this register must be made in the decoder disable status.
Table 2-1-1 shows the settings for bits 7 to 2 when this IC is connected to Sony’s CD DSP.
Figs. 2-1-1 (1) to (3) are input timing charts.

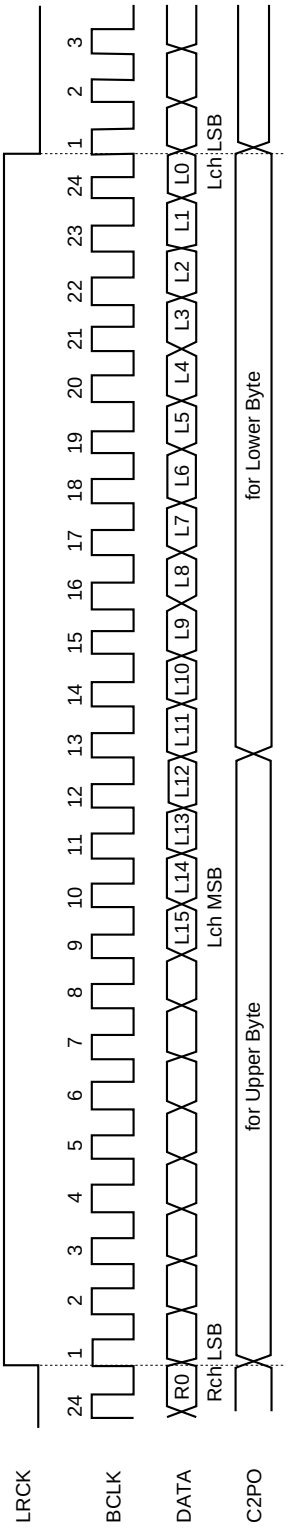


Fig. 2-1-1. (1) CDL30 and 35 Series Timing Chart

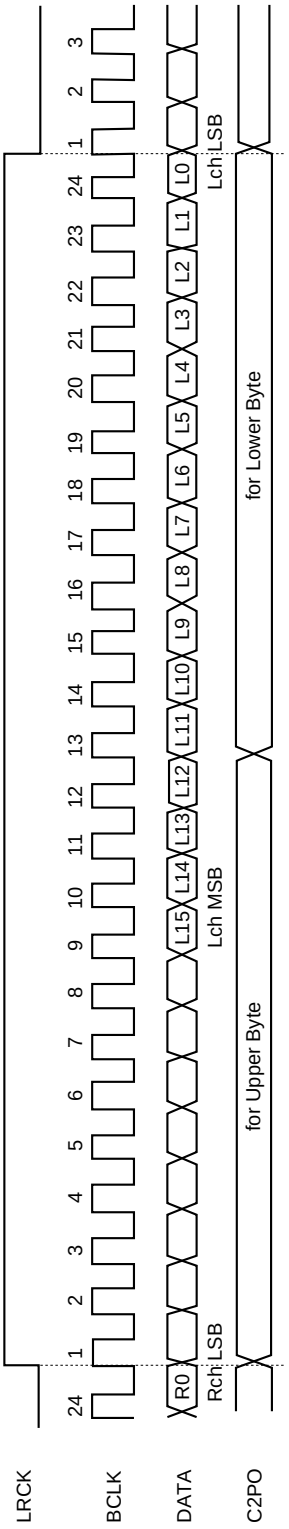


Fig. 2-1-1. (2) CDL40 Series Timing Chart (48-bit slot mode)

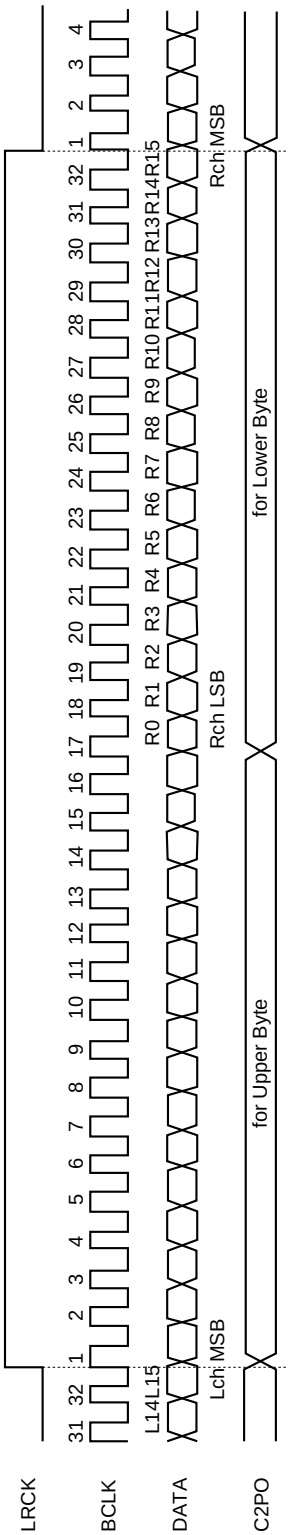


Fig. 2-1-1. (3) CDL40 Series Timing Chart (64-bit slot mode)

Sony CD DSP	DR VIF register						Timing chart
	bit7	bit6	bit5	bit4	bit3	bit2	
	c2po	lrck	bedg	bck1	bck0	lsb	
CDL30 Series CDL35 Series	L	L	L	L	H	L	Fig. 2-1-1. (1)
CDL40 Series (48-bit slot mode)	L	L	H	L	H	L	Fig. 2-1-1. (2)
CDL40 Series (64-bit slot mode)	L	H	L	H	X	H	Fig. 2-1-1. (3)

Table 2-1-1. DR VIF Register Settings

2-1-1. CONFIG1 (configuration 1) register

This register is set depending on the IC peripheral hardware. The sub CPU sets this register after the IC has been reset.

bit 7 : Reserved
Normally set low.

bit 6 : XSLOW
The number of clock signals per DMA cycle is determined by this bit.
High : 4 clock signals
Low : 12 clock signals
Set low when a low-speed SRAM is connected for V_{DD} = 3.5 V. When XSLOW is low, erasure correction and double speed playback are prohibited.

bit 5 : PRTYCTL (priority control)
Set high when double speed playback with erasure correction executed is performed by setting the clock frequency of the CD-ROM decoder to 18 MHz or below. In this case, buffer access for ECC has priority and the rate of data transfer to the host is reduced.
When a 9-bit/word SRAM has been connected to this IC, the C2 pointer is written from the BDBP pin into the buffer memory regardless of this bit value.

bits 4, 3 : RAMSZ1, 0 (RAM size 1, 0)

bit 2 : 9 BITRAM
These bits are set depending on the size of the SRAM connected to the IC.

RAMSZ1	RAMSZ0	9 BITRAM	SRAM size
"L"	"L"	"L"	32 Kw × 8b
"L"	"L"	"H"	32 Kw × 9b
"L"	"H"	"L"	64 Kw × 8b
"L"	"H"	"H"	64 Kw × 9b
"H"	"L"	"L"	128 Kw × 8b
"H"	"L"	"H"	128 Kw × 9b

bit 1 : CLKDIS (CLK disable)
High : The CLK pin is fixed low.
Low : A 16.9344 MHz clock signal is output from the CLK pin.

bit 0 : HCLKDIS (half CLK disable)
High : The HCLK pin is fixed low.
Low : An 8.4672 MHz clock signal is output from the HCLK pin.

2-1-3. CONFIG2 (configuration 2) register

This register is set depending on the IC peripheral hardware. The sub CPU sets this register after the IC has been reset.

bits 7, 6 : Reserved
Normally set low.

bit 5 : SPECTL (sound parameter error control)

bit 4 : SPMCTL (sound parameter majority control)
These two bits control the processing of the sound parameters for ADPCM decoding playback.

bit 3 : SMBF2 (sound map buffer 2)
Indicates the number of buffer surfaces for the sound map ADPCM.
High : 2 buffer surfaces for the sound map
Low : 3 buffer surfaces for the sound map

bit 2 : DAMIXEN (digital audio mixer enable)
High : Attenuator and mixer are not activated for CD-DA.
Low : Attenuator and mixer are activated for CD-DA.
bit 1 : DACODIS (DAC out disable)
High : Clock signals are output from the WCKO, LRCO and BCKO pins even for muting.
Low : The WCKO, LRCO and BCKO pins are set low for muting.
bit 0 : Reserved
Normally fixed low.

2-1-4. DECCTL (decoder control) register

bit 7 : ENDLADR (enable drive last address)
High : DLADR (drive last address) is enabled when this is high. When DADRC and DLADR become equal while the decoder is in the write-only, real-time correction or CD-DA mode, the data writing from the driver into the buffer is stopped.
Low : DLADR (drive last address) is disabled when this is low. Even when DADRC and DLADR become equal while the decoder is in the write-only, real-time correction or CD-DA mode, data writing from the driver into the buffer is not stopped.
bit 6 : ECCSTR (ECC strategy)
High : Errors are corrected with consideration given to the error flags of the data.
Low : Errors are corrected with no consideration given to the error flags of the data. In this case, there is no erasure correction. Set this bit low when the IC is connected to an 8-bit/word SRAM.
bit 5 : MODESEL (mode select)
bit 4 : FORMSEL (form select)
When AUTODIST is low, the sector is corrected in the MODE or FORM indicated below.

MODESEL	FORMSEL	
"L"	"L"	MODE1
"H"	"L"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

bit3 : AUTODIST (auto distinction)
High : Errors are corrected according to the MODE byte and FORM bit read from the drive.
Low : Errors are corrected according to the MODESEL and FORMSEL bits (bits 5 and 4).
bits 2 to 0 : DECMD2 to 0 (decoder mode 2 to 0)

DECMD2	DECMD1	DECMD0	
"L"	"L"	"X"	Decoder disable
"L"	"H"	"X"	Monitor-only mode
"H"	"L"	"L"	Write-only mode
"H"	"L"	"H"	Real-time correction mode
"H"	"H"	"L"	Repeat correction mode
"H"	"H"	"H"	CD-DA mode

When the CD-DA bit (bit 4) in the CHPCTL register is to be set high, set the decoder to the disable or CD-DA mode.

2-1-5. DLADR-L register
2-1-6. DLADR-M register
2-1-7. DLADR-H register

While the decoder is in the write-only, real-time correction or CD-DA mode, the last address is set for the buffer write data from the drive. When the ENDLADR bit (bit 7) of the DECCTL register is high and the data from the drive is written into the address assigned by DLADR while the decoder is in any of the above modes, all subsequent writing in the buffer is prohibited.

2-1-8. CHPCTL (chip control) register

bit 7 : SM MUTE (sound map mute)
When this is set high, the audio output is muted for sound map ADPCM playback.
bit 6 : RT MUTE (real-time mute)
When this is set high, the audio output is muted for real-time ADPCM playback.
bit 5 : CD-DA MUTE
When bit 4 is high and this bit is also set high for CD-DA (digital audio) disc playback, the audio output is muted. When bit 4 is low, this bit has no effect on the audio output.
bit 4 : CD-DA
High : Set high for playing back the audio signals of a CD-DA (digital audio) disc. Setting this bit high is prohibited for ADPCM decoding playback.
Low : Set low for not playing back the audio signals of a CD-DA (digital audio) disc.
bit 3 : SWOPN (sync window open)
High : A window for sync mark detection is opened. In this case, the sync protection circuit in the IC is disabled.
Low : The window for sync mark detection is controlled by the sync protection circuit in the IC.
bit 2 : RPSTART (repeat correction start)
Sector error correction starts when the decoder is set to the repeat correction mode, making this bit high. This bit is automatically set low when correction starts. There is therefore no need for the sub CPU to reset low.
bit 1 : DBLSPD (double speed)
Set high for double speed playback. Before changing the bit value, switch the CD DSP mode (normal speed playback or double speed playback).
bit 0 : RESERVED
Normally set low.

2-1-9. INTMSK (interrupt mask) register

By setting each bit of this register high, the interrupt request from the IC to the sub CPU is enabled depending on the corresponding interrupt status. (In other words, the INT pin is made active when its interrupt status is established.) The each bit value of this register has no effect on the corresponding interrupt status.
bit 7 : DRVOVRN (drive overrun)
The DRVOVRN status is established when the ENDLADR bit (bit 7) of the DECCTL register is set high and DADRC and DLADR become equal while the decoder is in the write-only or real-time correction mode. It is also established when they become equal while the decoder is in the CD-DA mode regardless of the ENDLADR bit value.
bit 6 : DECTOUT (decoder time out)
The DECTOUT status is established when the sync mark is not detected even after 3 sectors (40.6 ms at normal speed playback) have elapsed after the decoder has been set to the monitor-only, write-only or real-time correction mode.

bit 5 : RSLTEMPT (result empty)
The RSLTEMPT status is established when the host reads the result register and this register becomes empty. (This is used when the number of result bytes sent to the host is 9 or more.)

bit 4 : RTADPEND (real-time ADPCM end)
The RTADPEND status is established when real-time ADPCM decoding is completed for one sector.

bit 3 : HDMACMP (host DMA complete)
The HDMACMP status is established when DMA is completed by HXFRC.

bit 2 : DECINT (decoder interrupt)
The DECINT status is established when the sync mark is detected or inserted while the decoder is in the write-only, monitor-only or real-time correction mode. However, it is not established if the sync mark interval is less than 2352 bytes while the window for its detection is open. The status is established each time one correction is completed when the decoder is in the repeat correction mode.

bit 1 : HSTCMND (host command)
The HSTCMND status is established when the host writes a command in the command register.

bit 0 : HCRISD (host chip reset issued)
The HCRISD status is established when the host clears the IC. When HCRISD is high, the XHRS pin is low.

2-1-10. CLRCTL (clear control) register

When each bit of the register is set high, the corresponding chip, status, register, interrupt status and ADPCM playback are cleared. After clearing, the bit concerned is automatically set low. There is therefore no need for the sub CPU to reset low.

bit 7 : CHPRST (chip reset)
The inside of the IC is initialized when this bit is set high. It is automatically set low upon completion of the initialization.

bit 6 : CLRBUSY (clear busy)
The BUSYSTS bit of the HIFSTS register is cleared when this bit is set high.

bit 5 : CLRRSLT (clear result)
The RESULT register is cleared when this bit is set high.

bit 4 : RTADPCLR (real-time ADPCM clear)
(1) When this is set high for real-time ADPCM playback (when the RTADPBSY bit of the DECSTS register is high):
• ADPCM decoding during playback is suspended. (Noise may be generated.)
• The RTADPEND interrupt status is established.
(Note) The RTADPEN bit (bit 7 of the ADPMNT register) must be set low before this bit is set high.
(2) Setting this bit high when real-time ADPCM playback is not being performed has no effect whatsoever.

bits 3 to 1 : Reserved
Normally set low.

bit 0 : RESYNC
The CD DSP and this IC are synchronized when this bit is set high. Set the bit high by the sub CPU in the following cases:
(1) After the DRVIF register has been set
(2) After the DBLSPD bit (bit 1 of the CHPCTL register) has been set low.
This bit is automatically set low when the CD DSP and this IC are synchronized.

2-1-11. CLRINT (clear interrupt status) register

When each bit of this register is set high, the corresponding interrupt status is cleared. The bit concerned is automatically set low after its interrupt status has been cleared. There is therefore no need for the sub CPU to reset low.

bit 7 : DRVOVRN (drive overrun)
bit 6 : DECTOUT (decoder time out)
bit 5 : RSLTEMP (reset empty)
bit 4 : RTADPEND (real-time ADPCM end)
bit 3 : HDMACMP (host DMA complete)
bit 2 : DECINT (decoder interrupt)
bit 1 : HSTCMND (host command)
bit 0 : HCRISD (host chip reset issued)

2-1-12. HXFR-L (host transfer-low) register

2-1-13. HXFR-H (host transfer-high) register

bit 7 : DISHXFRC (disable host transfer counter)
High : The completion of the data transfer by HXFRC is disabled for data transfer between the host and buffer memory.
Low : The completion of the data transfer by HXFRC is enabled for data transfer between the host and buffer memory.
bits 6, 5 : Reserved
bit 4 : HADR16
HADR bit 16 (MSB)
bit 3 : HXFR11
HXFR (host transfer counter) bit 11 (MSB)
bit 2 : HXFR10
HXFR bit 10
bit 1 : HXFR9
HXFR bit 9
bit 0 : HXFR8
HXFR bit 8

The HXFR (host transfer) register sets the number of data transferred between the host and buffer memory. The sub CPU sets this number when data is transferred between the host and buffer memory by setting the DISHXFRC bit low.

2-1-14. HADR-L register

2-1-15. HADR-M register

2-1-16. HADR-H register

The HADR (host address) register is for the head addresses of data transfer between the host and buffer memory.

2-1-17. DADRC-L register

2-1-18. DADRC-M register

2-1-19. DADRC-H register

This counter keeps the address for writing the data from the drive into the buffer. When drive data is written into the buffer, the DADRC value is output from MA0 to 16. DADRC is incremented each time 1 byte of data is written from the drive into the buffer.
The sub CPU sets the head address for buffer writing into DADRC before the decoder operates in the write-only, real-time correction or CD-DA mode.
The sub CPU can set DADRC at any time. The contents of DADRC should not be changed while the decoder is operating in any of the above modes.

2-1-20. HIFCTL (host interface control) register

bits 7 to 3 : Reserved
The sub CPU sets these bits low.
bit 2 : HINT#2
The value of this bit becomes that of HINTSTS#2 in the HINTSTS register on the host side.
bit 1 : HINT#1
The value of this bit becomes that of HINTSTS#1 in the HINTSTS register on the host side.
bit 0 : HINT#0
The value of this bit becomes that of HINTSTS#0 in the HINTSTS register on the host side.

2-1-21. RESULT register

This register is used to transfer the command execution result to the host. It has an 8-byte FIFO configuration.

2-1-22. ADPMNT register

bit 7 : RTADPEN (real-time ADPCM enable)
The sub CPU sets this high to perform real-time ADPCM playback.
bits 6 to 0 : The upper 7 bits (bits 16 to 10) of the sector head address are written into these bits to perform real-time ADPCM playback.

2-1-23. RTCI (real-time coding information) register

Writes the coding information bytes when real-time ADPCM playback is performed.

bit 6 : EMPHASIS
Set high when an ADPCM sector where emphasis has been applied is played back.

bit 4 : BITLNGTH (bit length)
Indicates the bit length of the coding information for ADPCM playback.
High : 8 bits
Low : 4 bits

bit 2 : FS (sampling frequency)
Indicates the sampling frequency of ADPCM playback.
High : 18.9 kHz
Low : 37.8 kHz

bit 0 : S/M (stereo/mono)
Indicates the coding information stereo or mono for ADPCM playback.
High : Stereo
Low : Mono

bits 7, 5, 3, 1 : Reserved
Normally set low.

All the write registers except INTMSK are 00HEX when the IC is reset (either hard or soft reset). All the bits in the INTMSK register except the HCRISD bit (bit 0) are low when the IC is reset. The HCRISD bit is set low by hard or by soft reset by the sub CPU. The HCRISD bit value is not affected by soft resetting by the host. “Hard reset” means that the XRST pin is set low; “soft reset” means that the IC is reset by the sub CPU or host.

2-2. Read registers

In the descriptions of the ECCSTS, DECSTS, HDRFLG, HDR, SHDR and CMADR registers, the current sector denotes the sector with which these registers are valid for the decoder interrupt (DECINT). In the monitor-only or write-only mode, the sector sent from the CD DSP immediately before the decoder interrupt is called the current sector. In the real-time correction mode and repeat correction mode, the current sector is that in which error detection correction has been completed.

2-2-1. ECCSTS (ECC status) register

bit 7 : EDCALL0 (EDC ALL 0)
This is high when there are no error flags in all the 4 EDC parity bytes of the current sector and their values are all 00HEX.

bit 6 : ERINBLK (erasure in block)
(1) When the decoder is operating in the monitor-only, write-only or real-time mode which prohibits erasure correction, this indicates that at least a 1-byte error flag (C2PO) has been raised in the data excluding the sync mark from the current sector CD DSP.
(2) When the decoder is operating in the real-time correction mode which performs erasure correction, this indicates that at least a 1-byte error flag (MDBP) has been raised in the data excluding the sync mark from the current sector CD DSP.

bit 5 : CORINH (correction inhibit)
This is high if the current sector MODE and FORM could not be determined when the AUTODIST bit of the DECCTL register is set high. ECC or EDC is not executed in this sector. The CORINH bit is invalid when AUTODIST is set low. It is high in any of the conditions below when the AUTODIST bit is set high.
(1) When the C2 pointer of the MODE byte is high
(2) When the MODE byte is a value other than 01HEX or 02HEX
(3) When the MODE byte is 02HEX and the C2 pointer is high in the submode byte

bit 4 : CORDONE (correction done)
Indicates that there is an error corrected byte in the current sector.

bit 3 : EDCOK
Indicates that an EDC check has found no errors in the current sector.

bit 2 : ECCOK
Indicates that there are no more errors from the header byte to P parity byte in the current sector.
(Bit 2 = don't care in the MODE2, FORM2 sectors)

EDCOK	ECCOK	Description
"L"	"L"	Error(s) present in current sector
"L"	"H"	(1), (2) or (3) applies: (1) EDC overlocked (2) Error corrected (3) Error(s) present in header byte with FORM2
"H"	"L"	(1) EDC overlocked or (3) Error(s) present in P parity byte
"H"	"H"	No error(s) in current sector

bit 1 : CMODE (correction mode)
bit 0 : CFORM (correction form)
Indicates the MODE and FORM of the current sector the decoder has discriminated and corrected errors when the decoder is operating in the real-time correction or repeat correction mode.

CFORM	CMODE	
"X"	"L"	MODE1
"L"	"H"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

2-2-2. DECSTS (decoder status) register

bit 5 : RTADPBSY (real-time ADPCM busy)
This is high for real-time ADPCM playback.
bit 1 : SHRTSCT (short sector)
Indicates that the sync mark interval was less than 2351 bytes. This sector does not remain in the buffer memory.
bit 0 : NOSYNC
Indicates that the sync mark was inserted because one was not detected at the prescribed position.

2-2-3. HDRFLG (header flag) register

This register indicates the error flags of the header and sub header register bytes.

2-2-4. HDR (header) register

This is a 4-byte register which indicates the current sector header byte. By setting the address to 03HEX and reading out the data in sequence, the sub CPU can ascertain the values of the current sector header bytes from the minute byte.

2-2-5. SHDR (sub header) register

This is a 4-byte register which indicates the current sector sub header byte. By setting the address to 04HEX and reading out the data 4 times, the sub CPU can ascertain the values of the current sector sub header bytes in the sequence of the file, submode and data type bytes.

The contents of the HDRFLG, HDR, SHDR registers indicate:
(1) The corrected value in the real-time correction or repeat correction mode
(2) Value of the raw data from the drive in the monitor-only or write-only mode
The CMOME and CMODE bits (bits 1, 0) of ECCSTS indicate the FORM and MODE of the sector the decoder has discriminated by the raw data from the drive. Due to erroneous correction, the values of these bits may be at variance with those of the HDR register MODE byte and SHDR register submode byte bit 5.

2-2-6. CMADR (current minute address) register

This register indicates the upper 7 bits of the buffer memory address where the minute byte of the current sector (after error correction) is written in bits 6 to 0. (Remaining address bits are all low.)

2-2-7. INTSTS (interrupt status) register

The value of each bit in this register indicates that of the corresponding interrupt status. These bits are not affected by the values of the INTMSK register bits.

bit7 : DRVOVRN (drive overrun)
bit6 : DECTOUT (decoder time out)
bit5 : RSLTEMPT (RESULT empty)
bit4 : RTADPEND (real-time ADPCM end)
bit3 : HDMACMP (host DMA complete)
bit2 : DECINT (decoder interrupt)
bit1 : HSTCMND (host command)
bit0 : HCRISD (host chip reset issued)

2-2-8. ADPCI (ADPCM coding information) register

bit 7 : MUTE
This is high when the DA data is muted.
bit 6 : EMPHASIS
This is high when emphasis is applied to the ADPCM data.
bit 5 : ADPBUSY
This is high for ADPCM decoding.
bit 4 : BITLNGTH (bit length)
Indicates the bit length of the coding information for ADPCM playback.
High : 8 bits
Low : 4 bits
bit 2 : FS (sampling frequency)
Indicates the sampling frequency of ADPCM playback.
High : 18.9 kHz
Low : 37.8 kHz
bit 0 : S/M (stereo/mono)
Indicates the coding information stereo or mono for ADPCM playback.
High : Stereo
Low : Mono

2-2-9. HXFRC-L (host transfer counter-low) register

2-2-10. HXFRC-H (host transfer counter-high) register

The HXFRC counter indicates the number of remaining bytes in the data to be transferred between the host and buffer memory. If sound map data is to be transferred before the data is transferred (immediately after the host has set the BFRD and BFWR bits (bits 7 and 6) of the HCHPCTL register high), 2304 (900HEX) is loaded into HXFRC. At any other time, the HXFR (sub CPU register) value is loaded. HXFRC is decremented when data is read from the buffer memory (BFRD is high) or when the IC accepts data from the host (BFWR is high).

2-2-11. HADRC-L (host address counter-low) register

2-2-12. HADRC-M (host address counter-middle) register

This counter keeps the addresses which write or read the data with host into/from the buffer. If sound map data is to be transferred before the data is transferred (immediately after the host has set the BFRD and BFWR bits (bits 7 and 6) of the HCHPCTL register high), 600CHEX, 6A0CHEX or 740CHEX (1MRAM is low) is loaded into HADRC. At any other time, the HADR (sub CPU register) value is loaded.
When data from the host is written into the buffer or data to the host is read from the buffer, the HADRC value is output from MA0 to 16. HADRC is incremented each time one byte of data from the drive is read from the buffer (BFRD is high) or written into the buffer (BFWR is high).
The MSB (bit 16) of HADRC is read out from bit 4 of the HXFRC-H register.

2-2-13. DADRC-L (drive address counter-low) register

2-2-14. DADRC-M (drive address counter-middle) register

The MSB (bit 16) of DADRC is read out from bit 5 of the HXFRC-H register.

2-2-15. HIFSTS (host interface status) register

bit 7 : BUSYSTS (busy status)
This has the same value as BUSYSTS (bit 7) of the host HSTS register. It is set high when the host writes a command into the command register and low when the sub CPU sets CLRBUSY of the CLRCTL register.

bit 6 : RSLWRDY (result write ready)
The result register is not full when this bit is high. The sub CPU can write the result of the command execution into this register.

bit 5 : RSLEMPT (result empty)
The result register is empty when this bit is high. It indicates that all the status sent from the sub CPU to the host (result register) have been read out by the host.

bit 4 : PRMRRDY (parameter read ready)
The HSTPRM register is not empty when this bit is high. The sub CPU can read out the command parameters from the HSTPRM register.

bit 3 : DMABUSY (DMA busy)
This is high when data is being transferred between the buffer memory and the host.
It is high when the host sets BFRD (bit 7) or BFWR (bit 6) of the HCHPCTL register high. It is low in the case below:
- When the data transfer FIFO (WRDATA, RDDATA registers) is empty after the level of HXFRC has dropped to 00HEX.

bit 2 : HINTSTS#2 (host interrupt status #2)
This is high when the sub CPU writes data into HINT#2 (HIFCTL register bit 2) and low when the host writes “high” into CLRINT#2 (HCLRCTL register bit 2). It is used to monitor interrupts for the host.

bit 1 : HINTSTS#1 (host interrupt status #1)
This is high when the sub CPU writes data into HINT#1 (HIFCTL register bit 1) and low when the host writes “high” into CLRINT#1 (HCLRCTL register bit 1). It is used to monitor interrupts for the host.

bit 0 : HINTSTS#0 (host interrupt status #0)
This is high when the sub CPU writes data into HINT#0 (HIFCTL register bit 0) and low when the host writes “high” into CLRINT#0 (HCLRCTL register bit 0). It is used to monitor interrupts for the host.

2-2-16. HSTPRM (host parameter) register

The command parameters from the host are read out from this register. The register has an 8-byte FIFO configuration.

2-2-17. HSTCMD (host command) register

The command from the host are read out from this register.

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DRVIF	00	C2PO L 1st	LCH LOW	BCK RED	BCK MD1	BCK MD0	LSB 1st	"L"	"L"
CONFIG 1	01	"L"	XSLOW	PRTY CTL	RAM SZ1	RAM SZ0	9 bit RAM	CLK DIS	HCLK DIS
CONFIG 2	02	"L"	"L"	SPE CTL	SPM CTL	SM BF2	DAMIX EN	DACO DIS	"L"
DECCTL	03	EN DLADR	ECC STR	MODE SEL	FORM SEL	AUTO DIST	DEC MD2	DEC MD1	DEC MD0
DLADR-L	04	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DLADR-M	05	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
DLADR-H	06	"L"	"L"	"L"	"L"	"L"	"L"	"L"	bit16
CHPCTL	07	SM MUTE	RT MUTE	CDDA MUTE	CD-DA	SW OPEN	RPS TART	DBL SPD	"L"
	08	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
INTMSK	09	DRV OVRN	DEC TOUT	RSLT EMPT	RTADP END	HDMA CMP	DEC INT	HST CMND	HCR ISD
CLRCTL	0A	CHP RST	CLR BUSY	CLR RSLT	RTADP CLR	"L"	"L"	"L"	RE SYNC
CLRINT	0B	DRV OVRN	DEC TOUT	RSLT EMPT	RTADP END	HDMA CMP	DEC INT	HST CMND	HCR ISD
HXFR-L	0C	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HXFR-H	0D	DIS HXFRC	"L"	"L"	HADR bit16	bit11	bit10	bit9	bit8
HADR-L	0E	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HADR-M	0F	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
DADRC-L	10	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DADRC-M	11	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
DADRC-H	12	"L"	"L"	"L"	"L"	"L"	"L"	"L"	bit16
	13	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
	14	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
	15	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
HIFCTL	16	"L"	"L"	"L"	"L"	"L"	HINT #2	HINT #1	HINT #0
RESULT	17	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	18	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
ADPMNT	19	RTADP EN	bit16	bit15	bit14	bit13	bit12	bit11	bit10
	1A	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
RTCI	1B	"L"	EMPHASIS	"L"	BIT LNGTH	"L"	FS	"L"	S/M

Sub CPU write registers

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ECCSTS	00	EDC ALL0	ERIN BLK	COR INH	COR DONE	EDC OK	ECC OK	C MODE	C FORM
DECSTS	01	—	—	RTADP BSY	—	—	—	SHRT SCT	NO SYNC
HDRFLG	02	MIN	SEC	BLOCK	MODE	FILE	CHANNEL	SUB MODE	CI
HDR	03	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SHDR	04	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CMADR	05	—	bit16	bit15	bit14	bit13	bit12	bit11	bit10
INTSTS	07	DRV OVRN	DEC TOUT	RSLT EMPT	RTADP END	HDMA CMP	DEC INT	HST CMND	HCR ISD
ADPCI	08	—	EMPHASIS	—	BIT LNGTH	—	FS	—	S/M
	09	—	—	—	—	—	—	—	—
HXFRC-L	0A	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HXFRC-H	0B	—	—	DADRC bit16	HADRC bit16	bit11	bit10	bit9	bit8
HADRC-L	0C	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HADRC-M	0D	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
DADRC-L	0E	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DADRC-M	0F	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	10	—	—	—	—	—	—	—	—
HIFSTS	11	BUSY STS	RSLT WRDY	RSL EMPT	PRM RRDY	DMA BUSY	HINT STS2	HINT STS1	HINT STS0
HSTPRM	12	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HSTCMD	13	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

Sub CPU read registers

3. Host Registers

3-1. Write registers

3-1-1. ADDRESS register

bits 7 to 2 : Reserved
Normally set low.
bits 1, 0 : RA1, 0
These are the address expansion bits. The host read/write register is selected according to the combination of these bits with the HA1 and 0 inputs. Refer to the table at the end of this section for the register selection methods.

3-1-2. COMMAND register

This is the register in which the host writes the commands. When the host writes a command in it, an interrupt request can be output to the sub CPU. The control program specifies bit allocation and functions.

3-1-3. PARAMETER register

The host writes the command parameters required to execute commands in this register. The register has an 8-byte FIFO configuration.

3-1-4. HCHPCTL (host chip control) register

bit 7 : BFRD (buffer read)
The transfer of (drive) data from the buffer memory to the host is started by setting this bit high. The bit is automatically set low upon completion of the transfer.
bit 6 : BFWR (buffer write)
The transfer of data from the host to the buffer memory is started by setting this bit high. The bit is automatically set low upon completion of the transfer.
bit 5 : SMEN (sound map En)
This is set high to perform sound map ADPCM playback.

3-1-5. WRDATA (write data) register

This is the register for writing the data to the buffer memory from the host. Data can be written in the I/O mode or using DMAC. The register has a 2-byte FIFO configuration.

3-1-6. HINTMSK (HOST interrupt mask) register

Setting each bit in this register high enables an interrupt request from the IC to the host depending on the corresponding interrupt status. The value of each bit has no effect on the corresponding interrupt status.
bit 7 : Reserved
bit 4 : ENBFWRDY (enable buffer write ready interrupt)
bit 3 : ENBFEMPT (enable buffer write empty interrupt)
bits 2 to 0 : ENINT#2 to 0 (enable interrupt #2 to 0)

3-1-7. HCLRCTL (HOST clear control) register

When each bit of this register is set high, the chip, status, register, interrupt status and interrupt request to the host generated by the status are cleared.

bit 7 : CHPRST (chip reset)
The inside of the IC is initialized by setting this bit high. The bit is automatically set low upon completion of the initialization of the IC. There is therefore no need for the host to reset low. When the inside of the IC is initialized by setting bit high, the XHRS pin is set low.

bit 6 : CLRPRM (clear parameter)
The parameter register is cleared by setting this bit high. The bit is automatically set low upon completion of the clearing for the parameter register. There is therefore no need for the host to reset low.

bit 5 : SMADPCLR (sound map ADPCM clear)
This bit is set high to terminate sound map ADPCM decoding forcibly.
(1) When this bit has been set high for sound map ADPCM playback (when both SMEN and ADPBSY (HSTS register bit 2) are high):
- ADPCM decoding during playback is suspended. (Noise may be generated).
- The sound map and buffer management circuits in the IC are cleared, making the buffer empty. The BFEMPT interrupt status is established.

(Note) Set the SMEN bit low at the same time as this bit is set high.
(2) Setting this bit high when the sound map ADPCM playback is not being performed has no effect whatsoever

bit 4 : CLRBFWRDY (clear buffer write ready interrupt)

bit 3 : CLRBFEMPT (clear buffer write empty interrupt)

bits 2 to 0 : CLRINT#2 to 0 (clear interrupt #2 to 0)
bit 4 clears the corresponding interrupt status.

3-1-8. CI (coding information) register

This sets the coding information for sound map playback. The bit allocation is the same as that for the coding information bytes of the sub header.

bits 7, 5, 3, 1: Reserved

bit 6 : EMPHASIS
High : Emphasis ON
Low : Emphasis OFF

bit 4 : BITLNGTH
High : 8 bits
Low : 4 bits

bit 2 : FS
High : 18.9 kHz
Low : 37.8 kHz

bit 0 : S/M (stereo/mono)
High : Stereo
Low : Mono

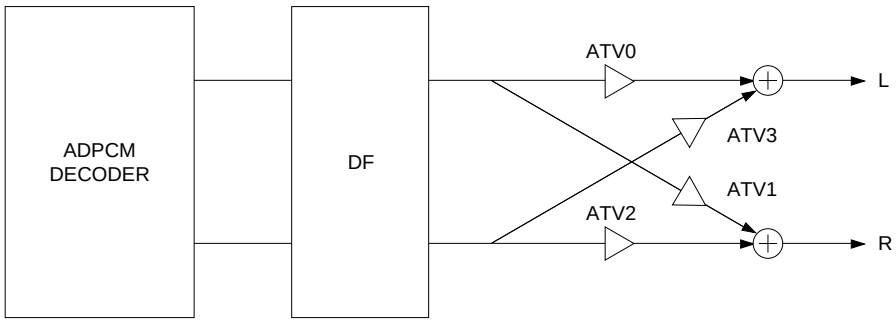
3-1-9. ATV (attenuation value) register 0

3-1-10. ATV (attenuation value) register 1

3-1-11. ATV (attenuation value) register 2

3-1-12. ATV (attenuation value) register 3

The attenuation values are set in these registers.



Setting 81HEX or higher into these registers is prohibited. When bits 7 to 0 of these registers are “b7” to “b0”, the attenuation (dB) of the attenuator is as follows:

$$\text{Attenuation}=20 \log (b7 \times 2^{0} + b6 \times 2^{-1} + b5 \times 2^{-2} + b4 \times 2^{-3} + b3 \times 2^{-4} + b2 \times 2^{-5} + b1 \times 2^{-6} + b0 \times 2^{-7})$$

The relationship expressed in the above formula and ATV register settings is given in the following table.

Setting	Attenuation	Setting	Attenuation	Setting	Attenuation
80	0.00	55	3.56	2A	9.68
7F	0.07	54	3.66	29	9.89
7E	0.14	53	3.76	28	10.10
7D	0.21	52	3.87	27	10.32
7C	0.28	51	3.97	26	10.55
7B	0.35	50	4.08	25	10.78
7A	0.42	4F	4.19	24	11.02
79	0.49	4E	4.30	23	11.26
78	0.56	4D	4.41	22	11.51
77	0.63	4C	4.53	21	11.77
76	0.71	4B	4.64	20	12.04
75	0.78	4A	4.76	1F	12.32
74	0.86	49	4.88	1E	12.60
73	0.93	48	5.00	1D	12.90
72	1.01	47	5.12	1C	13.20
71	1.08	46	5.24	1B	13.52
70	1.16	45	5.37	1A	13.84
6F	1.24	44	5.49	19	14.19
6E	1.32	43	5.62	18	14.54
6D	1.40	42	5.75	17	14.91
6C	1.48	41	5.89	16	15.30
6B	1.56	40	6.02	15	15.70
6A	1.64	3F	6.16	14	16.12
69	1.72	3E	6.30	13	16.57
68	1.80	3D	6.44	12	17.04
67	1.89	3C	6.58	11	17.54
66	1.97	3B	6.73	10	18.06
65	2.06	3A	6.88	0F	18.62
64	2.14	39	7.03	0E	19.22
63	2.23	38	7.18	0D	19.87
62	2.32	37	7.34	0C	20.56
61	2.41	36	7.50	0B	21.32
60	2.50	35	7.66	0A	22.14
5F	2.59	34	7.82	09	23.06
5E	2.68	33	7.99	08	24.08
5D	2.77	32	8.16	07	25.24
5C	2.87	31	8.34	06	26.58
5B	2.96	30	8.52	05	28.16
5A	3.06	2F	8.70	04	30.10
59	3.16	2E	8.89	03	32.60
58	3.25	2D	9.08	02	36.12
57	3.35	2C	9.28	01	42.14
56	3.45	2B	9.47	00	∞

Relationship between ATV register settings and attenuation (dB)

3-1-13. ADPCTL (ADPCM control) register

bit 5 : CHNGATV (change ATV register)
The host sets this bit high after the changes of the ATV 3 to 0 registers have been completed. The attenuator value in the IC is switched for the first time. There is no need for the host to set this bit low. The bit used to set the ATV3 to 0 registers of the host and to synchronize the IC audio playback.

bit 0 ADPMUTE (ADPCM mute)
Set high to mute the ADPCM sound for ADPCM decoding.

bits 7, 6, 4 to 1 : Reserved

Apart from ATV 2 and 0, all the write registers are initialized to 00HEX when reset (either hard or soft reset). The ATV 2 and 0 registers are initialized to 80HEX when reset.

3-2. Read registers

3-2-1. HSTS (host status) register

bit 7 : BUSYSTS (busy status)
This is high when the host writes a command into the command register and low when the sub CPU sets the CLRBUSY bit (bit 6) of the CLRCTL register.

bit 6 : DRQSTS (data request status)
Indicates to the host that the buffer memory data transfer request status is established. When transferring data in the I/O mode, the host should confirm that this bit is high before accessing the WRDATA or RDDATA register.

bit 5 : RSLRRDY (result read ready)
The result register is not empty when this bit is high. At this time, the host can read the result register.

bit 4 : PRMWRDY (parameter write ready)
The PARAMETER register is not full when this bit is high. At this time, the host writes data into the PARAMETER register.

bit 3 : PRMEMPT (parameter empty)
The PARAMETER register is empty when this bit is high.

bit 2 : ADPBUSY (ADPCM busy)
This bit is set high for ADPCM decoding.

bits 1, 0 : RA1, 0
The values of the RA1 and 0 bits for the ADDRESS register can be read from these bits.

3-2-2. RESULT register

The host reads the results of the command execution through this register. The register has ah 8-byte FIFO configuration.

3-2-3. RDDATA (read data) register

This register is where the data from the buffer memory is written from the host. Data can be read in the I/O mode or using DMAC. The register has a 2-byte FIFO configuration.

3-2-4. HINTMSK (host interrupt mask) register

The values written in the HINTMSK register can be read from this register.

3-2-5. HINTSTS (host interrupt status) register

bit 4 : BFWRDY (buffer write ready)

The BFWRDY status is established if there is area where writing is possible in the buffer of 1 sector or more for sound map playback. It is established in any of the following cases:

(1) When the host has set the SMEN bit (bit 5) of the HCHPCTL register high

(2) When there is sound map data area of 1 sector or more in the buffer memory (when the buffer is not full) after the sound map data equivalent to 1 sector from the host has been written into the buffer memory

(3) When an area for writing the sound map data has been created in the buffer memory by the completion of the sound map ADPCM decoding of one sector

bit 3 : BFEMPT (buffer empty)

The BFEMPT status is established when there is no more sector data in the buffer memory upon completion of the sound map ADPCM decoding of one sector for sound map playback.

bits 2 to 0 : INTSTS#2 to 0

The values of these bits are those of the corresponding bits for the sub CPU HIFCTL register.

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ADDRESS	0/	"L"	"L"	"L"	"L"	"L"	"L"	RA1	RA0
COMMAND	10	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PARAMETER	20	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HCHP CTL	30	BFRD	BFWR	SMEN	"L"	"L"	"L"	"L"	"L"
WR DATA	11	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HINT MSK	21	"L"	"L"	"L"	ENBF WRDY	ENBF EMPT	EN INT#2	EN INT#1	EN INT#0
HCLR CTL	31	CHP RST	CLR PRM	SMADP CLR	CLRBF WRDY	CLRBF EMPT	CLR INT#2	CLR INT#1	CLR INT#0
CI	12	"L"	EMPHASIS	"L"	BIT LNGTH	"L"	FS	"L"	S/M
ATV0	22	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ATV1	32	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ATV2	13	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ATV3	23	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ADP CTL	33	"L"	"L"	CHNG ATV	"L"	"L"	"L"	"L"	ADP MUTE

Host write registers

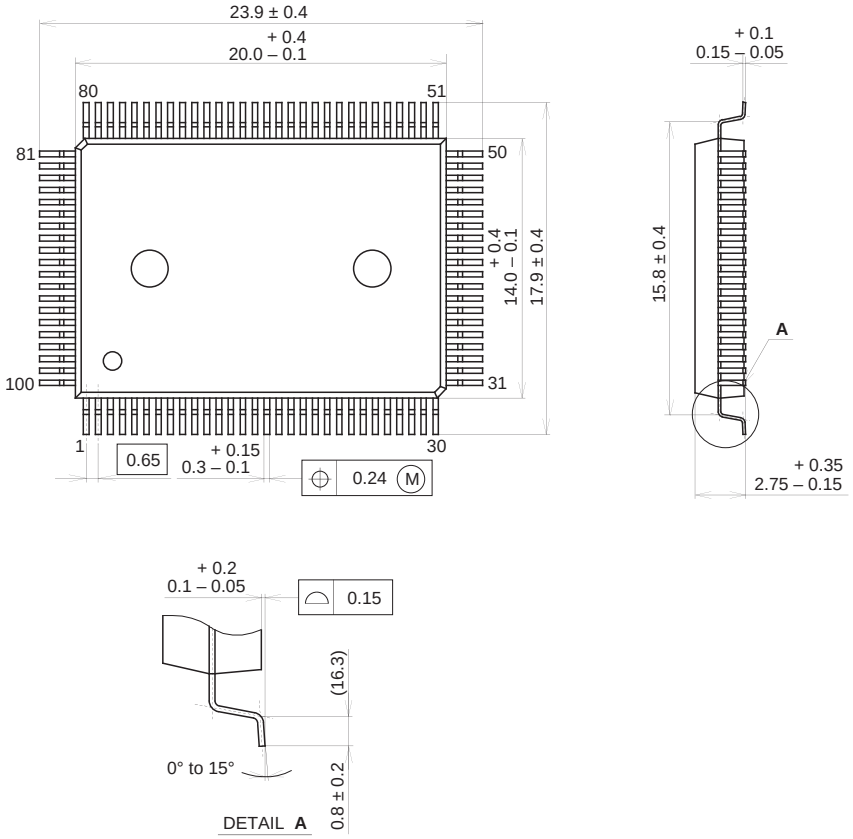
REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HSTS	0/	BUSY STS	DRQ STS	RSL RRDY	PRM WRDY	PRM EMPT	ADP BUSY	RA1	RA0
RESULT	1/	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RD DATA	2/	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HINT MSK	3/0	—	—	—	ENBF WRDY	ENBF EMPT	EN ENT#2	EN ENT#1	EN ENT#0
HINT STS	3/1	—	—	—	BF WRDY	BF EMPT	INT STS#2	INT STS#1	INT STS#0

Host read registers

Note) The left figures in the ADR column denote the HA1 and 0 pins and the right denote the RA1 and 0 pins.

Package Outline Unit : mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g