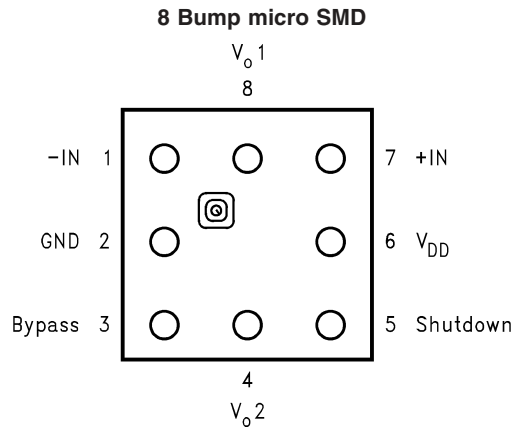


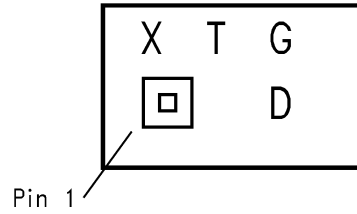
Connection Diagrams



10136023

Top View
Order Number LM4878IBP, LM4878IBPX
See NS Package Number BPA08B6B

micro SMD Marking



10136036

Top View
X - Date Code
T - Die Traceability
G - Boomer Family
D - LM4878IBP

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to $V_{DD} + 0.3V$
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2500V
ESD Susceptibility (Note 5)	250V
Junction Temperature	150°C

Soldering Information

See AN-1112 'Micro-SMD Wafers Level Chip Scale Package'.

Operating Ratings

Temperature Range

$$T_{MIN} \leq T_A \leq T_{MAX}$$

$$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$$

Supply Voltage

$$2.0V \leq V_{DD} \leq 5.5V$$

Electrical Characteristics $V_{DD} = 5V$ (Notes 1, 2, 9)

The following specifications apply for $V_{DD} = 5V$ and 8Ω Load unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM4878		Units (Limits)
			Typical	Limit	
			(Note 6)	(Note 7)	
V_{DD}	Supply Voltage			2.0 5.5	V (min) V (max)
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0V, I_o = 0A$	5.3	7	mA (max)
I_{SD}	Shutdown Current	$V_{PIN5} = 0V$	0.01	2	μA (max)
V_{OS}	Output Offset Voltage	$V_{IN} = 0V$	5	50	mV (max)
P_o	Output Power	THD = 0.2% (max); $f = 1\text{ kHz}$	1		W
THD+N	Total Harmonic Distortion+Noise	$P_o = 0.25\text{ Wrms}; A_{VD} = 2; 20\text{ Hz} \leq f \leq 20\text{ kHz}$	0.1		%
PSRR	Power Supply Rejection Ratio	$V_{DD} = 4.9V\text{ to }5.1V$	65		dB

Electrical Characteristics $V_{DD} = 3.3V$ (Notes 1, 2, 9)

The following specifications apply for $V_{DD} = 3.3V$ and 8Ω Load unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM4878		Units (Limits)
			Typical	Limit	
			(Note 6)	(Note 7)	
V_{DD}	Supply Voltage			2.0 5.5	V (min) V (max)
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0V, I_o = 0A$	4		mA (max)
I_{SD}	Shutdown Current	$V_{PIN5} = 0V$	0.01		μA (max)
V_{OS}	Output Offset Voltage	$V_{IN} = 0V$	5		mV (max)
P_o	Output Power	THD = 1% (max); $f = 1\text{ kHz}$.5	.45	W
THD+N	Total Harmonic Distortion+Noise	$P_o = 0.25\text{ Wrms}; A_{VD} = 2; 20\text{ Hz} \leq f \leq 20\text{ kHz}$	0.15		%
PSRR	Power Supply Rejection Ratio	$V_{DD} = 3.2V\text{ to }3.4V$	65		dB

Electrical Characteristics $V_{DD} = 2.6V$ (Notes 1, 2, 8, 9)

The following specifications apply for $V_{DD} = 2.6V$ and 8Ω Load unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM4878		Units (Limits)
			Typical	Limit	
			(Note 6)	(Note 7)	
V_{DD}	Supply Voltage			2.0 5.5	V (min) V (max)
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0V, I_o = 0A$	3.4		mA (max)
I_{SD}	Shutdown Current	$V_{PIN5} = 0V$	0.01		μA (max)

Electrical Characteristics $V_{DD} = 2.6V$ (Notes 1, 2, 8, 9)

The following specifications apply for $V_{DD} = 2.6V$ and 8Ω Load unless otherwise specified. Limits apply for $T_A = 25^\circ C$. (Continued)

Symbol	Parameter	Conditions	LM4878		Units (Limits)
			Typical	Limit	
			(Note 6)	(Note 7)	
V_{OS}	Output Offset Voltage	$V_{IN} = 0V$	5		mV (max)
P_o	Output Power (8Ω)	THD = 0.3% (max); $f = 1$ kHz	0.25		W
	Output Power (4Ω)	THD = 0.5% (max); $f = 1$ kHz	0.5		W
THD+N	Total Harmonic Distortion+Noise	$P_o = 0.25$ Wrms; $A_{VD} = 2$; 20 Hz $\leq f \leq 20$ kHz	0.25		%
PSRR	Power Supply Rejection Ratio	$V_{DD} = 2.5V$ to $2.7V$	65		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4878, $T_{JMAX} = 150^\circ C$. The typical junction-to-ambient thermal resistance is $150^\circ C/W$.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 5: Machine Model, 220 pF–240 pF discharged through all pins.

Note 6: Typicals are measured at $25^\circ C$ and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Low Voltage Circuit - See Fig. 4

Note 9: Shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of $2\mu A$.

Electrical Characteristics $V_{DD} = 5/3.3/2.6V$ Shutdown Input

Symbol	Parameter	Conditions	LM4878		Units (Limits)
			Typical	Limit	
V_{IH}	Shutdown Input Voltage High			1.2	V(min)
V_{IL}	Shutdown Input Voltage Low			0.4	V(max)

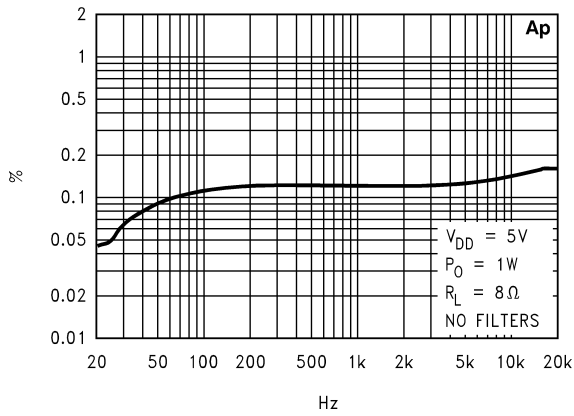
External Components Description

(Figure 1)

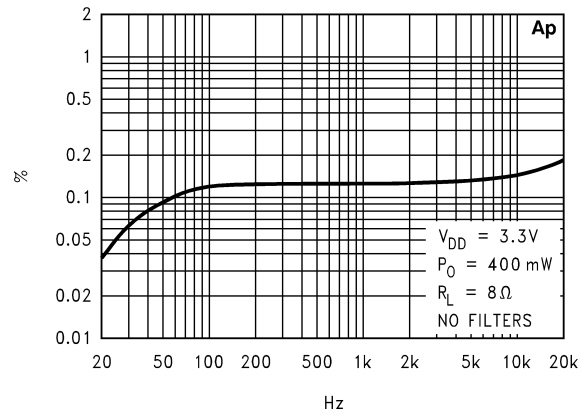
Components	Functional Description
1. R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f . This resistor also forms a high pass filter with C_i at $f_c = 1/(2\pi R_i C_i)$.
2. C_i	Input coupling capacitor which blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section, Proper Selection of External Components , for an explanation of how to determine the value of C_i .
3. R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i .
4. C_S	Supply bypass capacitor which provides power supply filtering. Refer to the Power Supply Bypassing section for information concerning proper placement and selection of the supply bypass capacitor.
5. C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, Proper Selection of External Components , for information concerning proper placement and selection of C_B .

Typical Performance Characteristics

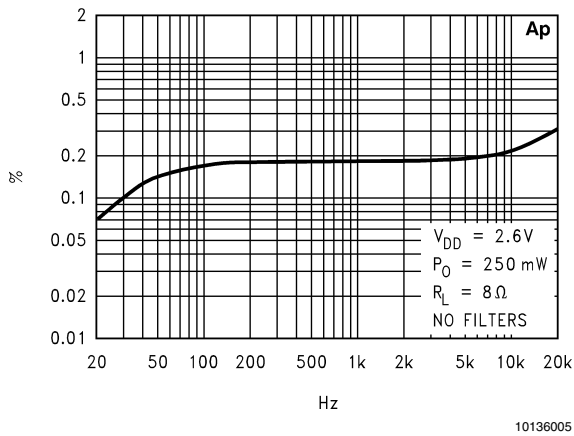
**THD+N vs Frequency
at 5V and 8Ω**



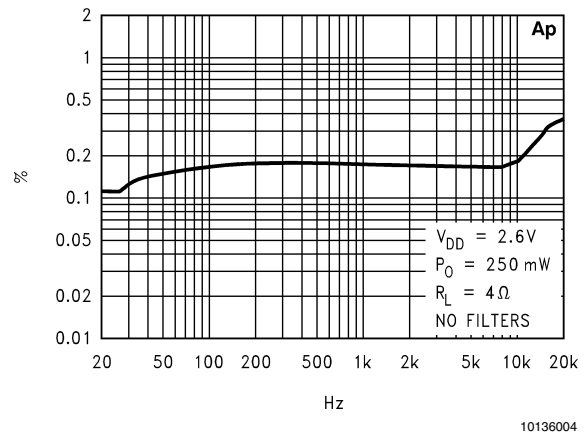
**THD+N vs Frequency
at 3.3V and 8Ω**



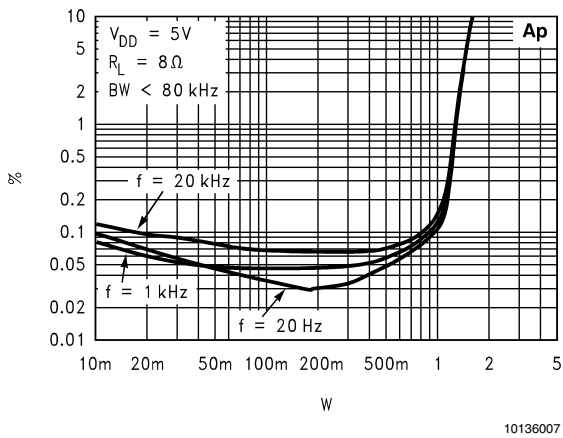
**THD+N vs Frequency
at 2.6V and 8Ω**



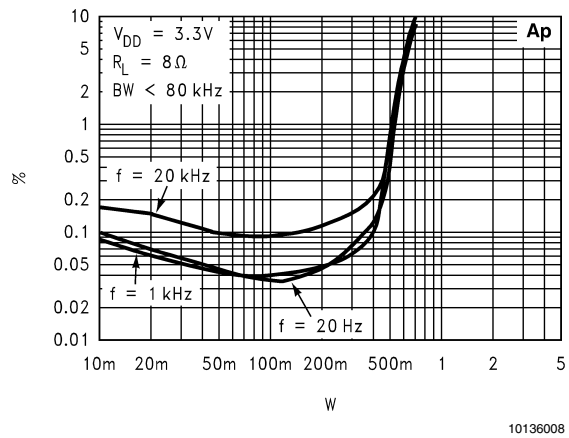
**THD+N vs Frequency
at 2.6V and 4Ω**



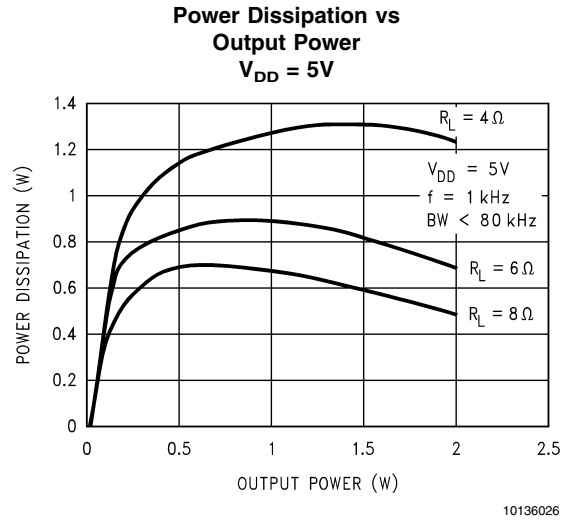
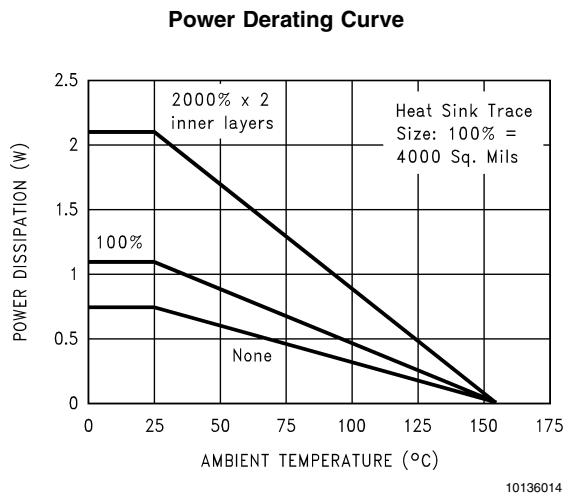
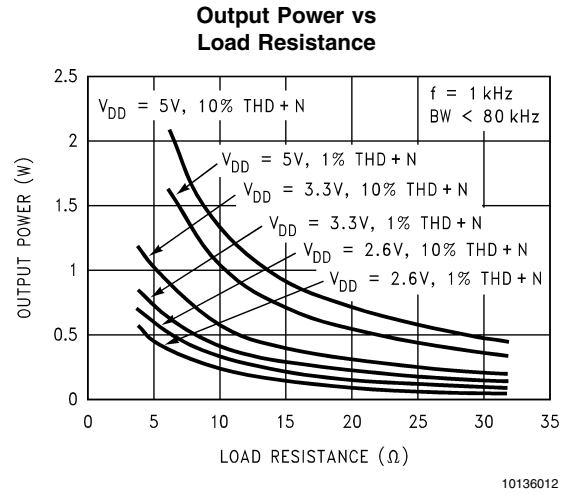
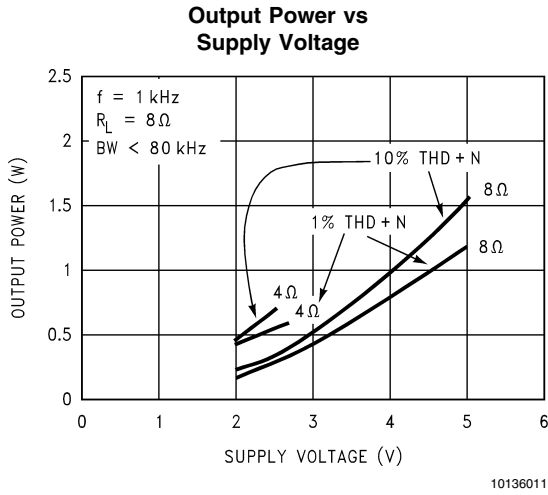
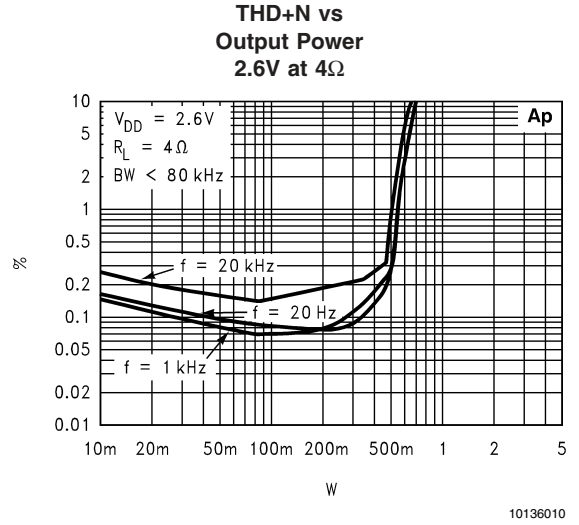
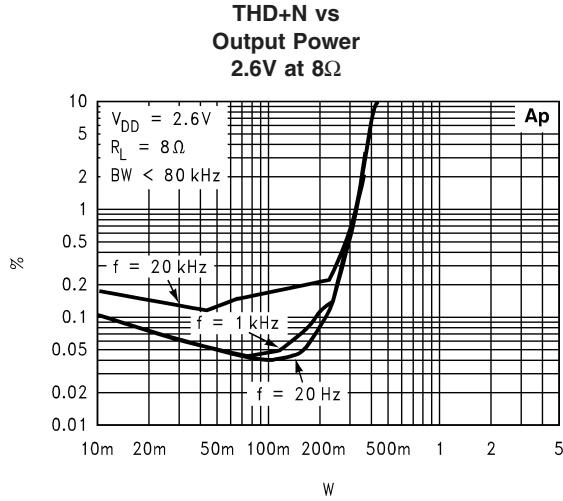
**THD+N vs Output Power
@ VDD = 5V**



**THD+N vs Output Power
@ VDD = 3.3V**

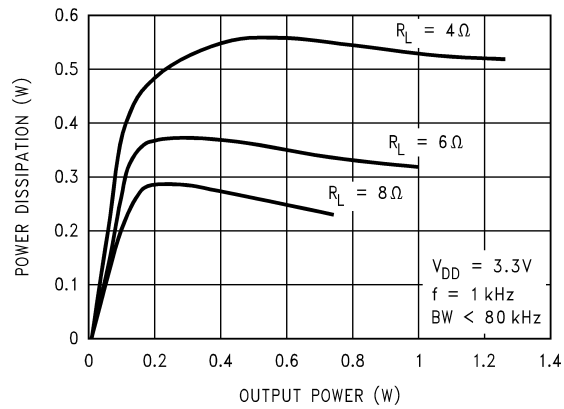


Typical Performance Characteristics (Continued)



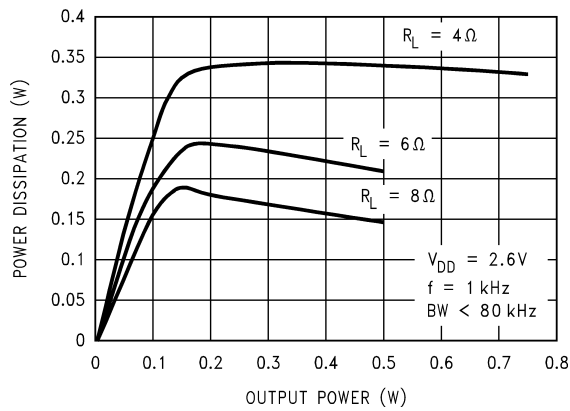
Typical Performance Characteristics (Continued)

**Power Dissipation vs
Output Power**
 $V_{DD} = 3.3V$



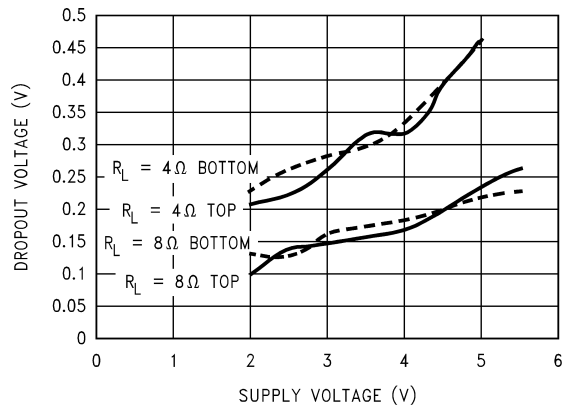
10136027

**Power Dissipation vs
Output Power**
 $V_{DD} = 2.6V$



10136028

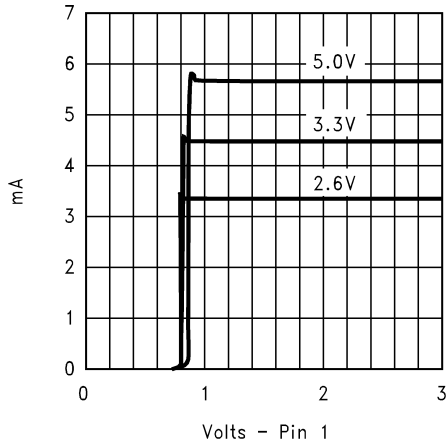
**Clipping Voltage vs
Supply Voltage**



10136015

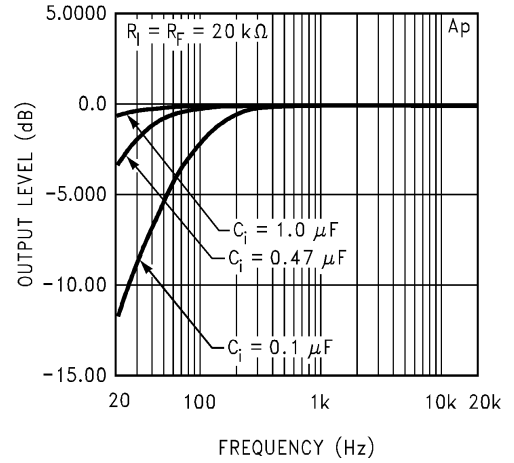
Typical Performance Characteristics (Continued)

Supply Current vs Shutdown Voltage
LM4878 @ VDD = 5/3.3/2.6V_{dc}



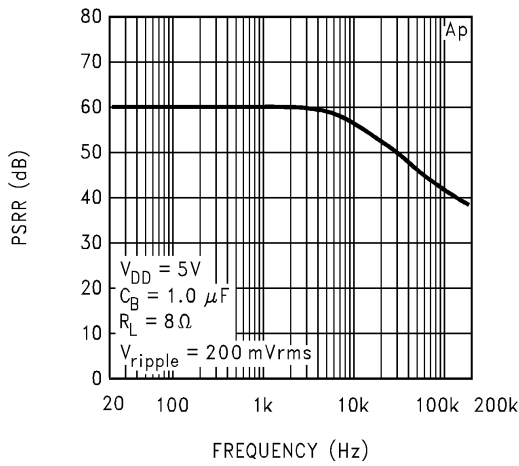
10136035

Frequency Response vs Input Capacitor Size



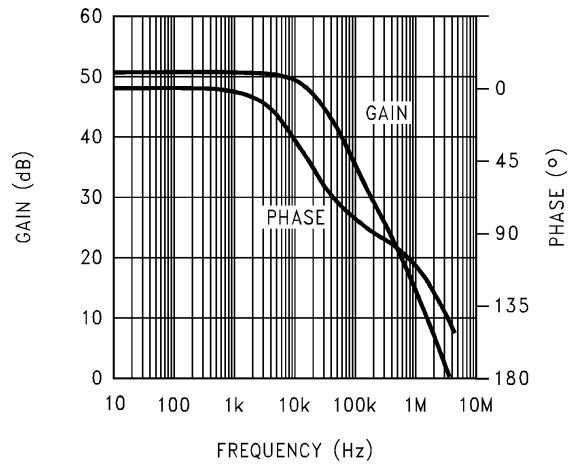
10136017

Power Supply Rejection Ratio



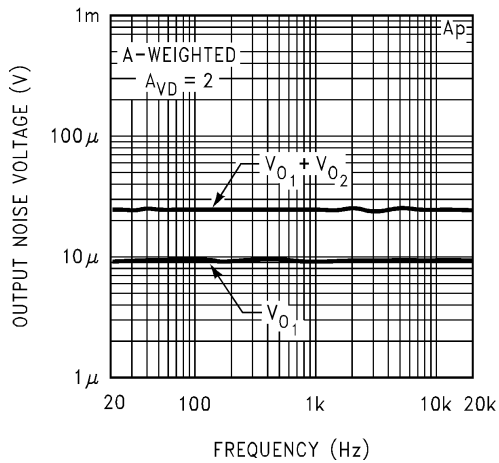
10136018

Open Loop Frequency Response



10136019

Noise Floor



10136016

Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4878 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 10 k Ω resistors. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f/R_i)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in LM4878, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4878 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced from a free air value of 150°C/W, resulting in higher P_{DMAX} . Additional copper foil can be added to any of the leads connected to the LM4878. It is especially effective when connected to V_{DD} , G_{ND} , and the output pins. Refer to the application information on the LM4878 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include re-

duced supply voltage, higher load impedance, or reduced ambient temperature. The National Reference Design board using a 5V supply and an 8 ohm load will run in a 110°C ambient environment without exceeding T_{JMAX} . Internal power dissipation is a function of output power. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 μ F Tantalum or electrolytic capacitor and a 0.1 μ F bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4878. The selection of a bypass capacitor, especially C_B , is dependent upon PSRR requirements, click and pop performance as explained in the section **Proper Selection of External Components**, system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4878 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the shutdown pin. The shutdown pin on the LM4878 has an internal 54K resistor connected to ground that enables the shutdown feature even if the shutdown pin is not connected to ground. By switching the shutdown pin to ground, the LM4878 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than 0.4V $_{DC}$, the idle current may be greater than the typical value of 0.01 μ A.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch to V_{DD} . When the switch is closed, the shutdown pin is connected to V_{DD} which enables the amplifier. This scheme guarantees that the shutdown pin will not float thus preventing unwanted state changes. J1 operates the shutdown function as shown in the Applications Circuit Figure 4. J1 must be installed to operate the part. A switch may be installed in place of J1 for easier evaluation of the shutdown function.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4878 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4878 is unity-gain stable which gives a designer maximum system flexibility. The LM4878 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 V $_{rms}$ are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the band-

Application Information (Continued)

width is dictated by the choice of external components shown in *Figure 1*. The input coupling capacitor, C_i , forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection Of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100 Hz to 150 Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i . A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally $1/2 V_{DD}$). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B , is the most critical component to minimize turn-on pops since it determines how fast the LM4878 turns on. The slower the LM4878's outputs ramp to their quiescent DC voltage (nominally $1/2 V_{DD}$), the smaller the turn-on pop. Choosing C_B equal to 1.0 μF along with a small value of C_i (in the range of 0.1 μF to 0.39 μF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1 μF , the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0 μF is recommended in all but the most cost sensitive designs.

LOW VOLTAGE APPLICATIONS (BELOW 3.0 V_{DD})

The LM4878 will function at voltages below 3 volts but this mode of operation requires the addition of a 1k Ω resistor from each of the differential output pins (pins 8 and 4) directly to ground. The addition of the pair of 1k Ω resistors (R4 & R5) assures stable operation below 3 Volt Vdd operation. The addition of the two resistors will however increase the idle current by as much as 5mA. This is because at 0v input both of the outputs of the LM4878's 2 internal opamps go to $1/2 V_{DD}$ (2.5 volts for a 5v power supply), causing current to flow through the 1K resistors from output to ground. See fig 4.

Jumper options have been included on the reference design, Fig. 4, to accommodate the low voltage application. J2 & J3 connect R4 and R5 to the outputs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8 Ω AUDIO AMPLIFIER

Given:

Power Output	1 Wrms
Load Impedance	8 Ω
Input Level	1 Vrms
Input Impedance	20 k Ω
Bandwidth	100 Hz–20 kHz \pm 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required V_{opeak} using Equation 2 and add the output voltage. Using this method, the minimum supply voltage would be $(V_{\text{opeak}} + (V_{\text{ODTOP}} + V_{\text{ODBOT}}))$, where V_{ODBOT} and V_{ODTOP} are extrapolated from the Dropout Voltage vs Supply Voltage curve in the **Typical Performance Characteristics** section.

$$V_{\text{opeak}} = \sqrt{(2R_L P_O)} \quad (2)$$

Using the Output Power vs Supply Voltage graph for an 8 Ω load, the minimum supply rail is 4.6V. But since 5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4878 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 3.

$$A_{VD} \geq \sqrt{(P_O R_L)} / (V_{IN}) = V_{\text{orms}} / V_{\text{inrms}} \quad (3)$$

$$R_f / R_i = A_{VD} / 2$$

From Equation 3, the minimum A_{VD} is 2.83; use $A_{VD} = 3$.

Since the desired input impedance was 20 k Ω , and with a A_{VD} impedance of 2, a ratio of 1.5:1 of R_f to R_i results in an allocation of $R_i = 20$ k Ω and $R_f = 30$ k Ω . The final design step is to address the bandwidth requirements which must be stated as a pair of -3 dB frequency points. Five times away from a -3 dB point is 0.17 dB down from passband response which is better than the required ± 0.25 dB specified.

$$f_L = 100 \text{ Hz} / 5 = 20 \text{ Hz}$$

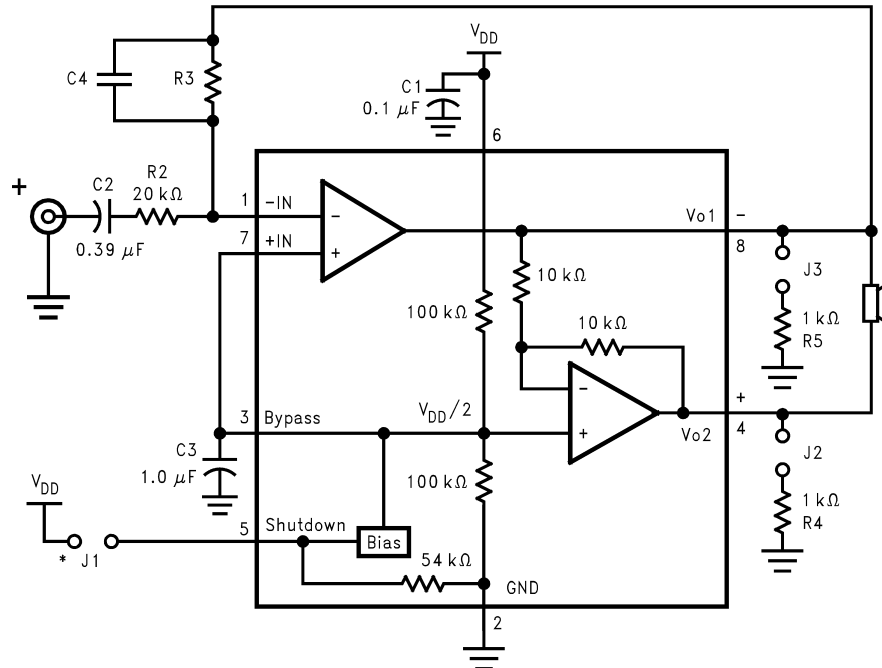
$$f_H = 20 \text{ kHz} * 5 = 100 \text{ kHz}$$

As stated in the **External Components** section, R_i in conjunction with C_i create a highpass filter.

$$C_i \geq 1 / (2\pi * 20 \text{ k}\Omega * 20 \text{ Hz}) = 0.397 \mu\text{F}; \text{ use } 0.39 \mu\text{F}$$

The high frequency pole is determined by the product of the desired frequency pole, f_H , and the differential gain, A_{VD} . With a $A_{VD} = 3$ and $f_H = 100$ kHz, the resulting GBWP = 150 kHz which is much smaller than the LM4878 GBWP of 4 MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4878 can still be used without running into bandwidth limitations.

Application Information (Continued)



* Shorting J1 takes the LM4878 out of shutdown mode.

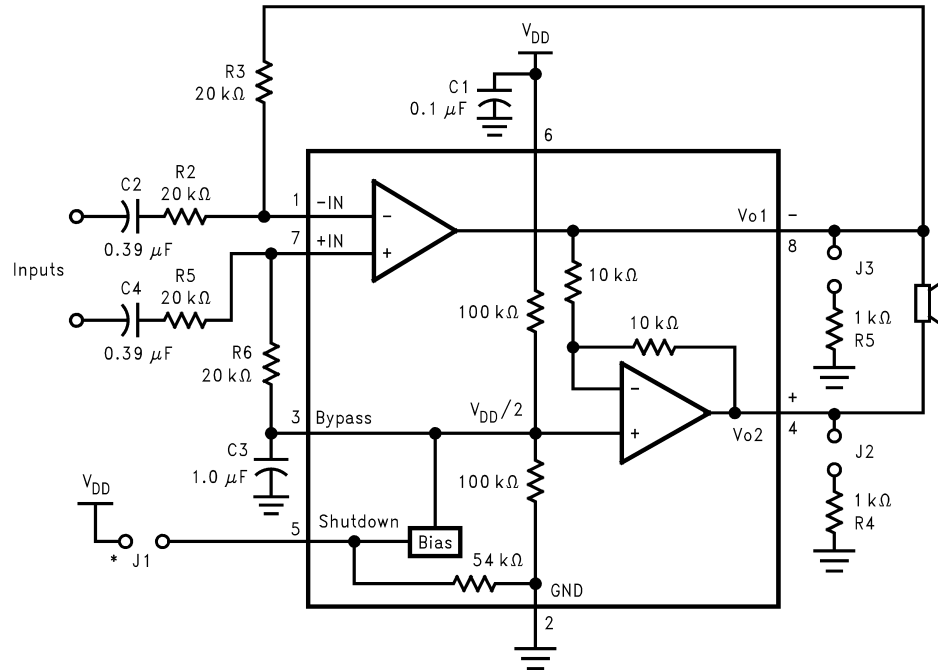
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FIGURE 2. Higher Gain Audio Amplifier

The LM4878 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor may be needed as shown in Figure 2 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken

when calculating the -3dB frequency. An incorrect combination of R_3 and C_4 can cause a frequency roll off below 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is $R_3 = 20\text{k}\Omega$ and $C_4 = 25\text{pf}$. These components result in a -3dB point of approximately 320 kHz. It is not recommended that the feedback resistor and capacitor be used to implement a band limiting filter below 100kHz.

Application Information (Continued)



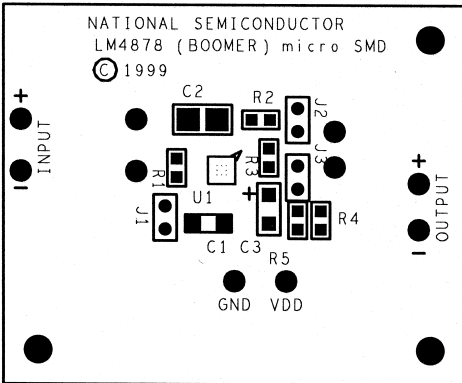
* Shorting J1 takes the LM4878 out of shutdown mode.

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FIGURE 3. Differential Amplifier Configuration for LM4878

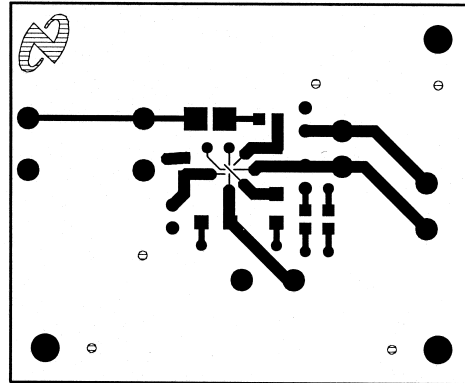
Application Information (Continued)

Silk Screen



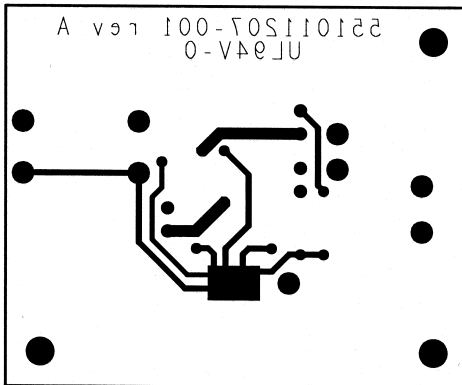
10136030

Top Layer



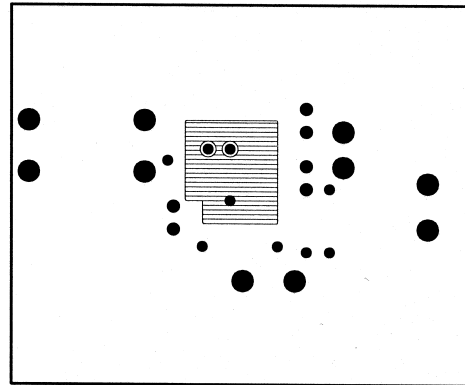
10136031

Bottom Layer



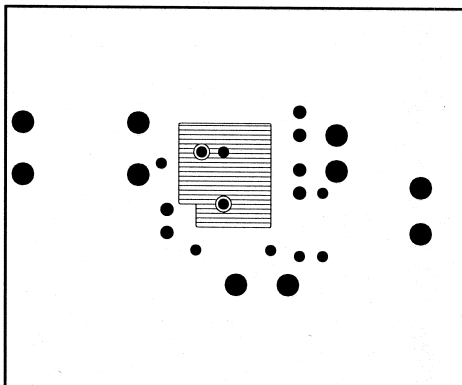
10136032

Inner Layer V_{DD}



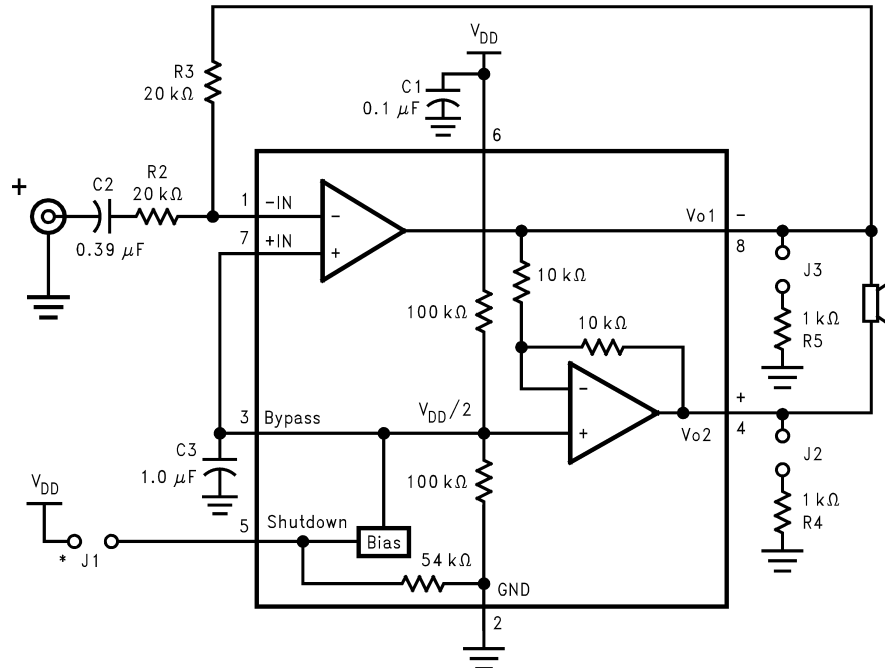
10136033

Inner Layer Ground



10136034

Application Information (Continued)



* Shorting J1 takes the LM4878 out of shutdown mode.

10136025

FIGURE 4. Reference Design Board and PCB Layout Guidelines

Mono LM4878 Reference Design Board - Assembly Part Number: 980011207-100 Revision: A Bill of Material

Item	Part Number	Part Description	Qty	Ref Designator
1	551011208-001	LM4878 Mono Reference Design Board PCB etch 001	1	
10	482911183-001	LM4878 Audio AMP micro SMD 8 Bumps	1	U1
20	151911207-001	Cer Cap 0.1uF 50V +80/-20% 1206	1	C1
21	151911207-002	Cer Cap 0.39uF 50V Z5U 20% 1210	1	C2
25	152911207-001	Tant Cap 1uF 16V 10% Size=A 3216	1	C3
30	472911207-001	Res 20K Ohm 1/10W 5% 0805	3	R2, R3
31	472911207-002	Res 1K Ohm 1/10W 5% 0805	2	R4, R5,
35	210007039-002	Jumper Header Vertical Mount 2X1 0.100	3	J1, J2, J3
36	210007582-001	Jumper Shunt 2 position 0.100	3	

Application Information (Continued)

PCB Layout Guidelines

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only 'rule-of-thumb' recommendations and the actual results will depend heavily on the final layout.

General Mixed Signal Layout Recommendation

Power and Ground Circuits

For 2 layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will take require a greater amount of design time but will not increase the final price of the board. The only extra parts required will be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A 'Pi-filter' can be helpful in minimizing High Frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

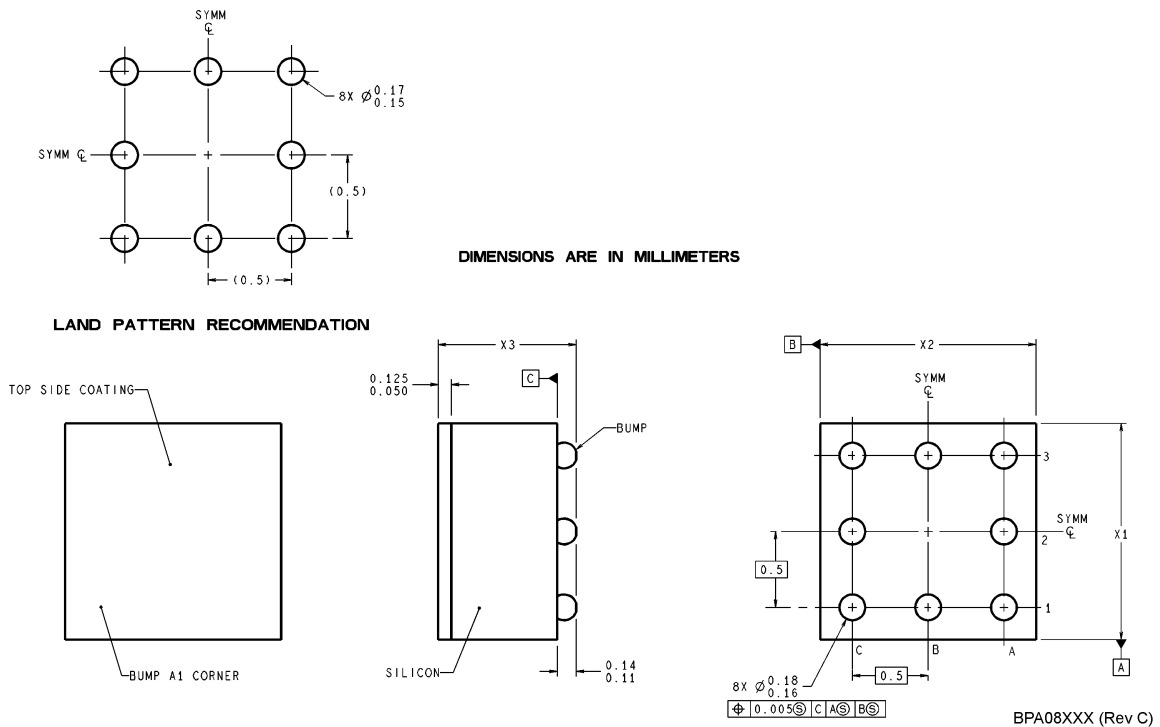
Placement of Digital and Analog Components

All digital components and high-speed digital signals traces should be located as far away as possible from the analog components and the analog circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Physical Dimensions inches (millimeters) unless otherwise noted



Note: Unless otherwise specified.

1. Epoxy coating.
2. 63Sn/37Pb eutectic bump.
3. Recommend non-solder mask defined landing pad.
4. Pin 1 is established by lower left corner with respect to text orientation pins are numbered counterclockwise.
5. Reference JEDEC registration MO-211, variation BC.

8-Bump micro SMD

Order Number LM4878IBP, LM4878IBPX

NS Package Number BPA08B6B

X1 = 1.31±0.03 X2 = 1.97±0.03 X3 = 0.850±0.10

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