

# SIEMENS

**HYB 514400BJ/BJL -50/-60/-70**

**HYB 514400BT/BTL-50/-60/-70**

**1 048 576 x 4 - Bit Dynamic RAM**

## INFORMATION NOTE NO.19

**Fifth Generation 1M x 4 - DRAM  
(Ultrashrink-Version)**

**Characterisation Data**



This information note is intended to provide technical information on the SIEMENS 1M x 4 fifth generation ("Hypershrink-Version") DYNAMIC ACCESS MEMORIES HYB514400B.

### **CHARACTERISTICS OF DC - PARAMETERS**

The SIEMENS HYB 514400B 1M x 4 DRAM device is guaranteed to meet certain DC parametric limits over the temperature range 0° to 70°C. This information note shows the actual performance levels that can typically be expected from devices. Samples out of three different production lots have been randomly selected and characterised.

Typical values of operation and standby currents as a function of temperature, voltage and cycle time are shown in fig.1 through fig. 5.

In fig. 6 the typical behaviour of  $V_{IHmin}$  (minimum TTL-level input high voltage),  $V_{ILmax}$  (maximum TTL-level input low voltage),  $V_{OH}/V_{OL}$  (output high and low voltage) as a function of supply voltage is shown.

### **CHARACTERISTICS OF AC - PARAMETERS**

Supply voltage and temperature dependence of row ( $t_{rac}$ ), column ( $t_{cac}$ ), address access times ( $t_{aa}$ ) and output enable access time ( $t_{oea}$ ) are the topics of fig. 7 and fig. 8.

All other AC - parameters measured at two voltages ( $V_{CC} = 4.5 V$  and  $5.5 V$ ) and two temperatures ( $+85^{\circ}C$  and  $-10^{\circ}C$ ) are put together in table 1.

### **PEAK CURRENT PROFILES**

Fig. 9 through 11 show the current profiles for Read Data "0", Read Data "1" and for a Write Cycle.

### **Influence of Capacitive Loads on Access Time**

All DRAM access times depend on output loading. The influence of capacitive loading from 50 pF to 150 pf is shown in fig. 12. Note that all parametric measurements in all other figures and tables are performed with a 100 pF load according to the data sheets for fast page mode DRAMs.

All measurements shown in this information note have been performed on an ADVANTEST 5361 dedicated memory test system.

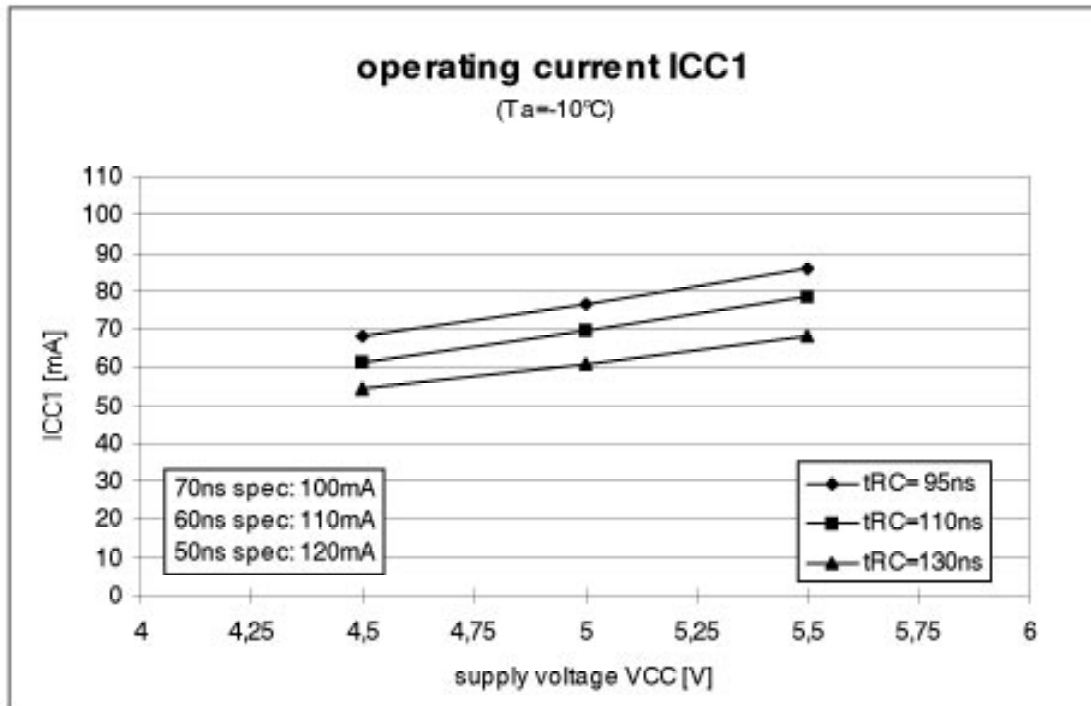
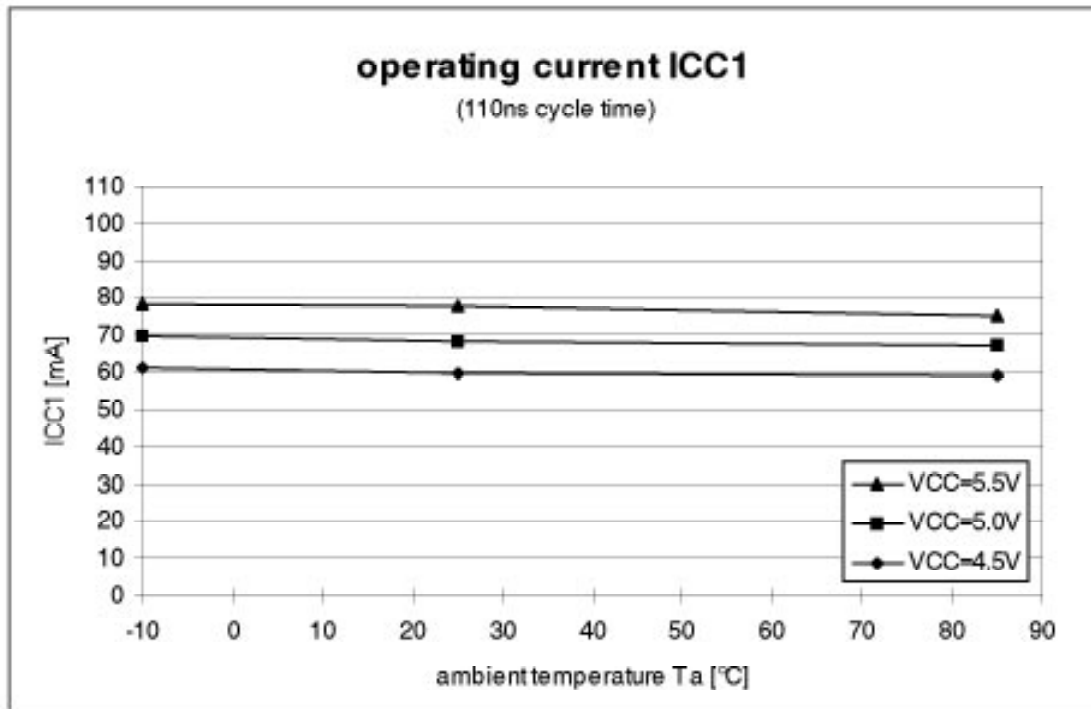


fig.1

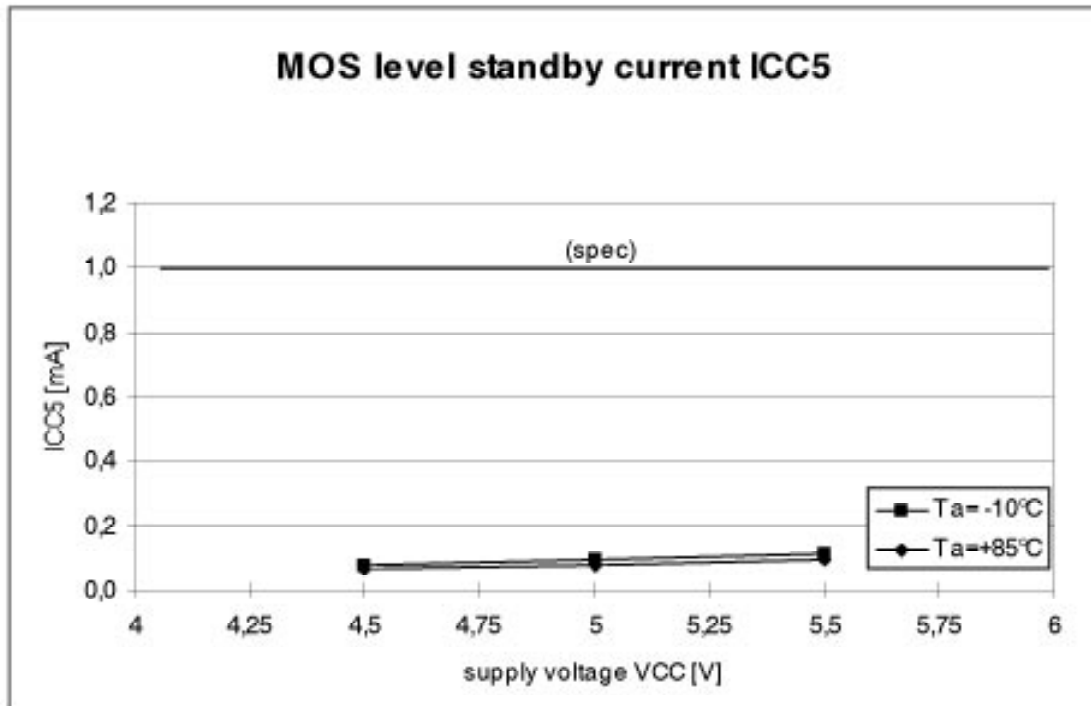
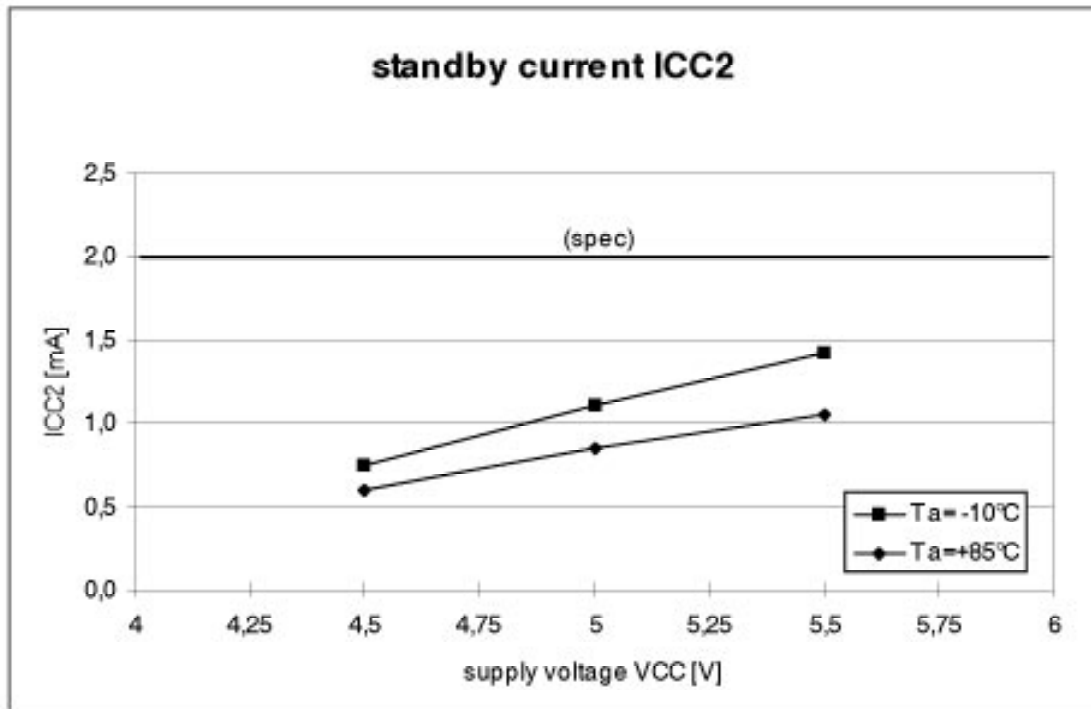


fig.2

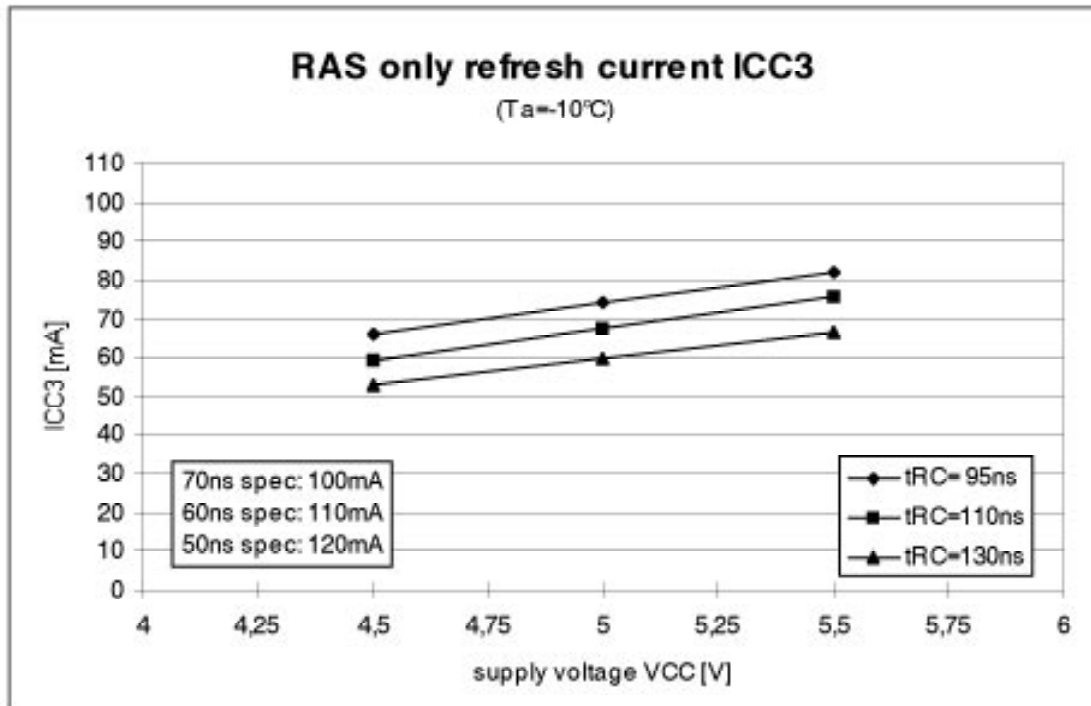
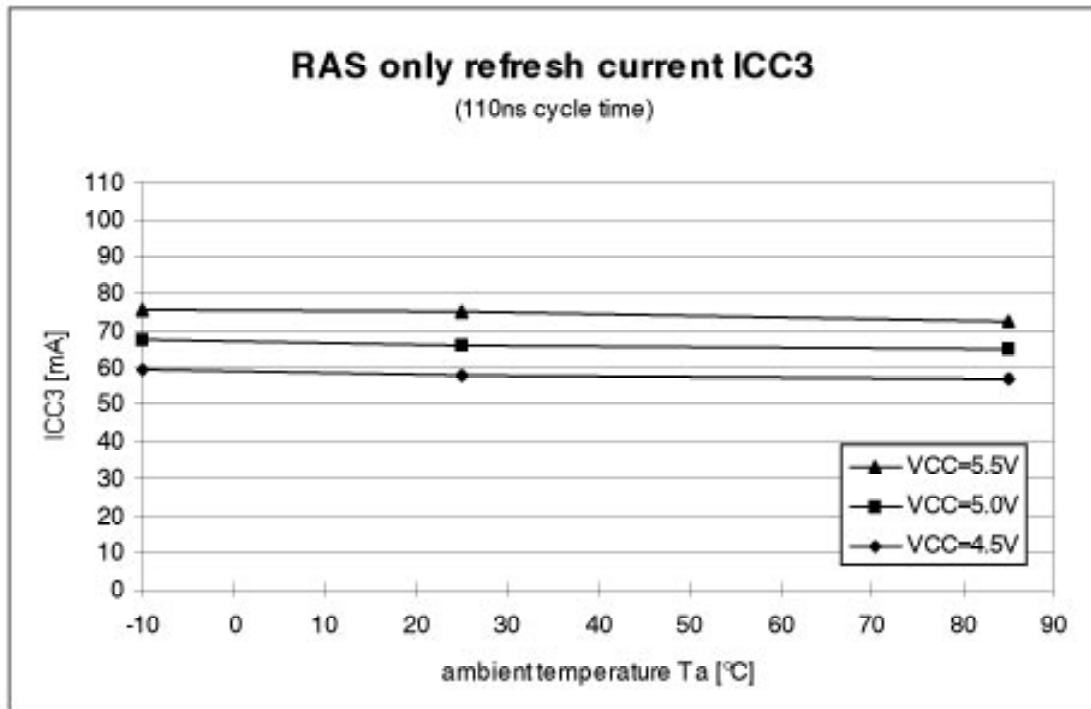


fig.3

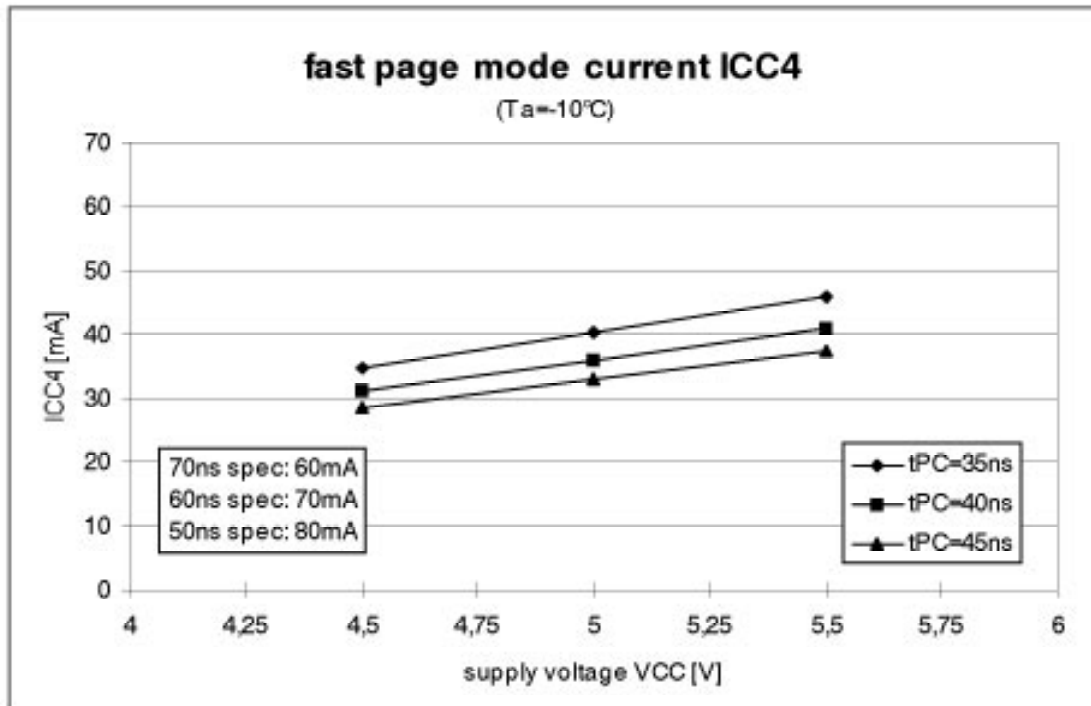
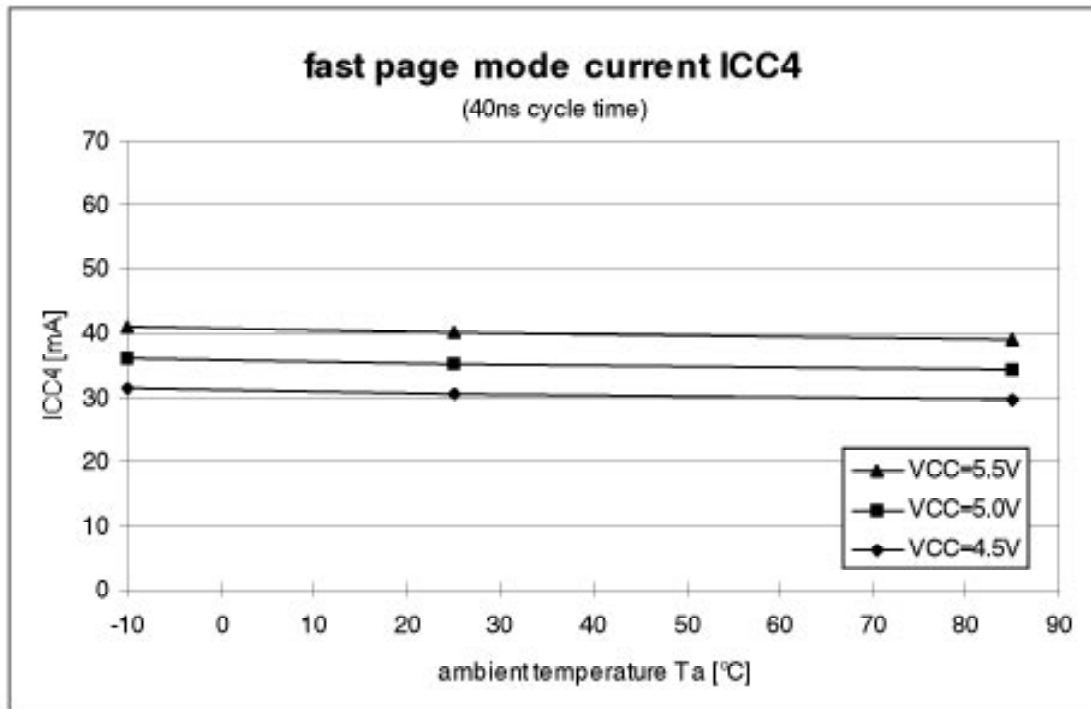


fig.4

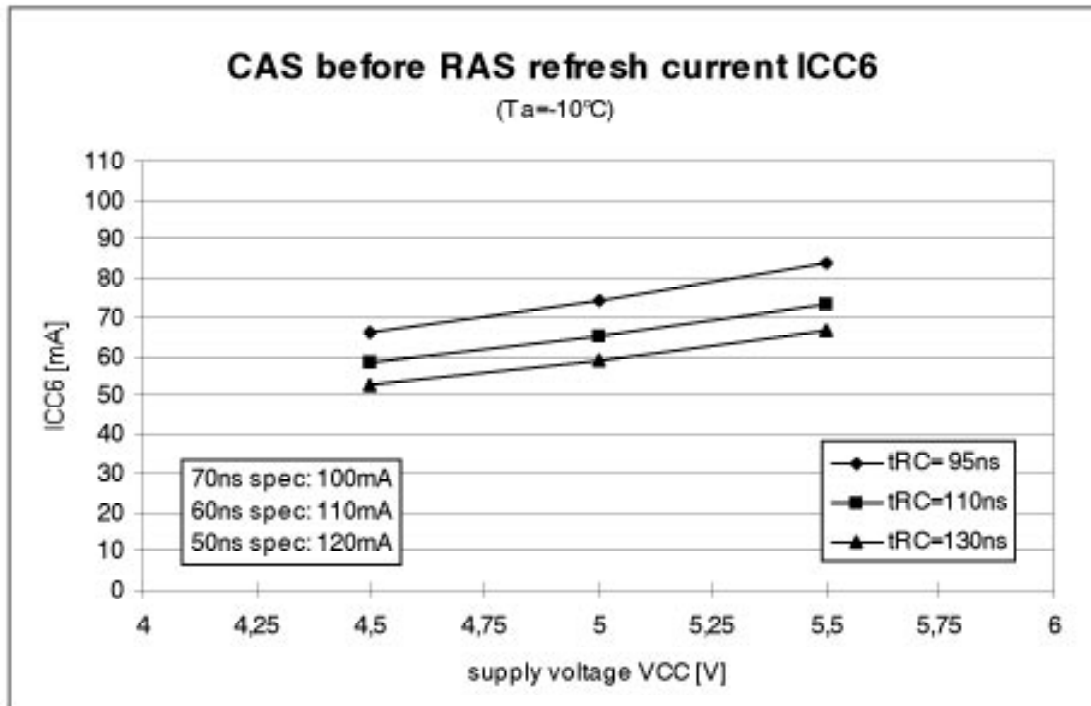
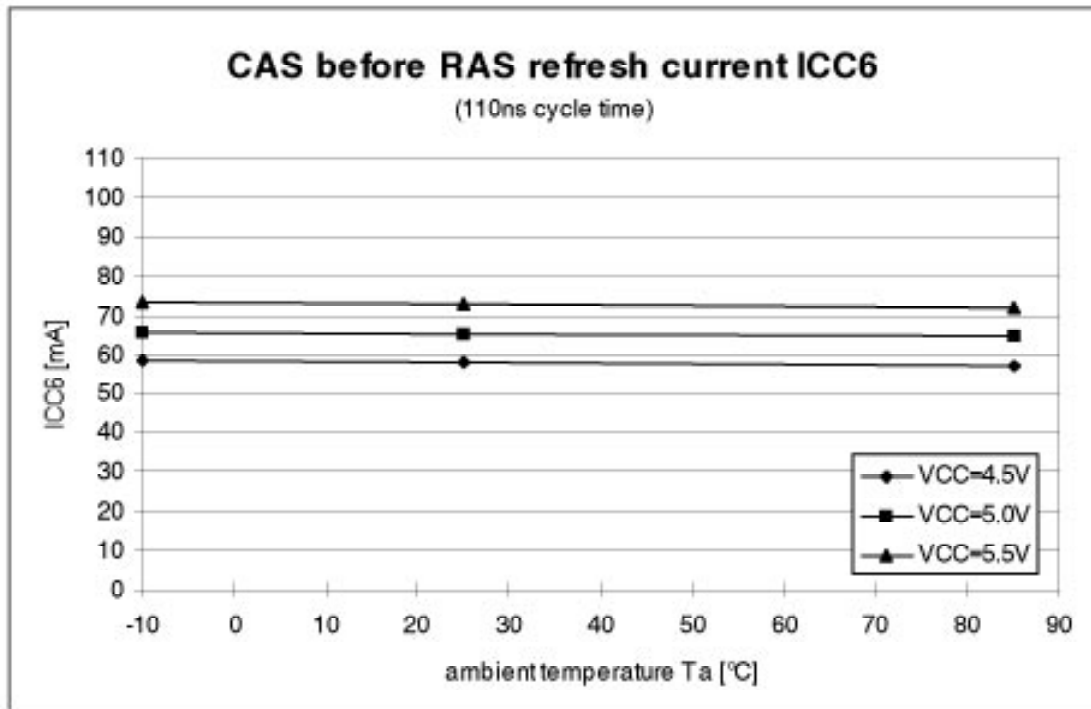


fig.5



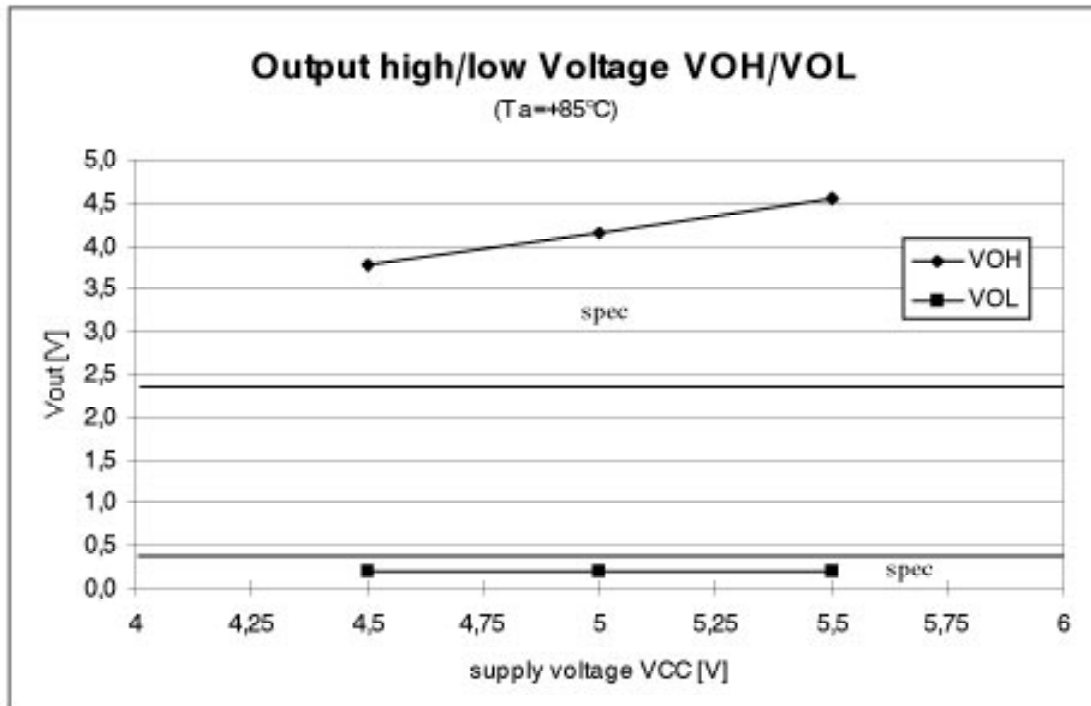
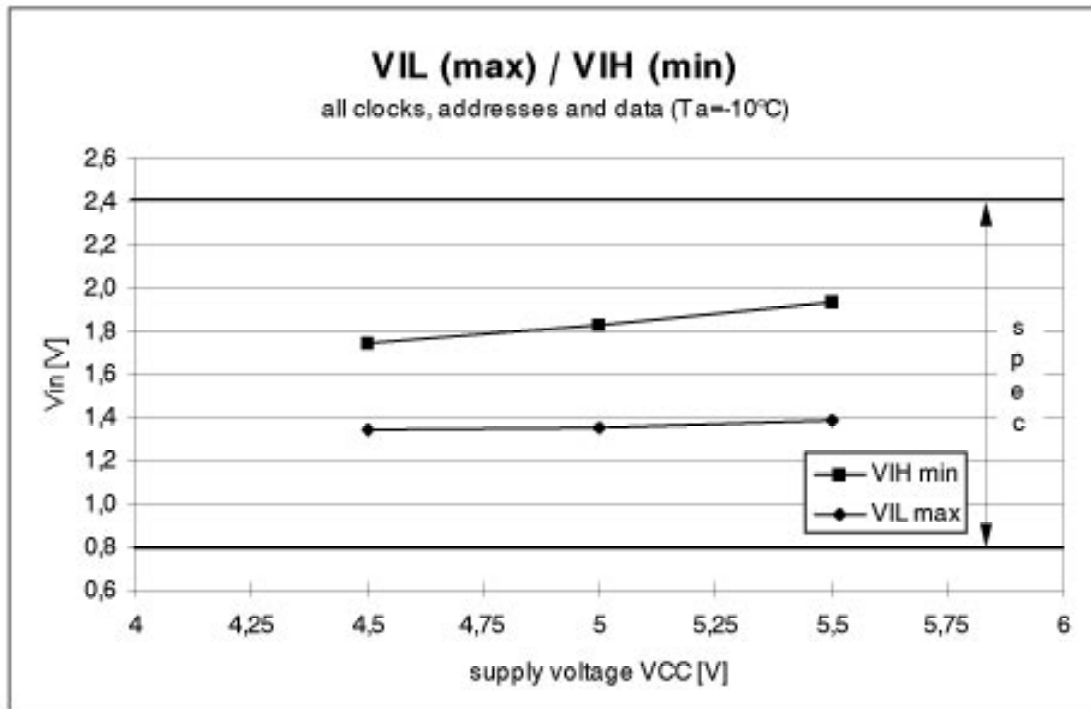


fig.6

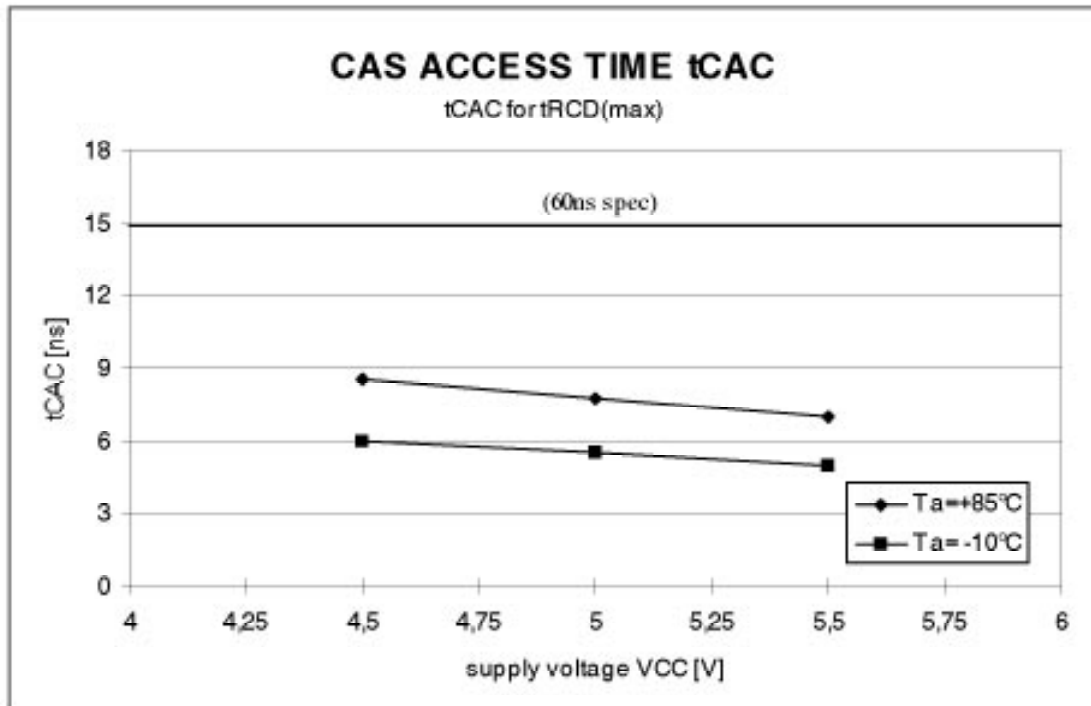
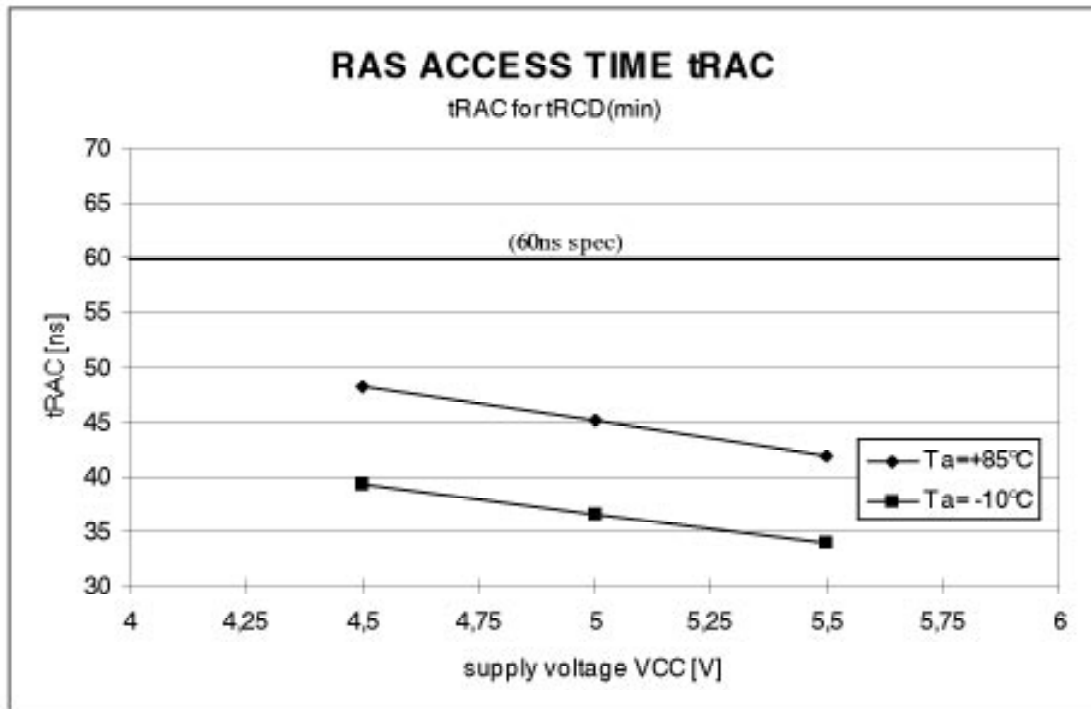


fig.7

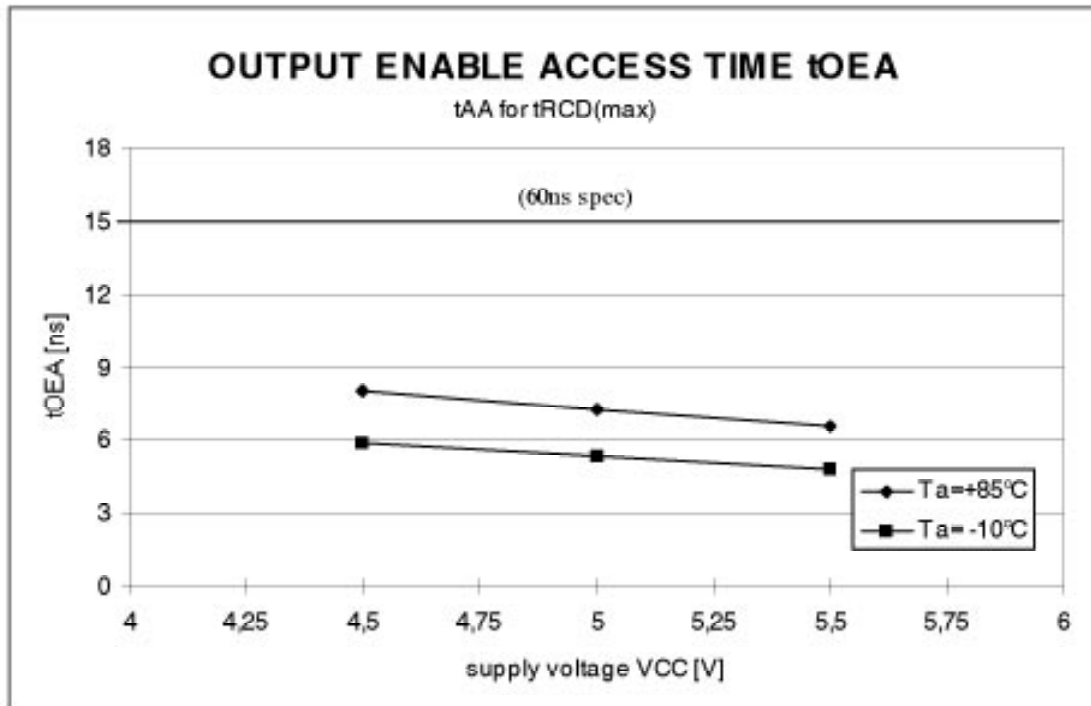
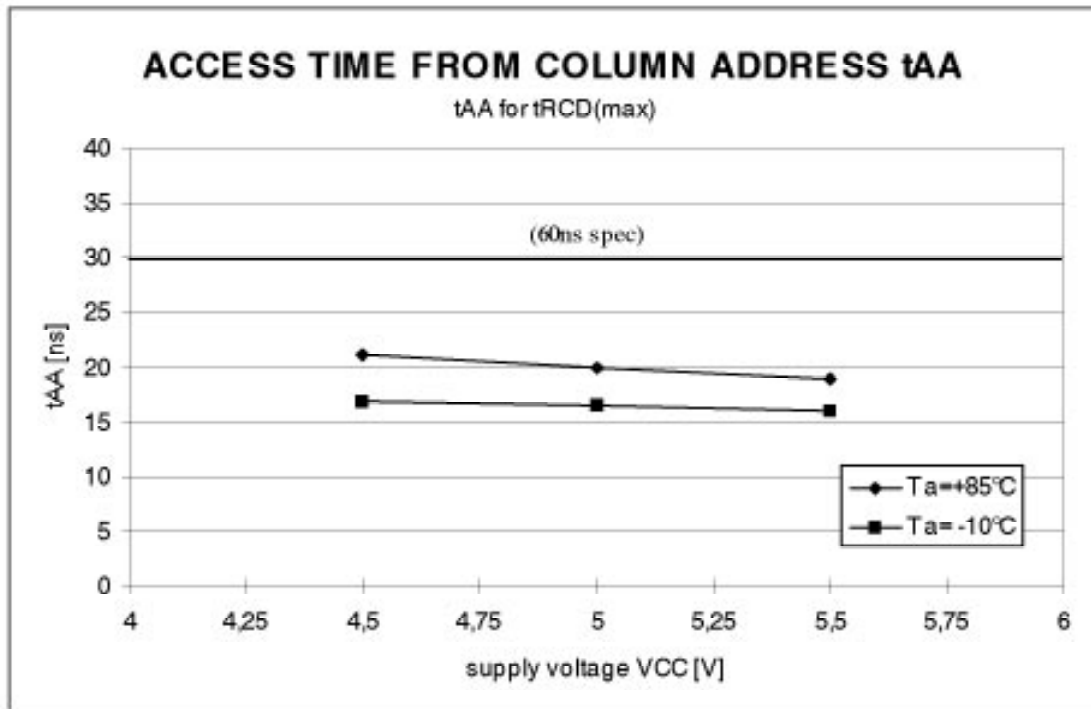


fig.8

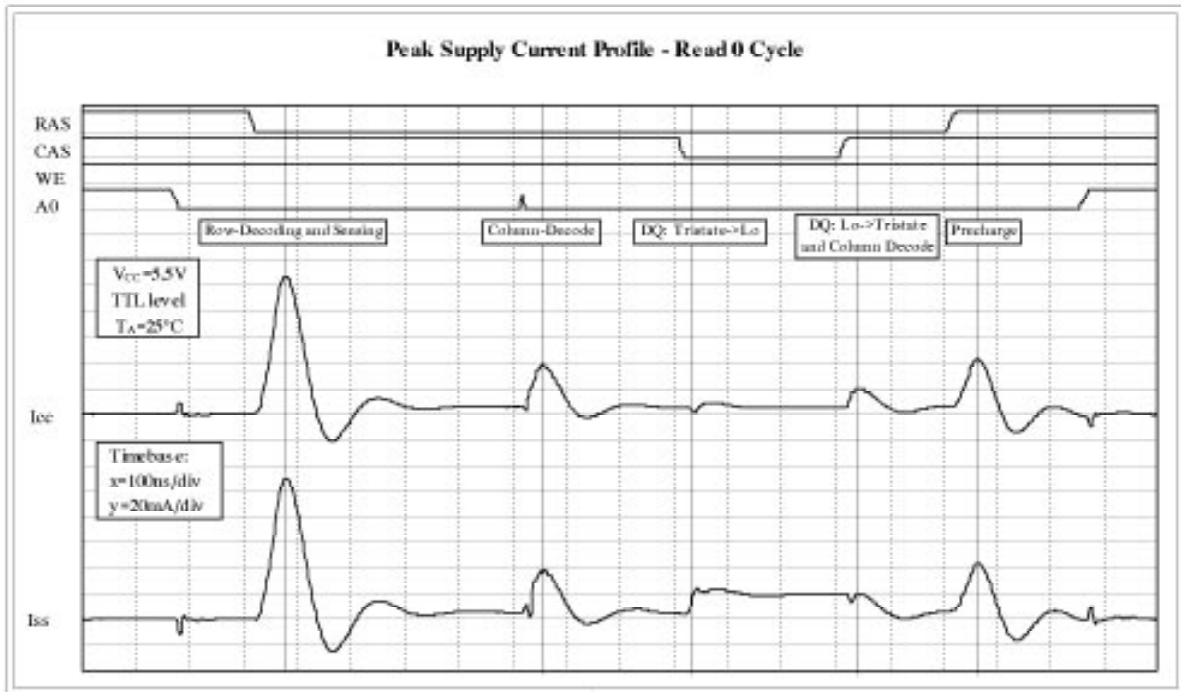


Fig.9

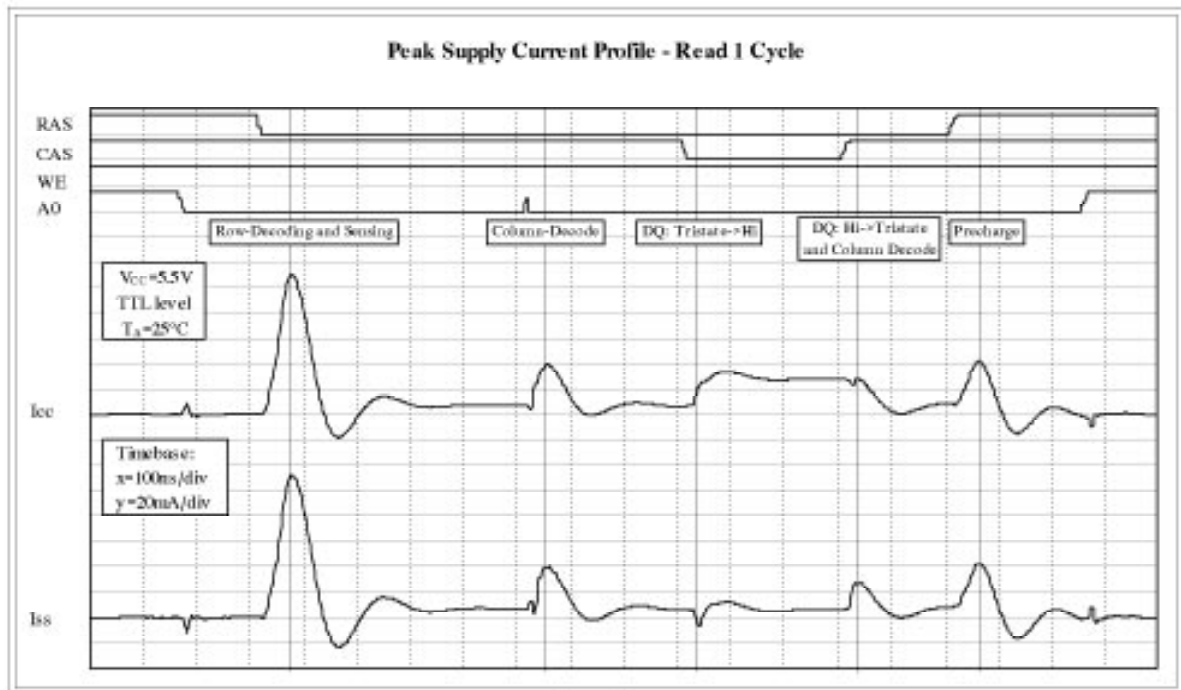


Fig.10

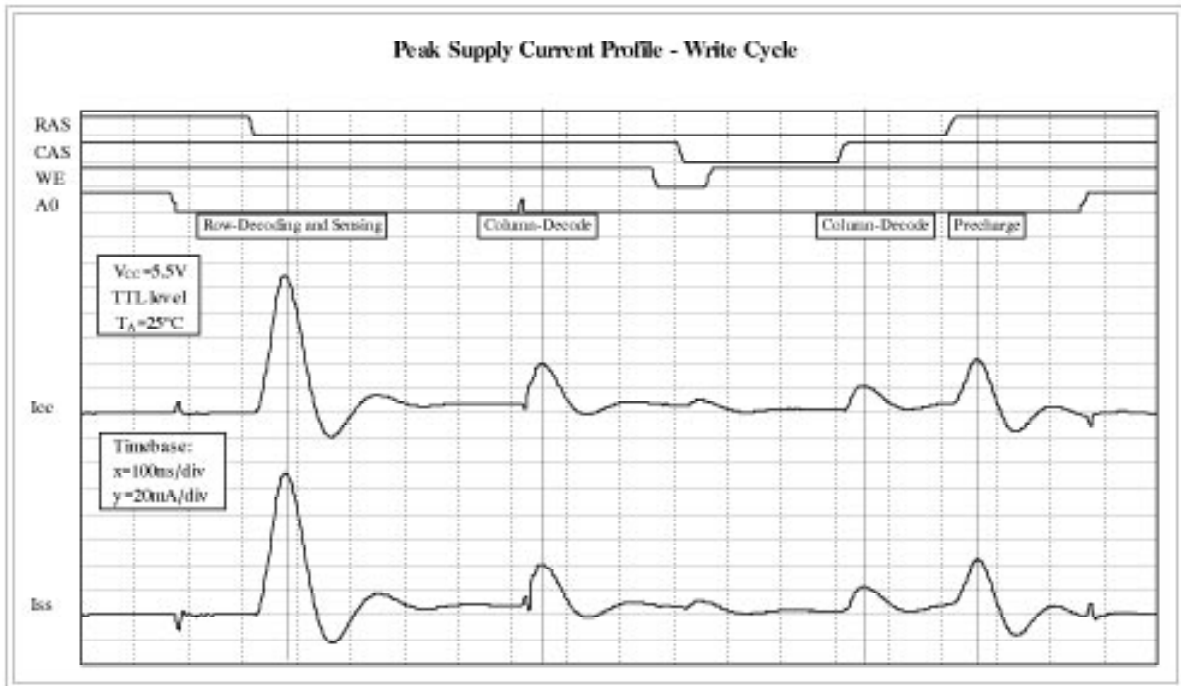


fig.11

**tcac versus capacitive load**

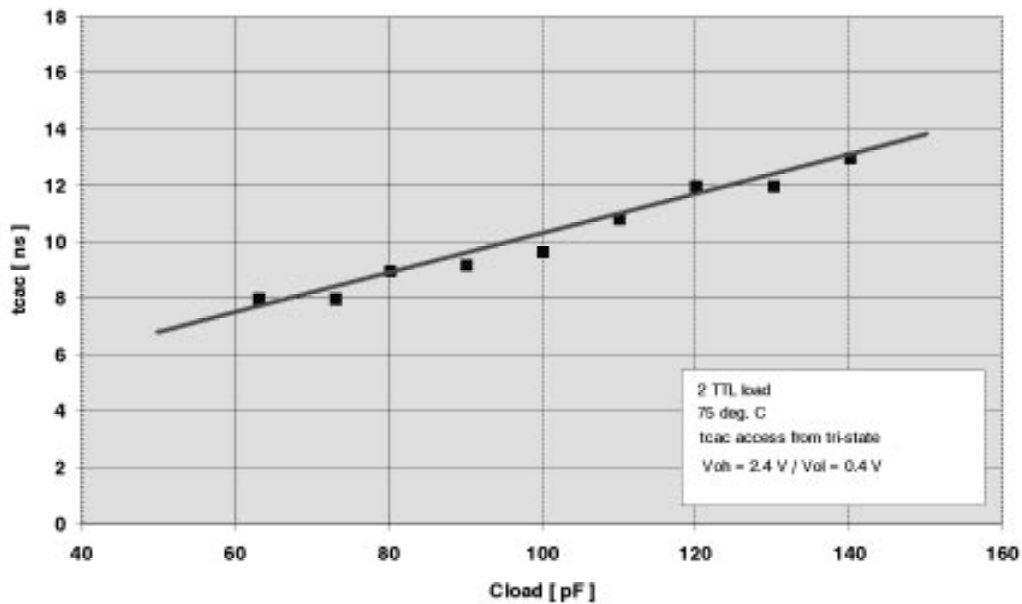


fig.12

**Table 1:**

## AC CHARACTERISTICS

Device : 1M x 4 DRAM

## COMMON PARAMETERS

Parameter	Spec -60ns		Measurement (tT = 5ns)				note
	Unit [ns]		Ta = -10°C		Ta = +85°C		
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V	
trc	110	-	72	67	83	75	1)
trp	40	-	15	13	22	19	
tras	60	10000	20	19	25	20	2)
tcas	15	10000	0	0	4	2	3)
tasr	0	-	-7	-6	-9	-7	
trah	10	-	1	0	2	1	
tasc	0	-	-9	-9	-9	-9	
tcah	15	-	3	2	5	3	
tar	50	-	<=25	<=25	29	<=25	
trcd (min)	20	-	5	5	6	6	
trcd (max)	-	-	33	29	40	35	4)
trad	15	30	6	5	7	6	
trsh	15	-	0	-1	1	0	
tcsh	60	-	34	29	43	37	
tcrp	5	-	-3	-2	-3	-2	
troh	10	-	-6	-7	-6	-7	
toez	0	20	7	7	7	7	

## READ CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
trac	-	60	39	34	48	42
tcac	-	15	6	5	9	7
taa	-	30	17	16	21	19
toea	-	15	6	5	8	7
trcs	0	-	-8	-7	-9	-8
trch	0	-	-7	-6	-8	-6
trrh	0	-	-7	-5	-7	-6
tral	30	-	<=5	<=5	7	6
toff	0	20	2	2	4	4

## WRITE CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
twcs	0	-	-6	-6	-7	-7
twch	10	-	-1	-2	1	0
twp	10	-	-1	-1	0	-1
trwl	15	-	-2	-3	-1	-2
tcwl	15	-	0	-1	2	0
tds	0	-	-6	-5	-7	-6
tdh	15	-	-1	-1	1	0
twcr	50	-	19	18	21	20
tdhr	50	-	<=20	<=20	21	<=20
toeh	20	-	-2	-3	-1	-3

## READ-MODIFY-WRITE CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C		note
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V	
trwc	160	-	103	97	113	106	
trwd	90	-	56	51	65	59	
tcwd	45	-	22	21	25	23	
tawd	60	-	34	33	37	36	

## REFRESH CYCLE CAS-BEFORE-RAS CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
tcsr	5	-	-4	-4	-3	-3
tchr	15	-	-7	-8	-7	-8
trpc	0	-	-7	-6	-8	-7
tcpn	10	-	-1	0	-1	0
twrp	10	-	-5	-3	-5	-4
twrh	10	-	-5	-5	-5	-5

### FAST PAGE MODE CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
tpc	40	-	<=32	<=32	<=32	<=32
tcp	10	-	-1	0	0	1
trasp	60	200000	20	19	25	20 <sup>2)</sup>
tcpa	-	35	21	19	26	24
tprwc	90	-	51	49	55	54

### TEST MODE CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
twts	10	-	-4	-4	-4	-4
twth	10	-	-4	-5	-4	-5

### CAS-BEFORE-RAS COUNTER TEST CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
tcpt	30	-	0	1	1	1

#### Notes:

- 1) all AC-parameters are measured with 0.85V / 2.35 V levels on clock and addresses and with  $t_f = 5ns$ .
- 2) the "min."-value is shown.
- 3)  $tcas(min.)$ -value in a write cycle is shown.
- 4)  $trcd(max.)$  is the reference point where the access time is controlled by  $tcac$ .



