NEC

User's Manual

μPD789167, 789177, 789167Y, 789177Y Subseries

8-Bit Single-Chip Microcontrollers

μPD789166	μPD789166Y	μPD789166(A1)
μPD789167	μPD789167Y	μPD789167(A1)
μPD789176	μPD789176Y	μPD789176(A1)
μPD789177	μPD789177Y	μPD789177(A1)
μPD78F9177	μPD78F9177Y	μPD78F9177A(A1)
μPD78F9177A	μPD78F9177AY	μPD789166(A2)
μPD789166(A)	μPD789166Y(A)	μPD789167(A2)
μPD789167(A)	μPD789167Y(A)	μPD789176(A2)
μPD789176(A)	μPD789176Y(A)	μPD789177(A2)
μPD789177(A)	μPD789177Y(A)	
μPD78F9177A(A)	μPD78F9177AY(A)	

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[MEMO]

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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Regional Information

Some information contained in this document may vary from country to country. Before using any NEC Electronics product in your application, please contact the NEC Electronics office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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INTRODUCTION

Readers

This manual is intended for user engineers who wish to understand the functions of the μPD789167, 789177, 789167Y, and 789177Y Subseries in order to design and develop its application systems and programs.

Target products:

- μPD789167 Subseries: μPD789166, 789167, 789166(A), 789167(A), 789166(A1), 789167(A1), 789166(A2), 789167(A2)
- μPD789177 Subseries: μPD789176, 789177, 78F9177, 78F9177A, 789176(A), 789177(A), 78F9177A(A), 789176(A1), 789177(A1), 78F9177A(A1), 789176(A2), 789177(A2)
- μPD789167Y Subseries: μPD789166Y, 789167Y, 789166Y(A), 789167Y(A)
- μPD789177Y Subseries: μPD789176Y, 789177Y, 78F9177Y, 78F9177AY, 789176Y(A), 789177Y(A), 78F9177AY(A)

The μPD789167, 789177, 789167Y, and 789177Y Subseries is a generic term for all the target devices in this manual.

The generic terms used in this manual indicate the following products.

"Standard quality grade products"... μPD789166, 789167, 789176, 789177, 78F9177, 78F9177A, 789166Y, 789167Y, 789176Y, 789177Y, 78F9177Y, 78F9177AY

"(A) products"... μPD789166(A), 789167(A), 789176(A), 789177(A), 78F9177A(A), 789166Y(A), 789167Y(A), 789176Y(A), 789177Y(A), 78F9177AY(A)

"(A1) products"... μPD789166(A1), 789167(A1), 789176(A1), 789177(A1), 78F9177A(A1)

"(A2) products"... μPD789166(A2), 789167(A2), 789176(A2), 789177(A2)

"Mask ROM versions"... μPD789166, 789167, 789176, 789177, 789166Y, 789167Y, 789176Y, 789177Y, 789166(A), 789167(A), 789176(A), 789177(A), 789166Y(A), 789167Y(A), 789176Y(A), 789177Y(A), 789166(A1), 789167(A1), 789176(A1), 789177(A1), 789166(A2), 789167(A2), 789176(A2), 789177(A2)

"Flash memory versions"... μPD78F9177, 78F9177A, 78F9177A(A), 78F9177A(A1), 78F9177Y, 78F9177AY, 78F9177AY(A)

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The μPD789167, 789177, 789167Y, 789177Y Subseries manual is divided into two parts: this manual and the instruction manual (common to the 78K/0S Series).

μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual (This manual)	78K/0S Series Instruction User's Manual
• Pin functions • Internal block functions • Interrupts • Other internal peripheral functions • Electrical specifications	• CPU function • Instruction set • Instruction description

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electric engineering, logic circuits, and microcontrollers.

◊ For users who use this document as the manual for the μPD789166(A), 789167(A), 789176(A), 789177(A), 789166Y(A), 789167Y(A), 789176Y(A), 789177Y(A), 789166(A1), 789167(A1), 789176(A1), 789177(A1), 789166(A2), 789167(A2), 789176(A2), 789177(A2), 78F9177A(A), 78F9177AY(A), and 78F9177A(A1)

→ The only differences between standard products and (A) products, (A1) products, and (A2) products are quality grades, power supply voltage, operating ambient temperature, minimum instruction execution time, and electrical specifications. (Refer to 1.10 Differences Between Standard Quality Grade Products and (A) Products, (A1) Products, and (A2) Products, and 2.10 Differences Between Standard Quality Grade Products and (A) Products.) For (A) products, (A1) products, and (A2) products, read the part numbers indicated in Chapters 3 to 22 in the following manner.

μPD789166 → μPD789166(A), 789166(A1), 789166(A2)
μPD789167 → μPD789167(A), 789167(A1), 789167(A2)
μPD789176 → μPD789176(A), 789176(A1), 789176(A2)
μPD789177 → μPD789177(A), 789177(A1), 789177(A2)
μPD789166Y → μPD789166Y(A)
μPD789167Y → μPD789167Y(A)
μPD789176Y → μPD789176Y(A)
μPD789177Y → μPD789177Y(A)
μPD78F9177A → μPD789177A(A), 78F9177A(A1)
μPD78F9177AY → μPD78F9177AY(A)

◊ To understand the overall functions of the μPD789167, 789177, 789167Y, and 789177Y Subseries

→ Read this manual in the order of the **CONTENTS**.

◊ How to read register formats

→ The name of a bit whose number is enclosed with < > is reserved in the assembler and is defined as an sfr variable by the #pragma sfr directive in the C compiler.

◊ To learn the detailed functions of a register whose register name is known

→ See **APPENDIX C REGISTER INDEX**.

◊ To learn the details of the instruction functions of the 78K/0S Series

→ Refer to **78K/0S Series Instructions User's Manual (U11047E)** separately available.

◊ To know the electrical specifications of the μPD789167, 789177, 789167Y, and 789177Y Subseries

→ Refer to **CHAPTER 23 ELECTRICAL SPECIFICATIONS (μPD78916x, 17x, 16xY, 17xY, 16x(A), 17x(A), 16xY(A), 17xY(A))**, **CHAPTER 25 ELECTRICAL SPECIFICATIONS (μPD78916x(A1), 78917x(A1), 78916x(A2), 78917x(A2))**, **CHAPTER 27 ELECTRICAL SPECIFICATIONS (μPD78F9177A, 78F9177AY, 78F9177A(A), 78F9177AY(A))**, **CHAPTER 28 ELECTRICAL SPECIFICATIONS (μPD78F9177, 78F9177AY)**, and **CHAPTER 30 ELECTRICAL SPECIFICATIONS (μPD78F9177A(A1))**.

Caution The application examples in this manual are created for "Standard" quality grade products for general electric equipment. When using the application examples in this manual for purposes which require "Special" quality grades, thoroughly examine the quality grade of each part and circuit actually used.

Differences between μPD789167, 789177, 789167Y, and 789177Y Subseries

The μPD789167, 789177, 789167Y, and 789177Y Subseries differ in their package type, A/D converter resolution, and serial interface configuration.

Item \ Subseries		μPD789167	μPD789177	μPD789167Y	μPD789177Y
Package		• 44-pin plastic LQFP		• 44-pin plastic LQFP • 48-pin plastic TQFP	
IC2 pin		Not provided		Provided	
A/D converter resolution		8 bits	10 bits	8 bits	10 bits
Serial interface configuration	3-wire serial I/O mode	1 channel			
	SMB0	Not provided		1 channel	

Configuration of This Manual This manual uses separate chapters to describe the functions that vary between the subseries. The chapters related to each subseries are listed below.

For information about a certain subseries, see only the chapters indicated by checkmarks in that subseries' column.

Chapter	μPD789167 Subseries	μPD789177 Subseries	μPD789167Y Subseries	μPD789177Y Subseries
CHAPTER 1 GENERAL (μPD789167 AND 789177 SUBSERIES)	√	√	–	–
CHAPTER 2 GENERAL (μPD789167Y AND 789177Y SUBSERIES)	–	–	√	√
CHAPTER 3 PIN FUNCTIONS (μPD789167 AND 789177 SUBSERIES	√	√	–	–
CHAPTER 4 PIN FUNCTIONS (μPD789167Y AND 789177Y SUBSERIES)	–	–	√	√
CHAPTER 5 CPU ARCHITECTURE	√	√	√	√
CHAPTER 6 PORT FUNCTIONS	√	√	√	√
CHAPTER 7 CLOCK GENERATOR	√	√	√	√
CHAPTER 8 16-BIT TIMER 90	√	√	√	√
CHAPTER 9 8-BIT TIMER/EVENT COUNTERS 80 TO 82	√	√	√	√
CHAPTER 10 WATCH TIMER	√	√	√	√
CHAPTER 11 WATCHDOG TIMER	√	√	√	√
CHAPTER 12 8-BIT A/D CONVERTER (μPD789167 AND 789167Y SUBSERIES)	√	–	√	–
CHAPTER 13 10-BIT A/D CONVERTER (μPD789177 AND 789177Y SUBSERIES)	–	√	–	√
CHAPTER 14 SERIAL INTERFACE 20	√	√	√	√
CHAPTER 15 SMB0 (μPD789167Y AND 789177Y SUBSERIES)	–	–	√	√
CHAPTER 16 MULTIPLIER	√	√	√	√
CHAPTER 17 INTERRUPT FUNCTIONS	√	√	√	√
CHAPTER 18 STANDBY FUNCTION	√	√	√	√
CHAPTER 19 RESET FUNCTION	√	√	√	√
CHAPTER 20 FLASH MEMORY VERSION	√	√	√	√
CHAPTER 21 MASK OPTION	√	√	√	√
CHAPTER 22 INSTRUCTION SET	√	√	√	√

Conventions

Data significance: Higher digits on the left and lower digits on the right
Active low representation: $\overline{\times\times\times}$ (overscore over pin or signal name)
Note: Footnote for item marked with **Note** in the text
Caution: Information requiring particular attention
Remark: Supplementary information
Numerical representation: Binary ... ×××× or ××××B
Decimal ... ××××
Hexadecimal ... ××××H

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual	This manual
78K/0S Series Instructions User's Manual	U11047E

★ Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U16656E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U16654E
	Language	U14872E
SM78K Series Ver. 2.52 System Simulator	Operation	U16768E
	External Parts User Open Interface Specifications	U15802E
ID78K0S-NS Ver. 2.52 Integrated Debugger	Operation	U16584E
PM plus Ver. 5.10		U16569E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
IE-789177-NS-EM1 Emulation Board	U14621E

Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP3 Flash Memory Programmer User's Manual	U13502E
PG-FP4 Flash Memory Programmer User's Manual	U15260E

Other Related Documents

Document Name	Document No.
SEMICONDUCTORS SELECTION GUIDE Product & Packages	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Device	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the "Semiconductor Device Mount Manual" website (http://www.necel.com/pkg/en/mount/index.html)

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

CONTENTS

1.1 Expanded-Specification Products and Conventional Products

The expanded-specification products and conventional products refer to the following products.

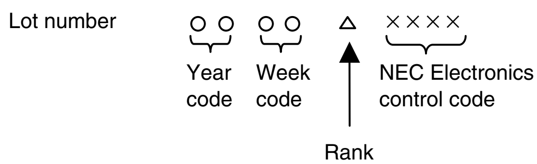
Expanded-specification product... Products with a rank[Note 1] other than K

- Mask ROM versions for which orders were received after December 1, 2001 (except (A1) products and (A2) products[Note 2]).
- μPD78F9177A, 78F9177A(A)

Conventional product... Products with rank[Note 1] K

- Products other than the above expanded-specification products.

Notes 1. The rank is indicated by the 5th digit from the left in the lot number marked on the package.



2. For the (A1) products and (A2) products, refer to 1.10 Differences Between Standard Quality Grade Products and (A) Products, (A1) Products, and (A2) Products.

Expanded-specification products and conventional products differ in operating frequency ratings. The differences are shown in Table 1-1.

Table 1-1. Differences Between Expanded-Specification Products and Conventional Products

Power Supply Voltage (V_{DD})	Guaranteed Operating Speed (Operating Frequency)	
	Conventional Products	Expanded-Specification Products
4.5 to 5.5 V	5 MHz (0.4 μs)	10 MHz (0.2 μs)
3.0 to 5.5 V	5 MHz (0.4 μs)	6 MHz (0.33 μs)
2.7 to 5.5 V	5 MHz (0.4 μs)	5 MHz (0.4 μs)
1.8 to 5.5 V	1.25 MHz (1.6 μs)	1.25 MHz (1.6 μs)

Remark The values in parentheses indicate the minimum instruction execution time.

1.2 Features

- ROM and RAM capacity

Item / Product Name	Program Memory (ROM)		Data Memory (Internal High-Speed RAM)
μPD789166, 789176, 789166(A), 789176(A), 789166(A1), 789176(A1), 789166(A2), 789176(A2)	Mask ROM	16 KB	512 bytes
μPD789167, 789177, 789167(A), 789177(A), 789167(A1), 789177(A1), 789167(A2), 789177(A2)		24 KB	
μPD78F9177, 78F9177A, 78F9177A(A), 78F9177A(A1)	Flash memory	24 KB	

- Minimum instruction execution time changeable from high-speed (0.2 μs: Main system clock 10.0 MHz operation[Note]) to ultra-low speed (122 μs: Subsystem clock 32.768 kHz operation)
- I/O port: 31
- Serial interface: 1 channel
  - 3-wire serial I/O mode/UART mode: 1 channel
- 8-bit resolution A/D converter: 8 channels (μPD789167 Subseries)
- 10-bit resolution A/D converter: 8 channels (μPD789177 Subseries)
- Timer: 6 channels
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 2 channels
  - 8-bit timer: 1 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- Vectored interrupt sources: 15
- Power supply voltage
  - V_{DD} = 1.8 to 5.5 V (μPD78916x, 78917x, 78916x(A), 78917x(A), 78F9177A, 78F9177A(A))
  - V_{DD} = 4.5 to 5.5 V (μPD78916x(A1), 78917x(A1), 78916x(A2), 78917x(A2))
- Operating ambient temperature
  - T_A = –40 to 85°C (μPD78916x, 78917x, 78916x(A), 78917x(A), 78F9177A, 78F9177A(A))
  - T_A = –40 to 110°C (μPD78916x(A1), 78917x(A1), 789177A(A1))
  - T_A = –40 to 125°C (μPD78916x(A2), 78917x(A2))

Note When V_{DD} = 4.5 to 5.5 V and the product is an expanded-specification product

1.3 Applications

Power windows, keyless entry, battery management units, side air bags, etc.

1.4 Ordering Information

	Part Number	Package	Internal ROM
	μPD789166GB-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789166GA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789167GB-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789167GA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789176GB-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789176GA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789177GB-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789177GA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
★	μPD789166GB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Mask ROM
★	μPD789166GA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
★	μPD789167GB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Mask ROM
★	μPD789167GA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
★	μPD789176GB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Mask ROM
★	μPD789176GA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
★	μPD789177GB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Mask ROM
★	μPD789177GA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789166GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789167GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789176GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789177GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789166GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789167GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789176GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789177GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789166GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789167GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789176GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789177GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD78F9177GB-8ES	44-pin plastic LQFP (10 × 10)	Flash memory
	μPD78F9177AGB-8ES	44-pin plastic LQFP (10 × 10)	Flash memory
	μPD78F9177AGA-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Flash memory
★	μPD78F9177GB-8ES-A	44-pin plastic LQFP (10 × 10)	Flash memory
★	μPD78F9177AGB-8ES-A	44-pin plastic LQFP (10 × 10)	Flash memory
★	μPD78F9177AGA-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Flash memory
	μPD78F9177AGB(A)-8ES	44-pin plastic LQFP (10 × 10)	Flash memory
	μPD78F9177AGB(A1)-8ES	44-pin plastic LQFP (10 × 10)	Flash memory

Remarks 1. ××× indicates ROM code suffix.

★ **2.** Products with additional order code “-A” are lead-free products.

1.5 Quality Grades

	Part Number	Package	Quality Grade
	μPD789166GB-×××-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD789166GA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD789167GB-×××-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD789167GA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD789176GB-×××-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD789176GA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD789177GB-×××-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD789177GA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD789166GB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD789166GA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD789167GB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD789167GA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD789176GB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD789176GA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD789177GB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD789177GA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD789166GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789167GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789176GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789177GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789166GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789167GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789176GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789177GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789166GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789167GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789176GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD789177GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD78F9177GB-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD78F9177AGB-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD78F9177AGA-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD78F9177GB-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD78F9177AGB-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD78F9177AGA-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD78F9177AGB(A)-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD78F9177AGB(A1)-8ES	44-pin plastic LQFP (10 × 10)	Special

Remarks 1. ××× indicates ROM code suffix.

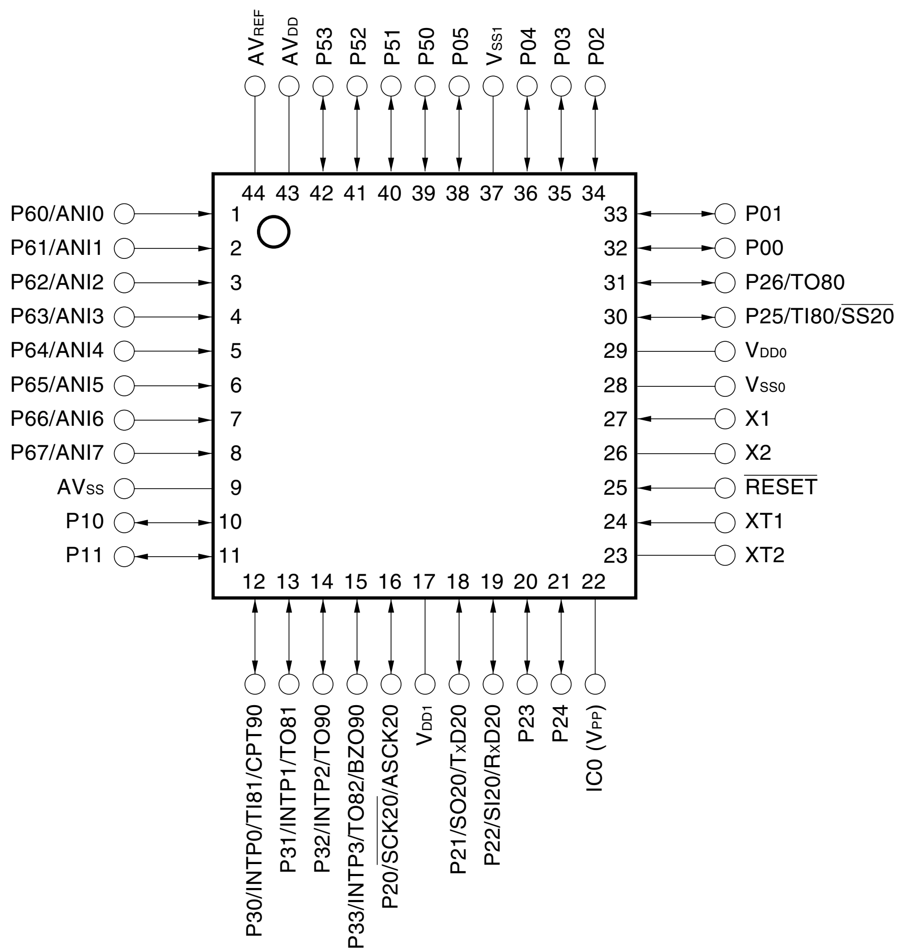
★ **2.** Products with additional order code "-A" are lead-free products.

Please refer to Quality Grades on NEC Semiconductor Devices (C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the devices and its recommended applications.

1.6 Pin Configuration (Top View)

★ • **44-pin plastic LQFP (10 × 10)**

μPD789166GB-×××-8ES
μPD789167GB-×××-8ES
μPD789176GB-×××-8ES
μPD789177GB-×××-8ES
μPD789166GB-×××-8ES-A
μPD789167GB-×××-8ES-A
μPD789176GB-×××-8ES-A
μPD789177GB-×××-8ES-A
μPD789166GB(A)-×××-8ES
μPD789167GB(A)-×××-8ES
μPD789176GB(A)-×××-8ES
μPD789177GB(A)-×××-8ES
μPD789166GB(A1)-×××-8ES
μPD789167GB(A1)-×××-8ES
μPD789176GB(A1)-×××-8ES
μPD789177GB(A1)-×××-8ES
μPD789166GB(A2)-×××-8ES
μPD789167GB(A2)-×××-8ES
μPD789176GB(A2)-×××-8ES
μPD789177GB(A2)-×××-8ES
μPD78F9177GB-8ES
μPD78F9177AGB-8ES
μPD78F9177GB-8ES-A
μPD78F9177AGB-8ES-A
μPD78F9177AGB(A)-8ES
μPD78F9177AGB(A1)-8ES



Cautions 1. Connect the IC0 (internally connected) pin directly to the V_{SS0} or V_{SS1} pin.

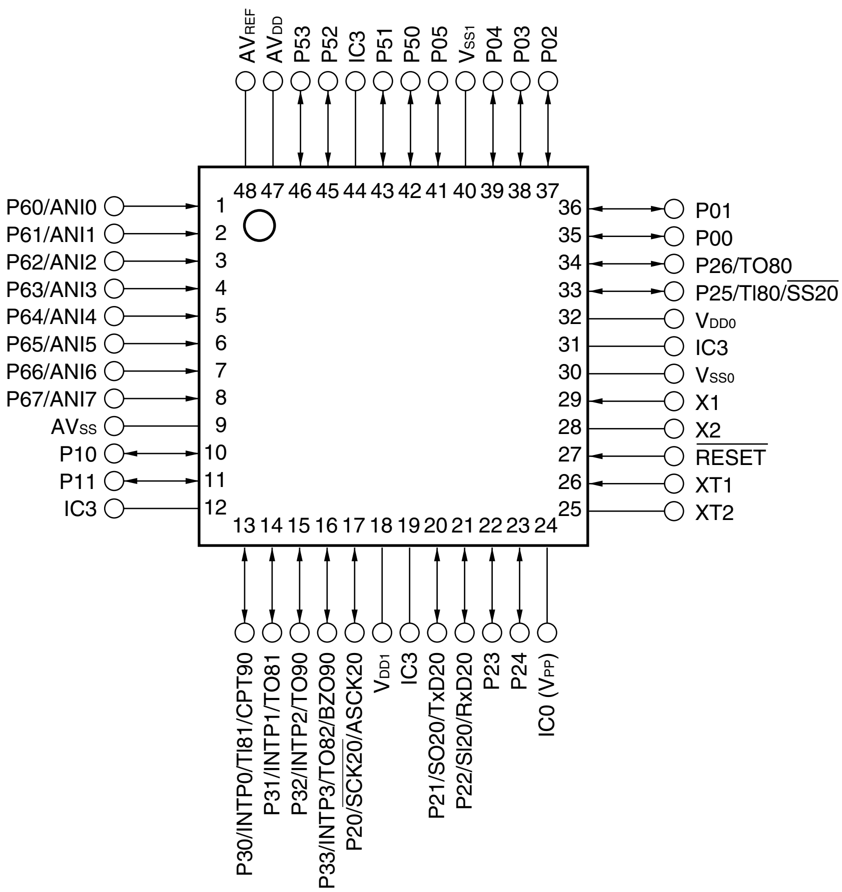
2. Connect the AV_{DD} pin to the V_{DD0} pin.

3. Connect the AV_{SS} pin to the V_{SS0} pin.

Remark Pin connections in parentheses are intended for the μPD78F9177, 78F9177A, 78F9177A(A), and 78F9177A(A1).

★ • **48-pin plastic TQFP (fine pitch) (7 × 7)**

μPD789166GA-×××-9EU μPD789166GA-×××-9EU-A μPD78F9177AGA-9EU
μPD789167GA-×××-9EU μPD789167GA-×××-9EU-A μPD78F9177AGA-9EU-A
μPD789176GA-×××-9EU μPD789176GA-×××-9EU-A
μPD789177GA-×××-9EU μPD789177GA-×××-9EU-A



Cautions 1. Connect the IC0 (internally connected) pin directly to the V_{SS0} or V_{SS1} pin.

2. Leave the IC3 pin open.

3. Connect the AV_{DD} pin to the V_{DD0} pin.

4. Connect the AV_{SS} pin to the V_{SS0} pin.

5. The pin configuration of the 48-pin package for (A), (A1), and (A2) products is undefined.

Remark Pin connections in parentheses are intended for the μPD78F9177A.

ANI0 to ANI7:	Analog input
ASCK20:	Asynchronous serial input
AV_{DD}:	Analog power supply
AV_{REF}:	Analog reference voltage
AV_{SS}:	Analog ground
BZO90:	Buzzer output
CPT90:	Capture trigger input
IC0, IC3:	Internally connected
INTP0 to INTP3:	Interrupt from peripherals
P00 to P05:	Port 0
P10, P11:	Port 1
P20 to P26:	Port 2
P30 to P33:	Port 3
P50 to P53:	Port 5
P60 to P67:	Port 6
$\overline{\text{RESET}}$:	Reset
RxD20:	Receive data
$\overline{\text{SCK20}}$:	Serial clock
SI20:	Serial input
SO20:	Serial output
$\overline{\text{SS20}}$:	Chip select input
TI80, TI81:	Timer input
TO80 to TO82, TO90:	Timer output
TxD20:	Transmit data
V_{DD0}, V_{DD1}:	Power supply
V_{PP}:	Programming power supply
V_{SS0}, V_{SS1}:	Ground
X1, X2:	Crystal (main system clock)
XT1, XT2:	Crystal (subsystem clock)

★1.7 78K/0S Series Lineup

The 78K/0S Series products are shown below. The subseries names are indicated in frames.

Solid frame: Products in mass production
Dashed frame: Products under development

Y Subseries products support SMB.

78K/0S Series

Small-scale package, general-purpose applications

44-pin	μPD789046	μPD789074 with added subsystem clock
42-/44-pin	μPD789026	On-chip UART and capable of low voltage (1.8 V) operation
30-pin	μPD789088	μPD789074 with enhanced timer and increased ROM, RAM capacity
30-pin	μPD789074	μPD789026 with enhanced timer
20-pin	μPD789062	RC oscillation version of the μPD789052
20-pin	μPD789052	μPD789860 without EEPROM, POC, and LVI

Small-scale package, general-purpose applications and A/D converter

44-pin	μPD789177	μPD789177Y	μPD789167 with enhanced A/D converter (10 bits)
44-pin	μPD789167	μPD789167Y	μPD789104A with enhanced timer
30-pin	μPD789134A		μPD789124A with enhanced A/D converter (10 bits)
30-pin	μPD789124A		RC oscillation version of the μPD789104A
30-pin	μPD789114A		μPD789104A with enhanced A/D converter (10 bits)
30-pin	μPD789104A		μPD789026 with added 8-bit A/D converter and multiplier

LCD drive

144-pin	μPD789835B	UART, 8-bit A/D, and dot LCD (Total display output pins: 96)
88-pin	μPD789830	UART and dot LCD (40 × 16)
80-pin	μPD789489	SIO, 10-bit A/D converter, and on-chip voltage booster type LCD (28 × 4)
80-pin	μPD789479	SIO, 8-bit A/D converter, and resistance division type LCD (28 × 4)
80-pin	μPD789417A	μPD789407A with enhanced A/D converter (10 bits)
80-pin	μPD789407A	SIO, 8-bit A/D converter, and resistance division type LCD (28 × 4)
64-pin	μPD789456	μPD789446 with enhanced A/D converter (10 bits)
64-pin	μPD789446	SIO, 8-bit A/D, and on-chip voltage booster type LCD (15 × 4)
64-pin	μPD789436	μPD789426 with enhanced A/D converter (10 bits)
64-pin	μPD789426	SIO, 8-bit A/D, and on-chip voltage booster type LCD (5 × 4)
64-pin	μPD789316	RC oscillation version of the μPD789306
64-pin	μPD789306	SIO and on-chip voltage booster type LCD (24 × 4)
52-pin	μPD789467	8-bit A/D and on-chip voltage booster type LCD (23 × 4)
52-pin	μPD789327	SIO and resistance division type LCD (24 × 4)

USB

44-pin	μPD789800	For PC keyboard and on-chip USB function

Inverter control

44-pin	μPD789842	On-chip inverter controller and UART

On-chip bus controller

44-pin	μPD789852	μPD789850A with enhanced functions such as timer and A/D converter
30-pin	μPD789850A	On-chip CAN controller

Keyless entry

30-pin	μPD789862	μPD789860 with enhanced timer, added SIO, and increased ROM, RAM capacity
20-pin	μPD789861	RC oscillation version of the μPD789860
20-pin	μPD789860	On-chip POC and key return circuit

Sensor

20-pin	μPD789864 (under development)	On-chip analog macro for sensor
20-pin	μPD789863 (under development)	RC oscillation version of the μPD789864

VFD drive

52-pin	μPD789871	On-chip VFD controller (Total display output pins: 25)

Meter control

64-pin	μPD789881	UART and resistance division type LCD (26 × 4)

Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences between the subseries are listed below.

Series for General-purpose applications and LCD drive

Subseries Name		Function: ROM Capacity	Timer: 8-Bit	Timer: 16-Bit	Timer: Watch	Timer: WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
Small-scale package, general-purpose applications	μPD789046	16 KB	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 KB to 16 KB			–							
	μPD789088	16 KB to 32 KB	3 ch							24		
	μPD789074	2 KB to 8 KB	1 ch									
	μPD789062	4 KB	2 ch	–					–	14		RC oscillation version
	μPD789052											–
Small-scale package, general-purpose applications and A/D converter	μPD789177	16 KB to 24 KB	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31	1.8 V	–
	μPD789167						8 ch	–				
	μPD789134A	2 KB to 8 KB	1 ch		–		–	4 ch		20		RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
LCD drive	μPD789835B	24 KB to 60 KB	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	37	1.8 V[Note]	Dot LCD supported
	μPD789830	24 KB	1 ch	1 ch			–			30	2.7 V	
	μPD789489	32 KB to 48 KB	3 ch					8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789479	24 KB to 48 KB					8 ch	–				
	μPD789417A	12 KB to 24 KB					–	7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 KB to 16 KB	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 KB to 16 KB					–		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											–
	μPD789467	4 KB to 24 KB		–			1 ch		–	18		
	μPD789327						–		1 ch	21		

Note Flash memory version: 3.0 V

Series for ASSP

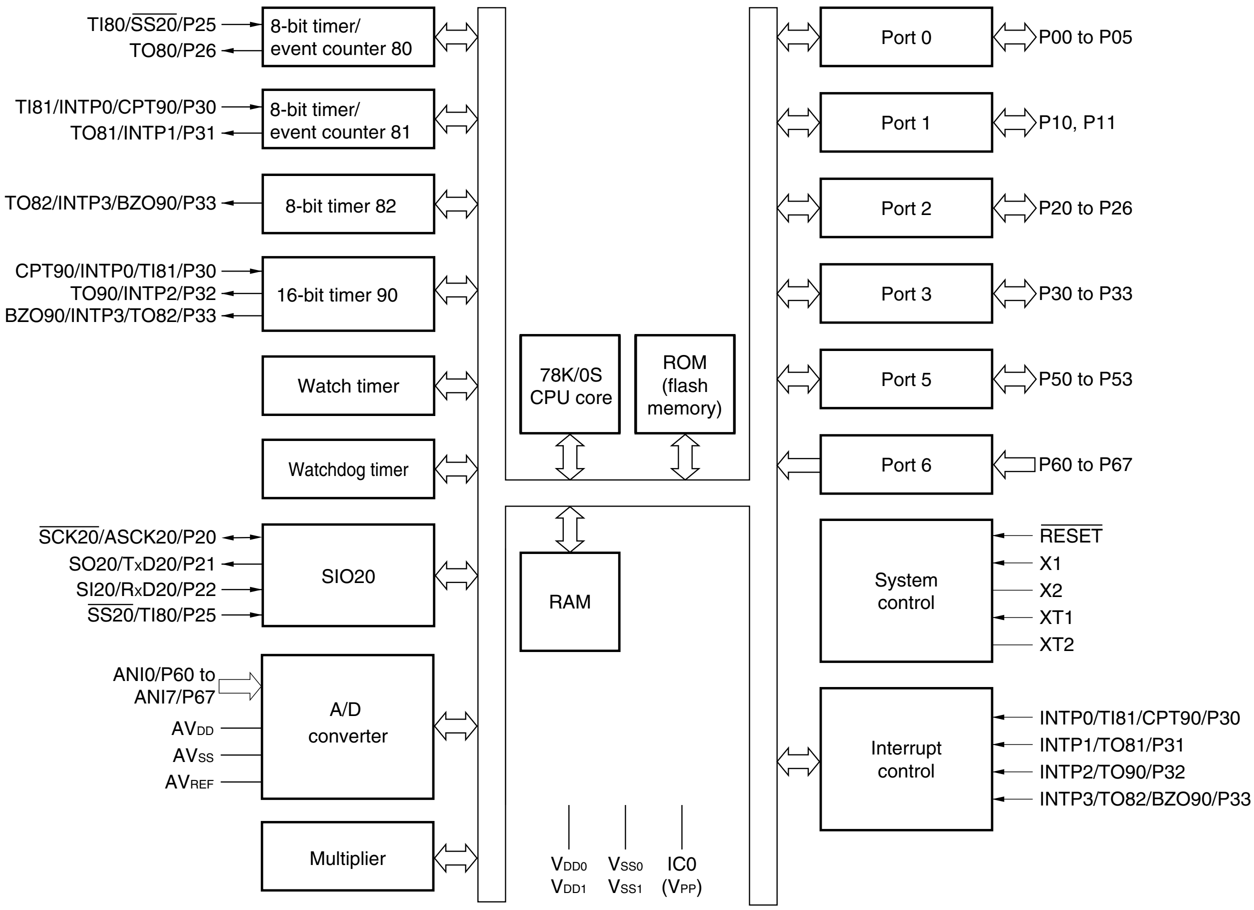
Subseries Name		ROM Capacity	Timer 8-Bit	Timer 16-Bit	Timer Watch	Timer WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
USB	μPD789800	8 KB	2 ch	–	–	1 ch	–	–	2 ch (USB: 1 ch)	31	4.0 V	–
Inverter control	μPD789842	8 KB to 16 KB	3 ch	**Note 1**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
On-chip bus controller	μPD789852	24 KB to 32 KB	3 ch	1 ch	–	1 ch	–	8 ch	3 ch (UART: 2 ch)	31	4.0 V	–
	μPD789850A	16 KB	1 ch				4 ch	–	2 ch (UART: 1 ch)	18		
Keyless entry	μPD789861	4 KB	2 ch	–	–	1 ch	–	–	–	14	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM
	μPD789862	16 KB	1 ch	2 ch					1 ch (UART: 1 ch)	22		
Sensor	μPD789864	4 KB	1 ch	**Note 2**	–	1 ch	–	4 ch	–	5	1.9 V	On-chip EEPROM
	μPD789863											RC oscillation version, on-chip EEPROM
VFD drive	μPD789871	4 KB to 8 KB	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
Meter control	μPD789881	16 KB	2 ch	1 ch	–	1 ch	–	–	1 ch (UART: 1 ch)	28	2.7 V[Note 3]	–

Notes 1. 10-bit timer: 1 channel

2. 12-bit timer: 1 channel

3. Flash memory version: 3.0 V

1.8 Block Diagram



Remarks 1. The size of the internal ROM varies depending on the product.

2. Pin connections in parentheses are intended for the μPD78F9177, 78F9177A, 78F9177A(A), and 78F9177A(A1).

1.9 Outline of Functions

Item \ Part Number		μPD789166, 789176, 789166(A), 789176(A), 789166(A1), 789176(A1), 789166(A2), 789176(A2)	μPD789167, 789177, 789167(A), 789177(A), 789167(A1), 789177(A1), 789167(A2), 789177(A2)	μPD78F9177, 78F9177A, 78F9177A(A), 78F9177A(A1)
Internal memory	ROM	Mask ROM		Flash memory
		16 KB	24 KB	24 KB
	High-speed RAM	512 bytes		
Minimum instruction execution time		Expanded-specification products of μPD78916x, 78917x, 78916x(A), 78917x(A), 78F9177A, 78F9177A(A) 0.2/0.8 μs (operation with main system clock operating at 10.0 MHz, V_{DD} = 4.5 to 5.5 V) • 122 μs (operation with subsystem clock operating at 32.768 kHz) Other than above products • 0.4/1.6 μs (operation with main system clock operating at 5.0 MHz) • 122 μs (operation with subsystem clock operating at 32.768 kHz)		
General-purpose registers		8 bits × 8 registers		
Instruction set		• 16-bit operations • Bit manipulations (such as set, reset, and test)		
Multiplier		8 bits × 8 bits = 16 bits		
I/O ports		Total: 31 • CMOS input: 8 • CMOS I/O: 17 • N-ch open-drain: 6		
A/D converter		• 8-bit resolution × 8 channels (μPD789167 Subseries) • 10-bit resolution × 8 channels (μPD789177 Subseries)		
Serial interface		• Switchable between 3-wire serial I/O and UART modes: 1 channel		
Timers		• 16-bit timer: 1 channel • 8-bit timer/event counter: 2 channels • 8-bit timer: 1 channel • Watch timer: 1 channel • Watchdog timer: 1 channel		
Timer output		Four outputs		
Buzzer output		One output		
Vectored interrupt sources	Maskable	Internal: 10, external: 4		
	Non-maskable	Internal: 1		
Power supply voltage		V_{DD} = 1.8 to 5.5 V (μPD78916x, 78917x, 78916x(A), 78917x(A), 78F9177, 78F9177A, 78F9177A(A) V_{DD} = 4.5 to 5.5 V (μPD78916x(A1), 78917x(A1), 78916x(A2), 78917x(A2), 78F9177A(A1)		
Operating ambient temperature		T_A = –40°C to +85°C (μPD78916x, 78917x, 78916x(A), 78917x(A), 78F9177, 78F9177A, 78F9177A(A) T_A = –40°C to +110°C (μPD78916x(A1), 78917x(A1), 78F9177A(A1) T_A = –40°C to +125°C (μPD78916x(A2), 78917x(A2)		
Package		• 44-pin plastic LQFP (10 × 10) ★ • 48-pin plastic TQFP (fine pitch) (7 × 7)[Note]		

Note μPD789166, 789167, 789176, 789177, and 78F9177A only

The timers are outlined below.

		16-Bit Timer 90	8-Bit Timer/Event Counter 80	8-Bit Timer/Event Counter 81	8-Bit Timer 82	Watch Timer	Watchdog Timer
Operating mode	Interval timer	–	1 channel	1 channel	1 channel	1 channel[Note 1]	1 channel[Note 2]
	External event counter	–	1 channel	1 channel	–	–	–
Function	Timer output	1 output	1 output	1 output	1 output	–	–
	PWM output	–	1 output	1 output	1 output	–	–
	Square-wave output	–	1 output	1 output	1 output	–	–
	Buzzer output	1 output	–	–	–	–	–
	Capture	1 input	–	–	–	–	–
	Interrupt sources	1	1	1	1	2	2

Notes 1. The watch timer can perform both watch timer and interval timer functions at the same time.

2. The watchdog timer provides a watchdog timer function and an interval timer function. Use either of the functions.

1.10 Differences Between Standard Quality Grade Products and (A) Products, (A1) Products, and (A2) Products

Standard quality grade products, (A) products, (A1) products, and (A2) products indicate the following products respectively.

Standard quality grade products... μPD789166, 789167, 789176, 789177, 78F9177, 78F9177A
(A) products... μPD789166(A), 789167(A), 789176(A), 789177(A), 78F9177A(A)
(A1) products... μPD789166(A1), 789167(A1), 789176(A1), 789177(A1), 78F9177A(A1)
(A2) products... μPD789166(A2), 789167(A2), 789176(A2), 789177(A2)

Table 1-2 shows the differences between the standard quality grade products and (A) products, (A1) products, and (A2) products.

Table 1-2. Differences Between Standard Quality Grade Products and (A) Products, (A1) Products, and (A2) Products

Item \ Part Number	Standard Quality Grade Products	(A) Products	(A1) Products	(A2) Products
Quality grade	Standard	Special		
Power supply voltage	V_{DD} = 1.8 to 5.5 V		V_{DD} = 4.5 to 5.5 V	
Operating ambient temperature	T_A = –40 to 85°C		T_A = –40 to 110°C	T_A = –40 to 125°C
Minimum instruction execution time	Expanded-specification product[Note]: 0.2 μs (at 10.0 MHz operation) Conventional product[Note]: 0.4 μs (at 5.0 MHz operation)		0.4 μs (at 5.0 MHz operation)	
Electrical specifications	Refer to the ELECTRICAL SPECIFICATIONS chapters.			

Note Refer to 1.1 Expanded-Specification Products and Conventional Products

2.1 Expanded-Specification Products and Conventional Products

The expanded-specification products and conventional products refer to the following products.

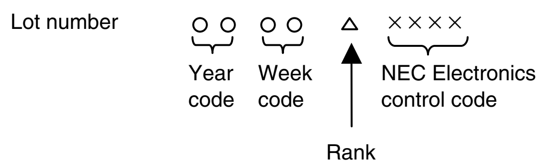
Expanded-specification product... Products with a rank[Note] other than K

- Mask ROM versions for which orders were received after December 1, 2001.
- μPD78F9177AY, 78F9177AY(A)

Conventional product... Products with rank[Note] K

- Products other than the above expanded-specification products.

Note The rank is indicated by the 5th digit from the left in the lot number marked on the package.



Expanded-specification products and conventional products differ in operating frequency ratings. The differences are shown in Table 2-1.

Table 2-1. Differences Between Expanded-Specification Products and Conventional Products

Power Supply Voltage (V_{DD})	Guaranteed Operating Speed (Operating Frequency)	
	Conventional Products	Expanded-Specification Products
4.5 to 5.5 V	5 MHz (0.4 μs)	10 MHz (0.2 μs)
3.0 to 5.5 V	5 MHz (0.4 μs)	6 MHz (0.33 μs)
2.7 to 5.5 V	5 MHz (0.4 μs)	5 MHz (0.4 μs)
1.8 to 5.5 V	1.25 MHz (1.6 μs)	1.25 MHz (1.6 μs)

Remark The values in parentheses indicate the minimum instruction execution time.

2.2 Features

• ROM and RAM capacity

Product Name \ Item	Program Memory (ROM)		Data Memory (Internal High-Speed RAM)
μPD789166Y, 789176Y, 789166Y(A), 789176Y(A)	Mask ROM	16 KB	512 bytes
μPD789167Y, 789177Y, 789167Y(A), 789177Y(A)		24 KB	
μPD78F9177Y, 78F9177AY, 78F9177AY(A)	Flash memory	24 KB	

- Minimum instruction execution time changeable from high-speed (0.2 μs: Main system clock 10.0 MHz operation[Note]) to ultra-low speed (122 μs: Subsystem clock 32.768 kHz operation)
- I/O port: 31
- Serial interface: 2 channels
  - 3-wire serial I/O mode/UART mode: 1 channel
  - SMB: 1 channel
- 8-bit resolution A/D converter: 8 channels (μPD789167Y Subseries)
- 10-bit resolution A/D converter: 8 channels (μPD789177Y Subseries)
- Timer: 6 channels
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 2 channels
  - 8-bit timer: 1 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- Vectored interrupt sources: 17
- Supply voltage: V_{DD} = 1.8 to 5.5 V
- Operating ambient temperature: T_A = –40 to +85°C

Note When V_{DD} = 4.5 to 5.5 V and the product is an expanded-specification product.

2.3 Applications

Power windows, keyless entry, battery management units, side air bags, etc.

2.4 Ordering Information

	Part Number	Package	Internal ROM
	μPD789166YGB-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789166YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789167YGB-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789167YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789176YGB-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789176YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789177YGB-×××-8ES	44-pin plastic LQFP (10 × 10)	Mask ROM
	μPD789177YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
★	μPD789166YGB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Mask ROM
★	μPD789166YGA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
★	μPD789167YGB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Mask ROM
★	μPD789167YGA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
★	μPD789176YGB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Mask ROM
★	μPD789176YGA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
★	μPD789177YGB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Mask ROM
★	μPD789177YGA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789166YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789167YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789176YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD789177YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Mask ROM
	μPD78F9177YGB-8ES	44-pin plastic LQFP (10 × 10)	Flash memory
	μPD78F9177YGA-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Flash memory
	μPD78F9177AYGB-8ES	44-pin plastic LQFP (10 × 10)	Flash memory
	μPD78F9177AYGA-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Flash memory
★	μPD78F9177YGB-8ES-A	44-pin plastic LQFP (10 × 10)	Flash memory
★	μPD78F9177YGA-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Flash memory
★	μPD78F9177AYGB-8ES-A	44-pin plastic LQFP (10 × 10)	Flash memory
★	μPD78F9177AYGA-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Flash memory
	μPD78F9177AYGB(A)-8ES	44-pin plastic LQFP (10 × 10)	Flash memory
	μPD78F9177AYGA(A)-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Flash memory

Remark ××× indicates ROM code suffix.

2.5 Quality Grades

	Part Number	Package	Quality Grade
	μPD789166YGB-×××-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD789166YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD789167YGB-×××-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD789167YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD789176YGB-×××-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD789176YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD789177YGB-×××-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD789177YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD789166YGB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD789166YGA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD789167YGB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD789167YGA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD789176YGB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD789176YGA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD789177YGB-×××-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD789177YGA-×××-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD789166YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Special
	μPD789167YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Special
	μPD789176YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Special
	μPD789177YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Special
	μPD78F9177YGB-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD78F9177YGA-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD78F9177AYGB-8ES	44-pin plastic LQFP (10 × 10)	Standard
	μPD78F9177AYGA-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD78F9177YGB-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD78F9177YGA-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
★	μPD78F9177AYGB-8ES-A	44-pin plastic LQFP (10 × 10)	Standard
★	μPD78F9177AYGA-9EU-A	48-pin plastic TQFP (fine pitch) (7 × 7)	Standard
	μPD78F9177AYGB(A)-8ES	44-pin plastic LQFP (10 × 10)	Special
	μPD78F9177AYGA(A)-9EU	48-pin plastic TQFP (fine pitch) (7 × 7)	Special

Remark ××× indicates ROM code suffix.

Please refer to Quality Grades on NEC Semiconductor Devices (C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

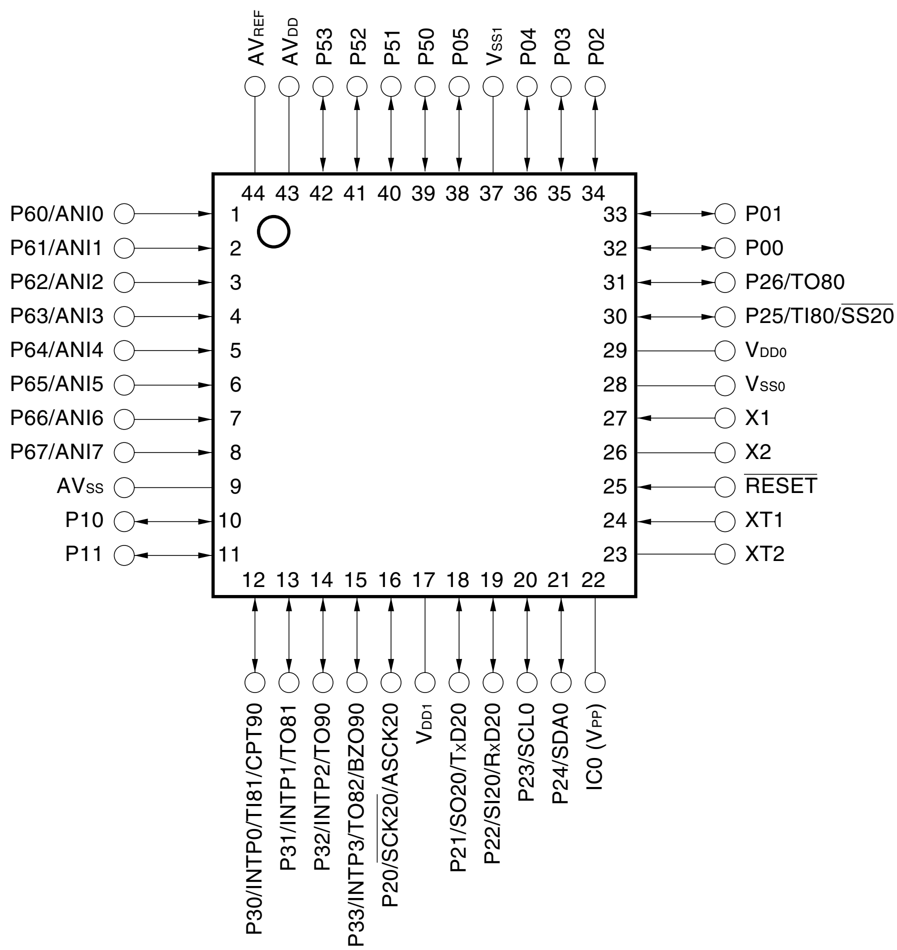
2.6 Pin Configuration (Top View)

★ • **44-pin plastic LQFP (10 × 10)**

μPD789166YGB-×××-8ES
μPD789167YGB-×××-8ES
μPD789176YGB -×××-8ES
μPD789177YGB -×××-8ES

μPD789166YGB-×××-8ES-A
μPD789167YGB-×××-8ES-A
μPD789176YGB -×××-8ES-A
μPD789177YGB -×××-8ES-A

μPD78F9177YGB-8ES
μPD78F9177AYGB-8ES
μPD78F9177YGB-8ES-A
μPD78F9177AYGB-8ES-A
μPD78F9177AYGB(A)-8ES



Cautions 1. Connect the IC0 (internally connected) pin directly to the V_{SS0} or V_{SS1} pin.

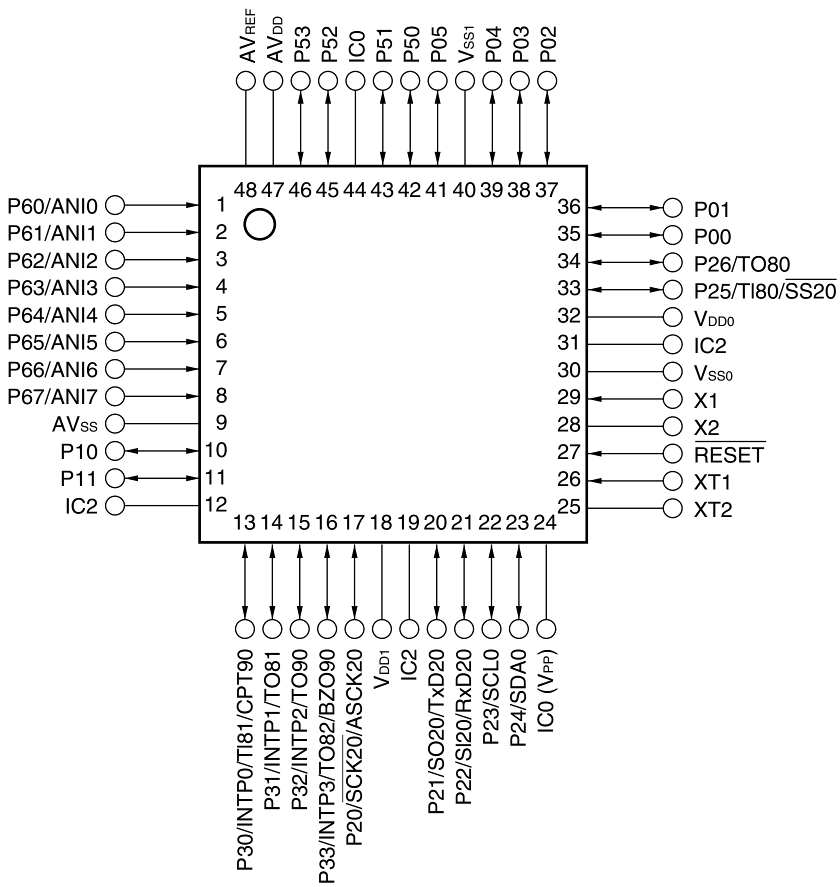
2. Connect the AV_{DD} pin to the V_{DD0} pin.

3. Connect the AV_{SS} pin to the V_{SS0} pin.

Remark Pin connections in parentheses are intended for the μPD78F9177Y, 78F9177AY, and 78F9177AY(A).

★ • **48-pin plastic TQFP (fine pitch) (7 × 7)**

μPD789166YGA-×××-9EU μPD789166YGA(A)-×××-9EU μPD78F9177YGA-9EU
μPD789167YGA-×××-9EU μPD789167YGA(A)-×××-9EU μPD78F9177AYGA-9EU
μPD789176YGA-×××-9EU μPD789176YGA(A)-×××-9EU μPD78F9177YGA-9EU-A
μPD789177YGA-×××-9EU μPD789177YGA(A)-×××-9EU μPD78F9177AYGA-9EU-A
μPD789166YGA-×××-9EU-A μPD78F9177AYGA(A)-9EU
μPD789167YGA-×××-9EU-A
μPD789176YGA-×××-9EU-A
μPD789177YGA-×××-9EU-A



Cautions 1. Connect the IC0 (internally connected) pin directly to the V_{SS0} or V_{SS1} pin.

2. Leave the IC2 pin open.

3. Connect the AV_{DD} pin to the V_{DD0} pin.

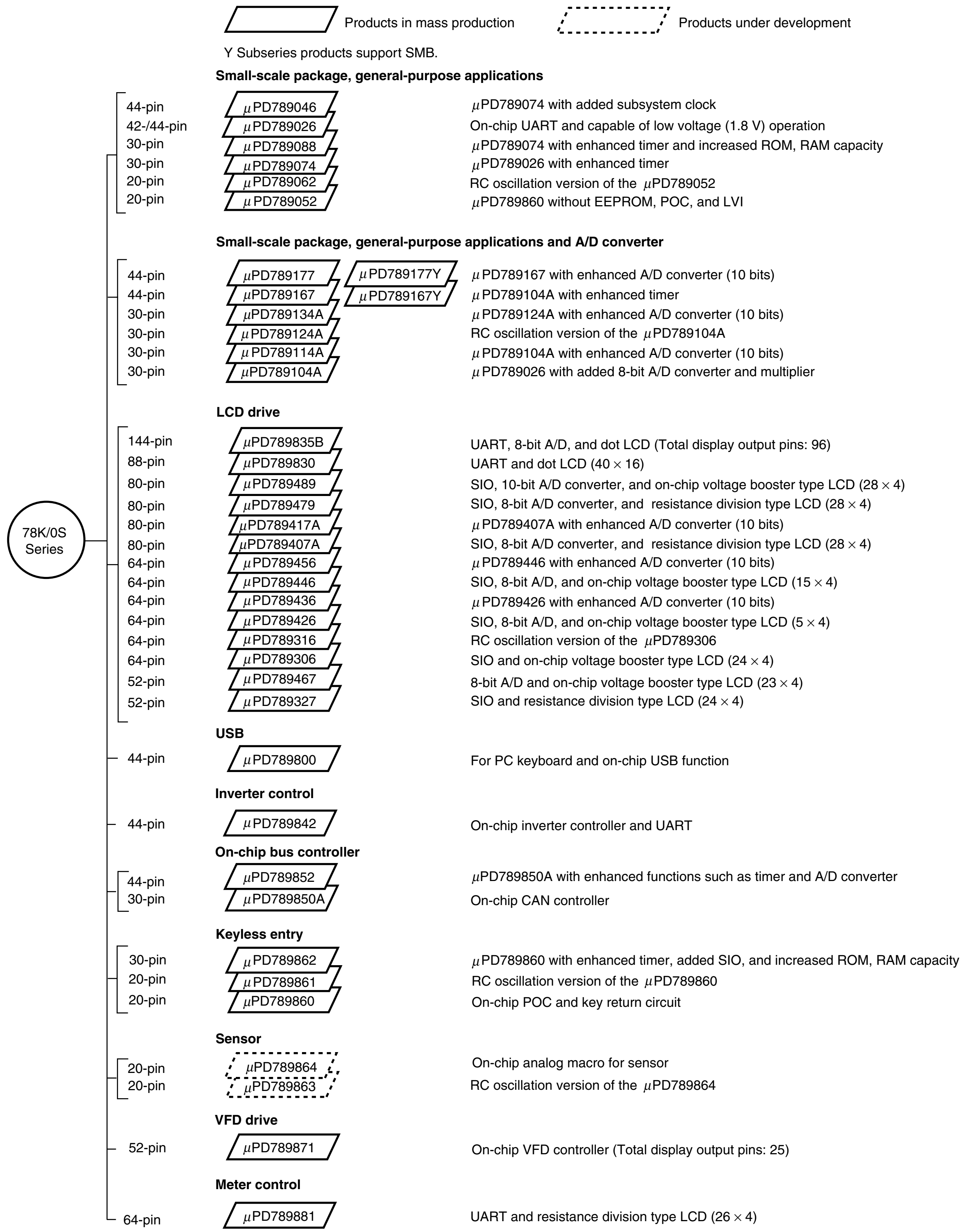
4. Connect the AV_{SS} pin to the V_{SS0} pin.

Remark Pin connections in parentheses are intended for the μPD78F9177Y, 78F9177AY, and 78F9177AY(A).

ANI0 to ANI7:	Analog input
ASCK20:	Asynchronous serial input
AV_{DD}:	Analog power supply
AV_{REF}:	Analog reference voltage
AV_{SS}:	Analog ground
BZO90:	Buzzer output
CPT90:	Capture trigger input
IC0, IC2:	Internally connected
INTP0 to INTP3:	Interrupt from peripherals
P00 to P05:	Port 0
P10, P11:	Port 1
P20 to P26:	Port 2
P30 to P33:	Port 3
P50 to P53:	Port 5
P60 to P67:	Port 6
$\overline{\text{RESET}}$:	Reset
RxD20:	Receive data
$\overline{\text{SCK20}}$:	Serial clock (for SIO20)
SCL0:	Serial clock (for SMB0)
SDA0:	Serial data
SI20:	Serial input
SO20:	Serial output
$\overline{\text{SS20}}$:	Chip select input
TI80, TI81:	Timer input
TO80 to TO82, TO90:	Timer output
TxD20:	Transmit data
V_{DD0}, V_{DD1}:	Power supply
V_{PP}:	Programming power supply
V_{SS0}, V_{SS1}:	Ground
X1, X2:	Crystal (main system clock)
XT1, XT2:	Crystal (subsystem clock)

★ 2.7 78K/0S Series Lineup

The 78K/0S Series products are shown below. The subseries names are indicated in frames.

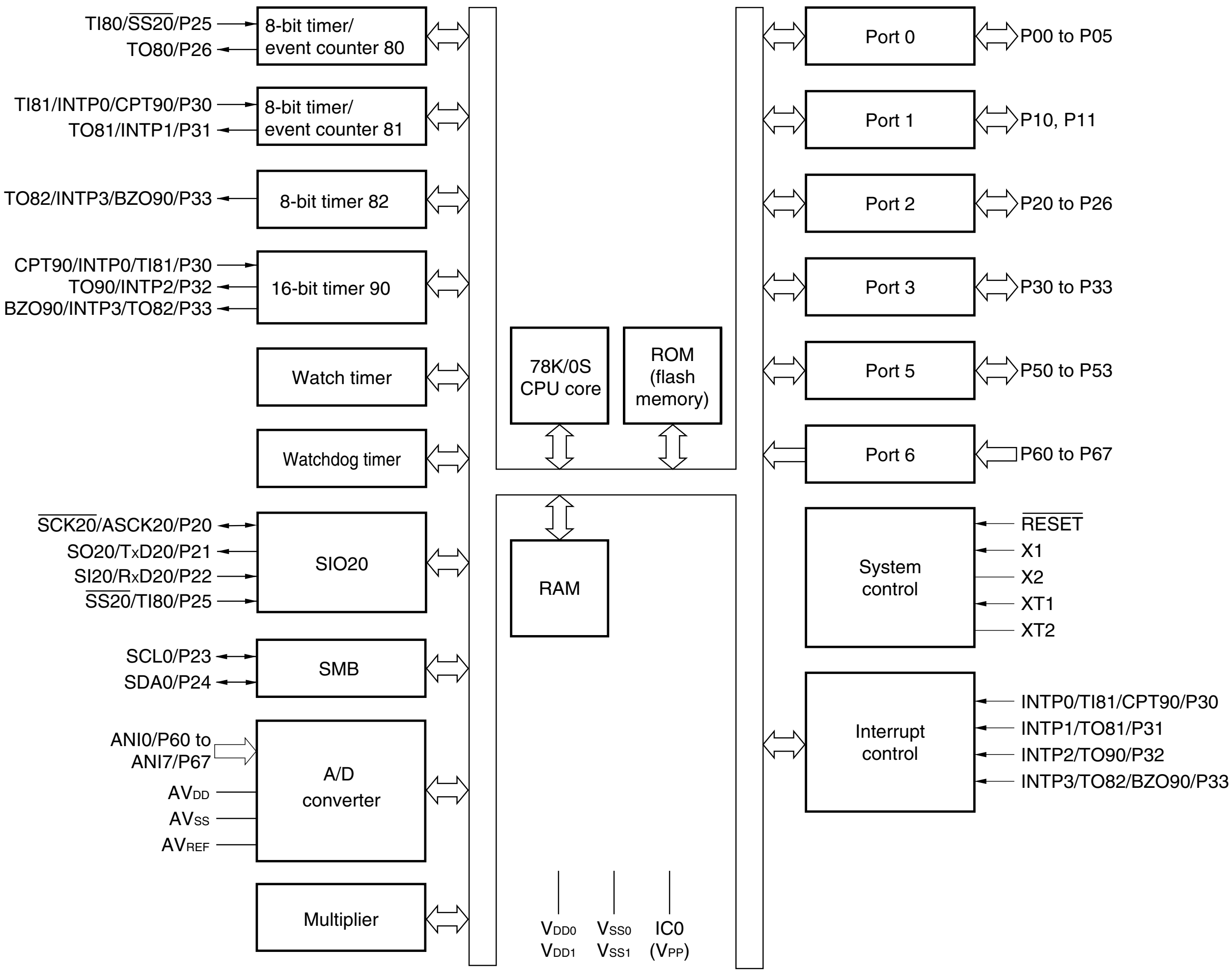


Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The functions of the Y Subseries are listed below.

Subseries Name \ Function		ROM Capacity	Serial Interface Configuration	I/O (pins)	V_{DD} MIN. Value	Remark
Small-scale package, general-purpose application + A/D converter	μPD789177Y	16 KB to 24 KB	3-wire/UART: 1 ch SMB: 1 ch	31	1.8 V	–
	μPD789167Y					

2.8 Block Diagram



Remarks 1. The size of the internal ROM varies depending on the model.

2. Pin connections in parentheses are intended for the μPD78F9177Y, 78F9177AY, and 78F9177AY(A).

2.9 Outline of Function

Item \ Part Number		μPD789166Y, 789176Y 789166Y(A), 789176Y(A)	μPD789167Y, 789177Y 789167Y(A), 789177Y(A)	μPD78F9177Y, 78F9177AY 78F9177AY(A)
Internal memory	ROM	Mask ROM		Flash Memory
		16 KB	24 KB	24 KB
	High-speed RAM	512 bytes		
Minimum instruction execution time		Expanded-specification products of μPD78916xY, 78917xY, 78916xY(A), 78917xY(A), 78F9177AY, 78F9177AY(A) • 0.2/0.8 μs (operation with main system clock operating at 10.0 MHz, V_{DD} = 4.5 to 5.5 V) • 122 μs (operation with subsystem clock operating at 32.768 kHz) Other than above products • 0.4/1.6 μs (operation with main system clock operating at 5.0 MHz) • 122 μs (operation with subsystem clock operating at 32.768 kHz)		
General-purpose registers		8 bits × 8 registers		
Instruction set		• 16-bit operations • Bit manipulations (such as set, reset, and test)		
Multiplier		8 bits × 8 bits = 16 bits		
I/O ports		Total: 31 • CMOS input: 8 • CMOS I/O: 17 • N-ch open-drain: 6		
A/D converter		• 8-bit resolution × 8 channels (μPD789167Y Subseries) • 10-bit resolution × 8 channels (μPD789177Y Subseries)		
Serial interface		• Switchable between 3-wire serial I/O and UART modes: 1 channel • SMB (System Management Bus): 1 channel		
Timers		• 16-bit timer: 1 channel • 8-bit timer/event counter: 2 channels • 8-bit timer: 1 channel • Watch timer: 1 channel • Watchdog timer: 1 channel		
Timer output		Four outputs		
Buzzer output		One output		
Vectored interrupt sources	Maskable	Internal: 12, external: 4		
	Nonmaskable	Internal: 1		
Power supply voltage		V_{DD} = 1.8 to 5.5 V		
Operating ambient temperature		T_A = –40 to +85°C		
Package		• 44-pin plastic LQFP (10 × 10)[Note] • 48-pin plastic TQFP (fine pitch) (7 × 7)		

Note μPD789166Y, 789167Y, 789176Y, 789177Y, 78F9177Y, 78F9177AY, and 78F9177AY(A) only

The timers are outlined below.

		16-Bit Timer 90	8-Bit Timer/Event Counter 80	8-Bit Timer/Event Counter 81	8-Bit Timer 82	Watch Timer	Watchdog Timer
Operating mode	Interval timer	–	1 channel	1 channel	1 channel	1 channel[Note 1]	1 channel[Note 2]
	External event counter	–	1 channel	1 channel	–	–	–
Function	Timer output	1 output	1 output	1 output	1 output	–	–
	PWM output	–	1 output	1 output	1 output	–	–
	Square-wave output	–	1 output	1 output	1 output	–	–
	Buzzer output	1 output	–	–	–	–	–
	Capture	1 input	–	–	–	–	–
	Interrupt sources	1	1	1	1	2	2

Notes 1. The watch timer can perform both watch timer and interval timer functions at the same time.

2. The watchdog timer provides a watchdog timer function and an interval timer function. Use either of the functions.

2.10 Differences Between Standard Quality Grade Products and (A) Products

Standard quality grade products and (A) products indicate the following products.

Standard quality grade products... μPD789166Y, 789167Y, 789176Y, 789177Y, 78F9177Y, 78F9177AY
(A) products... μPD789166Y(A), 789167Y(A), 789176Y(A), 789177Y(A), 78F9177AY(A)

Table 2-2 shows the differences between the standard quality grade products and (A) products

Table 2-2. Differences Between Standard Quality Grade Products and (A) Products

Item \ Part Number	Standard Quality Grade Products	(A) Products
Quality grade	Standard	Special
Power supply voltage	V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature	T_A = –40 to 85°C	
Minimum instruction execution time	Expanded-specification product[Note]: 0.2 μs (at 10.0 MHz operation) Conventional product[Note]: 0.4 μs (at 5.0 MHz operation)	
Electrical specifications	Refer to the ELECTRICAL SPECIFICATIONS chapters.	

Note Refer to **2.1 Expanded-Specification Products and Conventional Products**.

3.1 Pin Function List

(1) Port pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P05	I/O	Port 0 6-bit I/O port I/O mode can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of pull-up resistor option register 0 (PU0).	Input	–
P10, P11	I/O	Port 1 2-bit I/O port I/O mode can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of pull-up resistor option register 0 (PU0).	Input	–
P20	I/O	Port 2 7-bit I/O port I/O mode can be specified in 1-bit units. For P20 to P22, P25, and P26, an on-chip pull-up resistor can be specified by means of pull-up resistor option register B2 (PUB2). Only P23 and P24 can be used as N-ch open-drain I/O port pins.	Input	$\overline{\text{SCK20}}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				–
P24				–
P25				TI80/$\overline{\text{SS20}}$
P26				TO80
P30	I/O	Port 3 4-bit I/O port I/O mode can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of pull-up resistor option register B3 (PUB3).	Input	INTP0/TI81/CPT90
P31				INTP1/TO81
P32				INTP2/TO90
P33				INTP3/TO82/BZO90
P50 to P53	I/O	Port 5 4-bit N-ch open-drain I/O port I/O mode can be specified in 1-bit units. For a mask ROM version, an on-chip pull-up resistor can be specified by the mask option.	Input	–
P60 to P67	Input	Port 6 8-bit input-only port	Input	ANI0 to ANI7

(2) Non-port pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/TI81/CPT90
INTP1				P31/TO81
INTP2				P32/TO90
INTP3				P33/TO82/BZO90
SI20	Input	Serial data input to serial interface	Input	P22/RxD20
SO20	Output	Serial data output from serial interface	Input	P21/TxD20
$\overline{\text{SCK20}}$	I/O	Serial clock I/O for serial interface	Input	P20/ASCK20
$\overline{\text{SS20}}$	Input	Chip select input to serial interface	Input	P25/TI80
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{\text{SCK20}}$
RxD20	Input	Serial data input for asynchronous serial interface	Input	P22/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P21/SO20
TI80	Input	External count clock input to 8-bit timer/event counter (TM80)	Input	P25/$\overline{\text{SS20}}$
TI81	Input	External count clock input to 8-bit timer/event counter (TM81)	Input	P30/INTP0/CPT90
TO80	Output	8-bit timer/event counter (TM80) output	Input	P26
TO81	Output	8-bit timer/event counter (TM81) output	Input	P31/INTP1
TO82	Output	8-bit timer (TM82) output	Input	P33/INTP3/BZO90
TO90	Output	16-bit timer (TM90) output	Input	P32/INTP2
CPT90	Input	Capture edge input	Input	P30/INTP0/TI81
BZO90	Output	Buzzer output	Input	P33/INTP3/TO82
ANI0 to ANI7	Input	A/D converter analog input	Input	P60 to P67
AV_{REF}	–	A/D converter reference voltage	–	–
AV_{SS}	–	A/D converter ground potential	–	–
AV_{DD}	–	A/D converter analog power supply	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{\text{RESET}}$	Input	System reset input	Input	–
V_{DD0}	–	Positive power supply	–	–
V_{DD1}	–	Positive power supply (other than ports)	–	–
V_{SS0}	–	Ground potential	–	–
V_{SS1}	–	Ground potential (other than ports)	–	–
IC0	–	Internally connected. Connect this pin directly to the V_{SS0} or V_{SS1} pin.	–	–
IC3	–	Internally connected. Leave open.	–	–
V_{PP}	–	This pin is used to set flash memory programming mode and applies a high voltage when a program is written or verified.	–	–

3.2 Description of Pin Functions

3.2.1 P00 to P05 (Port 0)

These pins constitute a 6-bit I/O port and can be set to input or output port mode in 1-bit units by using port mode register 0 (PM0). When these pins are used as an input port, an on-chip pull-up resistor can be used by setting pull-up resistor option register 0 (PU0).

3.2.2 P10, P11 (Port 1)

These pins constitute a 2-bit I/O port and can be set to input or output port mode in 1-bit units by using port mode register 1 (PM1). When these pins are used as an input port, an on-chip pull-up resistor can be used by setting pull-up resistor option register 0 (PU0).

3.2.3 P20 to P26 (Port 2)

These pins constitute a 7-bit I/O port. In addition, these pins provide a function to perform I/O to/from the timer and to I/O the data and clock of the serial interface.

Port 2 can be set to the following operation modes in 1-bit units.

(1) Port mode

In port mode, P20 to P26 function as a 7-bit I/O port. Port 2 can be set to input or output mode in 1-bit units by using port mode register 2 (PM2). For P20 to P22, P25, and P26, whether to use on-chip pull-up resistors can be specified in 1-bit units by using pull-up resistor option register B2 (PUB2), regardless of the setting of port mode register 2 (PM2). P23 and P24 are N-ch open-drain I/O ports.

(2) Control mode

In this mode, P20 to P26 function as the timer I/O, the data I/O and the clock I/O of the serial interface.

(a) TI80

This is the external clock input pin for 8-bit timer/event counter 80.

(b) TO80

This is the timer output pin of 8-bit timer/event counter 80.

(c) SI20, SO20

These are the serial data I/O pins of the serial interface.

(d) $\overline{\text{SCK20}}$

This is the serial clock I/O pin of the serial interface.

(e) $\overline{\text{SS20}}$

This is the chip select input pin of the serial interface.

(f) RxD20, TxD20

These are the serial data I/O pins of the asynchronous serial interface.

(g) ASCK20

This is the serial clock input pin of the asynchronous serial interface.

Caution When using P20 to P26 as serial interface pins, the I/O mode and output latch must be set according to the function to be used. For details of the setting, see Table 14-2 Operating Mode Settings of Serial Interface 20.

3.2.4 P30 to P33 (Port 3)

These pins constitute a 4-bit I/O port. In addition, these pins function as the timer I/O and the external interrupt input.

Port 3 can be set to the following operation modes in 1-bit units.

(1) Port mode

In port mode, P30 to P33 function as a 4-bit I/O port. Port 3 can be set to input or output mode in 1-bit units by using port mode register 3 (PM3). Whether to use the on-chip pull-up resistor can be specified in 1-bit units by using pull-up resistor option register B3 (PUB3), regardless of the setting of port mode register 3 (PM3).

(2) Control mode

In this mode, P30 to P33 function as the timer I/O and the external interrupt input.

(a) TI81

This is the external clock input pin for 8-bit timer/event counter 81.

(b) TO90, TO81, TO82

These are the output pins of 16-bit timer 90, 8-bit timer/event counter 81, and 8-bit timer 82.

(c) CPT90

This is the capture edge input pin of 16-bit timer 90.

(d) BZO90

This is the buzzer output pin of 16-bit timer 90.

(e) INTP0 to INTP3

These are external interrupt input pins for which the valid edge (rising edge, falling edge, and both the rising and falling edges) can be specified.

3.2.5 P50 to P53 (Port 5)

These pins constitute a 4-bit N-ch open-drain I/O port. Port 5 can be set to input or output mode in 1-bit units by using port mode register 5 (PM5). For a mask ROM version, whether a pull-up resistor is to be incorporated can be specified by a mask option.

3.2.6 P60 to P67 (Port 6)

These pins constitute an 8-bit input-only port. They can function as A/D converter input pins as well as a general-purpose input port.

(1) Port mode

In port mode, P60 to P67 function as an 8-bit input-only port.

(2) Control mode

In control mode, P60 to P67 function as A/D converter analog inputs (ANI0 to ANI7).

3.2.7 $\overline{\text{RESET}}$

A low-level active system reset signal is input to this pin.

3.2.8 X1, X2

These pins are used to connect a crystal resonator for main system clock oscillation.

To supply an external clock, input the clock to X1 and input the inverted signal to X2.

3.2.9 XT1, XT2

These pins are used to connect a crystal resonator for subsystem clock oscillation.

To supply an external clock, input the clock to XT1 and input the inverted signal to XT2.

3.2.10 AV_{DD}

Analog power supply pin of the A/D converter. Always use the same potential as that of the V_{DD0} pin even when the A/D converter is not used.

3.2.11 AV_{SS}

This is a ground potential pin of the A/D converter. Always use the same potential as that of the V_{SS0} pin even when the A/D converter is not used.

3.2.12 AV_{REF}

This is the A/D converter reference voltage input pin. When the A/D converter is not used, connect this pin to V_{DD0} or V_{SS0}.

3.2.13 V_{DD0}, V_{DD1}

V_{DD0} is a positive power supply pin for ports.

V_{DD1} is a positive power supply pin for other than ports.

3.2.14 V_{SS0}, V_{SS1}

V_{SS0} is a ground potential for ports pin.

V_{SS1} is a ground potential pin for other than ports.

3.2.15 V_{PP} (flash memory version only)

High voltage application pin for flash memory programming mode setting and program write/verify.

Connect this pin in either of the following ways.

- Independently connect to a 10 kΩ pull-down resistor.
- By using a jumper on the board, connect directly to the dedicated flash programmer in the programming mode or to V_{SS} in the normal operation mode.

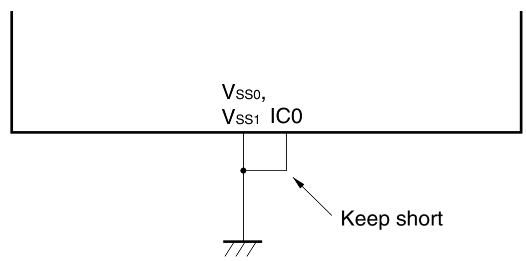
★ If the wiring between the V_{PP} pin and V_{SS} pin is very long or external noise is superimposed on the V_{PP} pin, the user program may not run correctly.

3.2.16 IC0 (mask ROM version only)

The IC0 (internally connected) pin is used to set the μPD789167 and 789177 Subseries to test mode before shipment. In normal operation mode, directly connect this pin to the V_{SS0} or V_{SS1} pin with as short a wiring length as possible.

If a potential difference is generated between the IC0 pin and V_{SS0} or V_{SS1} pin due to a long wiring length or external noise superimposed on the IC0 pin, the user program may not run correctly.

- Directly connect the IC0 pin to the V_{SS0} or V_{SS1} pin.



3.2.17 IC3

The IC3 pin is internally connected. Leave this pin open.

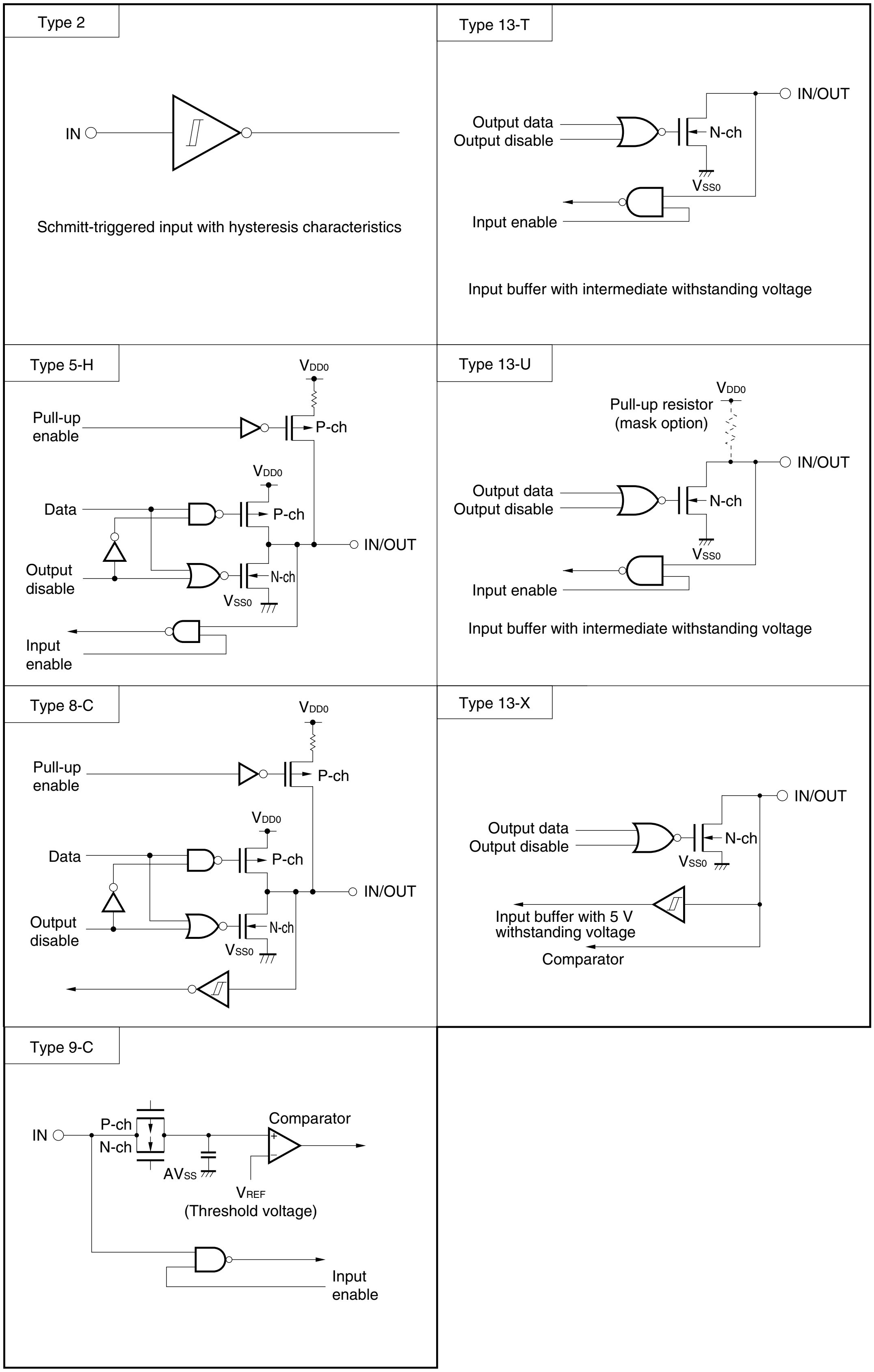
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.
For the I/O circuit configuration of each type, refer to **Figure 3-1**.

Table 3-1. Types of I/O Circuits for Each Pin and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P05	5-H	I/O	Input: Independently connect to V_{DD0}, V_{DD1} V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P10, P11			
P20/$\overline{SCK20}$/ASCK20	8-C		
P21/SO20/TxD20			
P22/SI20/RxD20			
P23	13-X		Input: Independently connect to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P24			
P25/TI80/$\overline{SS20}$	8-C		Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P26/TO80			
P30/INTP0/TI81/CPT90			Input: Independently connect to V_{SS0} or V_{SS1} via a resistor. Output: Leave open.
P31/INTP1/TO81			
P32/INTP2/TO90			
P33/INTP3/TO82/BZO90			
P50 to P53 (mask ROM version)	13-U		Input: Connect to V_{SS0} or V_{SS1}. Output: Leave open.
P50 to P53 (flash memory version)	13-T		
P60/ANI0 to P67/ANI7	9-C	Input	Connect directly to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1}.
XT1	–	Input	Connect directly to V_{SS0} or V_{SS1}.
XT2		–	Leave open.
$\overline{RESET}$	2	Input	–
IC0 (mask ROM version)	–	–	Connect directly to V_{SS0} or V_{SS1}.
IC3			Leave open.
V_{PP} (flash memory version)			Independently connect via a 10 kΩ pull-down resistor, or connect directly to V_{SS0} or V_{SS1}.

Figure 3-1. Pin I/O Circuits



4.1 Pin Function List

(1) Port pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P05	I/O	Port 0 6-bit I/O port I/O mode can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of pull-up resistor option register 0 (PU0).	Input	–
P10, P11	I/O	Port 1 2-bit I/O port I/O mode can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of pull-up resistor option register 0 (PU0).	Input	–
P20	I/O	Port 2 7-bit I/O port I/O mode can be specified in 1-bit units. For P20 to P22, P25, and P26, an on-chip pull-up resistor can be specified by means of pull-up resistor option register B2 (PUB2). Only P23 and P24 can be used as N-ch open-drain I/O port pins.	Input	$\overline{SCK20}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				SCL0
P24				SDA0
P25				TI80/$\overline{SS20}$
P26				TO80
P30	I/O	Port 3 4-bit I/O port I/O mode can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of pull-up resistor option register B3 (PUB3).	Input	INTP0/TI81/CPT90
P31				INTP1/TO81
P32				INTP2/TO90
P33				INTP3/TO82/BZO90
P50 to P53	I/O	Port 5 4-bit N-ch open-drain I/O port I/O mode can be specified in 1-bit units. For a mask ROM version, an on-chip pull-up resistor can be specified by the mask option.	Input	–
P60 to P67	Input	Port 6 8-bit input-only port	Input	ANI0 to ANI7

(2) Non-port pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/TI81/CPT90
INTP1				P31/TO81
INTP2				P32/TO90
INTP3				P33/TO82/BZO90
SI20	Input	Serial data input to serial interface	Input	P22/RxD20
SO20	Output	Serial data output from serial interface	Input	P21/TxD20
$\overline{SCK20}$	I/O	Serial clock I/O for serial interface	Input	P20/ASCK20
$\overline{SS20}$	Input	Chip select input to serial interface	Input	P25/TI80
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{SCK20}$
RxD20	Input	Serial data input for asynchronous serial interface	Input	P22/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P21/SO20
SCL0	I/O	SMB0 clock I/O	Input	P23
SDA0	I/O	SMB0 data I/O	Input	P24
TI80	Input	External count clock input to 8-bit timer/event counter (TM80)	Input	P25/$\overline{SS20}$
TI81	Input	External count clock input to 8-bit timer/event counter (TM81)	Input	P30/INTP0/CPT90
TO80	Output	8-bit timer/event counter (TM80) output	Input	P26
TO81	Output	8-bit timer/event counter (TM81) output	Input	P31/INTP1
TO82	Output	8-bit timer (TM82) output	Input	P33/INTP3/BZO90
TO90	Output	16-bit timer (TM90) output	Input	P32/INTP2
CPT90	Input	Capture edge input	Input	P30/INTP0/TI81
BZO90	Output	Buzzer output	Input	P33/INTP3/TO82
ANI0 to ANI7	Input	A/D converter analog input	Input	P60 to P67
AV_{REF}	–	A/D converter reference voltage	–	–
AV_{SS}	–	A/D converter ground potential	–	–
AV_{DD}	–	A/D converter analog power supply	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{RESET}$	Input	System reset input	Input	–
V_{DD0}	–	Positive power supply	–	–
V_{DD1}	–	Positive power supply (other than ports)	–	–
V_{SS0}	–	Ground potential	–	–
V_{SS1}	–	Ground potential (other than ports)	–	–
IC0	–	Internally connected. Connect this pin directly to the V_{SS0} or V_{SS1} pin.	–	–
IC2	–	Internally connected. Leave this pin open.	–	–
V_{PP}	–	This pin is used to set flash memory programming mode and applies a high voltage when a program is written or verified.	–	–

4.2 Description of Pin Functions

4.2.1 P00 to P05 (Port 0)

These pins constitute a 6-bit I/O port and can be set to input or output port mode in 1-bit units by using port mode register 0 (PM0). When these pins are used as an input port, an on-chip pull-up resistor can be used by setting pull-up resistor option register 0 (PU0).

4.2.2 P10, P11 (Port 1)

These pins constitute a 2-bit I/O port and can be set to input or output port mode in 1-bit units by using port mode register 1 (PM1). When these pins are used as an input port, an on-chip pull-up resistor can be used by setting pull-up resistor option register 0 (PU0).

4.2.3 P20 to P26 (Port 2)

These pins constitute a 7-bit I/O port. In addition, these pins provide a function to perform I/O to/from the timer and to I/O the data and clock of the serial interface.

Port 2 can be set to the following operation modes in 1-bit units.

(1) Port mode

In port mode, P20 to P26 function as a 7-bit I/O port. Port 2 can be set to input or output mode in 1-bit units by using port mode register 2 (PM2). For P20 to P22, P25, and P26, whether to use on-chip pull-up resistors can be specified in 1-bit units by using pull-up resistor option register B2 (PUB2), regardless of the setting of port mode register 2 (PM2). P23 and P24 are N-ch open-drain I/O ports.

(2) Control mode

In this mode, P20 to P26 function as the timer I/O, the data I/O and the clock I/O of the serial interface.

(a) TI80

This is the external clock input pin for 8-bit timer/event counter 80.

(b) TO80

This is the timer output pin of 8-bit timer/event counter 80.

(c) SI20, SO20

These are the serial data I/O pins of the serial interface.

(d) $\overline{\text{SCK20}}$

This is the serial clock I/O pin of the serial interface.

(e) $\overline{\text{SS20}}$

This is the chip select input pin of the serial interface.

(f) RxD20, TxD20

These are the serial data I/O pins of the asynchronous serial interface.

(g) ASCK20

This is the serial clock input pin of the asynchronous serial interface.

(h) SCL0

This is the clock I/O pin of SMB0.

(i) SDA0

This is the data I/O pin of SMB0.

Caution When using P20 to P26 as serial interface pins, the I/O mode and output latch must be set according to the function to be used. For details of the setting, see Table 14-2 Operating Mode Setting of Serial Interface 20.

4.2.4 P30 to P33 (Port 3)

These pins constitute a 4-bit I/O port. In addition, these pins function as the timer I/O and the external interrupt input.

Port 3 can be set to the following operation modes in 1-bit units.

(1) Port mode

In port mode, P30 to P33 function as a 4-bit I/O port. Port 3 can be set to input or output mode in 1-bit units by using port mode register 3 (PM3). Whether to use the on-chip pull-up resistor can be specified in 1-bit units by using pull-up resistor option register B3 (PUB3), regardless of the setting of port mode register 3 (PM3).

(2) Control mode

In this mode, P30 to P33 function as the timer I/O and the external interrupt input.

(a) TI81

This is the external clock input pin for 8-bit timer/event counter 81.

(b) TO90, TO81, TO82

These are the output pins of 16-bit timer 90, 8-bit timer/event counter 81, and 8-bit timer 82.

(c) CPT90

This is the capture edge input pin of 16-bit timer 90.

(d) BZO90

This is the buzzer output pin of 16-bit timer 90.

(e) INTP0 to INTP3

These are external interrupt input pins for which the valid edge (rising edge, falling edge, and both the rising and falling edges) can be specified.

4.2.5 P50 to P53 (Port 5)

These pins constitute a 4-bit N-ch open-drain I/O port. Port 5 can be set to input or output mode in 1-bit units by using port mode register 5 (PM5). For a mask ROM version, whether a pull-up resistor is to be incorporated can be specified by a mask option.

4.2.6 P60 to P67 (Port 6)

These pins constitute an 8-bit input-only port. They can function as A/D converter input pins as well as a general-purpose input port.

(1) Port mode

In port mode, P60 to P67 function as an 8-bit input-only port.

(2) Control mode

In control mode, P60 to P67 function as A/D converter analog inputs (ANI0 to ANI7).

4.2.7 $\overline{\text{RESET}}$

A low-level active system reset signal is input to this pin.

4.2.8 X1, X2

These pins are used to connect a crystal resonator for main system clock oscillation.

To supply an external clock, input the clock to X1 and input the inverted signal to X2.

4.2.9 XT1, XT2

These pins are used to connect a crystal resonator for subsystem clock oscillation.

To supply an external clock, input the clock to XT1 and input the inverted signal to XT2.

4.2.10 AV_{DD}

Analog power supply pin of the A/D converter. Always use the same potential as that of the V_{DD0} pin even when the A/D converter is not used.

4.2.11 AV_{SS}

This is a ground potential pin of the A/D converter. Always use the same potential as that of the V_{SS0} pin even when the A/D converter is not used.

4.2.12 AV_{REF}

This is the A/D converter reference voltage input pin. When the A/D converter is not used, connect this pin to V_{DD0} or V_{SS0}.

4.2.13 V_{DD0}, V_{DD1}

V_{DD0} is a positive power supply pin for ports.

V_{DD1} is a positive power supply pin for other than ports.

4.2.14 V_{SS0}, V_{SS1}

V_{SS0} is a ground potential pin for ports.

V_{SS1} is a ground potential pin for other than ports.

4.2.15 V_{PP} (flash memory version only)

High voltage apply pin for flash memory programming mode setting and program write/verify.

Connect this pin in either of the following ways.

- Independently connect to a 10 kΩ pull-down resistor.
- By using a jumper on the board, connect directly to the dedicated flash programmer in the programming mode or to V_{SS} in the normal operation mode.

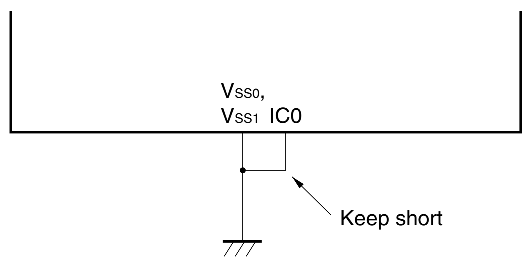
★ If the wiring between the V_{PP} pin and V_{SS} pin is very long or external noise is superimposed on the V_{PP} pin, the user program may not run correctly.

4.2.16 IC0 (mask ROM version only)

The IC0 (internally connected) pin is used to set the μPD789167Y and 789177Y Subseries to test mode before shipment. In normal operation mode, directly connect this pin to the V_{SS0} or V_{SS1} pin with as short a wiring length as possible.

If a potential difference is generated between the IC0 pin and V_{SS0} or V_{SS1} pin due to a long wiring length or external noise superimposed on the IC0 pin, the user program may not run correctly.

- Directly connect the IC0 pin to the V_{SS0} or V_{SS1} pin.



4.2.17 IC2

The IC2 pin is internally connected. Leave this pin open.

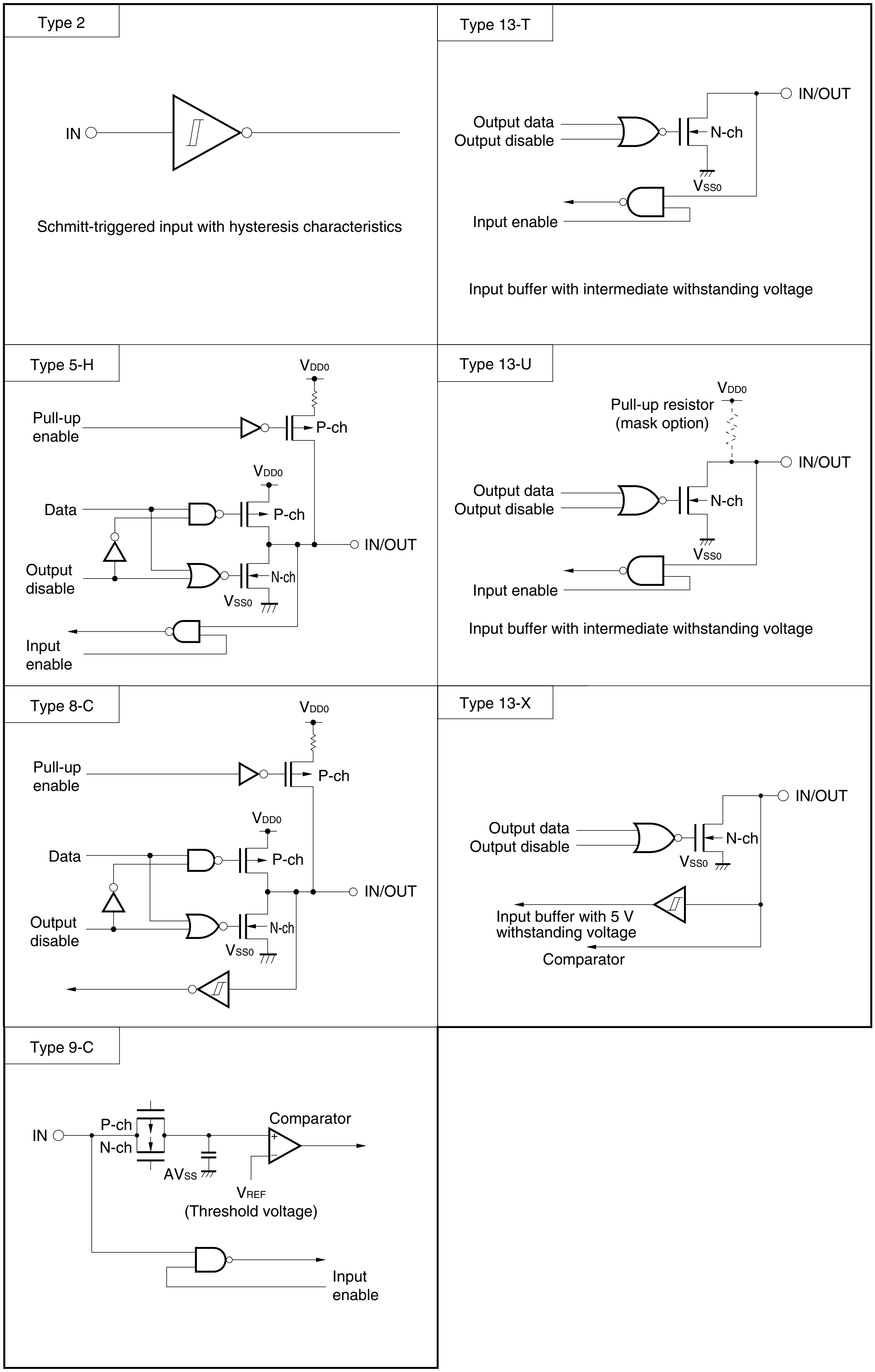
4.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 4-1.
For the I/O circuit configuration of each type, refer to **Figure 4-1**.

Table 4-1. Types of I/O Circuits for Each Pin and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P05	5-H	I/O	Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P10, P11			
P20/$\overline{\text{SCK20}}$/ASCK20	8-C		
P21/SO20/TxD20			
P22/SI20/RxD20			
P23/SCL0	13-X		Input: Independently connect to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P24/SDA0			
P25/TI80/$\overline{\text{SS20}}$	8-C		Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P26/TO80			
P30/INTP0/TI81/CPT90			Input: Independently connect to V_{SS0} or V_{SS1} via a resistor. Output: Leave open.
P31/INTP1/TO81			
P32/INTP2/TO90			
P33/INTP3/TO82/BZO90			
P50 to P53 (mask ROM version)	13-U		Input: Connect to V_{SS0} or V_{SS1}. Output: Leave open.
P50 to P53 (flash memory version)	13-T		
P60/ANI0 to P67/ANI7	9-C	Input	Connect directly to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1}.
XT1	–	Input	Connect directly to V_{SS0} or V_{SS1}.
XT2		–	Leave open.
$\overline{\text{RESET}}$	2	Input	–
IC0 (mask ROM version)	–	–	Connect directly to V_{SS0} or V_{SS1}.
IC2			Leave open.
V_{PP} (flash memory version)			Independently connect via a 10 kΩ pull-down resistor, or connect directly to V_{SS0} or V_{SS1}.

Figure 4-1. Pin I/O Circuits



5.1 Memory Space

Products in the μPD789167, 789177, 789167Y, and 789177Y Subseries can each access up to 64 KB of memory space. Figures 5-1 through 5-3 show the memory maps.

Figure 5-1. Memory Map (μPD789166, μPD789176, μPD789166Y, and μPD789176Y)

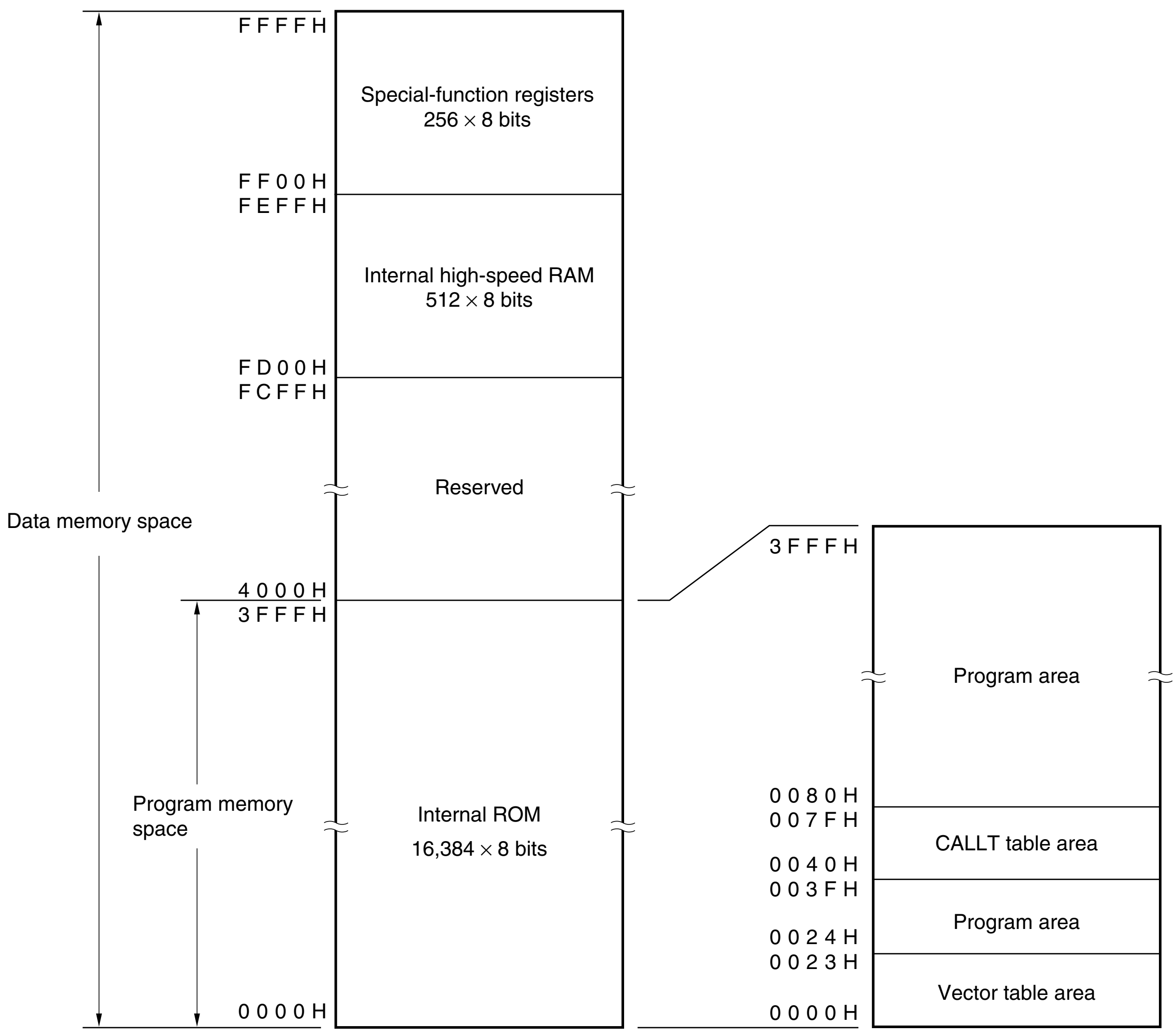


Figure 5-2. Memory Map (μPD789167, μPD789177, μPD789167Y, and μPD789177Y)

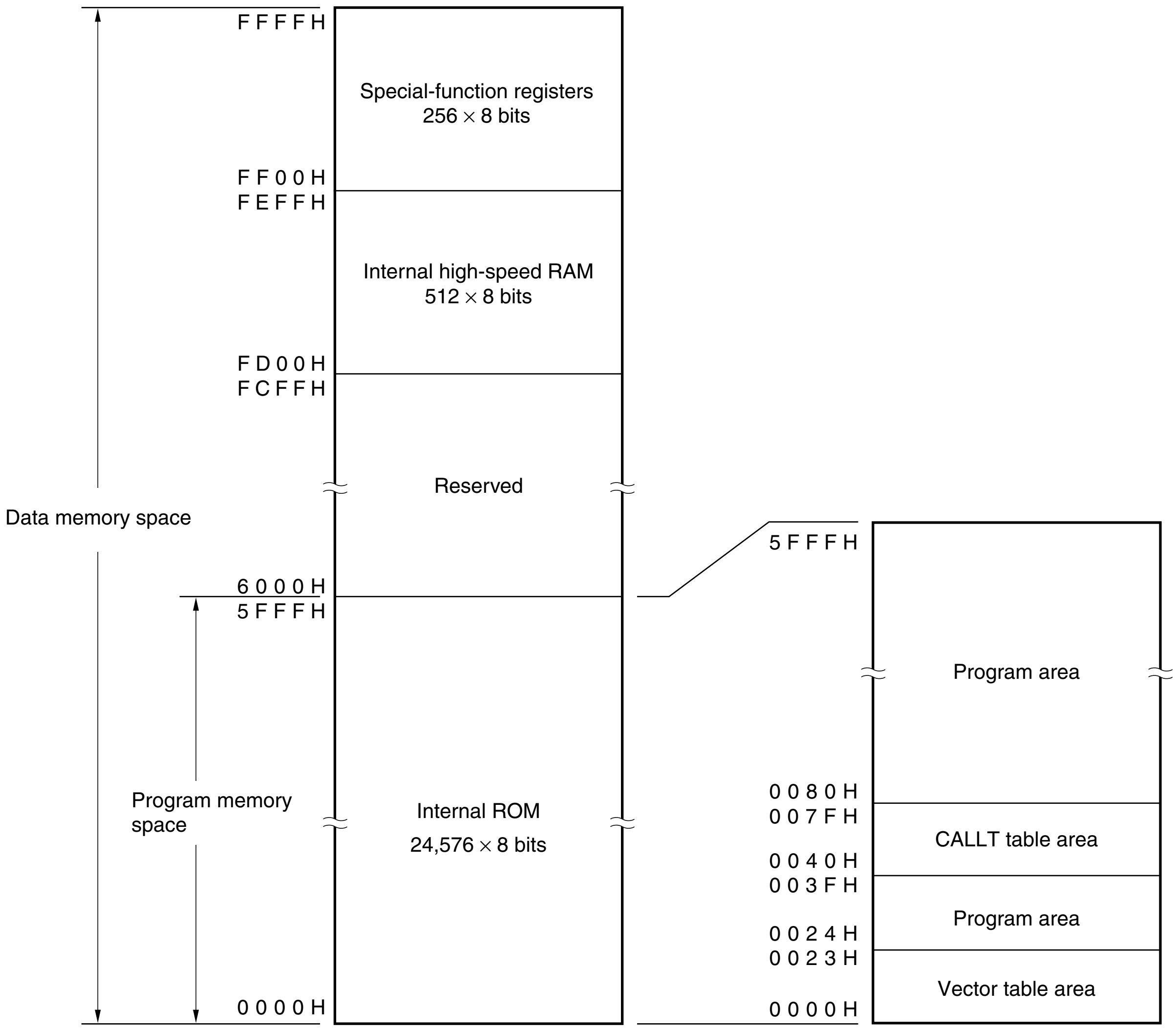
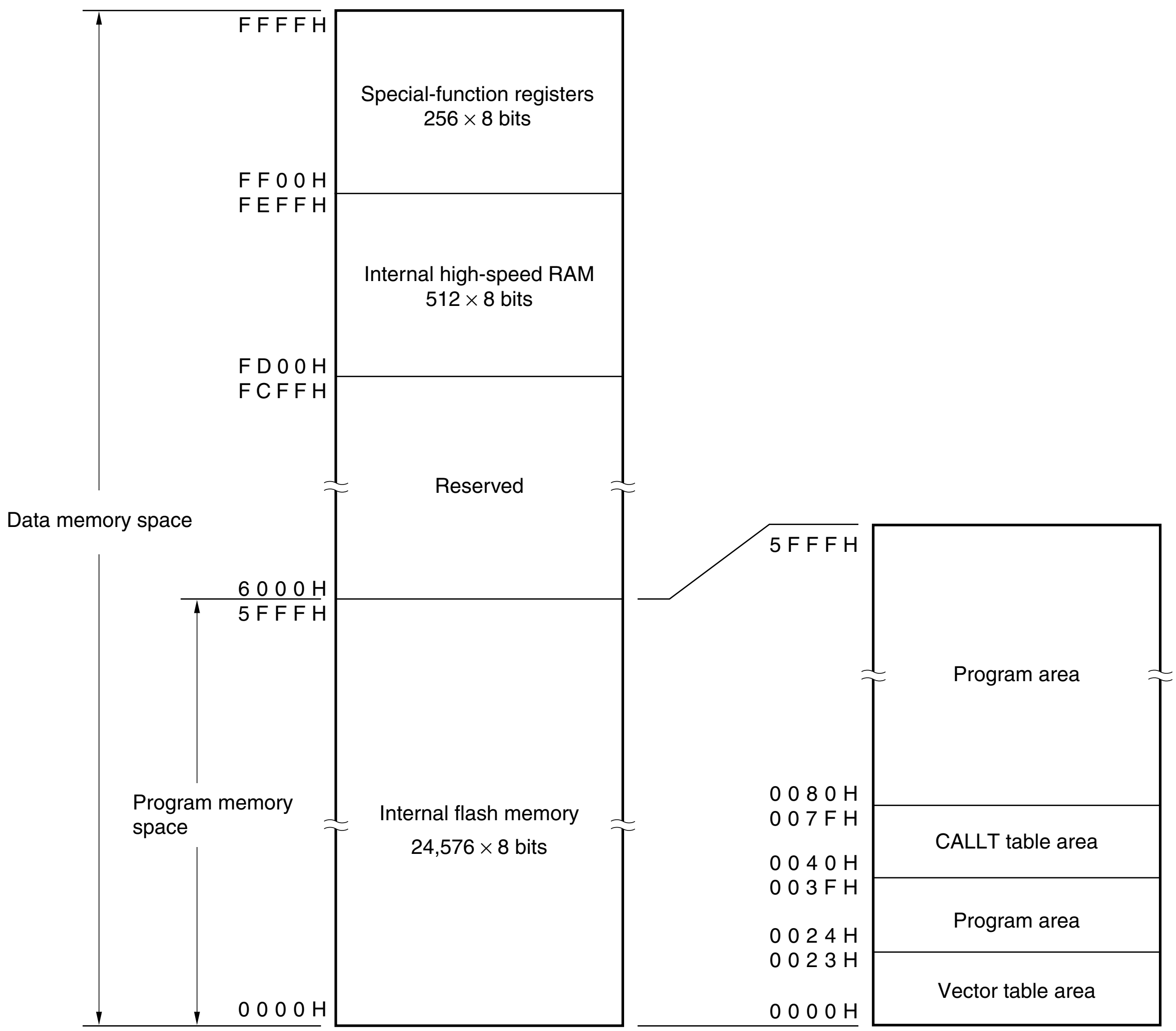


Figure 5-3. Memory Map (μPD78F9177, μPD78F9177Y, μPD78F9177A, and μPD78F9177AY)



5.1.1 Internal program memory space

The internal program memory space stores programs and table data. This space is usually addressed by the program counter (PC).

The μPD789167, 789177, 789167Y, and 789177Y Subseries provide the following internal ROM (or flash memory) containing the following capacities.

Table 5-1. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
μPD789166, μPD789176, μPD789166Y, μPD789176Y	Mask ROM	16,384 × 8 bits
μPD789167, μPD789177, μPD789167Y, μPD789177Y		24,576 × 8 bits
μPD78F9177, μPD78F9177Y, μPD78F9177A, μPD 78F9177AY	Flash memory	24,576 × 8 bits

The following areas are allocated to the internal program memory space.

(1) Vector table area

A 36-byte area of addresses 0000H to 0023H is reserved as a vector table area. This area stores program start addresses to be used when branching by $\overline{\text{RESET}}$ input or interrupt request generation. Of a 16-bit program address, the lower 8 bits are stored in an even address, and the higher 8 bits are stored in an odd address.

Table 5-2. Vector Table

Vector Table Address	Interrupt Request	Vector Table Address	Interrupt Request
0000H	$\overline{\text{RESET}}$ input	0014H	INTWTI
0004H	INTWDT	0016H	INTTM80
0006H	INTP0	0018H	INTTM81
0008H	INTP1	001AH	INTTM82
000AH	INTP2	001CH	INTTM90
000CH	INTP3	001EH	INTSMB0 Note
000EH	INTSR20/INTCSI20	0020H	INTSMBOV0 Note
0010H	INTST20	0022H	INTAD0
0012H	INTWT		

Note For the μPD789167Y and 789177Y Subseries only

(2) CALLT instruction table area

The subroutine entry address of a 1-byte call instruction (CALLT) can be stored in a 64-byte area of addresses 0040H to 007FH.

5.1.2 Internal data memory (internal high-speed RAM) space

The μPD789167, 789177, 789167Y, and 789177Y Subseries provide a 512-byte internal high-speed RAM.

The internal high-speed RAM can also be used as a stack memory.

5.1.3 Special-function register (SFR) area

Special-function registers (SFRs) of on-chip peripheral hardware are allocated to an area of FF00H to FFFFH (see **Table 5-3**).

5.1.4 Data memory addressing

Each of the μPD789167, 789177, 789167Y, 789177Y Subseries is provided with a wide range of addressing modes to make memory manipulation as efficient as possible. A data memory area (FD00H to FFFFH) can be accessed using a unique addressing mode according to its use, such as a special-function register (SFR). Figures 5-4 through 5-6 illustrate the data memory addressing modes.

Figure 5-4. Data Memory Addressing Modes (μPD789166, μPD789176, μPD789166Y, and μPD789176Y)

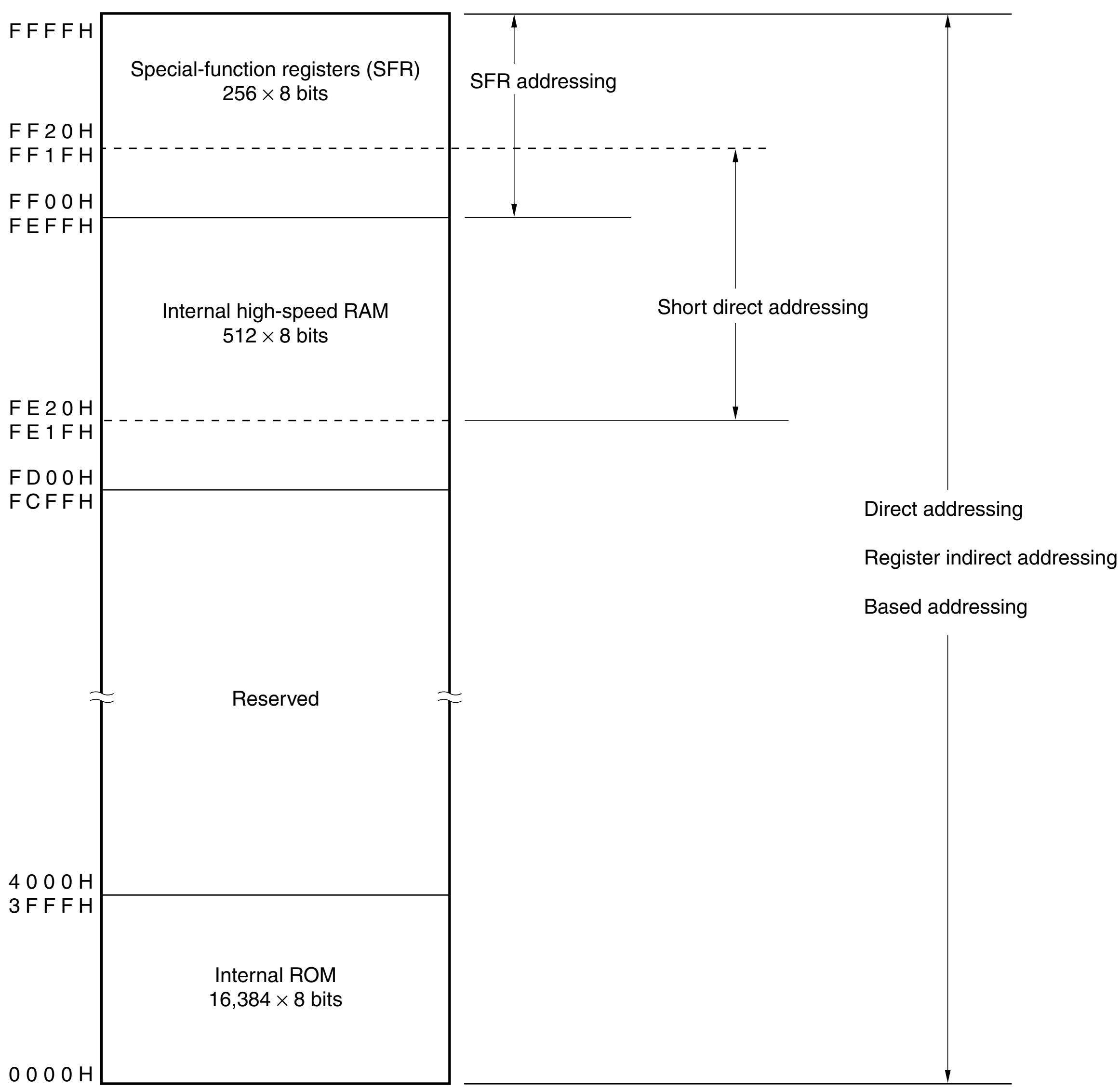


Figure 5-5. Data Memory Addressing Modes (μPD789167, μPD789177, μPD789167Y, and μPD789177Y)

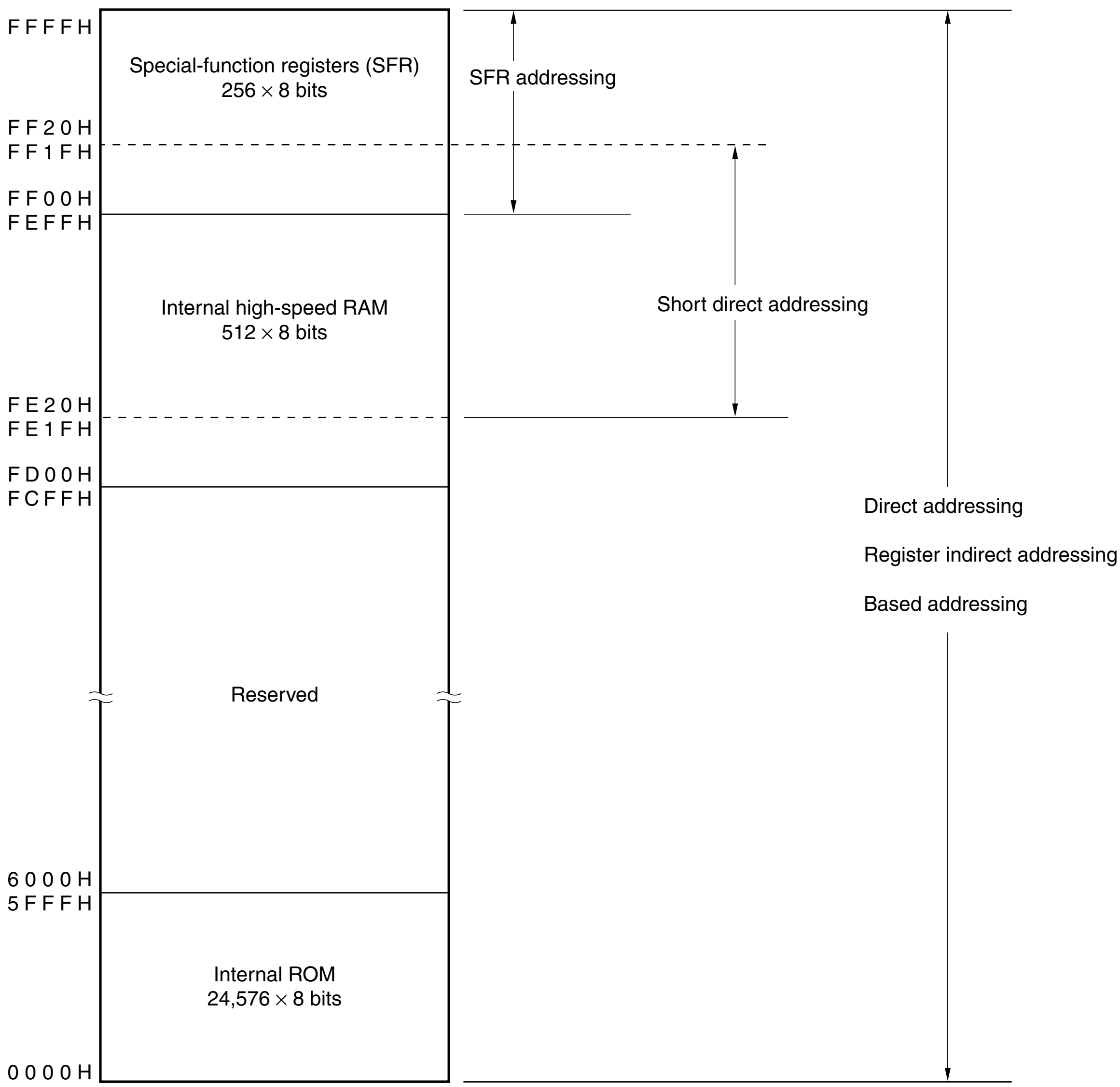
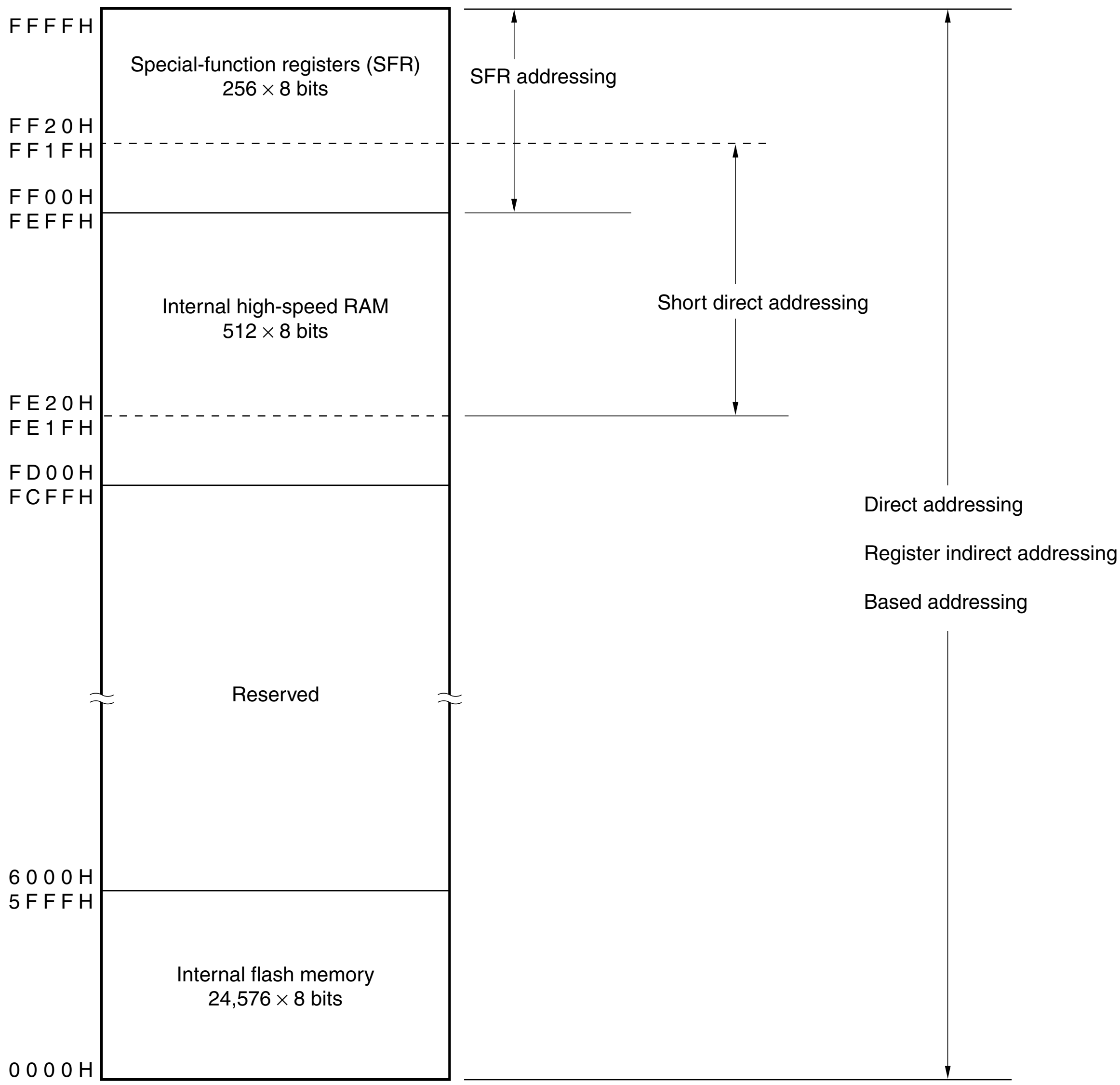


Figure 5-6. Data Memory Addressing Modes (μPD78F9177, μPD78F9177Y, μPD78F9177A, and μPD78F9177AY)



5.2 Processor Registers

The μPD789167, 789177, 789167Y, and 789177Y Subseries provide the following on-chip processor registers.

5.2.1 Control registers

The control registers have special functions to control the program sequence statuses and stack memory. The control registers include a program counter, a program status word, and a stack pointer.

(1) Program counter (PC)

The program counter is a 16-bit register which holds the address information of the next program to be executed.

In normal operation, the PC is automatically incremented according to the number of bytes of the instruction to be fetched. When a branch instruction is executed, immediate data or register contents are set.

$\overline{\text{RESET}}$ input sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 5-7. Program Counter Configuration

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags to be set/reset by instruction execution.

Program status word contents are automatically stacked upon interrupt request generation or PUSH PSW instruction execution and are automatically restored upon execution of the RETI and POP PSW instructions.

$\overline{\text{RESET}}$ input sets the PSW to 02H.

Figure 5-8. Program Status Word Configuration

	7							0
PSW	IE	Z	0	AC	0	0	1	CY

(a) Interrupt enable flag (IE)

This flag controls interrupt request acknowledgment operations of the CPU.

When IE = 0, the interrupt disabled (DI) status is set. All interrupt requests except non-maskable interrupt are disabled.

When IE = 1, the interrupt enabled (EI) status is set. Interrupt request acknowledgment is controlled with an interrupt mask flag for various interrupt sources.

This flag is reset to 0 upon DI instruction execution or interrupt acknowledgment and is set to 1 upon EI instruction execution.

(b) Zero flag (Z)

When the operation result is zero, this flag is set to 1. It is reset to 0 in all other cases.

(c) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set to 1. It is reset to 0 in all other cases.

(d) Carry flag (CY)

This flag stores an overflow or underflow that occurs upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register used to hold the start address of the memory stack area. Only the internal high-speed RAM area can be set as the stack area.

Figure 5-9. Stack Pointer Configuration

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The SP is decremented ahead of writing (saving) to the stack memory and is incremented after reading (restoring) from the stack memory.

Each stack operation saves/restores data as shown in Figures 5-10 and 5-11.

★ **Caution Since $\overline{\text{RESET}}$ input makes SP contents undefined, be sure to initialize the SP before using the stack.**

Figure 5-10. Data to Be Saved to Stack Memory

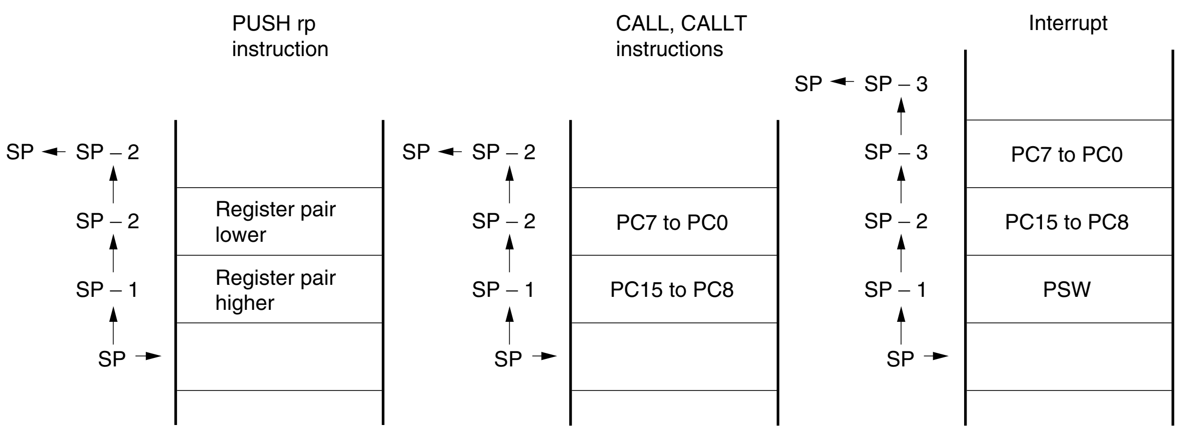
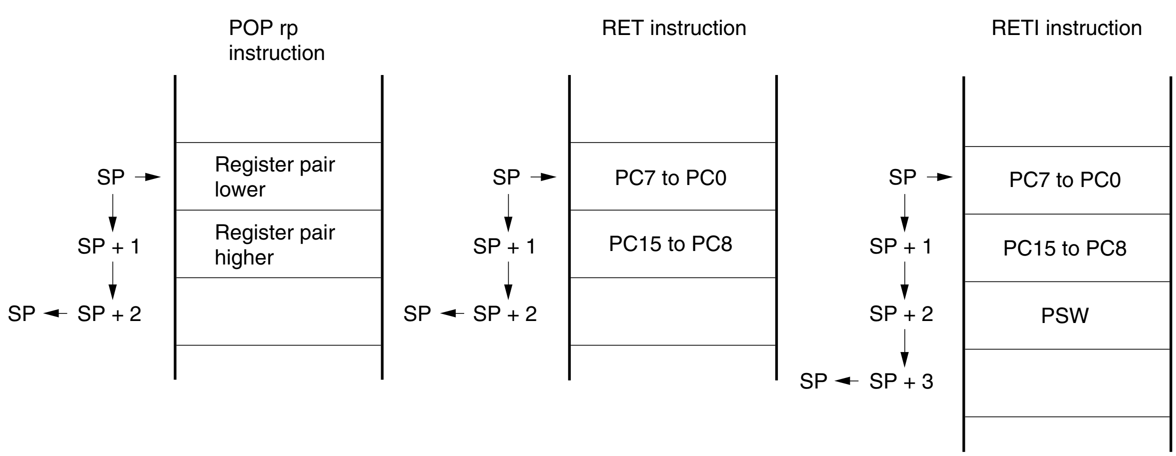


Figure 5-11. Data to Be Restored from Stack Memory



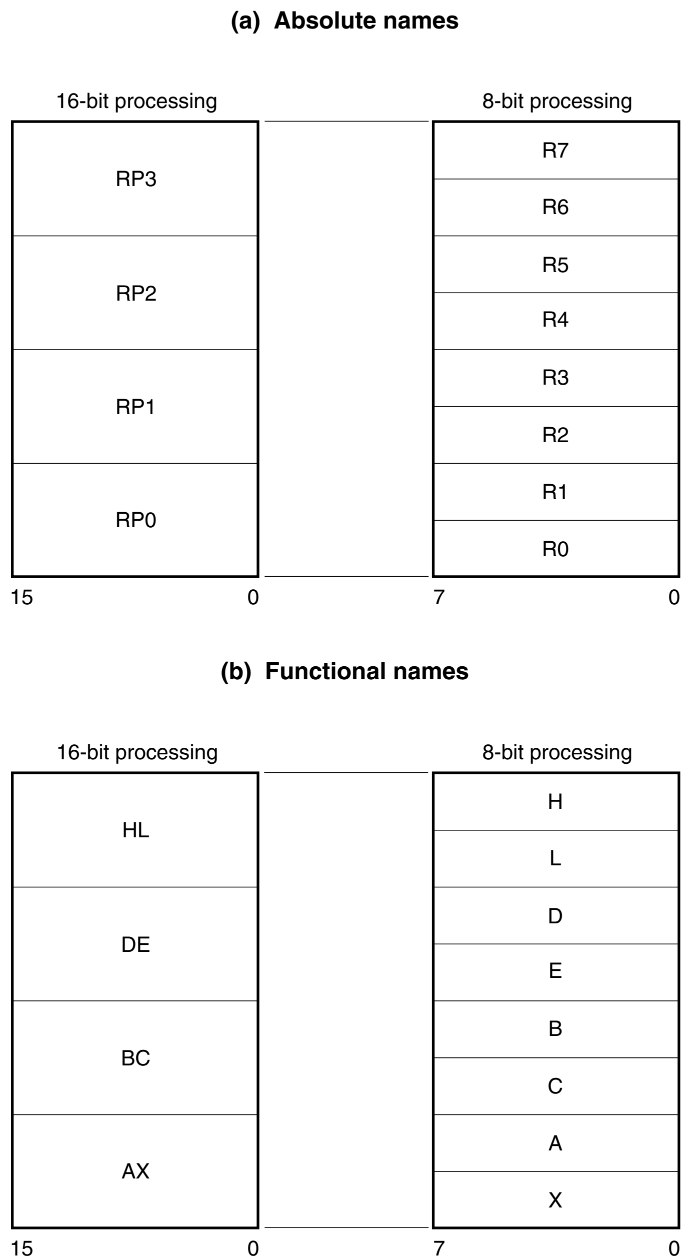
5.2.2 General-purpose registers

The general-purpose registers consist of eight 8-bit registers (X, A, C, B, E, D, L, and H).

In addition that each register can be used as an 8-bit register, two 8-bit registers in pairs can be used as a 16-bit register (AX, BC, DE, and HL).

They can be described in terms of functional names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

Figure 5-12. General-Purpose Register Configuration



5.2.3 Special-function registers (SFR)

Unlike a general-purpose register, each special-function register has a special function.

They are allocated to the 256-byte area FF00H to FFFFH.

The special-function registers can be manipulated, like the general-purpose registers, with operation, transfer, and bit manipulation instructions. Manipulatable bit units (1, 8, and 16) differ depending on the special-function register type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describes a symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit). This manipulation can also be specified with an address.

- 8-bit manipulation
  Describes a symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr). This manipulation can also be specified with an address.

- 16-bit manipulation
  Describes a symbol reserved by the assembler for the 16-bit manipulation instruction operand. When specifying an address, describe an even address.

Table 5-3 lists the special-function registers. The meanings of the symbols in this table are as follows.

- Symbol
  Indicates the addresses of the implemented special-function registers. The symbols shown in this column are reserved words in the assembler, and have already been defined as sfr variables by the #pragma sfr directive in the C compiler. Therefore, these symbols can be used as instruction operands if an assembler or integrated debugger is used.

- R/W
  Indicates whether the special-function register can be read or written.
  R/W: Read/write
  R: Read only
  W: Write only

- Bit units for manipulation
  Indicates the bit units (1, 8, and 16) in which the special-function register can be manipulated.

- After reset
  Indicates the status of the special-function register when the $\overline{\text{RESET}}$ signal is input.

Table 5-3. Special-Function Registers (1/2)

Address	Special-Function Register (SFR) Name	Symbol		R/W	Bit Units for Manipulation			After Reset
					1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0		R/W	√	√	–	00H
FF01H	Port 1	P1			√	√	–	
FF02H	Port 2	P2			√	√	–	
FF03H	Port 3	P3			√	√	–	
FF05H	Port 5	P5			√	√	–	
FF06H	Port 6	P6		R	√	√	–	
FF10H	16-bit multiplication result storage register 0	MUL0L	MUL0		–	–	√[Notes 2, 3]	Undefined
FF11H		MUL0H						
FF14H	A/D conversion result register 0	ADCR0			–	√[Note 1]	√[Note 2]	
FF15H								
FF16H	16-bit compare register 90	CR90L	CR90	W	–	–	√[Notes 2, 3]	FFFFH
FF17H		CR90H						
FF18H	16-bit timer counter 90	TM90L	TM90	R	–	–	√[Notes 2, 3]	0000H
FF19H		TM90H						
FF1AH	16-bit capture register 90	TCP90L	TCP90		–	–	√[Notes 2, 3]	Undefined
FF1BH		TCP90H						
FF20H	Port mode register 0	PM0		R/W	√	√	–	FFH
FF21H	Port mode register 1	PM1			√	√	–	
FF22H	Port mode register 2	PM2			√	√	–	
FF23H	Port mode register 3	PM3			√	√	–	
FF25H	Port mode register 5	PM5			√	√	–	
FF32H	Pull-up resistor option register B2	PUB2			√	√	–	00H
FF33H	Pull-up resistor option register B3	PUB3			√	√	–	
FF42H	Timer clock selection register 2	TCL2			–	√	–	
FF48H	16-bit timer mode control register 90	TMC90			√	√	–	
FF49H	Buzzer output control register 90	BZC90			√	√	–	
FF4AH	Watch timer mode control register	WTM			√	√	–	
FF50H	8-bit compare register 80	CR80		W	–	√	–	Undefined
FF51H	8-bit timer counter 80	TM80		R	–	√	–	00H
FF53H	8-bit timer mode control register 80	TMC80		R/W	√	√	–	

Notes 1. When using this register with an 8-bit A/D converter (μPD789167 or 789167Y Subseries), the register can be accessed in 8-bit units. At this time, the address is FF15H.

When using this register with a 10-bit A/D converter (μPD789177 or 789177Y Subseries), the register can be accessed only in 16-bit units. When the μPD78F9177 or μPD78F9177A, the flash memory counterpart of the μPD789166 or μPD789167, is used, the register can be accessed in 8-bit units. However, only an object file assembled with the μPD789166 or μPD789167 can be used. The same is also true for the μPD78F9177Y or μPD78F9177AY, the flash memory counterpart of the μPD789166Y or μPD789167Y. When the μPD78F9177Y or μPD78F9177AY is used, the register can be accessed in 8-bit units. However, only an object file assembled with the μPD789166Y and μPD789167Y can be used.

2. 16-bit access is allowed only with short direct addressing.

3. MUL0, CR90, TM90, and TCP90 are designed only for 16-bit access. With direct addressing, however, they can also be accessed in 8-bit mode.

Table 5-3. Special-Function Registers (2/2)

Address	Special-Function Register (SFR) Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1 Bit	8 Bits	16 Bits	
FF54H	8-bit compare register 81	CR81	W	–	√	–	Undefined
FF55H	8-bit timer counter 81	TM81	R	–	√	–	00H
FF57H	8-bit timer mode control register 81	TMC81	R/W	√	√	–	
FF58H	8-bit compare register 82	CR82	W	–	√	–	Undefined
FF59H	8-bit timer counter 82	TM82	R	–	√	–	00H
FF5BH	8-bit timer mode control register 82	TMC82	R/W	√	√	–	
FF70H	Asynchronous serial interface mode register 20	ASIM20		√	√	–	
FF71H	Asynchronous serial interface status register 20	ASIS20	R	√	√	–	
FF72H	Serial operation mode register 20	CSIM20	R/W	√	√	–	
FF73H	Baud rate generator control register 20	BRGC20		–	√	–	
FF74H	Transmission shift register 20	TXS20 / SIO20	W	–	√	–	FFH
	Reception buffer register 20	RXB20	R	–	√	–	Undefined
FF78H	SMB control register 0[Note]	SMBC0	R/W	√	√	–	00H
FF79H	SMB status register 0[Note]	SMBS0	R	√	√	–	
FF7AH	SMB clock selection register 0[Note]	SMBCL0	R/W	√	√	–	
FF7BH	SMB slave address register 0[Note]	SMBSVA0		√	√	–	
FF7CH	SMB mode register 0[Note]	SMBM0		√	√	–	20H
FF7DH	SMB input level setting register 0[Note]	SMBVI0		√	√	–	00H
FF7EH	SMB shift register 0[Note]	SMB0		√	√	–	
FF80H	A/D converter mode register 0	ADM0		√	√	–	
FF84H	A/D input selection register 0	ADS0		√	√	–	
FFD0H	Multiplication data register A0	MRA0	W	√	√	–	Undefined
FFD1H	Multiplication data register B0	MRB0		√	√	–	
FFD2H	Multiplier control register 0	MULC0	R/W	√	√	–	00H
FFE0H	Interrupt request flag register 0	IF0		√	√	–	
FFE1H	Interrupt request flag register 1	IF1		√	√	–	
FFE4H	Interrupt mask flag register 0	MK0		√	√	–	FFH
FFE5H	Interrupt mask flag register 1	MK1		√	√	–	
FFECH	External interrupt mode register 0	INTM0		–	√	–	00H
FFEDH	External interrupt mode register 1	INTM1		–	√	–	
FFF0H	Suboscillation mode register	SCKM		√	√	–	
FFF2H	Subclock control register	CSS		√	√	–	
FFF7H	Pull-up resistor option register 0	PU0		√	√	–	
FFF9H	Watchdog timer mode register	WDTM		√	√	–	
FFFAH	Oscillation stabilization time selection register	OSTS		–	√	–	04H
FFFBH	Processor clock control register	PCC		√	√	–	02H

Note For the μPD789167Y and 789177Y Subseries only

5.3 Instruction Address Addressing

An instruction address is determined by the program counter (PC) contents. The PC contents are normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to the PC and branched by the following addressing (for details of each instruction, refer to **78K/0S Series Instruction User's Manual (U11047E)**).

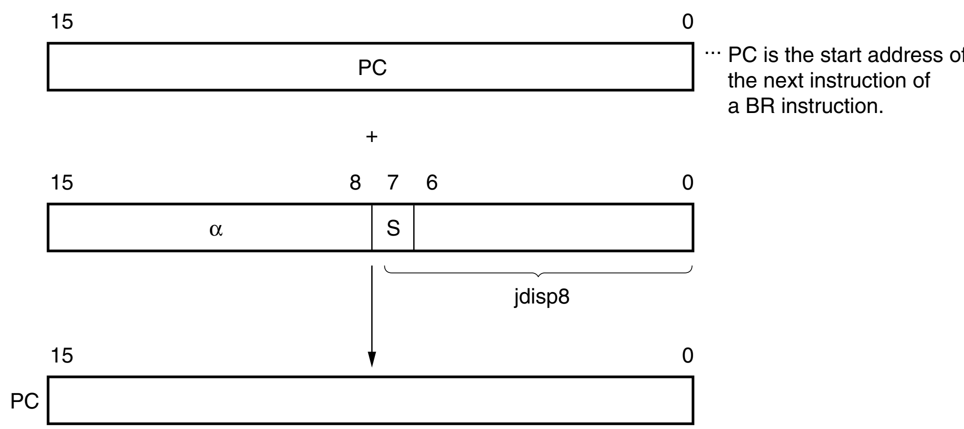
5.3.1 Relative addressing

[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (–128 to +127) and bit 7 becomes a sign bit. In other words, the range of branch in relative addressing is between –128 and +127 of the start address of the following instruction.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, α indicates all bits "0".
When S = 1, α indicates all bits "1".

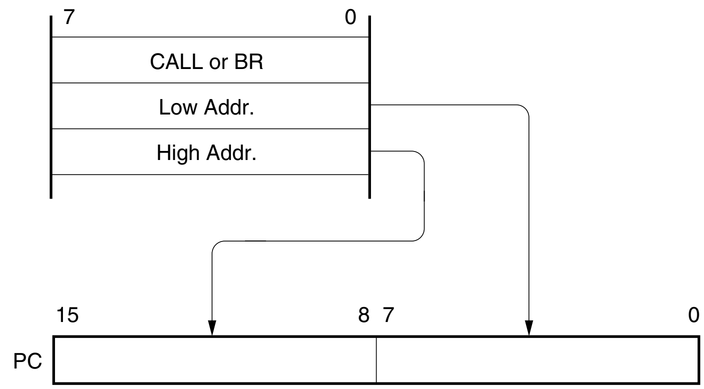
5.3.2 Immediate addressing

[Function]

Immediate data in the instruction word is transferred to the program counter (PC) and branched.
This function is carried out when the CALL !addr16 and BR !addr16 instructions are executed.
CALL !addr16 and BR !addr16 instructions can be used to branch to all the memory spaces.

[Illustration]

In case of CALL !addr16 and BR !addr16 instructions



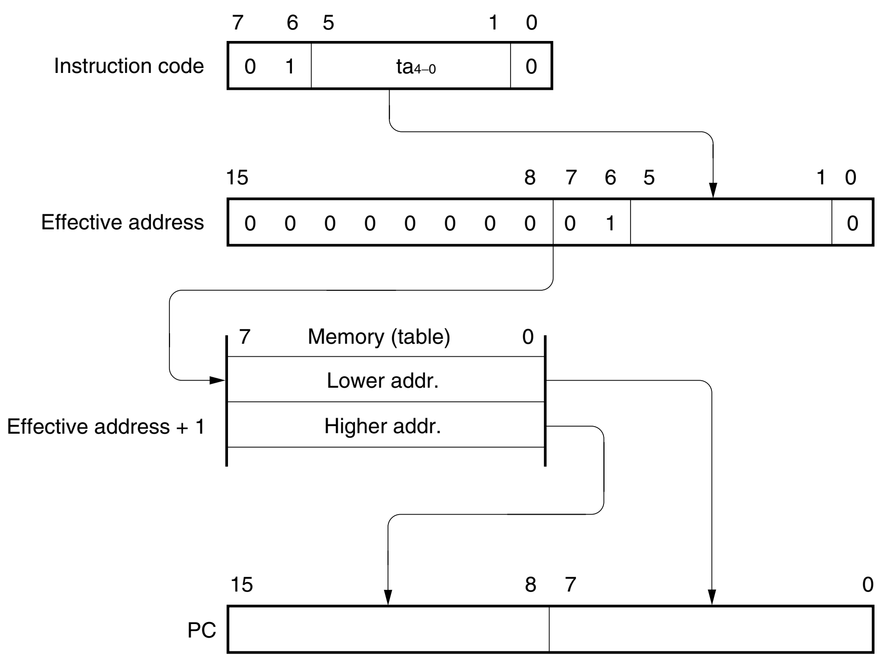
5.3.3 Table indirect addressing

[Function]

Table contents (branch destination address) of the particular location to be addressed by the immediate data of an instruction code from bit 1 to bit 5 are transferred to the program counter (PC) and branched.

Table indirect addressing is carried out when the CALLT [addr5] instruction is executed. This instruction can be used to branch to all the memory spaces according to the address stored in the memory table 40H to 7FH.

[Illustration]



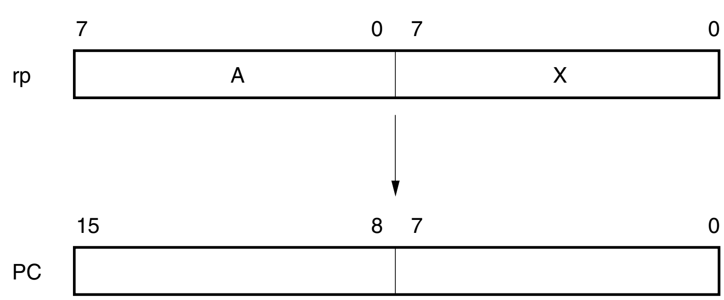
5.3.4 Register addressing

[Function]

Register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) and branched.

This function is carried out when the BR AX instruction is executed.

[Illustration]



5.4 Operand Address Addressing

The following methods are available to specify the register and memory (addressing) which undergo manipulation during instruction execution.

5.4.1 Direct addressing

[Function]

The memory indicated by immediate data in an instruction word is directly addressed.

[Operand format]

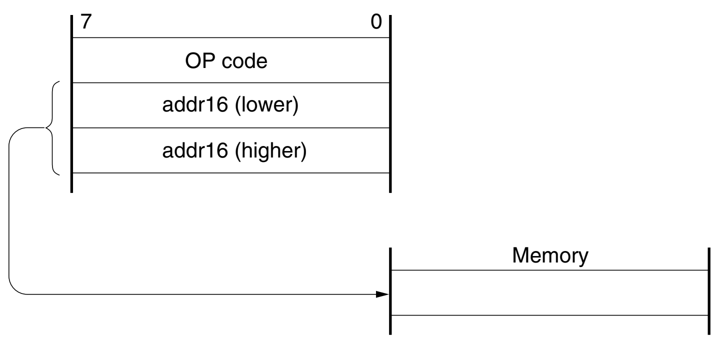
Identifier	Description
addr16	Label or 16-bit immediate data

[Description example]

MOV A, !FE00H; When setting !addr16 to FE00H

Instruction code	0	0	1	0	1	0	0	1	OP code
	0	0	0	0	0	0	0	0	00H
	1	1	1	1	1	1	1	0	FEH

[Illustration]



5.4.2 Short direct addressing

[Function]

The memory to be manipulated in the fixed space is directly addressed with 8-bit data in an instruction word.

The fixed space where this addressing is applied to is the 256-byte space FE20H to FF1FH. An internal high-speed RAM and special-function registers (SFR) are mapped at FE20H to FEFFH and FF00H to FF1FH, respectively.

The SFR area (FF00H to FF1FH) where short direct addressing is applied is a part of the overall SFR area. In this area, ports which are frequently accessed in a program and a compare register of the timer counter are mapped, and these SFRs can be manipulated with a small number of bytes and clocks.

When 8-bit immediate data is at 20H to FFH, bit 8 of an effective address is set to 0. When it is at 00H to 1FH, bit 8 is set to 1. See [Illustration] below.

[Operand format]

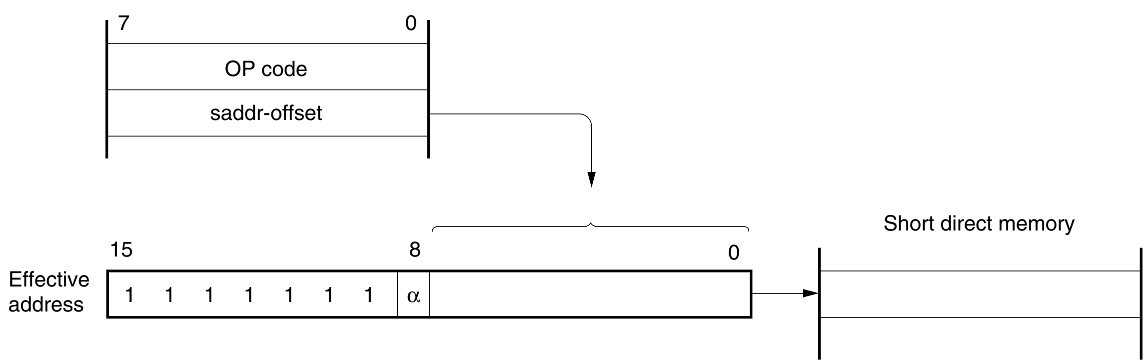
Identifier	Description
saddr	Label or FE20H to FF1FH immediate data
saddrp	Label or FE20H to FF1FH immediate data (even address only)

[Description example]

MOV FE90H, #50H; When setting saddr to FE90H and the immediate data to 50H

Instruction code	1	1	1	1	0	1	0	1	OP code
	1	0	0	1	0	0	0	0	90H (saddr-offset)
	0	1	0	1	0	0	0	0	50H (immediate data)

[Illustration]



When 8-bit immediate data is 20H to FFH, $\alpha = 0$.
When 8-bit immediate data is 00H to 1FH, $\alpha = 1$.

5.4.3 Special-function register (SFR) addressing

[Function]

The memory-mapped special-function registers (SFR) are addressed with 8-bit immediate data in an instruction word.

This addressing is applied to the 256-byte space FF00H to FFFFH. However, the SFRs mapped at FF00H to FF1FH can also be accessed with short direct addressing.

[Operand format]

Identifier	Description
sfr	Special-function register name

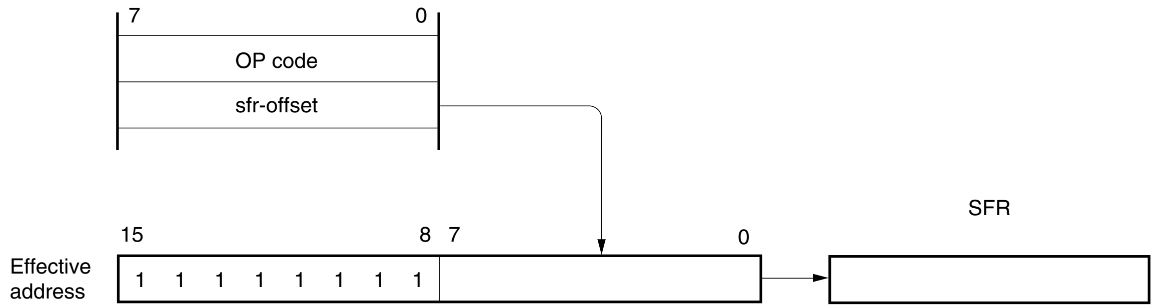
[Description example]

MOV PM0, A; When selecting PM0 for sfr

Instruction code

1	1	1	0	0	1	1	1
0	0	1	0	0	0	0	0

[Illustration]



5.4.4 Register addressing

[Function]

The general-purpose registers are accessed as operands. The general-purpose register to be accessed is specified by the register specification code and functional name in the instruction code.

Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the instruction code.

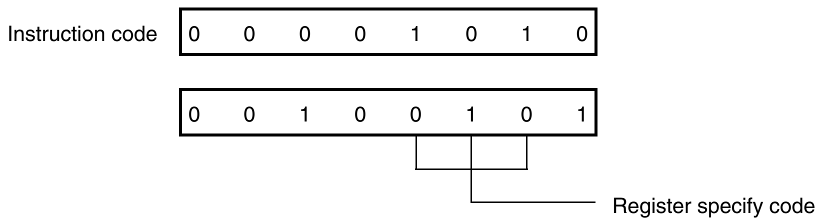
[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

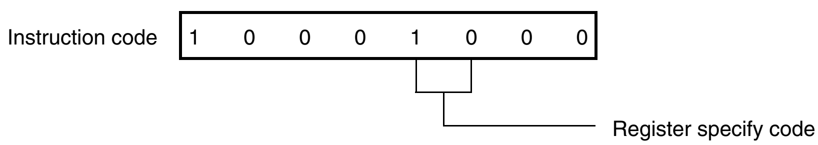
'r' and 'rp' can be described with absolute names (R0 to R7 and RP0 to RP3) as well as function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

[Description example]

MOV A, C; When selecting the C register for r



INCW DE; When selecting the DE register pair for rp



5.4.5 Register indirect addressing

[Function]

The memory is addressed with the contents of the register pair specified as an operand. The register pair to be accessed is specified with the register pair specify code in the instruction code. This addressing can be carried out for all the memory spaces.

[Operand format]

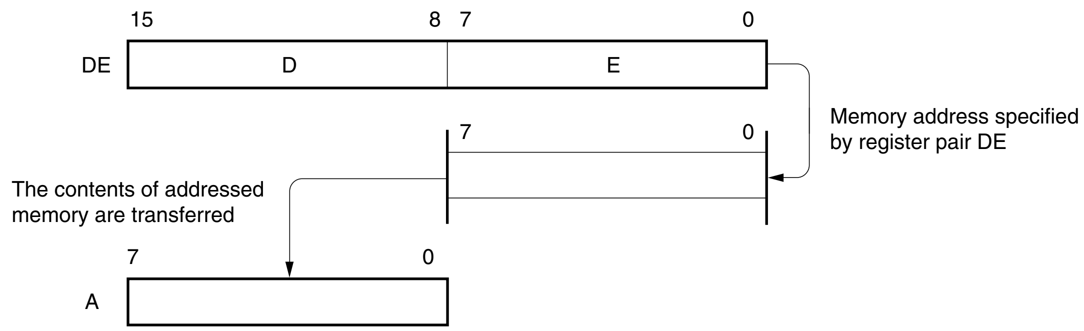
Identifier	Description
–	[DE], [HL]

[Description example]

MOV A, [DE]; When selecting register pair [DE]

Instruction code	0	0	1	0	1	0	1	1

[Illustration]



5.4.6 Based addressing

[Function]

8-bit immediate data is added to the contents of the base register, that is, the HL register pair, and the sum is used to address the memory. Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be carried out for all the memory spaces.

[Operand format]

Identifier	Description
–	[HL+byte]

[Description example]

MOV A, [HL+10H]; When setting byte to 10H

Instruction code	0	0	1	0	1	1	0	1
	0	0	0	1	0	0	0	0

5.4.7 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call, and RETURN instructions are executed or the register is saved/reset upon generation of an interrupt request.

Stack addressing can be used to access the internal high-speed RAM area only.

[Description example]

In the case of PUSH DE

Instruction code	1	0	1	0	1	0	1	0

CHAPTER 6 PORT FUNCTIONS

6.1 Port Functions

The μPD789167, 789177, 789167Y, and 789177Y Subseries are provided with the ports shown in Figure 6-1. These ports are used to enable several types of control. Table 6-1 lists the functions of each port.

These ports, while originally designed as digital I/O ports, have alternate functions, as summarized in **3.1 Pin Function List** (μPD789167 and 789177 Subseries) and **4.1 Pin Function List** (μPD789167Y and 789177Y Subseries).

Figure 6-1. Port Types

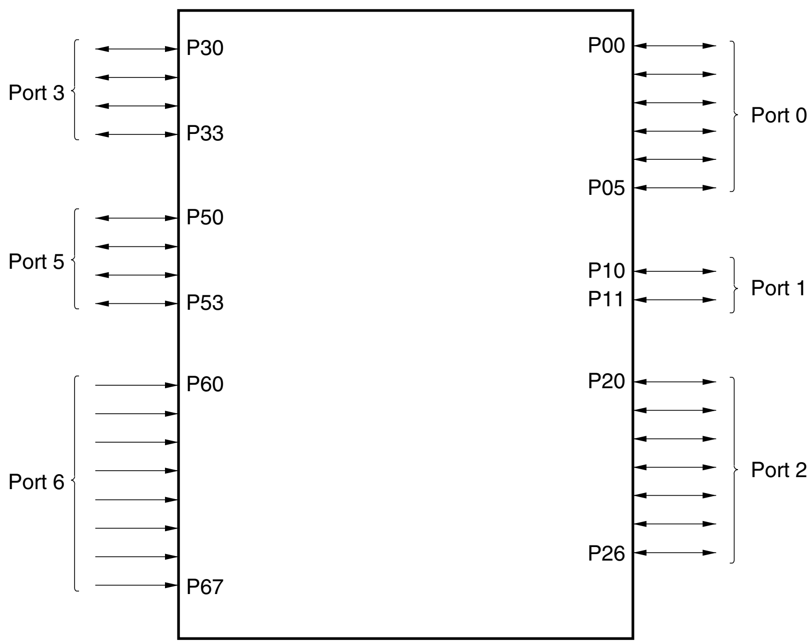


Table 6-1. Port Functions

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P05	I/O	Port 0 6-bit I/O port I/O mode can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of pull-up resistor option register 0 (PU0).	Input	–
P10, P11	I/O	Port 1 2-bit I/O port I/O mode can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of pull-up resistor option register 0 (PU0).	Input	–
P20	I/O	Port 2 7-bit I/O port I/O mode can be specified in 1-bit units. For P20 to P22, P25, and P26, an on-chip pull-up resistor can be specified by means of pull-up resistor option register B2 (PUB2). Only P23 and P24 can be used as N-ch open-drain I/O port pins.	Input	$\overline{\text{SCK20}}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				SCL0[Note]
P24				SDA0[Note]
P25				TI80/$\overline{\text{SS20}}$
P26				TO80
P30	I/O	Port 3 4-bit I/O port I/O mode can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of pull-up resistor option register B3 (PUB3).	Input	INTP0/TI81/CPT90
P31				INTP1/TO81
P32				INTP2/TO90
P33				INTP3/TO82/BZO90
P50 to P53	I/O	Port 5 4-bit N-ch open-drain I/O port I/O mode can be specified in 1-bit units. For a mask ROM version, an on-chip pull-up resistor can be specified by a mask option.	Input	–
P60 to P67	Input	Port 6 8-bit input-only port	Input	ANI0 to ANI7

Note For the μPD789167Y and 789177Y Subseries only

6.2 Port Configuration

Ports have the following hardware configuration.

Table 6-2. Configuration of Port

Parameter	Configuration
Control registers	Port mode registers (PMm: m = 0 to 3, 5) Pull-up resistor option register 0 (PU0) Pull-up resistor option registers B2, B3 (PUB2, PUB3)
Ports	Total: 31 (CMOS I/O: 17, CMOS input: 8, N-ch open-drain I/O: 6)
Pull-up resistors	• Mask ROM versions Total: 21 (software control: 17, mask option control: 4) • Flash memory versions Total: 17 (software control only)

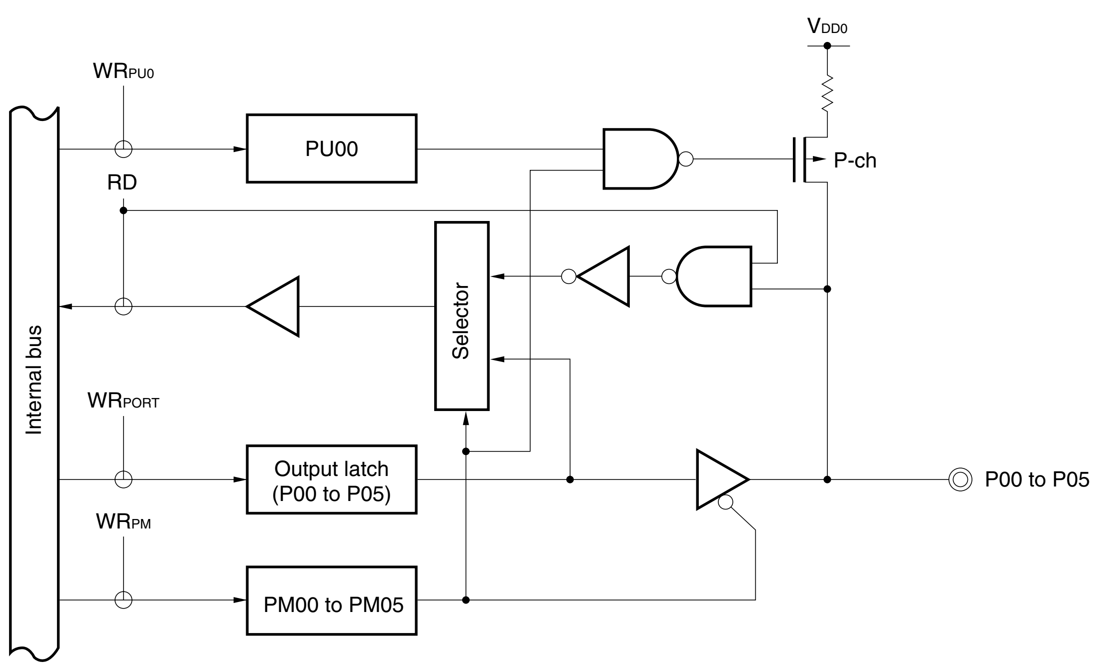
6.2.1 Port 0

This is a 6-bit I/O port with output latches. Port 0 can be set to input or output mode in 1-bit units by using port mode register 0 (PM0). When the P00 to P05 pins are used as input port pins, on-chip pull-up resistors can be connected in 6-bit units by using pull-up resistor option register 0 (PU0).

$\overline{\text{RESET}}$ input sets port 0 to input mode.

Figure 6-2 shows a block diagram of port 0.

Figure 6-2. Block Diagram of P00 to P05



PU0: Pull-up resistor option register 0
PM: Port mode register
RD: Port 0 read signal
WR: Port 0 write signal

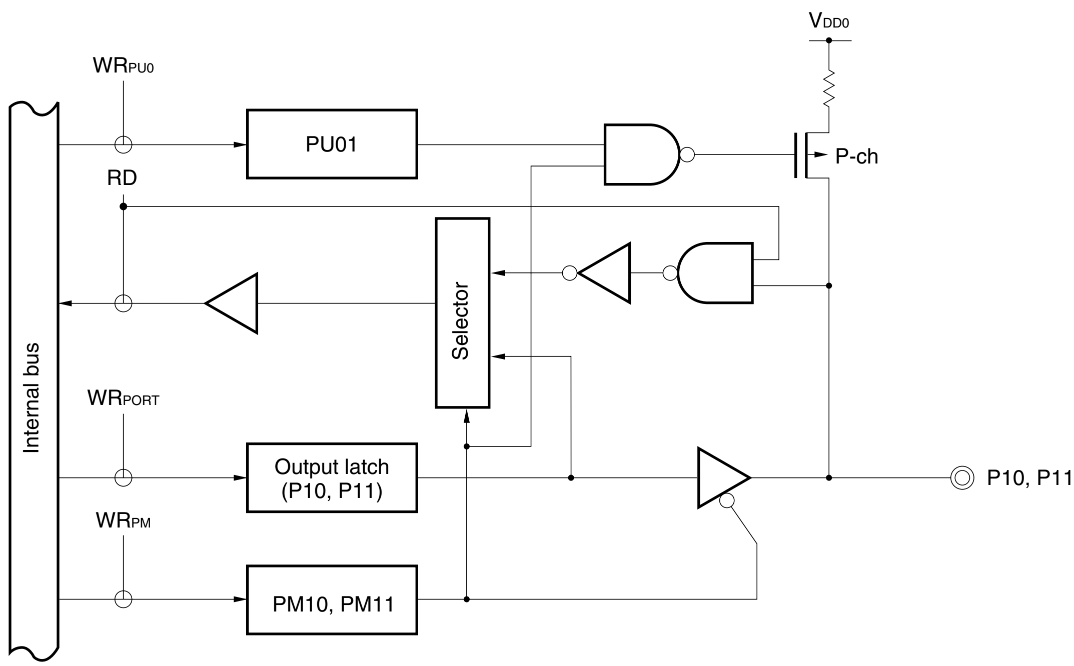
6.2.2 Port 1

This is a 2-bit I/O port with output latches. Port 1 can be set to input or output mode in 1-bit units by using the port mode register 1 (PM1). When the P10 and P11 pins are used as input port pins, on-chip pull-up resistors can be connected in 2-bit units by using pull-up resistor option register 0 (PU0).

$\overline{\text{RESET}}$ input sets port 1 to input mode.

Figure 6-3 shows a block diagram of port 1.

Figure 6-3. Block Diagram of P10 and P11



PU0: Pull-up resistor option register 0
PM: Port mode register
RD: Port 1 read signal
WR: Port 1 write signal

6.2.3 Port 2

This is a 7-bit I/O port with output latches. Port 2 can be set to input or output mode in 1-bit units by using port mode register 2 (PM2). For the P20 to P22, P25, and P26 pins, on-chip pull-up resistors can be connected in 1-bit units by using pull-up resistor option register B2 (PUB2).

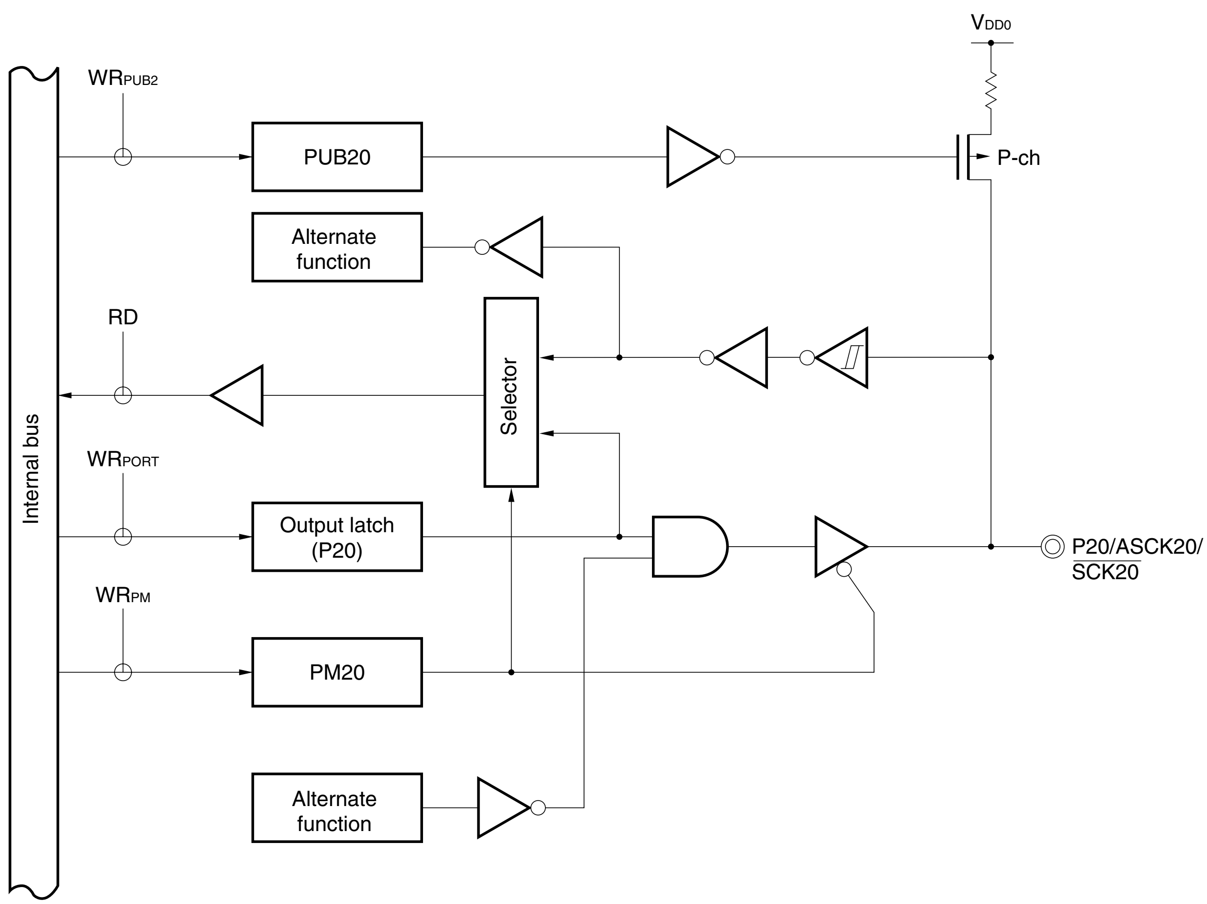
The port is also used as a data I/O and clock I/O to and from the serial interface, and as the timer I/O.

$\overline{\text{RESET}}$ input sets port 2 to input mode.

Figures 6-4 through 6-8 show block diagrams of port 2.

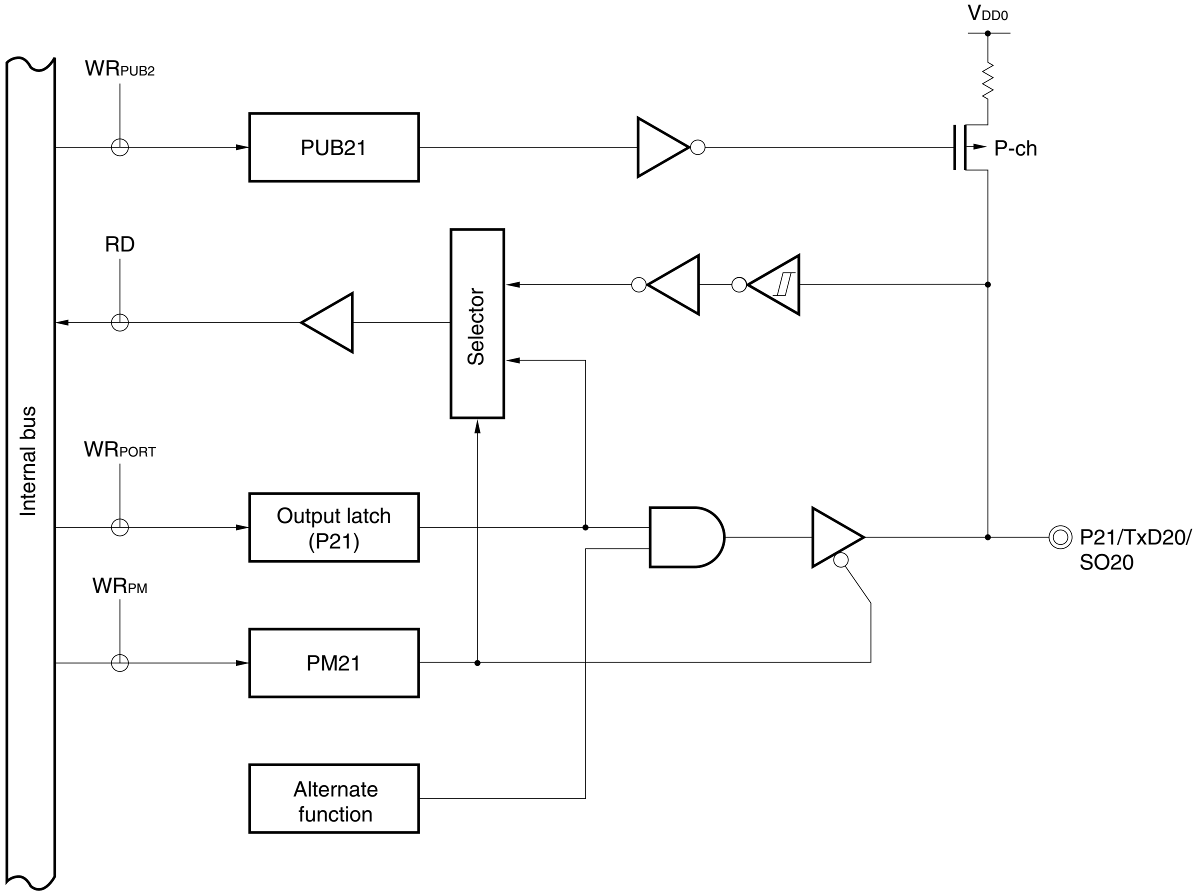
Caution When using the pins of port 2 as the serial interface, the I/O and output latches must be set according to the function to be used. For details of the settings, see Table 14-2 Operating Mode Settings of Serial Interface 20.

Figure 6-4. Block Diagram of P20



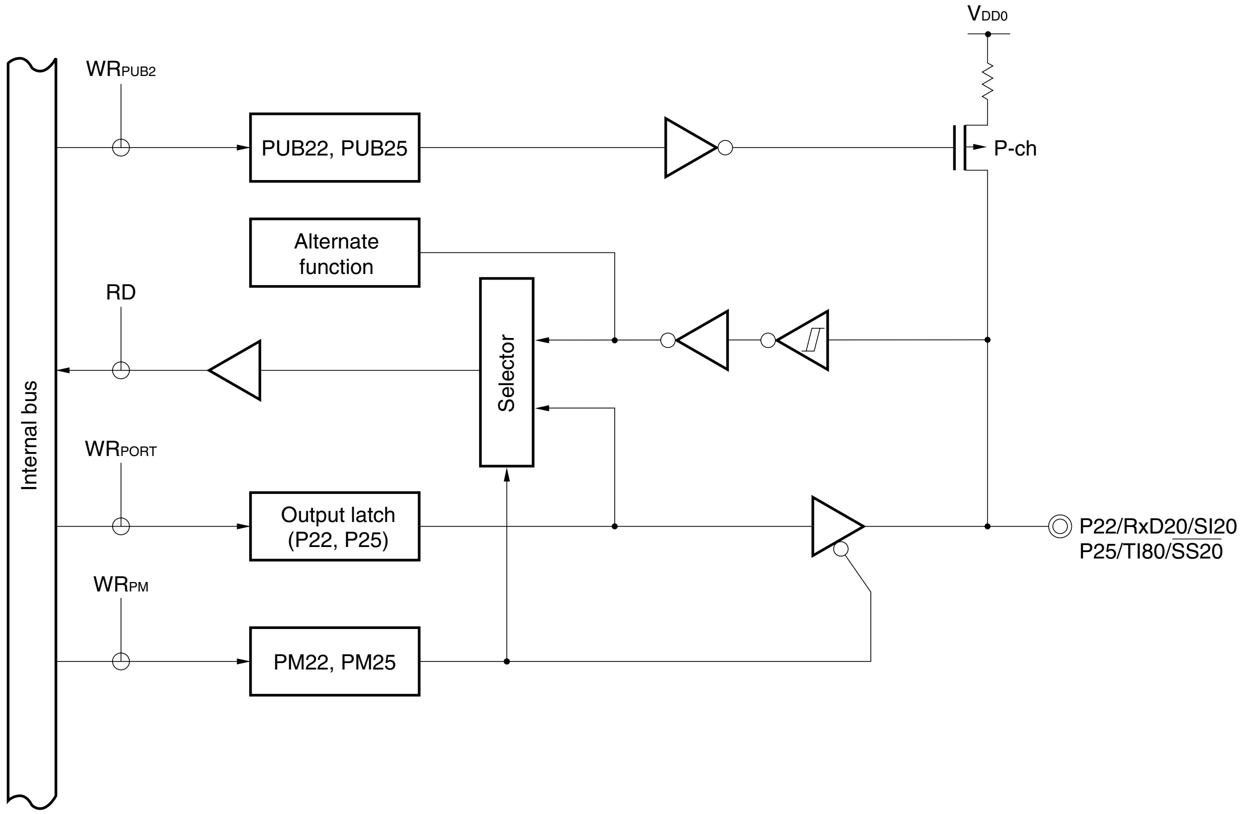
PUB2: Pull-up resistor option register B2
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

Figure 6-5. Block Diagram of P21



PUB2: Pull-up resistor option register B2
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

Figure 6-6. Block Diagram of P22 and P25



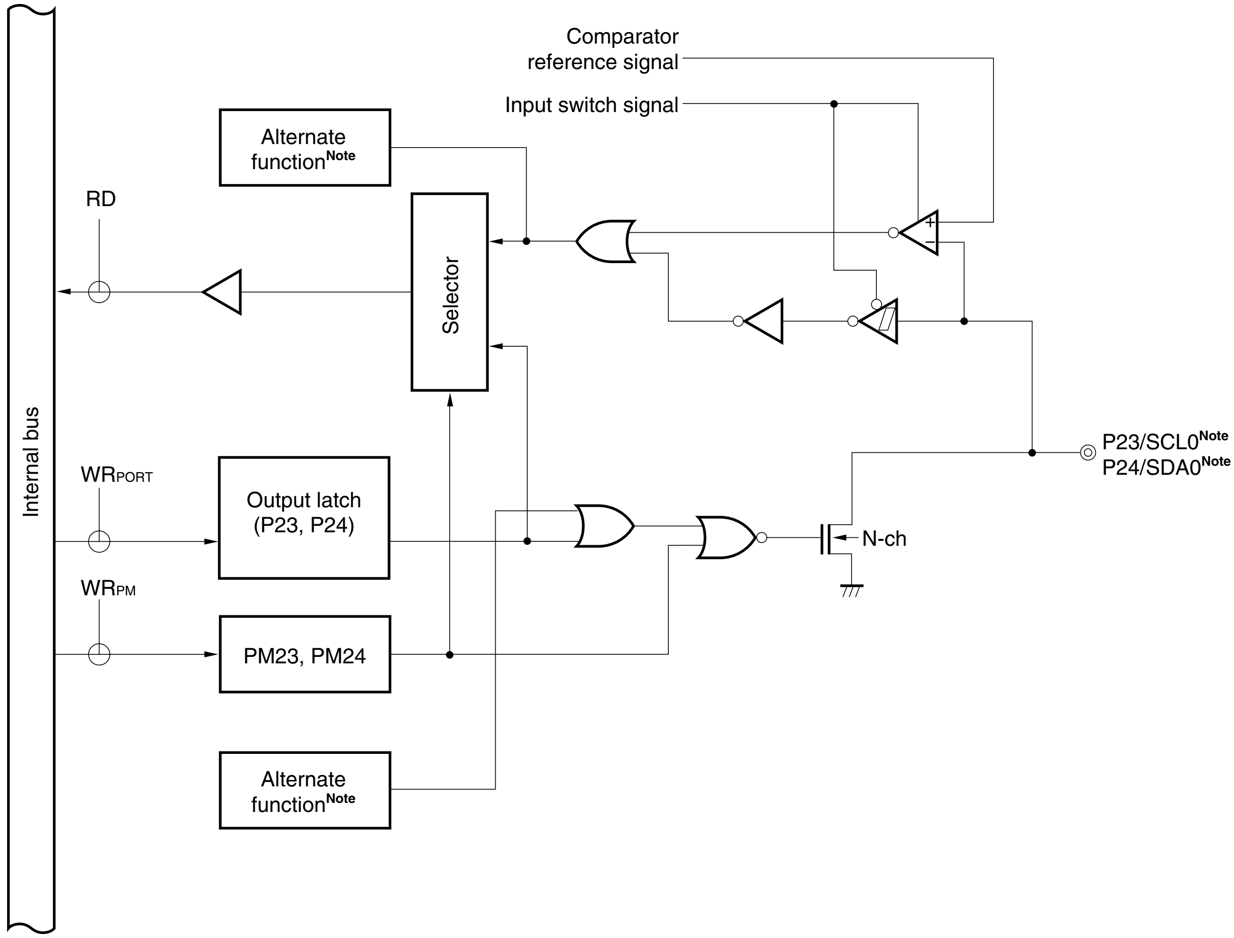
PUB2: Pull-up resistor option register B2

PM: Port mode register

RD: Port 2 read signal

WR: Port 2 write signal

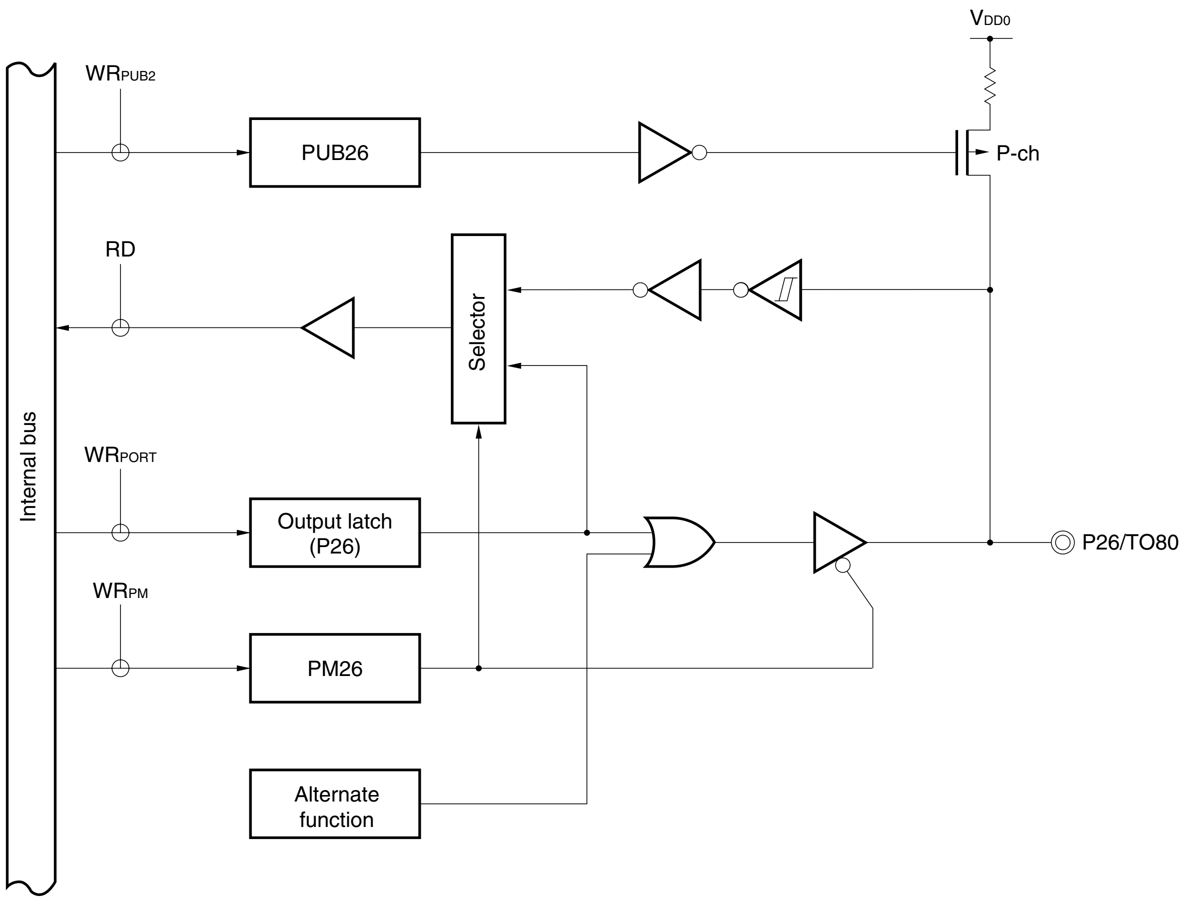
Figure 6-7. Block Diagram of P23 and P24



PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

Note This function is provided for the μPD789167Y and 789177Y Subseries only. For the μPD789167 and 789177 Subseries, P23 and P24 cannot be used as alternate-function pins.

Figure 6-8. Block Diagram of P26



PUB2: Pull-up resistor option register B2
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

6.2.4 Port 3

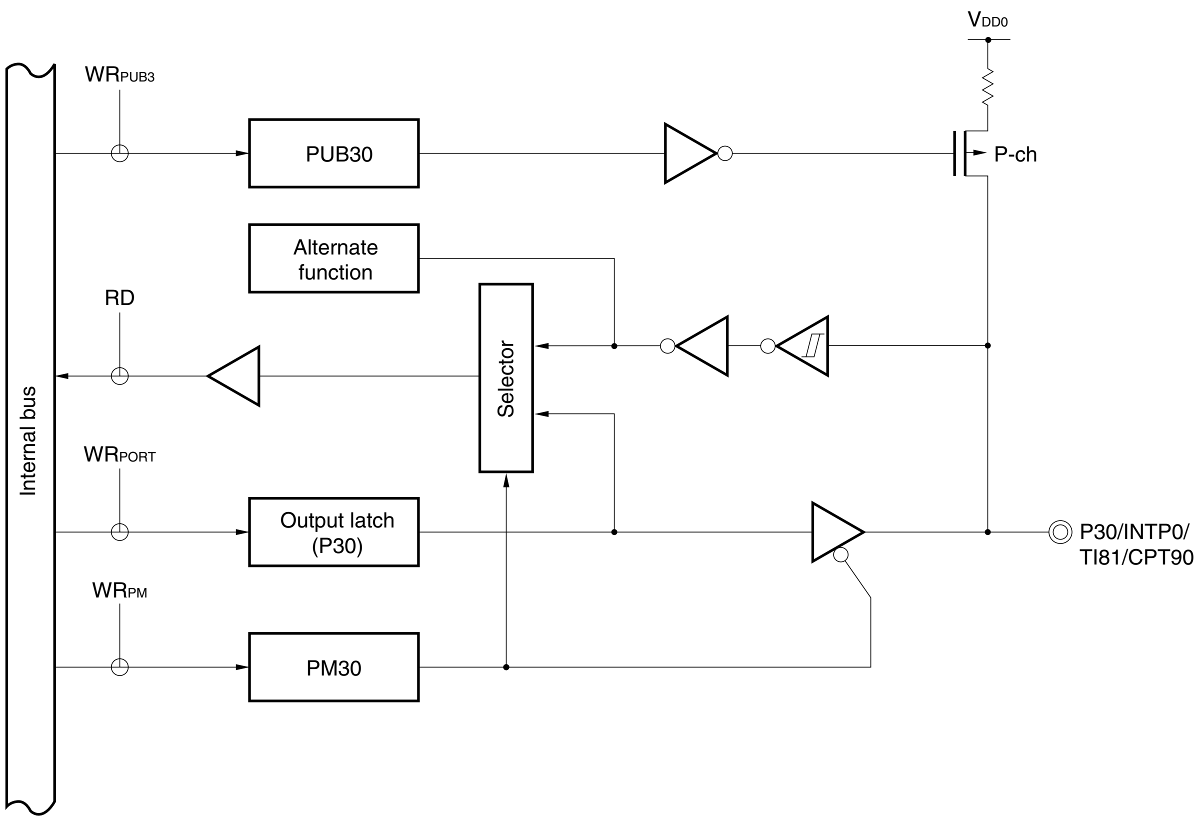
This is a 4-bit I/O port with output latches. Port 3 can be set to input or output mode in 1-bit units by using port mode register 3 (PM3). For the P30 to P33 pins, on-chip pull-up resistors can be connected in 1-bit units by using pull-up resistor option register B3 (PUB3).

The port is also used as an external interrupt input, capture input, timer output, and buzzer output.

$\overline{\text{RESET}}$ input sets port 3 to input mode.

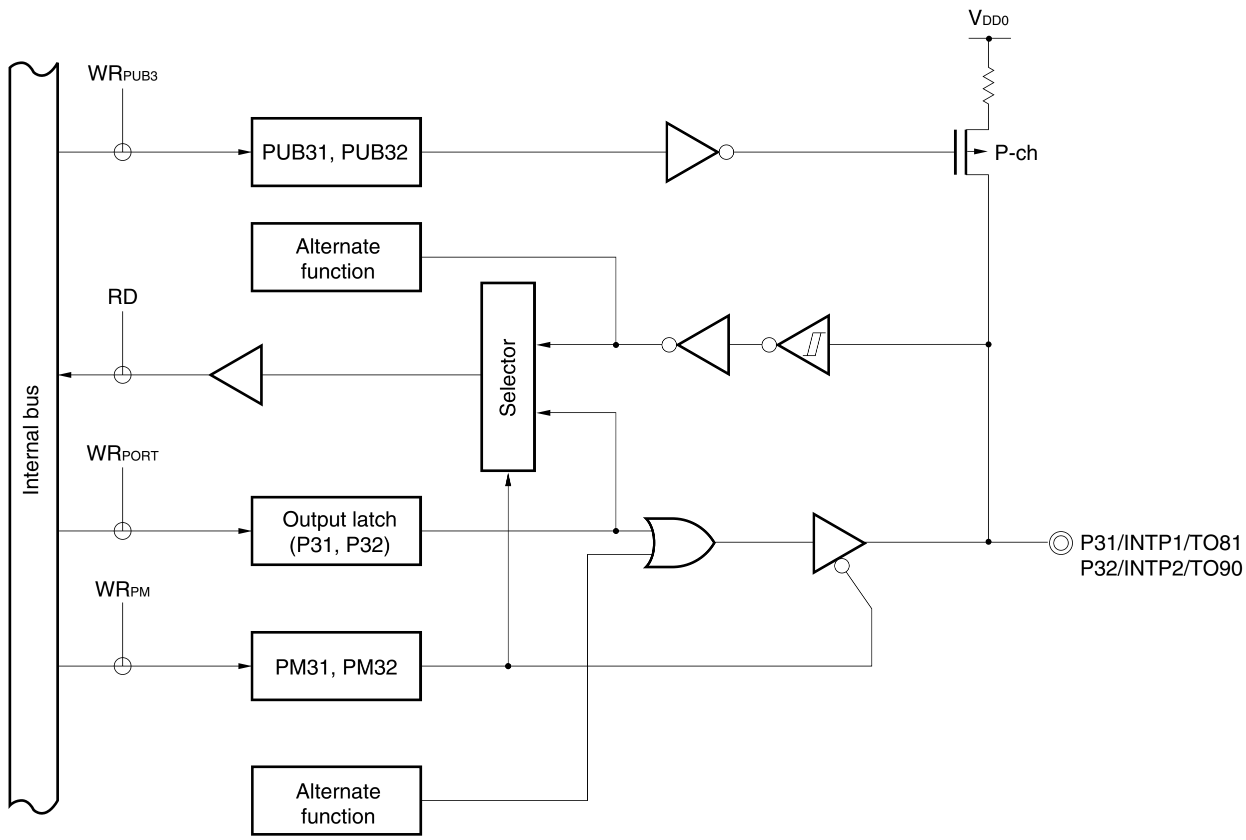
Figures 6-9 through 6-11 show block diagrams of port 3.

Figure 6-9. Block Diagram of P30



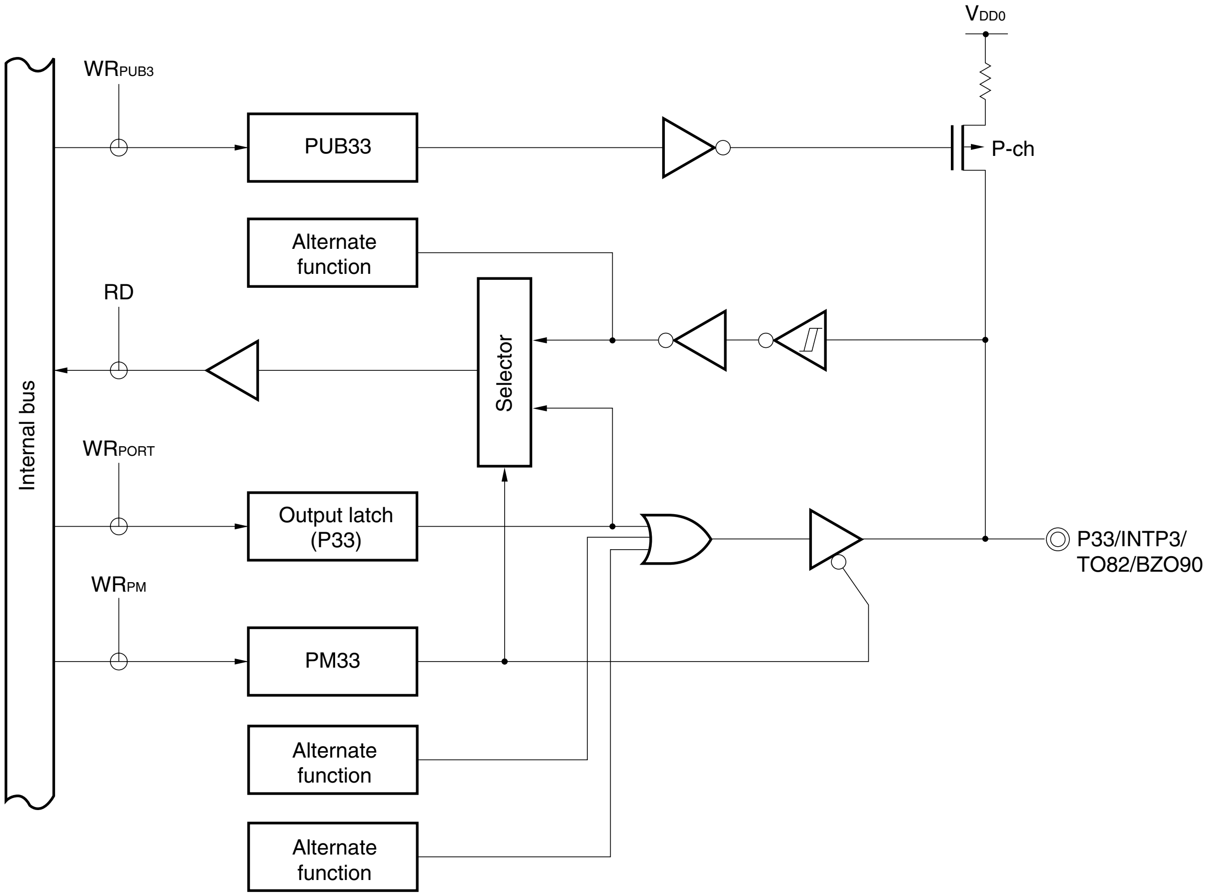
PUB3: Pull-up resistor option register B3
PM: Port mode register
RD: Port 3 read signal
WR: Port 3 write signal

Figure 6-10. Block Diagram of P31 and P32



PUB3: Pull-up resistor option register B3
PM: Port mode register
RD: Port 3 read signal
WR: Port 3 write signal

Figure 6-11. Block Diagram of P33



PUB3: Pull-up resistor option register B3

PM: Port mode register

RD: Port 3 read signal

WR: Port 3 write signal

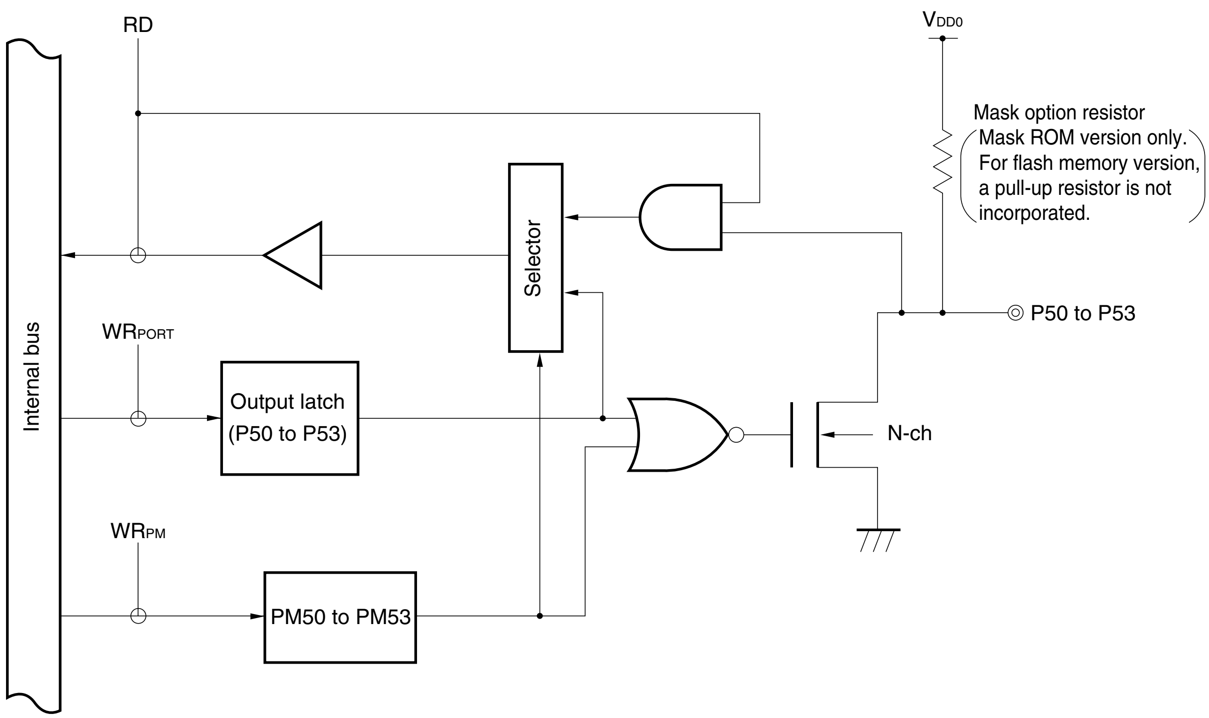
6.2.5 Port 5

This is a 4-bit N-ch open-drain I/O port with output latches. Port 5 can be set to input or output mode in 1-bit units by using port mode register 5 (PM5). For a mask ROM version, whether a pull-up resistor is to be incorporated can be specified by the mask option.

RESET input sets port 5 to input mode.

Figure 6-12 shows a block diagram of port 5.

Figure 6-12. Block Diagram of P50 to P53



PM: Port mode register
RD: Port 5 read signal
WR: Port 5 write signal

Caution When using port 5 of the μPD78F9177 and 78F9177Y as an input port, be sure to observe the restrictions listed below.

- **When V_{DD} = 1.8 to 5.5 V**
  Use within the range of T_A = 25 to 85°C
- **When T_A = –40 to 85°C**
  Use within the range of V_{DD} = 2.7 to 5.5 V
- **When T_A = –40 to 85°C and V_{DD} = 1.8 to 5.5 V**
  Issue three consecutive read instructions when reading port 5.

If the above restrictions are not observed, the input value may be read incorrectly.
Note, however, that these restrictions do not apply when port 5 pins are used as output pins, or when the product is other than the μPD78F9177 or 78F9177Y.

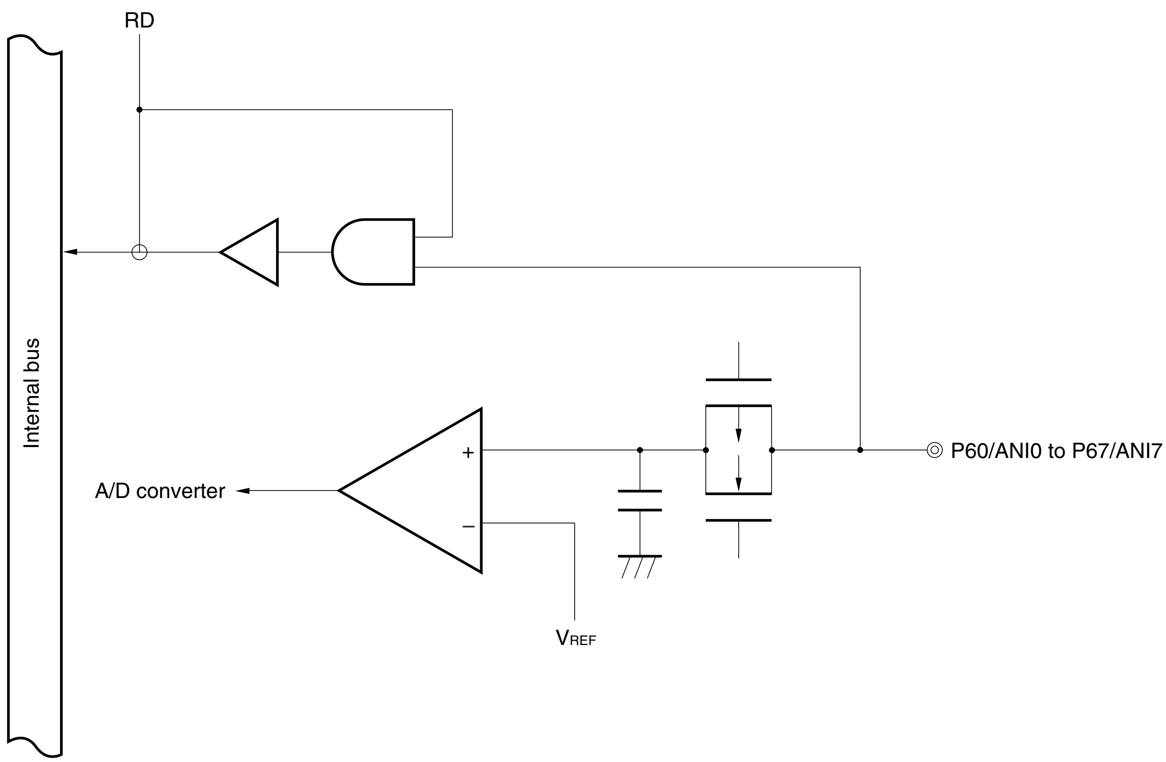
6.2.6 Port 6

This is an 8-bit input port.

The port is also used as an analog input to the A/D converter.

Figure 6-13 shows a block diagram of port 6.

Figure 6-13. Block Diagram of P60 to P67



6.3 Port Function Control Registers

The following two types of registers are used to control the ports.

- Port mode registers (PM0 to PM3, and PM5)
- Pull-up resistor option registers (PU0, PUB2, and PUB3)

(1) Port mode registers (PM0 to PM3, and PM5)

The port mode registers separately set each port bit to either input or output.

Each port mode register is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input writes FFH into the port mode registers.

When port pins are used for alternate functions, the corresponding port mode register and output latch must be set or reset as described in Table 6-3.

Caution When port 3 is acting as an output port and its output level is changed, an interrupt request flag is set, because this port is also used as the input for an external interrupt. To use port 3 in output mode, therefore, the interrupt mask flag must be set to 1 in advance.

Figure 6-14. Format of Port Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	1	PM05	PM04	PM03	PM02	PM01	PM00	FF20H	FFH	R/W
PM1	1	1	1	1	1	1	PM11	PM10	FF21H	FFH	R/W
PM2	1	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	1	1	1	1	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM5	1	1	1	1	PM53	PM52	PM51	PM50	FF25H	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 : n = 0 to 5, m = 1 : n = 0, 1; m = 2 : n = 0 to 6, m = 3 : n = 0 to 3; m = 5 : n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Table 6-3. Port Mode Register and Output Latch Settings for Using Alternate Functions

Pin Name	Alternate Function		PM××	P××
	Name	I/O		
P25	TI80	Input	1	×
P26	TO80	Output	0	0
P30	INTP0	Input	1	×
	TI81	Input	1	×
	CPT90	Input	1	×
P31	INTP1	Input	1	×
	TO81	Output	0	0
P32	INTP2	Input	1	×
	TO90	Output	0	0
P33	INTP3	Input	1	×
	TO82	Output	0	0
	BZO90	Output	0	0

Caution **When using the pins of port 2 as the serial interface, the I/O or output latch must be set according to the function to be used. For details of the settings, see Table 14-2 Operating Mode Settings of Serial Interface 20.**

Remark ×: don't care
PM××: Port mode register
P××: Port output latch

(2) Pull-up resistor option register 0 (PU0)

Pull-up resistor option register 0 (PU0) sets whether an on-chip pull-up resistor on each port is used. On the port which is specified to use the on-chip pull-up resistor in PU0, the pull-up resistor can be internally used only for the bits set to input mode. No on-chip pull-up resistors can be used for the bits set to output mode regardless of the setting of PU0. On-chip pull-up resistors cannot be used even when the pins are used as the alternate-function output pins.

PU0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears PU0 to 00H.

Figure 6-15. Format of Pull-up Resistor Option Register 0

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After reset	R/W
PU0	0	0	0	0	0	0	PU01	PU00	FFF7H	00H	R/W

PU0m	Pm on-chip pull-up resistor selection (m = 0, 1)
0	On-chip pull-up resistor not used
1	On-chip pull-up resistor used

Caution **Bits 2 to 7 must all be set to 0.**

(3) Pull-up resistor option registers B2 and B3 (PUB2 and PUB3)

These registers specify whether an on-chip pull-up resistor is connected to each pin of ports 2 and 3. The pin specified by PUB2 or PUB3 is connected to on-chip pull-up resistor regardless of the setting of the port mode register.

PUB2 and PUB3 are set with a 1-bit or 8-bit manipulation instruction.

$\overline{\text{RESET}}$ input clears this register to 00H.

Figure 6-16. Format of Pull-up Resistor Option Register B2

Symbol	7	<6>	<5>	4	3	<2>	<1>	<0>	Address	After reset	R/W
PUB2	0	PUB26	PUB25	0	0	PUB22	PUB21	PUB20	FF32H	00H	R/W

PUB2n	P2n on-chip pull-up resistor selection (n = 0 to 2, 5, 6)
0	On-chip pull-up resistor not used
1	On-chip pull-up resistor used

Caution Bits 3, 4, and 7 must all be set to 0.

Figure 6-17. Format of Pull-up Resistor Option Register B3

Symbol	7	6	5	4	<3>	<2>	<1>	<0>	Address	After reset	R/W
PUB3	0	0	0	0	PUB33	PUB32	PUB31	PUB30	FF33H	00H	R/W

PUB3n	P3n on-chip pull-up resistor selection (n = 0 to 3)
0	On-chip pull-up resistor not used
1	On-chip pull-up resistor used

Caution Bits 4 to 7 must all be set to 0.

6.4 Operation of Port Functions

The operation of a port differs depending on whether the port is set to input or output mode, as described below.

6.4.1 Writing to I/O port

(1) In output mode

A value can be written to the output latch of a port by using a transfer instruction. The contents of the output latch can be output from the pins of the port.

The data once written to the output latch is retained until new data is written to the output latch.

(2) In input mode

A value can be written to the output latch by using a transfer instruction. However, the status of the port pin is not changed because the output buffer is OFF.

The data once written to the output latch is retained until new data is written to the output latch.

Caution A 1-bit memory manipulation instruction is executed to manipulate 1 bit of a port. However, this instruction accesses the port in 8-bit units. When this instruction is executed to manipulate a bit of a port consisting both of inputs and outputs, therefore, the contents of the output latch of the pin that is set to input mode and not subject to manipulation become undefined.

6.4.2 Reading from I/O port

(1) In output mode

The contents of the output latch can be read by using a transfer instruction. The contents of the output latch are not changed.

(2) In input mode

The status of a pin can be read by using a transfer instruction. The contents of the output latch are not changed.

6.4.3 Arithmetic operation of I/O port

(1) In output mode

An arithmetic operation can be performed with the contents of the output latch. The result of the operation is written to the output latch. The contents of the output latch are output from the port pins.

The data once written to the output latch is retained until new data is written to the output latch.

(2) In input mode

The contents of the output latch become undefined. However, the status of the pin is not changed because the output buffer is OFF.

Caution A 1-bit memory manipulation instruction is executed to manipulate 1 bit of a port. However, this instruction accesses the port in 8-bit units. When this instruction is executed to manipulate a bit of a port consisting both of inputs and outputs, therefore, the contents of the output latch of the pin that is set to input mode and not subject to manipulation become undefined.

CHAPTER 7 CLOCK GENERATOR

7.1 Clock Generator Functions

The clock generator generates the clock to be supplied to the CPU and peripheral hardware. The following two types of system clock oscillators are used.

- **Main system clock oscillator**
  <Expanded-specification products>
  This circuit oscillates at 1.0 to 10.0 MHz. Oscillation can be stopped by executing the STOP instruction or setting the processor clock control register (PCC).
  <Conventional products>
  This circuit oscillates at 1.0 to 5.0 MHz. Oscillation can be stopped by executing the STOP instruction or setting the processor clock control register (PCC).
- **Subsystem clock oscillator**
  This circuit oscillates at 32.768 kHz. Oscillation can be stopped by setting the suboscillation mode register (SCKM).

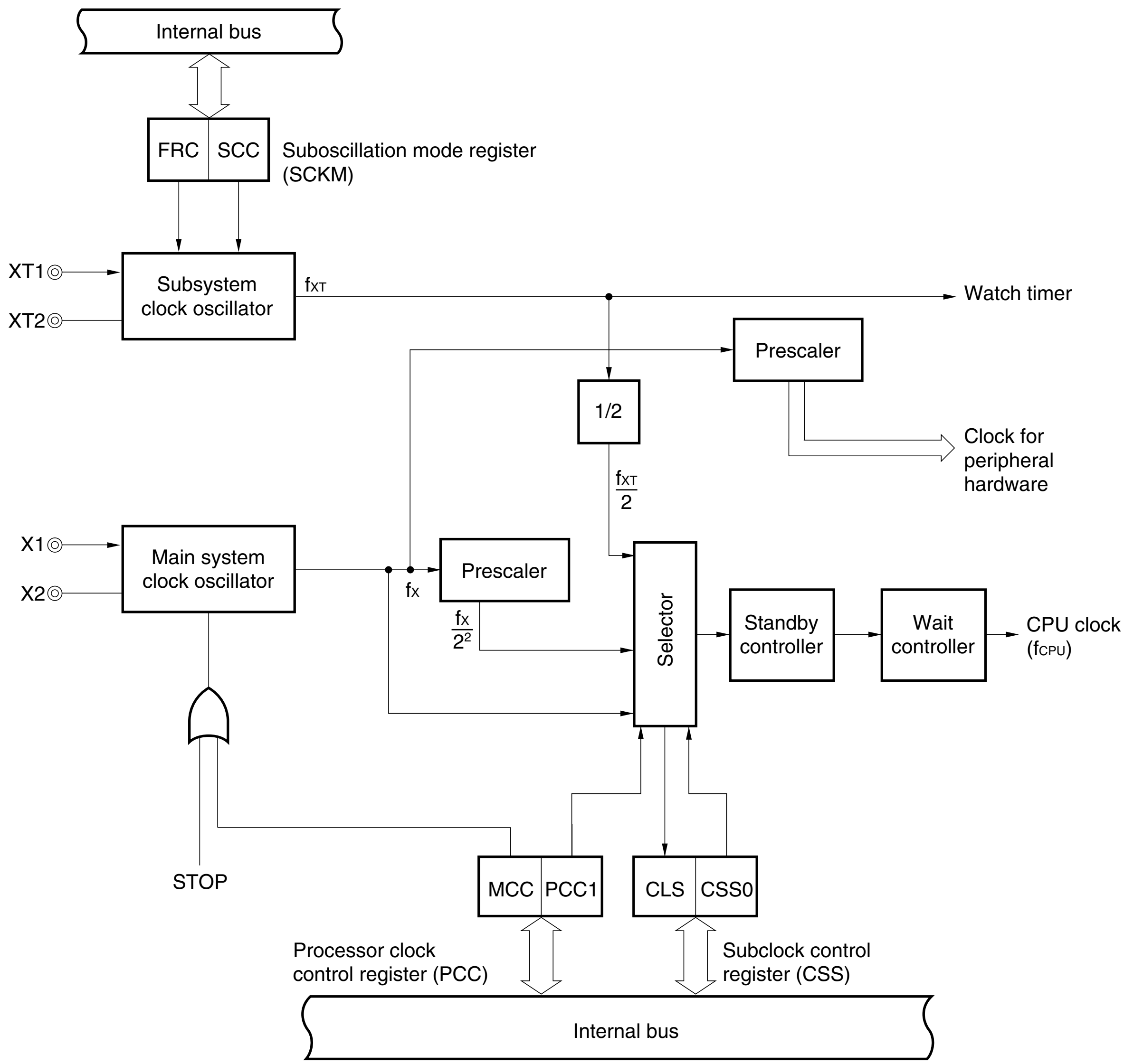
7.2 Clock Generator Configuration

The clock generator consists of the following items of hardware.

Table 7-1. Configuration of Clock Generator

Item	Configuration
Control registers	Processor clock control register (PCC) Suboscillation mode register (SCKM) Subclock control register (CSS)
Oscillator	Main system clock oscillator Subsystem clock oscillator

Figure 7-1. Block Diagram of Clock Generator



7.3 Registers Controlling Clock Generator

The clock generator is controlled by the following registers.

- Processor clock control register (PCC)
- Suboscillation mode register (SCKM)
- Subclock control register (CSS)

(1) Processor clock control register (PCC)

PCC selects the CPU clock and the ratio of division.
PCC is set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input sets PCC to 02H.

Figure 7-2. Format of Processor Clock Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PCC	MCC	0	0	0	0	0	PCC1	0	FFFBH	02H	R/W

MCC	Control of main system clock oscillator operation
0	Operation enabled
1	Operation disabled

CSS0	PCC1	CPU clock (f_{CPU}) selection[Note 1]	Minimum instruction execution time: $2/f_{CPU}$	
			At f_X = 10.0 MHz[Note 2] or f_{XT} = 32.768 kHz operation	At f_X = 5.0 MHz or f_{XT} = 32.768 kHz operation
0	0	f_X	0.2 μs	0.4 μs
0	1	$f_X/2^2$	0.8 μs	1.6 μs
1	0	$f_{XT}/2$	122 μs	122 μs
1	1			

Notes 1. The CPU clock is selected according to a combination of the PCC1 flag in the processor clock control register (PCC) and the CSS0 flag in the subclock control register (CSS). See **7.3 (3) Subclock control register (CSS)**.

2. Expanded-specification products only.

Cautions 1. Bits 0 and 2 to 6 must all be set to 0.

2. MCC can be set only when the subsystem clock has been selected as the CPU clock.

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

(2) Suboscillation mode register (SCKM)

SCKM specifies whether to use a feedback resistor for the subsystem clock, and controls the oscillation of the clock.

SCKM is set with a 1-bit or 8-bit memory manipulation instruction.

RESET input clears SCKM to 00H.

Figure 7-3. Format of Suboscillation Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
SCKM	0	0	0	0	0	0	FRC	SCC	FFF0H	00H	R/W

FRC	Use of feedback resistor[Note]
0	On-chip feedback resistor used
1	On-chip feedback resistor not used

SCC	Control of subsystem clock oscillator operation
0	Operation enabled
1	Operation disabled

Note The feedback resistor is necessary to adjust the bias point of the oscillation waveform to close to the mid point of the supply voltage. Only when the subclock is not used, the power consumption in STOP mode can be further reduced by setting FRC = 1.

Caution Bits 2 to 7 must all be set to 0.

(3) Subclock control register (CSS)

CSS specifies whether the main system or subsystem clock oscillator is to be used. It also specifies how the CPU clock operates.

CSS is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSS to 00H.

Figure 7-4. Format of Subclock Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
CSS	0	0	CLS	CSS0	0	0	0	0	FFF2H	00H	R/W[Note]

CLS	CPU clock operation status
0	Operation based on the (divided) main system clock
1	Operation based on the subsystem clock

CSS0	Selection of main system or subsystem clock oscillator
0	(Divided) output from the main system clock oscillator
1	Output form the subsystem clock oscillator

Note Bit 5 is read-only.

Caution Bits 0 to 3, 6, and 7 must all be set to 0.

7.4 System Clock Oscillators

7.4.1 Main system clock oscillator

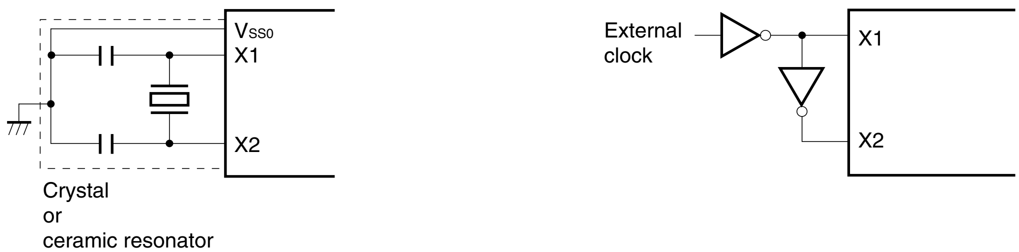
The main system clock oscillator is oscillated by the crystal or ceramic resonator (5.0 MHz TYP.) connected across the X1 and X2 pins.

An external clock can also be input to the circuit. In this case, input the clock signal to the X1 pin, and input the reversed signal to the X2 pin.

Figure 7-5 shows the external circuit of the main system clock oscillator.

Figure 7-5. External Circuit of Main System Clock Oscillator

(a) Crystal or ceramic oscillation **(b) External clock**



Caution When using the main system or subsystem clock oscillator, wire in the area enclosed by the broken lines in Figures 7-5 and 7-6 as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

7.4.2 Subsystem clock oscillator

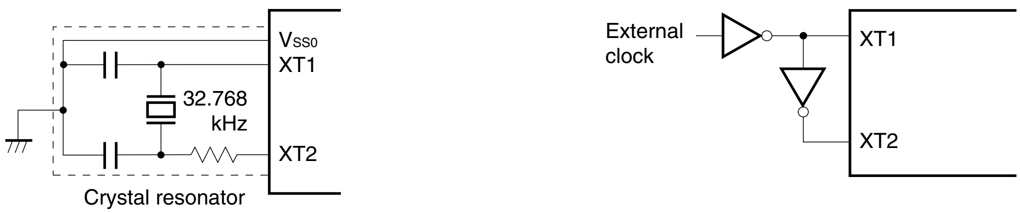
The subsystem clock oscillator is oscillated by the crystal resonator (32.768 kHz TYP.) connected across the XT1 and XT2 pins.

An external clock can also be input to the circuit. In this case, input the clock signal to the XT1 pin, and input the inverted signal to the XT2 pin.

Figure 7-6 shows the external circuit of the subsystem clock oscillator.

Figure 7-6. External Circuit of Subsystem Clock Oscillator

(a) Crystal oscillation **(b) External clock**



Caution When using the main system or subsystem clock oscillator, wire in the area enclosed by the broken lines in Figures 7-5 and 7-6 as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

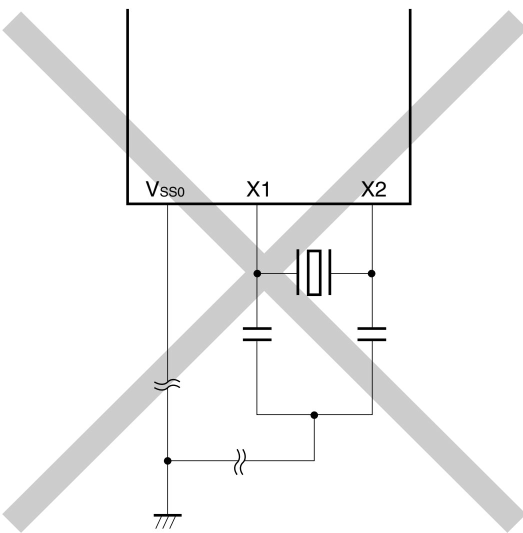
The subsystem clock oscillator is designed as low-amplitude circuit for reducing current consumption. Particular care is therefore required with the wiring method when the subsystem clock is used.

7.4.3 Examples of incorrect oscillator connection

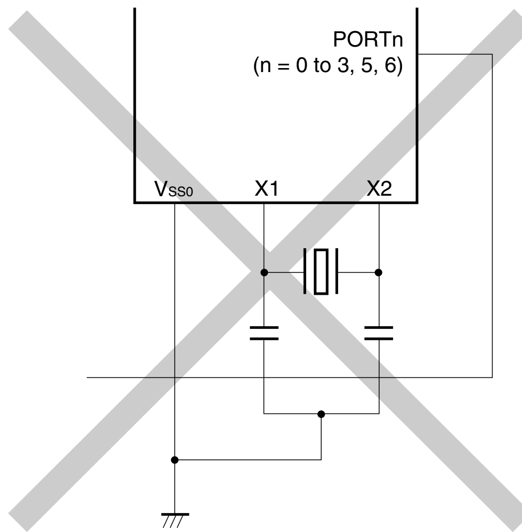
Figure 7-7 shows examples of incorrect oscillator connections.

Figure 7-7. Examples of Incorrect Oscillator Connection (1/2)

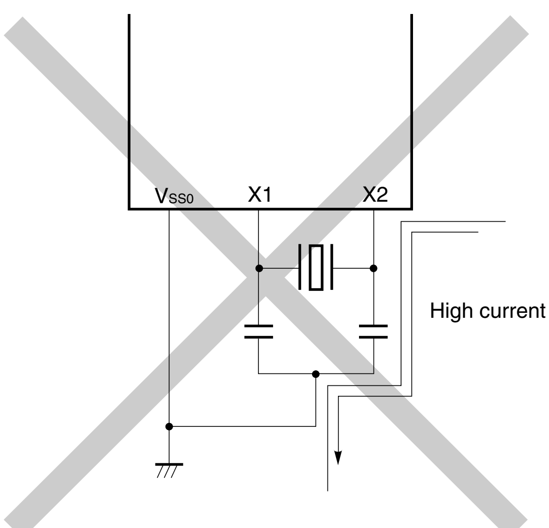
(a) Wiring too long



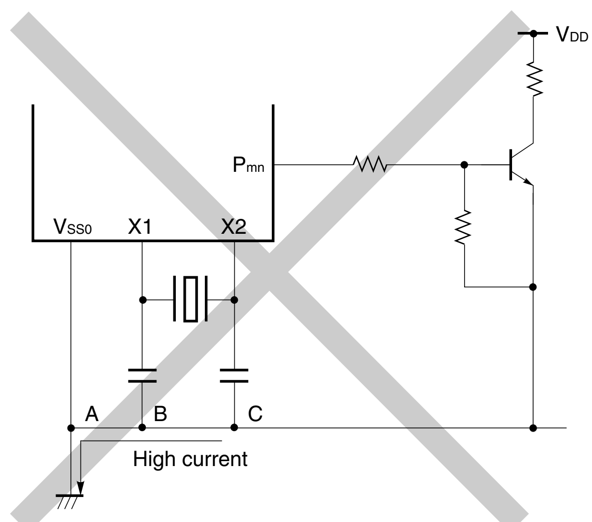
(b) Crossed signal line



(c) Wiring near high alternating current



(d) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)

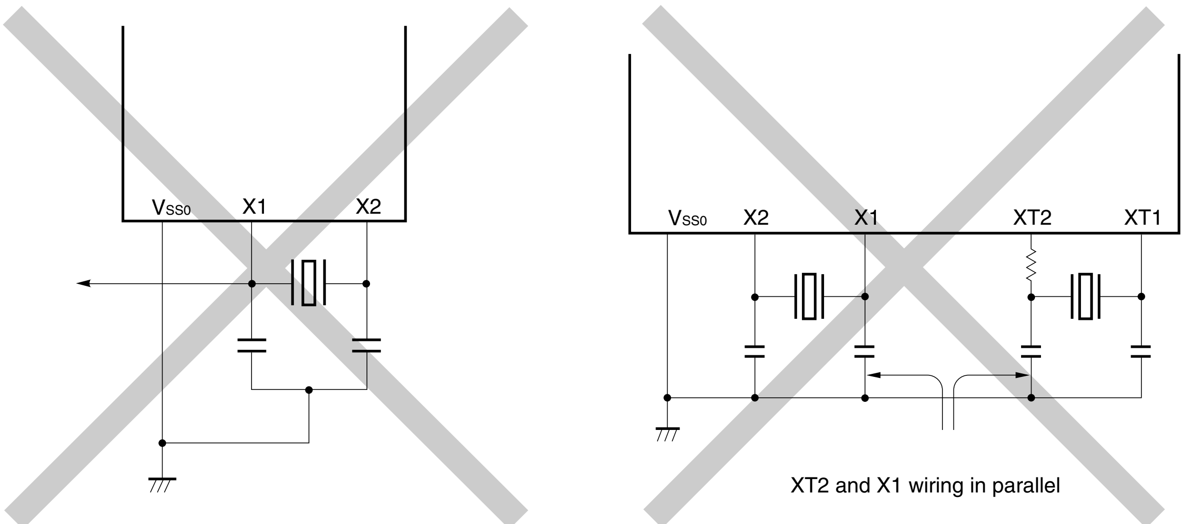


Remark When using the subsystem clock, read X1 and X2 as XT1 and XT2, respectively, and connect a resistor to the XT2 pin in series.

Figure 7-7. Examples of Incorrect Oscillator Connection (2/2)

(e) Signals are fetched

(f) Signal conductors of the main and subsystem clocks are parallel and near to each other



Remark When using the subsystem clock, read X1 and X2 as XT1 and XT2, respectively, and connect a resistor to the XT2 pin in series.

Caution If the X1 wire is in parallel with the XT2 wire, crosstalk noise may occur between the X1 and XT2, resulting in a malfunction.
To avoid this, do not lay the X1 and XT2 wires in parallel.

7.4.4 Scaler

The scaler divides the main system clock oscillator output (fx) and generates clocks.

7.4.5 When no subsystem clocks are used

If it is not necessary to use subsystem clocks for low power consumption operations and watch operations, connect the XT1 and XT2 pins as follows.

XT1: Connect to V_{SS0} or V_{SS1}
XT2: Open

In this state, however, some current may leak via the internal feedback resistor of the subsystem clock oscillator when the main system clock stops. To minimize the leakage current, the internal feedback resistor can be removed by setting bit 1 (FRC) of the suboscillation mode register (SCKM). In this case, also connect the XT1 and XT2 pins as described above.

7.5 Clock Generator Operation

The clock generator generates the following clocks and controls operation modes of the CPU, such as standby mode.

- Main system clock f_X
- Subsystem clock f_{XT}
- CPU clock f_{CPU}
- Clock to peripheral hardware

The operation of the clock generator is determined by the processor clock control register (PCC), suboscillation mode register (SCKM), and subclock control register (CSS), as follows.

(a) The slow mode (0.8 μs: at 10.0 MHz operation) of the main system clock is selected when the $\overline{\text{RESET}}$ signal is generated (PCC = 02H). While a low level is input to the $\overline{\text{RESET}}$ pin, oscillation of the main system clock is stopped.

(b) Three types of minimum instruction execution time (0.2 μs and 0.8 μs: main system clock (at 10.0 MHz operation), 122 μs: subsystem clock (at 32.768 kHz operation)) can be selected by the PCC, SCKM, and CSS settings.

(c) Two standby modes, STOP and HALT, can be used with the main system clock selected. In a system where no subsystem clock is used, setting bit 1 (FRC) of SCKM so that the built-in feedback resistor cannot be used reduces current drain during STOP mode. In a system where a subsystem clock is used, setting the SCKM bit 0 to 1 can cause the subsystem clock to stop oscillation.

(d) CSS bit 4 (CSS0) can be used to select the subsystem clock so that a low current operation operation is used (122 μs: at 32.768 kHz operation).

(e) With the subsystem clock selected, it is possible to cause the main system clock to stop oscillating by using bit 7 (MCC) of PCC. HALT mode can be used, but STOP mode cannot.

(f) The clock for the peripheral hardware is generated by dividing the frequency of the main system clock. The subsystem clock is supplied to 16-bit timer 90, 8-bit timer 82, and the watch timer only. So, even in standby mode, 16-bit timer 90, 8-bit timer 82, and the watch function can continue operating. The other hardware stops when the main system clock stops, because it operates based on the main system clock (except for an external clock).

7.6 Changing Setting of System Clock and CPU Clock

7.6.1 Time required for switching between system clock and CPU clock

The CPU clock can be selected by using bit 1 (PCC1) of the processor clock control register (PCC) and bit 4 (CSS0) of the subclock control register (CSS).

Actually, the specified clock is not selected immediately after the setting of PCC has been changed, and the old clock is used for the duration of several instructions after that (see **Table 7-2**).

Table 7-2. Maximum Time Required for Switching CPU Clock

Set Value Before Switching		Set Value After Switching					
CSS0	PCC1	CSS0	PCC1	CSS0	PCC1	CSS0	PCC1
		0	0	0	1	1	×
0	0			4 clocks		$2f_X/f_{XT}$ clocks (612 clocks)[306 clocks]	
	1	2 clocks				$f_X/2f_{XT}$ clocks (152 clocks)[76 clocks]	
1	×	2 clocks		2 clocks			

Remarks 1. Two clocks are the minimum instruction execution time of the CPU clock before switching.

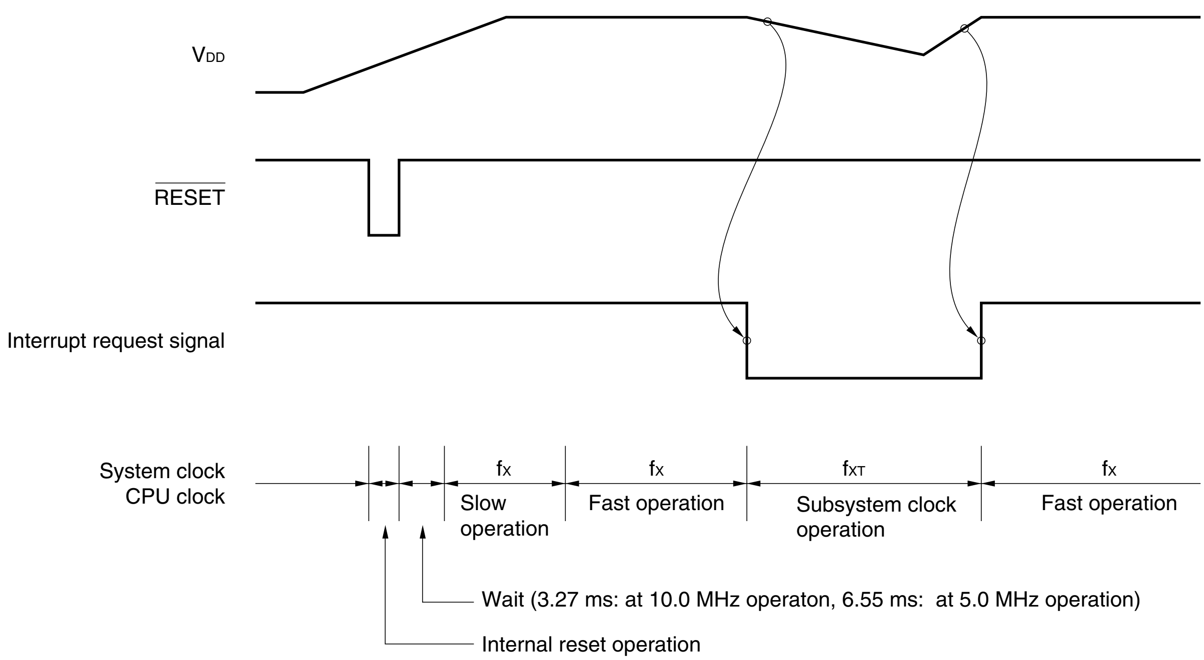
2. The values in paraentheses ( ) apply to operation at f_X = 10.0 MHz or f_{XT} = 32.768 kHz.
The values in brackets [ ] apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

3. ×: don't care

7.6.2 Switching between system clock and CPU clock

The following figure illustrates how the CPU clock and system clock switch.

Figure 7-8. Switching Between System Clock and CPU Clock



<1> The CPU is reset when the $\overline{\text{RESET}}$ pin is made low on power application. The effect of resetting is released when the $\overline{\text{RESET}}$ pin is later made high, and the main system clock starts oscillating. At this time, the time during which oscillation stabilizes (2^{15}/fx) is automatically secured.
After that, the CPU starts instruction execution at the slow speed of the main system clock (0.8 μs: at 10.0 MHz operation).

<2> After the time required for the V_{DD} voltage to rise to the level at which the CPU can operate at the high speed has elapsed, bit 1 (PCC1) of the processor clock control register (PCC) and bit 4 (CSS0) of the subclock control register (CSS0) are rewritten so that the high speed operation can be selected.

<3> When a drop of the V_{DD} voltage is detected with an interrupt request signal, the clock is switched to the subsystem clock. (At this moment, the subsystem clock must be in the oscillation stabilized status.)

<4> When a recover of the V_{DD} voltage is detected with an interrupt request signal, bit 7 (MCC) of PCC is set to 0 to make the main system clock start oscillating. After the time required for the oscillation to stabilize has elapsed, PCC1 and CSS0 are rewritten so that high-speed operation can be selected again.

Caution When the main system clock is stopped and the subsystem clock is operating, allow sufficient time for the oscillation to stabilize by coding the program before switching again from the subsystem clock to the main system clock.

CHAPTER 8 16-BIT TIMER 90

8.1 16-Bit Timer 90 Functions

16-bit timer 90 has the following functions.

- Timer interrupt
- Timer output
- Buzzer output
- Count value capture

(1) Timer interrupt
An interrupt is generated when a count value and compare value matches.

(2) Timer output
Timer output can be controlled when a count value and compare value matches.

(3) Buzzer output
Buzzer output can be controlled by software.

(4) Count value capture
The count value of 16-bit timer counter 90 (TM90) is latched into the capture register in synchronization with the capture trigger and retained.

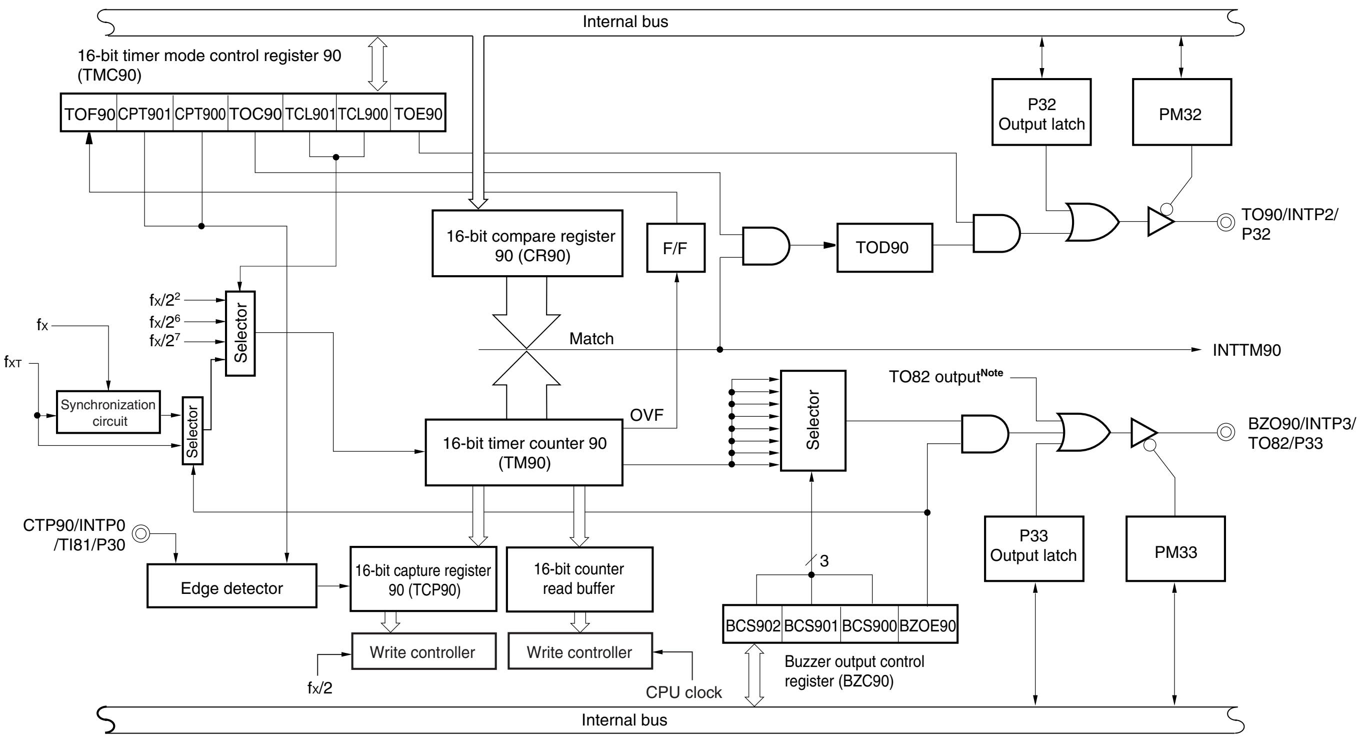
8.2 16-Bit Timer 90 Configuration

16-bit timer 90 consists of the following hardware.

Table 8-1. Configuration of 16-Bit Timer 90

Item	Configuration
Timer counter	16 bits × 1 (TM90)
Registers	Compare register: 16 bits × 1 (CR90) Capture register: 16 bits × 1 (TCP90)
Timer outputs	1 (TO90)
Control registers	16-bit timer mode control register 90 (TMC90) Buzzer output control register 90 (BZC90) Port mode register 3 (PM3)

Figure 8-1. Block Diagram of 16-Bit Timer 90



Note See **Figure 9-3 Block Diagram of 8-Bit Timer 82**.

(1) 16-bit compare register 90 (CR90)

The value specified in CR90 is compared with the count in 16-bit timer register 90 (TM90). If they match, an interrupt request (INTTM90) is issued by CR90.

CR90 is set with an 8-bit or 16-bit memory manipulation instruction. Any value from 0000H to FFFFH can be set.

$\overline{\text{RESET}}$ input sets CR90 to FFFFH.

Cautions 1. CR90 is designed to be manipulated with a 16-bit memory manipulation instruction. It can also be manipulated with 8-bit memory manipulation instructions, however. When an 8-bit memory manipulation instruction is used to set CR90, it must be accessed using direct addressing.

2. To re-set CR90 during a count operation, it is necessary to disable interrupts in advance, using interrupt mask flag register 1 (MK1). It is also necessary to disable inversion of the timer output data, using 16-bit timer mode control register 90 (TMC90). If the value in CR90 is rewritten in the interrupt-enabled state, an interrupt request may occur at the moment of rewrite.

(2) 16-bit timer counter 90 (TM90)

TM90 is used to count the number of pulses.

The contents of TM90 are read with an 8-bit or 16-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TM90 to 0000H.

Cautions 1. The count becomes undefined when STOP mode is released, because the count operation is performed during the oscillation stabilization time.

2. TM90 is designed to be manipulated with a 16-bit memory manipulation instruction. It can also be manipulated with 8-bit memory manipulation instructions, however. When an 8-bit memory instruction is used to manipulate TM90, it must be accessed using direct addressing.

3. When an 8-bit memory manipulation instruction is used to manipulate TM90, the lower and higher bytes must be read as a pair, in this order.

(3) 16-bit capture register 90 (TCP90)

TCP90 captures the contents of TM90.

It is set with an 8-bit or 16-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes TCP90 undefined.

Caution TCP90 is designed to be manipulated with a 16-bit memory manipulation instruction. It can also be manipulated with 8-bit memory manipulation instructions, however. When an 8-bit memory manipulation instruction is used to manipulate TCP90, it must be accessed using direct addressing.

(4) 16-bit counter read buffer 90

This buffer is used to latch and hold the count for TM90.

8.3 Registers Controlling 16-Bit Timer 90

The following three registers control 16-bit timer 90.

- 16-bit timer mode control register 90 (TMC90)
- Buzzer output control register 90 (BZC90)
- Port mode register 3 (PM3)

(1) 16-bit timer mode control register 90 (TMC90)

16-bit timer mode control register 90 (TMC90) controls the setting of the count clock, capture edge, etc.
TMC90 is set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears TMC90 to 00H.

Figure 8-2. Format of 16-Bit Timer Mode Control Register 90

Symbol	7	<6>	5	4	3	2	1	<0>	Address	After reset	R/W
TMC90	TOD90	TOF90	CPT901	CPT900	TOC90	TCL901	TCL900	TOE90	FF48H	00H	R/W[Note 1]

TOD90	Timer output data
0	Timer output of 0
1	Timer output of 1

TOF90	Overflow flag control
0	Reset or cleared by software
1	Set when the 16-bit timer overflows

CPT901	CPT900	Capture edge selection
0	0	Capture operation disabled
0	1	Captured at the rising edge of the CPT90 pin
1	0	Captured at the falling edge of the CPT90 pin
1	1	Captured at both the rising and falling edges of the CPT90 pin

TOC90	Timer output data inversion control
0	Inversion disabled
1	Inversion enabled

TCL901	TCL900	16-bit time counter 90 count clock (fcl) section		
			At f_X = 10.0 MHz[Note 2] or f_{XT} = 32.768 kHz operation	At f_X = 5.0 MHz or f_{XT} = 32.768 kHz operation
0	0	$f_X/2^2$	2.5 MHz	1.25 MHz
0	1	$f_X/2^6$	156 kHz	78.1 kHz
1	0	$f_X/2^7$	78.1 kHz	39.1 kHz
1	1	f_{XT}	32.768 kHz	

TOE90	16-bit timer counter 90 output control
0	Output disabled (port mode)
1	Output enabled

Notes 1. Bit 7 is read-only.

2. Expanded-specification products only.

Caution **Disable interrupts in advance by using the interrupt mask flag register (MK1) to change the data of TCL901 and TCL900. Also, prevent the timer output data from being inverted by setting TOC90 to 1.**

Remarks 1. fX: Main system clock oscillation frequency
2. fXT: Subsystem clock oscillation frequency

(2) Buzzer output control register 90 (BZC90)

This register selects the buzzer frequency based on fcl selected with the count clock select bits (TCL901 and TCL900), and controls the output of a square wave.

BZC90 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears BZC90 to 00H.

Figure 8-3. Format of Buzzer Output Control Register 90

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
BZC90	0	0	0	0	BCS902	BCS901	BCS900	BZOE90	FF49H	00H	R/W Note 1

BCS902	BCS901	BCS900	Buzzer frequency selection
0	0	0	$fcl/2^4$
0	0	1	$fcl/2^5$
0	1	0	$fcl/2^8$
0	1	1	$fcl/2^9$
1	0	0	$fcl/2^{10}$
1	0	1	$fcl/2^{11}$
1	1	0	$fcl/2^{12}$
1	1	1	$fcl/2^{13}$

BZOE90	Buzzer port output control
0	Disable buzzer port output.
1	Enable buzzer port output. Note 2

Notes 1. Bits 4 to 7 must all be set to 0.
2. When setting BZOE90 to 1, TOE82 must be set to 0. (See **Figure 9-6 Format of 8-Bit Timer Mode Control Register 82**.)

Caution If the subclock is selected as the count clock (TCL901 = 1, TCL900 = 1: see Figure 8-2 Format of 16-Bit Timer Mode Control Register 90), the subclock is not synchronized when buzzer port output is enabled. In this case, the capture function and TM90 read function are disabled. In addition, the count value of TM90 is undefined.

Table 8-2. Buzzer Frequency of 16-Bit Timer 90

BCS902	BCS901	BCS900	Buzzer Frequency						
			At fX = 10.0 MHz[Note] operation			At fX = 5.0 MHz operation			At fXT = 32.768 kHz operation
			fcl = fX/2^2	fcl = fX/2^6	fcl = fX/2^7	fcl = fX/2^2	fcl = fX/2^6	fcl = fX/2^7	fcl = fXT
0	0	0	156 kHz	9.76 kHz	4.88 kHz	78.1 kHz	4.88 kHz	2.44 kHz	2.05 kHz
0	0	1	78.1 kHz	4.88 kHz	2.44 kHz	39.1 kHz	2.44 kHz	1.22 kHz	1.02 kHz
0	1	0	9.76 kHz	610 Hz	305 Hz	4.88 kHz	305 Hz	152 Hz	128 Hz
0	1	1	4.88 kHz	305 Hz	152 Hz	2.44 kHz	152 Hz	76 Hz	64 Hz
1	0	0	2.44 kHz	152 Hz	76 Hz	1.22 kHz	76 Hz	38 Hz	32 Hz
1	0	1	1.22 kHz	76 Hz	38 Hz	610 Hz	38 Hz	19 Hz	16 Hz
1	1	0	610 Hz	38 Hz	19 Hz	305 Hz	19 Hz	10 Hz	8 Hz
1	1	1	305 Hz	19 Hz	10 Hz	153 Hz	10 Hz	5 Hz	4 Hz

Note Expanded-specification products only.

Remarks 1. fX: Main system clock oscillation frequency
2. fXT: Subsystem clock oscillation frequency

(3) Port mode register 3 (PM3)

PM3 is used to set each bit of port 3 to input or output.

When the P32/INTP2/TO90 pin is used for timer output, reset the output latch of P32 and PM32 to 0; when the P33/INTP3/TO82/BZO90 pin is used for buzzer output,[Note] reset the output latch of P33 and PM33 to 0.

PM3 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets PM3 to FFH.

Note Never output the TO82 and BZO90 signals at the same time.

Figure 8-4. Format of Port Mode Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM3	1	1	1	1	PM33	PM32	PM31	PM30	FF23H	FFH	R/W

PM3n	P3n pin I/O mode (n = 2 or 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

8.4 Operation of 16-Bit Timer 90

8.4.1 Operation as timer interrupt

16-bit timer 90 can generate interrupts repeatedly each time the free-running counter value reaches the value set to CR90. Since this counter is not cleared and holds the count even after an interrupt is generated, the interval time is equal to one cycle of the count clock set in TCL901 and TCL900.

To operate 16-bit timer 90 as a timer interrupt, the following settings are required.

- Set count values in CR90
- Set 16-bit timer mode control register 90 (TMC90) as shown in Figure 8-5.

Figure 8-5. Settings of 16-Bit Timer Mode Control Register 90 for Timer Interrupt Operation

	TOD90	TOF90	CPT901	CPT900	TOC90	TCL901	TCL900	TOE90
TMC90	–	0/1	0/1	0/1	0/1	0	0/1	0/1

TCL901, TCL900: Setting of count clock (see **Table 8-3**)

Caution If both the CPT901 and CPT900 flags are set to 0, the capture edge is disabled.

When the count value of 16-bit timer counter 90 (TM90) matches the value set in CR90, counting of TM90 continues and an interrupt request signal (INTTM90) is generated.

Table 8-3 shows interval time, and Figure 8-6 shows timing of the timer interrupt operation.

Caution When rewriting the value in CR90 during a count operation, be sure to execute the following processing.

<1> Set interrupts to disabled (set TMMK90 (bit 4 of interrupt mask flag register 1 (MK1)) to 1).

<2> Disable inversion control of timer output data (set TOC90 to 0)

If the value in CR90 is rewritten in the interrupt-enabled state, an interrupt request may occur at the moment of rewrite.

Table 8-3. Interval Time of 16-Bit Timer 90

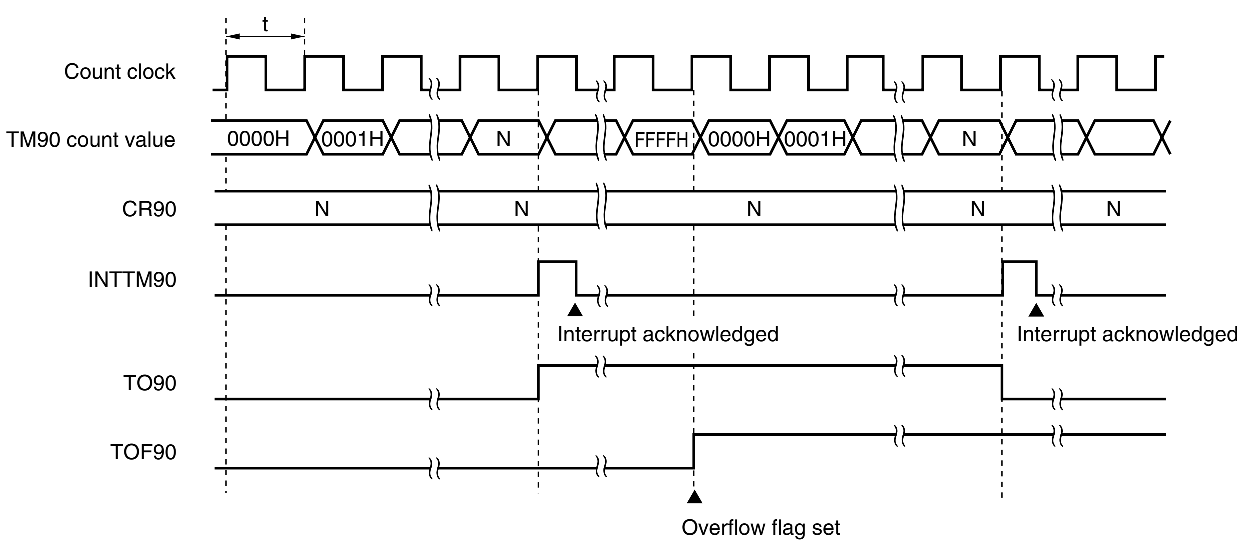
TCL901	TCL900	Count Clock			Interval Time		
			At fx = 10.0 MHz[Note] or fXT = 32.768 kHz operation	At fx = 5.0 MHz or fXT = 32.768 kHz operation		At fx = 10.0 MHz[Note] or fXT = 32.768 kHz operation	At fx = 5.0 MHz or fXT = 32.768 kHz operation
0	0	2^2/fx	0.4 μs	0.8 μs	2^{18}/fx	26.2 ms	52.4 ms
0	1	2^6/fx	6.4 μs	12.8 μs	2^{22}/fx	419 ms	839 ms
1	0	2^7/fx	12.8 μs	25.6 μs	2^{23}/fx	839 ms	1.68 s
1	1	1/fXT	30.5 μs		2^{16}/fXT	2.0 s	

Note Expanded-specification products only

Remarks 1. fx: Main system clock oscillation frequency

2. fXT: Subsystem clock oscillation frequency

Figure 8-6. Timing of Timer Interrupt Operation



Remark N = 0000H to FFFFH

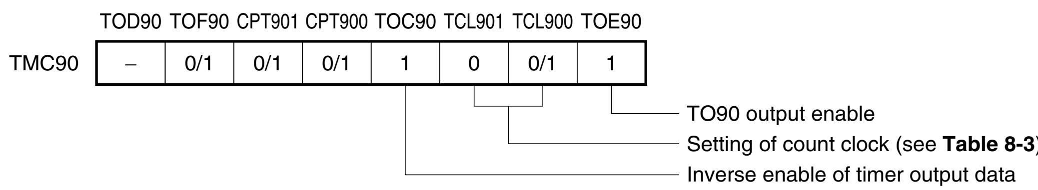
8.4.2 Operation as timer output

16-bit timer 90 can invert the timer output repeatedly each time the free-running counter value reaches the value set to CR90. Since this counter is not cleared and holds the count even after the timer output is inverted, the interval time is equal to one cycle of the count clock set in TCL901 and TCL900.

To operate the 16-bit timer as a timer output, the following settings are required.

- Set P32 to output mode (PM32 = 0).
- Reset the output latch of P32 to 0.
- Set the count value in CR90.
- Set 16-bit timer mode control register 90 (TMC90) as shown in Figure 8-7.

Figure 8-7. Settings of 16-Bit Timer Mode Control Register 90 for Timer Output Operation

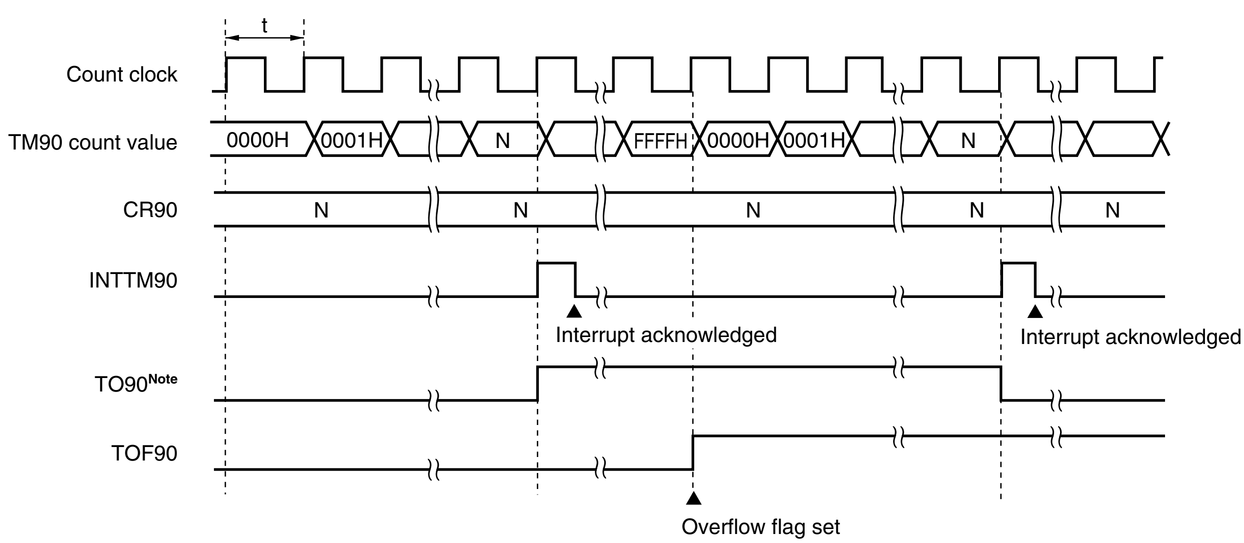


Caution If both the CPT901 flag and CPT900 flag are set to 0, the capture edge is disabled.

When the count value of 16-bit timer counter 90 (TM90) matches the value set in CR90, the output status of the TO90/P32/INTP2 pin is inverted. This enables timer output. At that time, the TM90 count is continued and an interrupt request signal (INTTM90) is generated.

Figure 8-8 shows the timing of timer output (see **Table 8-3** for the interval time of the 16-bit timer).

Figure 8-8. Timer Output Timing



Note The TO90 initial value becomes low level during output enable (TOE90 = 1).

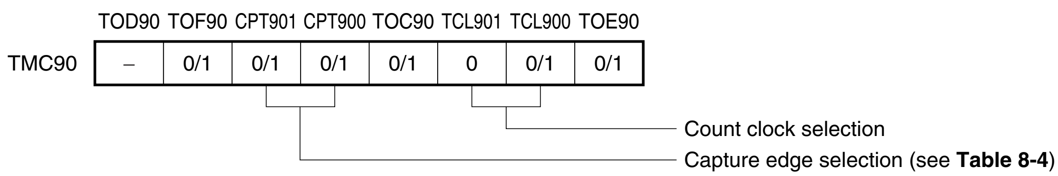
Remark N = 0000H to FFFFH

8.4.3 Capture operation

The capture operation consists of latching the count value of 16-bit timer register 90 (TM90) into a capture register in synchronization with a capture trigger, and retaining the count value.

Set TMC90 as shown in Figure 8-9 to allow the 16-bit timer to start the capture operation.

Figure 8-9. Settings of 16-Bit Timer Mode Control Register 90 for Capture Operation



16-bit capture register 90 (TCP90) starts a capture operation after a CPT90 capture trigger edge is detected, and latches and retains the count value of 16-bit timer register 90. TCP90 fetches the count value within 2 clocks and retains the count value until the next capture edge detection.

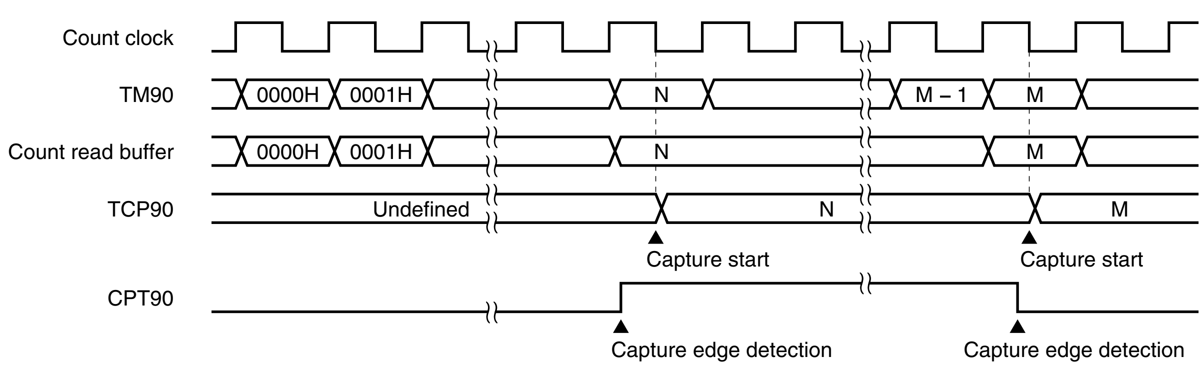
Table 8-4 and Figure 8-10 shows the settings of the capture edge and capture operation timing, respectively.

Table 8-4. Settings of Capture Edge

CPT901	CPT900	Capture Edge Selection
0	0	Capture operation prohibited
0	1	CPT90 pin rising edge
1	0	CPT90 pin falling edge
1	1	CPT90 pin both edges

Caution Because TCP90 is rewritten when a capture trigger edge is detected during TCP90 read, disable capture trigger edge detection during TCP90 read.

Figure 8-10. Capture Operation Timing (Both Edges of CPT90 Pin Are Specified)



8.4.4 16-bit timer counter 90 readout

The count value of 16-bit timer counter 90 (TM90) is read out with a 16-bit manipulation instruction.

TM90 readout is performed via a counter read buffer. The counter read buffer latches the TM90 count value. The buffer operation is held pending at the CPU clock falling edge after the read signal of the TM90 lower byte rises and the count value is retained. The counter read buffer value in the retention state can be read out as the count value.

Cancellation of pending is performed at the CPU clock falling edge after the read signal of the TM90 higher byte falls.

$\overline{\text{RESET}}$ input clears TM90 to 0000H and TM90 starts freerunning.

Figure 8-11 shows the timing of 16-bit timer counter 90 readout.

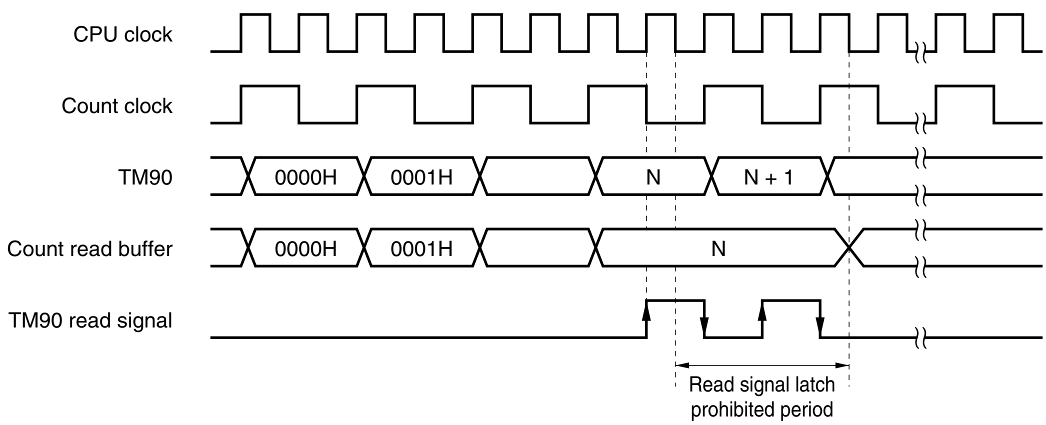
Cautions 1. The count value after releasing the stop mode becomes undefined because the count operation is executed during the oscillation stabilization time.

2. Though TM90 is designed for a 16-bit transfer instruction, 8-bit transfer instruction can also be used.

When using the 8-bit transfer instruction, execute it using direct addressing.

3. When using the 8-bit transfer instruction, execute in the order from lower byte to higher byte in pairs. If only the lower byte is read, the pending state of the counter read buffer is not canceled, and if only the higher byte is read, an undefined count value is read.

Figure 8-11. 16-Bit Timer Counter 90 Readout Timing



Remark N = 0000H to FFFFH

8.4.5 Buzzer output operation

The buzzer frequency is set using buzzer output control register 90 (BZC90) based on the count clock selected with TCL901 and TCL900 of TMC90 (source clock). A square wave of the set buzzer frequency is output.

Table 8-5 shows the buzzer frequency.

Set the 16-bit timer as follows to use it for buzzer output.

- Set P33 to output mode (PM33 = 0).
- Reset output latch of P33 to 0.
- Set a count clock by using TCL901 and TCL900.
- Set BZC90 as shown in Figure 8-12.
- Clear TOE82 of 8-bit timer mode control register 82 (TMC82) to 0 to disable the output of 8-bit timer 82.

Figure 8-12. Settings of Buzzer Output Control Register 90 for Buzzer Output Operation

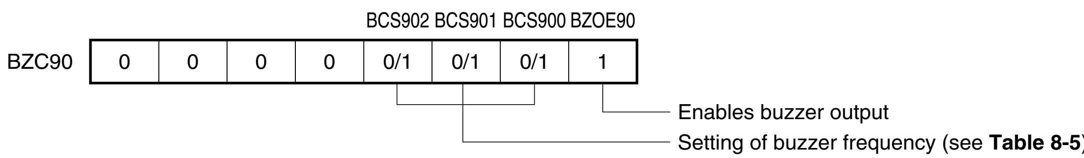


Table 8-5. Buzzer Frequency of 16-Bit Timer 90

BCS902	BCS901	BCS900	Buzzer Frequency						
			At fx = 10.0 MHz[Note] operation			At fx = 5.0 MHz operation			At fXT = 32.768 kHz operation
			fcl = fx/2^2	fcl = fx/2^6	fcl = fx/2^7	fcl = fx/2^2	fcl = fx/2^6	fcl = fx/2^7	fcl = fXT
0	0	0	156 kHz	9.76 kHz	4.88 kHz	78.1 kHz	4.88 kHz	2.44 kHz	2.05 kHz
0	0	1	78.1 kHz	4.88 kHz	2.44 kHz	39.1 kHz	2.44 kHz	1.22 kHz	1.02 kHz
0	1	0	9.76 kHz	610 Hz	305 Hz	4.88 kHz	305 Hz	152 Hz	128 Hz
0	1	1	4.88 kHz	305 Hz	152 Hz	2.44 kHz	152 Hz	76 Hz	64 Hz
1	0	0	2.44 kHz	152 Hz	76 Hz	1.22 kHz	76 Hz	38 Hz	32 Hz
1	0	1	1.22 kHz	76 Hz	38 Hz	610 Hz	38 Hz	19 Hz	16 Hz
1	1	0	610 Hz	38 Hz	19 Hz	305 Hz	19 Hz	10 Hz	8 Hz
1	1	1	305 Hz	19 Hz	10 Hz	153 Hz	10 Hz	5 Hz	4 Hz

Note Expanded-specification products only

Remarks 1. fx: Main system clock oscillation frequency

2. fXT: Subsystem clock oscillation frequency

8.5 Notes on 16-Bit Timer 90

8.5.1 Notes on using 16-bit timer 90

Usable functions differ according to the settings of the count clock selection, CPU clock operation, system clock oscillation status, and BZOE90 (bit 0 of buzzer output control register 90 (BZC90)).

Refer to the following table.

Count Clock	CPU Clock	System Clock		BZOE90	Capture	TM90 Read	Buzzer Output	Timer Output	Timer Interrupt
		Main System Clock	Subsystem Clock						
$f_X/2^2$, $f_X/2^6$, $f_X/2^7$	Main	Oscillating	Oscillating/Stopped	1/0	√	√ Note 1	**Note 2**	√	√
		Stopped			×	×	×	×	×
	Sub	Oscillating	Oscillating		√	×	**Note 2**	√	√
		Stopped			×	×	×	×	×
f_{XT}	Main	Oscillating	Oscillating	0	√	√	×	√	√
				1	×	×	√	√	√
			Stopped	1/0	×	×	×	×	×
		Stopped (STOP mode)	Oscillating	0	×	×	×	×	×
				1	×	×	√	√	√
			Stopped	1/0	×	×	×	×	×
	Sub	Oscillating	Oscillating	0	√	√	×	√	√
				1	×	×	√	√	√
		Stopped		0	×	×	×	×	×
				1	×	×	√	√	√

Notes 1. TM90 is enabled only when the CPU clock is in high-speed mode.

2. Output is enabled when BZOE90 = 1.

Cautions 1. The capture function uses fx/2 for control (refer to Figure 8-1 Block Diagram of 16-Bit Timer 90). Therefore, the capture function cannot be used when the main system clock is stopped.

2. The read function of TM90 uses the CPU clock for control (refer to Figure 8-1), and reads an undefined value when the CPU clock is slower than the count clock (values are not guaranteed). When reading TM90, set the count clock to the same speed as the CPU clock (when the CPU clock is the main system clock, high-speed mode is set), or select a clock slower than the CPU clock.

3. When the subsystem clock is selected as the count clock and BZOE90 is set to 0, the subsystem clock selected as the TM90 count clock is one that has been synchronized with the main system clock (refer to Figure 8-1). Therefore, when the main system clock oscillation is stopped, the timer operation is stopped because the clock supplied to 16-bit timer 90 is stopped (timer interrupt is not generated).

Moreover, when the subsystem clock is selected as the count clock and BZOE90 is set to 1, the capture and TM90 read values are not guaranteed because the subsystem clock is not synchronized. Therefore, be sure to set BZOE90 to 0 when using the capture and TM90 read functions (when the subsystem clock is selected as the count clock, buzzer output, and the capture and TM90 read functions cannot be used at the same time).

Make the following settings to enable low-current consumption when stopping the main system clock oscillation and releasing the HALT mode.

Count clock:	Subsystem clock
CPU clock:	Subsystem clock
Main system clock:	Oscillation stopped
BZOE90:	1 (Buzzer output enable)

At this time, when the setting of P33, the buzzer output alternate function pin, is “PM33 = 0, P33 = 0”, a square wave of the buzzer frequency is output from P33. When making the above settings, perform either of the following.

- Set P33 to input mode (PM33 = 1)
- If P33 cannot be set input mode, set the port latch value of P33 to 1 (P33 = 1) (in this case a high level is output from P33)

8.5.2 Restrictions on rewriting of 16-bit compare register 90

(1) When rewriting the compare register (CR90), be sure to disable interrupts (TMMK90 = 1), and disable inversion control of timer output (TOC90 = 0) first.
If CR90 is rewritten with interrupts enabled, an interrupt request may be generated at the moment of rewrite.

(2) The interval time may be double the intended time depending on to the timing at which the compare register (CR90) is rewritten. Likewise, the timer output waveform may be shorter or double the intended output.
To avoid this, rewrite using one of the following procedures.

<Preventing method A> Rewriting by 8-bit access

<1> Disable interrupts (TMMK90 = 1), and disable inversion control of timer output (TOC90 = 0)
<2> Rewrite the higher byte of CR90 (16 bits) first
<3> Next, rewrite the lower byte of CR90 (16 bits)
<4> Clear the interrupt request flag (TMIF90)
<5> After more than half the cycle of the count clock has passed from the start of the interrupt, enable timer interrupt and timer output inversion

<Program example A> (When count clock = 64/fX, CPU clock = fx)

```
TM90_VCT: SET1  TMMK90;     Timer interrupt disable (6 clocks)
          CLR1  TMC90.3;    Timer output inversion disable (6 clocks)
          MOV   A, #xxH;    Higher byte rewrite value setting (6 clocks)
          MOV   !0FF17H,A;  CR90 higher byte rewriting (8 clocks)
          MOV   A, #yyH;    Lower byte rewrite value setting (6 clocks)
          MOV   !0FF16H,A;  CR90 lower byte rewriting (8 clocks)
          CLR1  TMIF90;     Interrupt request flag clearing (6 clocks)
          CLR1  TMMK90;     Timer interrupt enable (6 clocks)
          SET1  TMC90.3;    Timer output inversion enable
```

(More than 32 clocks in total[Note])

Note This is because the INTTM90 signal is set to the high level for a period of half the cycle of the count clock after an interrupt is generated, so the output will be inverted if TOC90 is set to 1 during this period.

<Preventing method B> Rewriting by 16-bit access

<1> Disable interrupt (TMMK90 = 1), and disable inversion control of timer output (TOC90 = 0)

<2> Rewrite CR90 (16 bits)

<3> Wait for more than one cycle of the count clock

<4> Clear the interrupt request flag (TMIF90)

<5> Enable timer interrupt and timer output inversion

<Program example B> (When count clock = 64/fx, CPU clock = fx)

```
TM90_VCT:  SET1   TMMK90;      Timer interrupt disable
           CLR1   TMC90.3;     Timer output inversion disable
           MOVW   AX, #xxyyH;  CR90 rewrite value setting
           MOVW   CR90, AX;    CR90 rewriting
           NOP                 }
           NOP                 }
            :                  }  NOP 32 (Wait for 64/fx)Note
           NOP                 }
           NOP                 }
           CLR1   TMIF90;      Interrupt request flag clearing
           CLR1   TMMK90;      Timer interrupt enable
           SET1   TMC90.3;     Timer output inversion enable
```

Note Wait for more than one cycle of the count clock after the CR90 rewriting instruction (MOVW CR90, AX) before clearing the interrupt request flag (TMIF90).

9.1 Functions of 8-Bit Timer/Event Counters 80 to 82

8-bit timer/event counters 80 and 81 and 8-bit timer 82 have the following functions.

- Interval timer (TM80, TM81, TM82)
- External event counter (TM80, TM81 only)
- Square wave output (TM80, TM81, TM82)
- PWM output (TM80, TM81, TM82)

(1) 8-bit interval timer

When an 8-bit timer/event counter is used as an interval timer, it generates an interrupt at any time interval set in advance.

Table 9-1. Interval Time of 8-Bit Timer/Event Counter 80

Minimum Interval Time	Maximum Interval Time	Resolution
$1/f_X$ (100 ns) [200 ns]	$2^8/f_X$ (25.6 μs) [51.2 μs]	$1/f_X$ (100 ns) [200 ns]
$2^3/f_X$ (0.8 μs) [1.6 μs]	$2^{11}/f_X$ (204.8 μs) [409.6 μs]	$2^3/f_X$ (0.8 μs) [1.6 μs]

Remarks 1. f_X: Main system clock oscillation frequency

2. The values in parentheses ( ) apply to operation at f_X = 10.0 MHz (expanded-specification products only).

3. The values in brackets [ ] apply to operation at f_X = 5.0 MHz.

Table 9-2. Interval Time of 8-Bit Timer/Event Counter 81

Minimum Interval Time	Maximum Interval Time	Resolution
$2^4/f_X$ (1.6 μs) (3.2 μs)	$2^{12}/f_X$ (409.6 μs) [819.2 μs]	$2^4/f_X$ (1.6 μs) [3.2 μs]
$2^8/f_X$ (25.6 μs) (51.2 μs)	$2^{16}/f_X$ (6.55 ms) [13.1 ms]	$2^8/f_X$ (25.6 μs) [51.2 μs]

Remarks 1. f_X: Main system clock oscillation frequency

2. The values in parentheses ( ) apply to operation at f_X = 10.0 MHz (expanded-specification products only).

3. The values in brackets [ ] apply to operation at f_X = 5.0 MHz.

Table 9-3. Interval Time of 8-Bit Timer 82

Minimum Interval Time	Maximum Interval Time	Resolution
$2^5/f_X$ (3.2 μs) [6.4 μs]	$2^{13}/f_X$ (0.82 ms) [1.64 ms]	$2^5/f_X$ (3.2 μs) [6.4 μs]
$2^7/f_X$ (12.8 μs) [25.6 μs]	$2^{15}/f_X$ (3.27 ms) [6.55 ms]	$2^7/f_X$ (12.8 μs) [25.6 μs]
$1/f_{XT}$ (30.5 μs) [30.5 μs]	$2^8/f_{XT}$ (7.81 ms) [7.81 ms]	$1/f_{XT}$ (30.5 μs) [30.5 μs]

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

3. The values in parentheses ( ) apply to operation at f_X = 10.0 MHz or f_{XT} = 32.768 kHz (expanded-specification products only).

4. The values in brackets [ ] apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

(2) External event counter

The number of pulses of an externally input signal can be counted.

(3) Square wave output

A square wave of arbitrary frequency can be output.

Table 9-4. Square Wave Output Range of 8-Bit Timer/Event Counter 80

Minimum Pulse Width	Maximum Pulse Width	Resolution
$1/f_X$ (100 ns) [200 ns]	$2^8/f_X$ (25.6 μs) [51.2 μs]	$1/f_X$ (100 ns) [200 ns]
$2^3/f_X$ (0.8 μs) [1.6 μs]	$2^{11}/f_X$ (204.8 μs) [409.6 μs]	$2^3/f_X$ (0.8 μs) [1.6 μs]

Remarks 1. f_X: Main system clock oscillation frequency

2. The values in parentheses ( ) apply to operation at f_X = 10.0 MHz. (expanded-specification products only)

3. The values in brackets [ ] apply to operation at f_X = 5.0 MHz.

Table 9-5. Square Wave Output Range of 8-Bit Timer/Event Counter 81

Minimum Pulse Width	Maximum Pulse Width	Resolution
$2^4/f_X$ (1.6 μs) [3.2 μs]	$2^{12}/f_X$ (409.6 μs) [819.2 μs]	$2^4/f_X$ (1.6 μs) [3.2 μs]
$2^8/f_X$ (25.6 μs) [51.2 μs]	$2^{16}/f_X$ (6.55 ms) [13.1 ms]	$2^8/f_X$ (25.6 μs) [51.2 μs]

Remarks 1. f_X: Main system clock oscillation frequency

2. The values in parentheses ( ) apply to operation at f_X = 10.0 MHz. (expanded-specification products only)

3. The values in brackets [ ] apply to operation at f_X = 5.0 MHz.

Table 9-6. Square Wave Output Range of 8-Bit Timer 82

Minimum Pulse Width	Maximum Pulse Width	Resolution
$2^5/f_X$ (3.2 μs) [6.4 μs]	$2^{13}/f_X$ (819 μs) [1.64 ms]	$2^5/f_X$ (3.2 μs) [6.4 μs]
$2^7/f_X$ (12.8 μs) [25.6 μs]	$2^{15}/f_X$ (3.27 ms) [6.55 ms]	$2^7/f_X$ (12.8 μs) [25.6 μs]
$1/f_{XT}$ (30.5 μs) [30.5 μs]	$2^8/f_{XT}$ (7.81 ms) [7.81 ms]	$1/f_{XT}$ (30.5 μs) [30.5 μs]

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

3. The values in parentheses ( ) apply to operation at f_X = 10.0 MHz or f_{XT} = 32.768 kHz. (expanded-specification products only)

4. The values in brackets [ ] apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

(4) PWM output

8-bit resolution PWM output can be produced.

9.2 Configuration of 8-Bit Timer/Event Counters 80 to 82

8-bit timer/event counters 80 to 82 consist of the following hardware.

Table 9-7. Configuration of 8-Bit Timer/Event Counters 80 to 82

Item	Configuration
Timer counter	8 bits × 3 (TM80 to TM82)
Register	Compare register: 8 bits × 3 (CR80 to CR82)
Timer outputs	3 (TO80 to TO82)
Control registers	8-bit timer mode control register 80 to 82 (TMC80 to TMC82) Port mode register 2, 3 (PM2, PM3)

Figure 9-1. Block Diagram of 8-Bit Timer/Event Counter 80

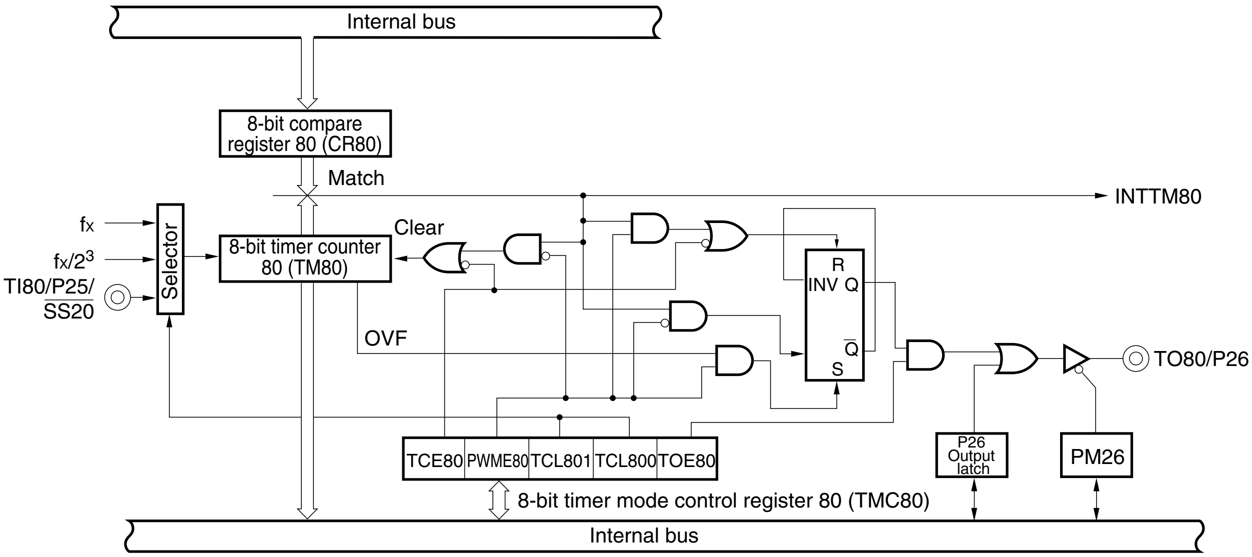


Figure 9-2. Block Diagram of 8-Bit Timer/Event Counter 81

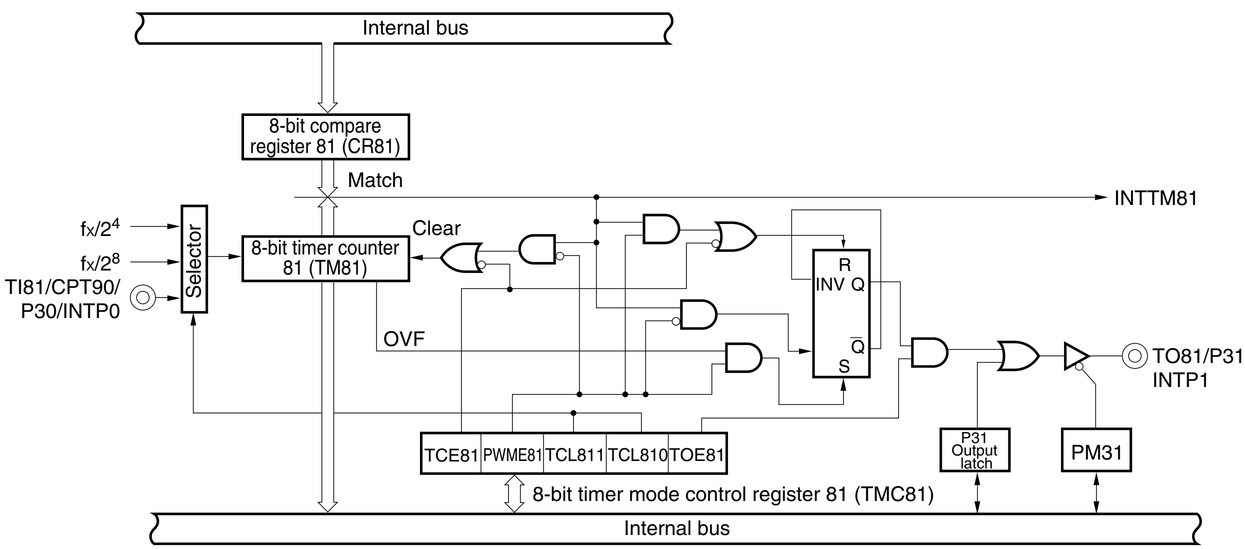
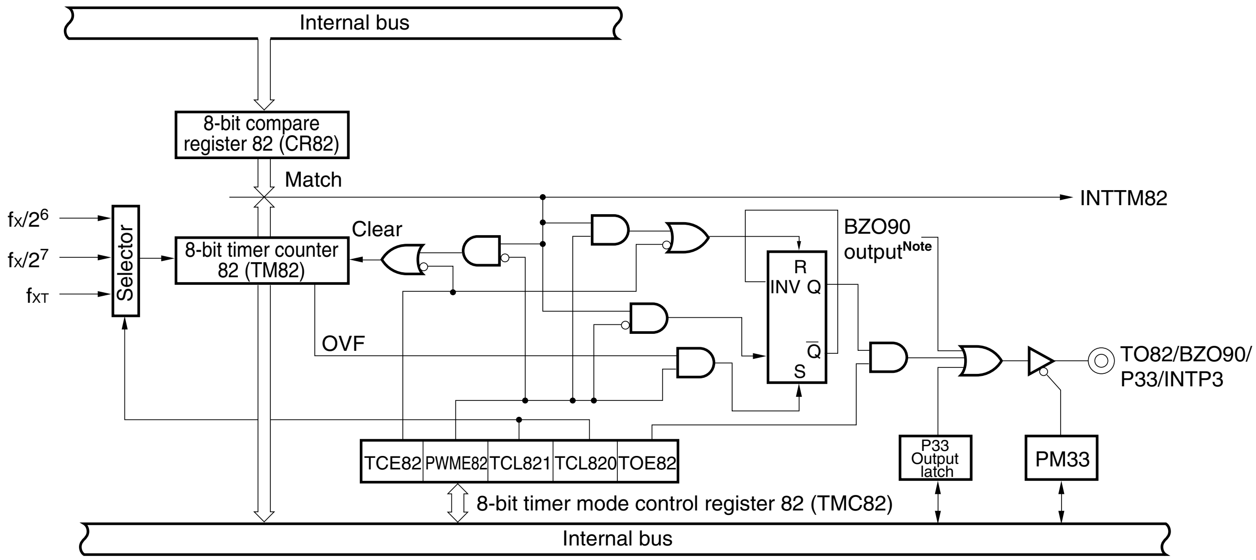


Figure 9-3. Block Diagram of 8-Bit Timer 82



Note See **Figure 8-1 Block Diagram of 16-Bit Time 90**.

(1) 8-bit compare register 8n (CR8n)

A value specified in CR8n is compared with the count in 8-bit timer counter 8n (TM8n). If they match, an interrupt request (INTTM8n) is issued.

CR8n is set with an 8-bit memory manipulation instruction. Any value from 00H to FFH can be set.

$\overline{\text{RESET}}$ input makes CR8n undefined.

Cautions 1. Before rewriting CR8n, stop the timer operation once. If CR8n is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

2. Do not clear CR8n to 00H in PWM output mode (when PWME8n = 1: bit 6 of 8-bit timer mode control register 8n (TMC8n)); otherwise, PWM output may not be produced normally.

Remark n = 0 to 2

(2) 8-bit timer counter 8n (TM8n)

TM8n is used to count the number of pulses.

Its contents are read with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TM8n to 00H.

Remark n = 0 to 2

9.3 8-Bit Timer/Event Counters 80 to 82 Control Registers

The following two types of registers are used to control the 8-bit timer/event counter.

- 8-bit timer mode control registers 80, 81, and 82 (TMC80, TMC81, and TMC82)
- Port mode registers 2 and 3 (PM2 and PM3)

(1) 8-bit timer mode control register 80 (TMC80)

TMC80 determines whether to enable or disable 8-bit timer counter 80 (TM80), specifies the count clock for TM80, and controls the operation of the output controller of 8-bit timer/event counter 80.

TMC80 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TMC80 to 00H.

Figure 9-4. Format of 8-Bit Timer Mode Control Register 80

Symbol	<7>	<6>	5	4	3	2	1	<0>	Address	After reset	R/W
TMC80	TCE80	PWME80	0	0	0	TCL801	TCL800	TOE80	FF53H	00H	R/W

TCE80	TM80 operation control
0	Operation disabled (TM80 is cleared to 00H)
1	Operation enabled

PWME80	PWM output selection
0	Timer counter operation mode
1	PWM output operation mode

TCL801	TCL800	8-bit timer counter 80 count clock selection		
			At fx = 10.0 MHz[Note] operation	At fx = 5.0 MHz operation
0	0	fx	10.0 MHz	5.0 MHz
0	1	$fx/2^3$	1.25 MHz	625 kHz
1	0	Rising edge of TI80		
1	1	Falling edge of TI80		

TOE80	8-bit timer/event counter 80 output control
0	Output disabled (port mode)
1	Output enabled

Note Expanded-specification products only.

Cautions 1. Always stop the timer before setting TMC80.

2. For PWM mode operation, the interrupt mask flag (TMMK80) must be set.

Remarks fx: Main system clock oscillation frequency

(2) 8-bit timer mode control register 81 (TMC81)

TMC81 determines whether to enable or disable 8-bit timer counter 81 (TM81), specifies the count clock for TM81, and controls the operation of the output controller of 8-bit timer/event counter 81.

TMC81 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TMC81 to 00H.

Figure 9-5. Format of 8-Bit Timer Mode Control Register 81

Symbol	<7>	<6>	5	4	3	2	1	<0>	Address	After reset	R/W
TMC81	TCE81	PWME81	0	0	0	TCL811	TCL810	TOE81	FF57H	00H	R/W

TCE81	TM81 operation control
0	Operation disabled (TM81 is cleared to 00H)
1	Operation enabled

PWME81	PWM output selection
0	
1	

TCL811	TCL810	8-bit timer counter 81 count clock selection		
			At fx = 10.0 MHz[Note] operation	At fx = 5.0 MHz operation
0	0	$f_X/2^4$	625 kHz	312 kHz
0	1	$f_X/2^8$	39.1 kHz	19.5 kHz
1	0	Rising edge of TI81		
1	1	Falling edge of TI81		

TOE81	8-bit timer/event counter 81 output control
0	Output disabled (port mode)
1	Output enabled

Note Expanded-specification products only.

Cautions 1. Always stop the timer before setting TMC81.

2. For PWM mode operation, the interrupt mask flag (TMMK81) must be set.

Remark fx: Main system clock oscillation frequency

(3) 8-bit timer mode control register 82 (TMC82)

TMC82 determines whether to enable or disable 8-bit timer counter 82 (TM82) and specifies the count clock for TM82. It also controls the operation of the output controller of 8-bit timer 82.

TMC82 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TMC82 to 00H.

Figure 9-6. Format of 8-Bit Timer Mode Control Register 82

Symbol	<7>	<6>	5	4	3	2	1	<0>	Address	After reset	R/W
TMC82	TCE82	PWME82	0	0	0	TCL821	TCL820	TOE82	FF5BH	00H	R/W

TCE82	TM82 operation control
0	Operation disabled (TM82 is cleared to 00H)
1	Operation enabled

PWME82	PWM output selection
0	Timer counter operation mode
1	PWM output operation mode

TCL821	TCL820	8-bit time counter 82 count clock section		
			At f_X = 10.0 MHz[Note 1] or f_{XT} = 32.768 kHz operation	At f_X = 5.0 MHz or f_{XT} = 32.768 kHz operation
0	0	$f_X/2^5$	312 kHz	156 kHz
0	1	$f_X/2^7$	78.1 kHz	39.1 kHz
1	0	f_{XT}	32.768 kHz	
1	1	Setting prohibited		

TOE82	8-bit timer 82 output control
0	Output disabled (port mode)
1	Output enabled[Note 2]

Notes 1. Expanded-specification products only.

2. When TOE82 is set to 1, BZOE90 must be set to 0 (see **Figure 8-3 Format of Buzzer Output Control Register 90**).

Cautions 1. Always stop the timer before setting TMC82.

2. For PWM mode operation, the interrupt mask flag (TMMK82) must be set.

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

(4) Port mode registers 2 and 3 (PM2 and PM3)

PM2 and PM3 specify whether each bit of port 2 and port 3 is used for input or output.
To use the P26/TO80 pin for timer output, the PM26 and P26 output latch must be reset to 0.
To use the P31/TO81/INTP1 pin for timer output, the PM31 and P31 output latch must be reset to 0.
To use the P33/INTP3/TO82/BZO90 pin for timer output, the PM33 and P33 output latch must be reset to 0.
PM2 and PM3 are set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input sets PM2 and PM3 to FFH.

Figure 9-7. Format of Port Mode Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM2	1	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W

PM26	P26 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 9-8. Format of Port Mode Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM3	1	1	1	1	PM33	PM32	PM31	PM30	FF23H	FFH	R/W

PM31	P31 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

PM33	P33 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

9.4 Operation of 8-Bit Timer/Event Counters 80 to 82

9.4.1 Operation as interval timer

The interval timer repeatedly generates an interrupt at time intervals specified by the count value set in 8-bit compare register 8n (CR8n) in advance.

To operate 8-bit timer/event counters 80 to 82 as an interval timer, the following settings are required.

<1> Set 8-bit timer counter 8n (TM8n) to operation disable (by setting TCE8n (bit 7 of 8-bit timer mode control register 8n (TMC8n)) to 0).
<2> Set the count clock of 8-bit timer/event counters 80 to 82 (see **Tables 9-8** to **9-10**).
<3> Set a count value in CR8n.
<4> Set TM8n to operation enabled (TCE8n = 1).

When the count value of 8-bit timer counter 8n (TM8n) matches the value set in CR8n, TM8n is cleared to 00H and continues counting. At the same time, an interrupt request signal (INTTM8n) is generated.

Tables 9-8 to 9-10 show interval time, and Figure 9-9 shows the timing of interval timer operation.

Cautions 1. Before rewriting CR8n, stop the timer operation once. If CR8n is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

2. If the count clock setting and TM8n operation-enabled are set in TCM8n simultaneously using an 8-bit memory manipulation instruction, an error of more than a clock in one cycle may occur after the timer start. Therefore, always follow the above procedure when operating the 8-bit timer/event counter as an interval timer.

Remark n = 0 to 2

Table 9-8. Interval Time of 8-Bit Timer/Event Counter 80

TCL801	TCL800	Minimum Interval Time	Maximum Interval Time	Resolution
0	0	1/fx (100 ns) [200 ns]	2^8/fx (25.6 μs) [51.2 μs]	1/fx (100 ns) [200 ns]
0	1	2^3/fx (0.8 μs) [1.6 μs]	2^{11}/fx (204.8 μs) [409.6 μs]	2^3/fx (0.8 μs) [1.6 μs]
1	0	TI80 input cycle	$2^8 \times$ TI80 input cycle	TI80 input edge cycle
1	1	TI80 input cycle	$2^8 \times$ TI80 input cycle	TI80 input edge cycle

Remarks 1. fx: Main system clock oscillation frequency

2. The values in parentheses ( ) apply to operation at fx = 10.0 MHz. (expanded-specification products only)

3. The values in brackets [ ] apply to operation at fx = 5.0 MHz.

Table 9-9. Interval Time of 8-Bit Timer/Event Counter 81

TCL811	TCL810	Minimum Interval Time	Maximum Interval Time	Resolution
0	0	2^4/fx (1.6 μs) [3.2 μs]	2^{12}/fx (409.6 μs) [819.2 μs]	2^4/fx (1.6μs) [3.2 μs]
0	1	2^8/fx (25.6 μs) [51.2 μs]	2^{16}/fx (6.55 ms) [13.1 ms]	2^8/fx (25.6 μs) [51.2 μs]
1	0	TI81 input cycle	$2^8 \times$ TI81 input cycle	TI81 input edge cycle
1	1	TI81 input cycle	$2^8 \times$ TI81 input cycle	TI81 input edge cycle

Remarks 1. fx: Main system clock oscillation frequency

2. The values in parentheses ( ) apply to operation at fx = 10.0 MHz. (expanded-specification products only)

3. The values in brackets [ ] apply to operation at fx = 5.0 MHz.

Table 9-10. Interval Time of 8-Bit Timer 82

TCL821	TCL820	Minimum Interval Time	Maximum Interval Time	Resolution
0	0	2^5/fx (3.2 μs) [6.4 μs]	2^{13}/fx (819 μs) [1.64 ms]	2^5/fx (3.2 μs) [6.4 μs]
0	1	2^7/fx (12.8 μs) [25.6 μs]	2^{15}/fx (3.27 ms) [6.55 ms]	2^7/fx (12.8 μs) [25.6 μs]
1	0	1/fXT (30.5 μs) [30.5 μs]	2^8/fXT (7.81 ms) [7.81 ms]	1/fXT (30.5 μs) [30.5 μs]
1	1	Setting prohibited		

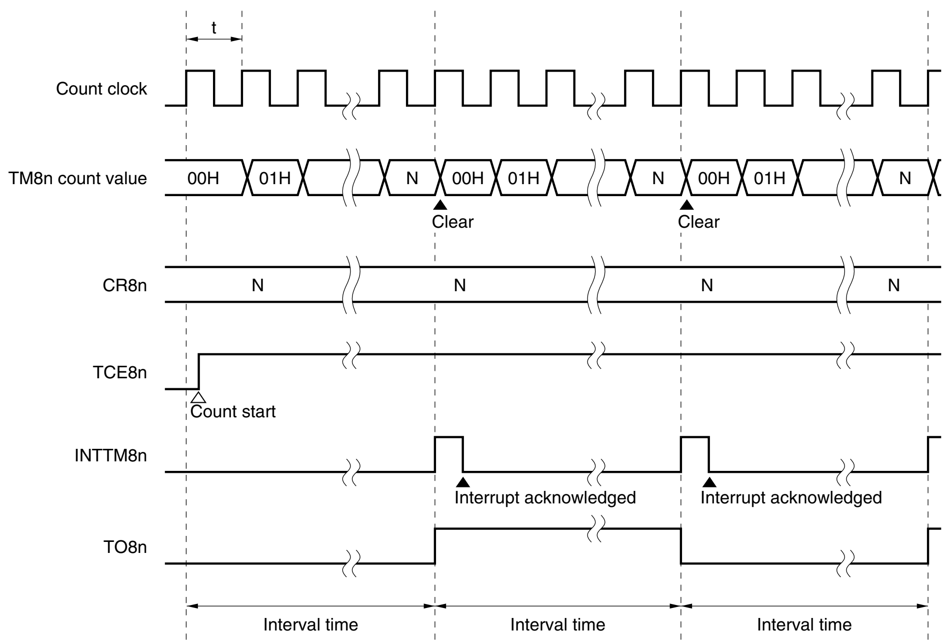
Remarks 1. fx: Main system clock oscillation frequency

2. fXT: Subsystem clock oscillation frequency

3. The values in parentheses ( ) apply to operation at fx = 10.0 MHz or fXT = 32.768 kHz (expanded-specification products only).

4. The values in brackets [ ] apply to operation at fx = 5.0 MHz or fXT = 32.768 kHz.

Figure 9-9. Interval Timer Operation Timing



Remarks 1. Interval time = (N + 1) $\times$ t : N = 00H to FFH

2. n = 0 to 2

9.4.2 Operation as external event counter[Note]

The external event counter counts the number of external clock pulses input to the TI80/P25/$\overline{SS20}$ or TI81/P30/INTP0/CPT90 pin by using 8-bit timer counters 80 or 81 (TM80 or TM81).

To operate 8-bit timer/event counter 8n as an external event counter, the following settings are required.

<1> Set P25 or P30 to input mode (PM25 = 1, PM30 = 1).

<2> Set 8-bit timer register 8n (TM8n) to operation disabled (by setting TCE8n (bit 7 of 8-bit timer mode control register 8n (TMC8n)) to 0).

<3> Specify the rising/falling edges of TI8n (see **Tables 9-4** and **9-5**).

<4> Set a count value in CR8n.

<5> Set TM8n to operation enabled (TCE8n = 1).

Note Only TM80 and TM81 have this function.

Each time the valid edge specified by bit 1 (TCL8n0) of TMC8n is input, the value TM8n is incremented.

When the count value of TM8n matches the value set in CR8n, TM8n is cleared to 0 and continues counting. At the same time, an interrupt request signal (INTTM8n) is generated.

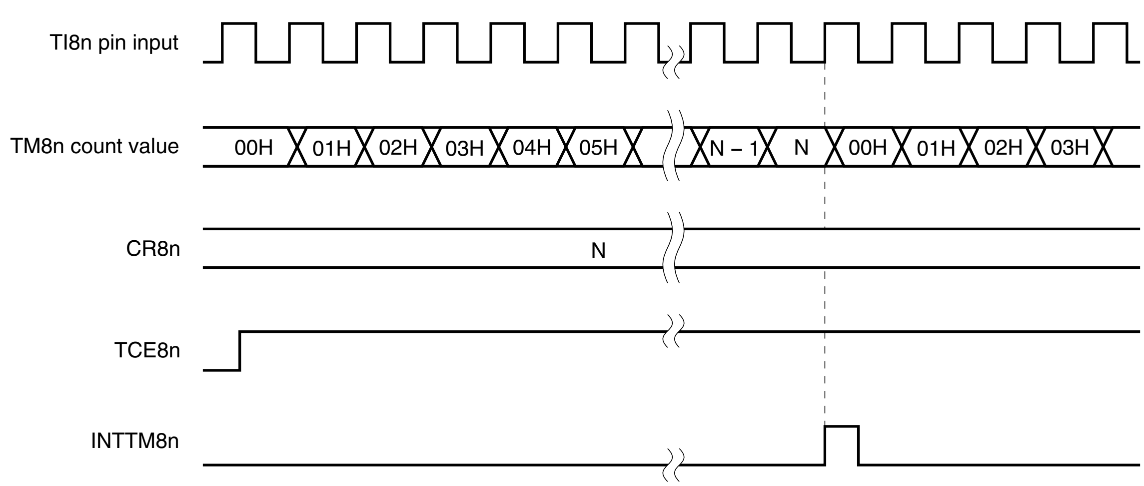
Figure 9-10 shows the timing of the external event counter operation (with rising edge specified).

Cautions 1. Before rewriting CR8n, stop the timer operation once. If CR8n is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

2. If the count clock setting and TM8n operation-enabled are set in TCM8n simultaneously using an 8-bit memory manipulation instruction, an error of more than a clock in one cycle may occur after the timer start. Therefore, always follow the above procedure when operating the 8-bit timer/event counter as an external event counter.

Remark n = 0, 1

★ **Figure 9-10. External Event Counter Operation Timing (with Rising Edge Specified)**



Remarks 1. N = 00H to FFH

2. n = 0, 1

9.4.3 Operation as square wave output

The 8-bit timer/event counter can generate output square waves of an arbitrary frequency at intervals specified by the count value set in 8-bit compare registers 8n (CR8n) in advance.

To operate 8-bit timer/event counters 8n for square wave output, the following settings are required.

<1> Set P26, P31, or P33 to output mode (PM26 = 0, PM31 = 0, PM33 = 0).
<2> Reset the output latches of P26, P31, or P33 to 0.
<3> Set 8-bit timer counter 8n (TM8n) to operation disable (by setting TCE8n (bit 7 of 8-bit timer mode control register 8n (TMC8n)) to 1).
<4> Set the count clock of 8-bit timer/event counter 8n and set TO8n to output enable (TOE8n (bit 0 of TMC8n) = 1).
<5> Set count value in CR8n.
<6> Set TM8n to operation enable (TCE8n = 1).

When the count value of TM8n matches the value set in CR8n, the TO8n pin output will be inverted. Through application of this mechanism, square waves of any frequency can be output. As soon as a match occurs, TM8n will be cleared to 00H and resumes to count, generating an interrupt request signal (INTTM8n).

Setting 0 for bit 7 (TCE8n) of TMC8n clears the square-wave output to 0.

Tables 9-11 through 9-13 show square wave output range, and Figure 9-11 shows timing of square wave output.

Cautions 1. Before rewriting CR8n, stop the timer operation once. If CR8n is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

2. If the count clock setting and TM8n operation-enabled are set in TCM8n simultaneously using an 8-bit memory manipulation instruction, an error of more than a clock in one cycle may occur after the timer start. Therefore, always follow the above procedure when operating the 8-bit timer/event counter for square wave output.

Remark n = 0 to 2

Table 9-11. Square Wave Output Range of 8-Bit Timer/Event Counter 80

TCL801	TCL800	Minimum Pulse Width	Maximum Pulse Width	Resolution
0	0	1/fx (100 ns) [200 ns]	2^8/fx (25.6 μs) [51.2 μs]	1/fx (100 ns) [200 ns]
0	1	2^3/fx (0.8μs) [1.6 μs]	2^{11}/fx (204.8 μs) [409.6 μs]	2^3/fx (0.8 μs) [1.6 μs]

Remarks 1. fx: Main system clock oscillation frequency

2. The values in parentheses ( ) apply to operation at fx = 10.0 MHz. (expanded-specification products only)

3. The values in brackets [ ] apply to operation at fx = 5.0 MHz.

Table 9-12. Square Wave Output Range of 8-Bit Timer/Event Counter 81

TCL811	TCL810	Minimum Pulse Width	Maximum Pulse Width	Resolution
0	0	2^4/fx (1.6 μs) [3.2 μs]	2^{12}/fx (409.6μs) [819.2 μs]	2^4/fx (1.6 μs) [3.2 μs]
0	1	2^8/fx (25.6 μs) [51.2 μs]	2^{16}/fx (6.55 ms) [13.1 ms]	2^8/fx (25.6 μs) [51.2 μs]

Remarks 1. fx: Main system clock oscillation frequency

2. The values in parentheses ( ) apply to operation at fx = 10.0 MHz. (expanded-specification products only)

3. The values in brackets [ ] apply to operation at fx = 5.0 MHz.

Table 9-13. Square Wave Output Range of 8-Bit Timer 82

TCL821	TCL820	Minimum Pulse Width	Maximum Pulse Width	Resolution
0	0	2^5/fx (3.2 μs) [6.4 μs]	2^{13}/fx (819 μs) [1.64 ms]	2^5/fx (3.2 μs) [6.4 μs]
0	1	2^7/fx (12.8 μs) [25.6 μs]	2^{15}/fx (3.27 ms) [6.55 ms]	2^7/fx (12.8 μs) [25.6 μs]
1	0	1/fXT (30.5 μs) [30.5 μs]	2^8/fXT (7.81 ms) [7.81 ms]	1/fXT (30.5 μs) [30.5 μs]

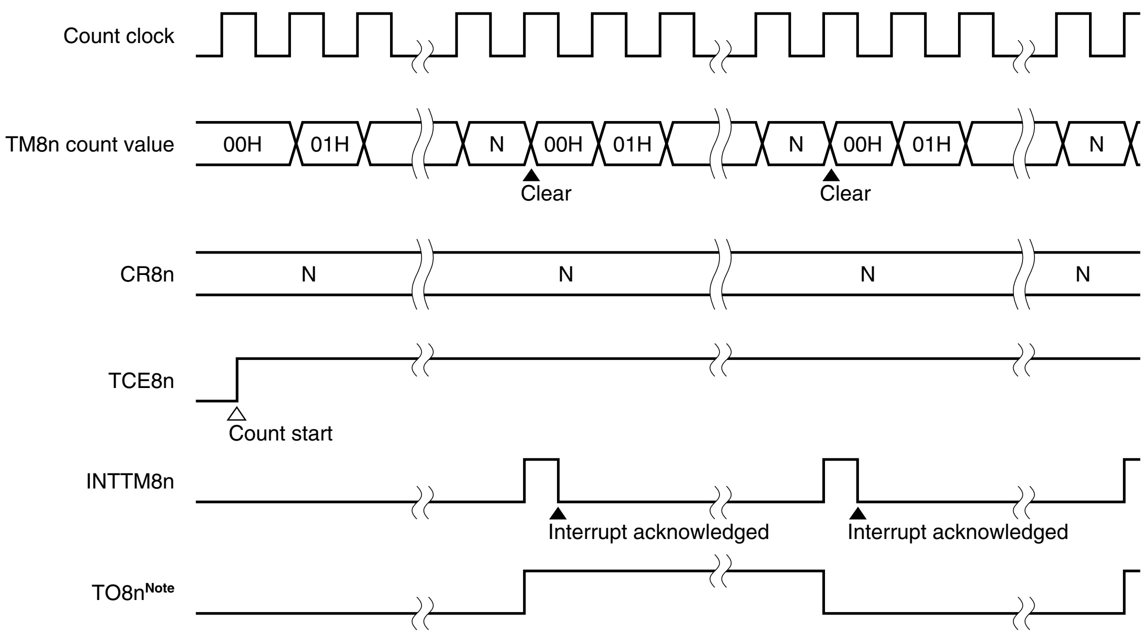
Remarks 1. fx: Main system clock oscillation frequency

2. fXT: Subsystem clock oscillation frequency

3. The values in parentheses ( ) apply to operation at fx = 10.0 MHz or fXT = 32.768 kHz. (expanded-specification products only)

4. The values in brackets [ ] apply to operation at fx = 5.0 MHz or fXT = 32.768 kHz.

Figure 9-11. Square Wave Output Timing



Note The initial value of TO8n is low for output enable (TOE8n = 1).

Remark n = 0 to 2

9.4.4 PWM output operation

PWM output enables generation of an interrupt repeatedly at intervals specified by the count value set in 8-bit compare register 8n (CR8n) in advance.

To use 8-bit timer/event counter 8n for PWM output, the following settings are required.

<1> Set P26, P31, or P33 to output mode (PM26 = 0, PM31 = 0, PM33 = 0).

<2> Reset the output latches of P26, P31, or P33 to 0.

<3> Set 8-bit timer counter 8n (TM8n) to operation disable (by setting TCE8n (bit 7 of 8-bit timer mode control register 8n (TMC8n)) to 0).

<4> Set the count clock of 8-bit timer/event counter 8n, and set TO8n to output enable (TOE8n (bit 0 of TMC8n) = 1), and to PWM output mode (PWME8n = 1).

<5> Set a count value in CR8n.

<6> Set TM8n to operation enable (TCE8n = 1).

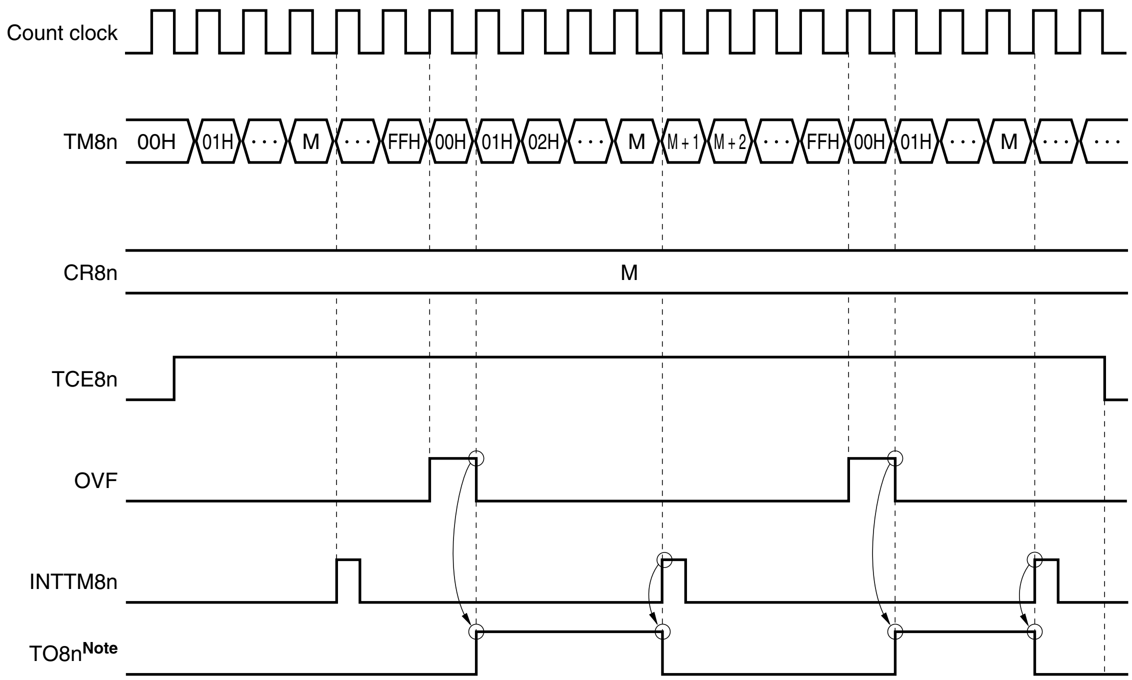
When the count value of TM8n matches the value set in CR8n, TM8n continues counting, and an interrupt request signal (INTTM8n) is generated.

Cautions 1. Before rewriting CR8n, stop the timer. If CR8n is rewritten in the timer operation-enabled state, a high-level signal may be output for the next cycle (256 count pulses) (for details, see 9.5 (4) Timer operation after compare register is rewritten during PWM output).

2. If the count clock setting and TM8n operation-enabled are set in TCM8n simultaneously using an 8-bit memory manipulation instruction, an error of more than a clock in one cycle may occur after the timer start. Therefore, always follow the above procedure when operating the 8-bit timer/event counter for PWM output.

Remark n = 0 to 2

Figure 9-12. PWM Output Timing



M = 01H to FFH

Note The initial value of TO8n is low for output enable (TOE8n = 1).

Caution Do not set CR8n to 00H in PWM output mode; otherwise, PWM may not be output normally.

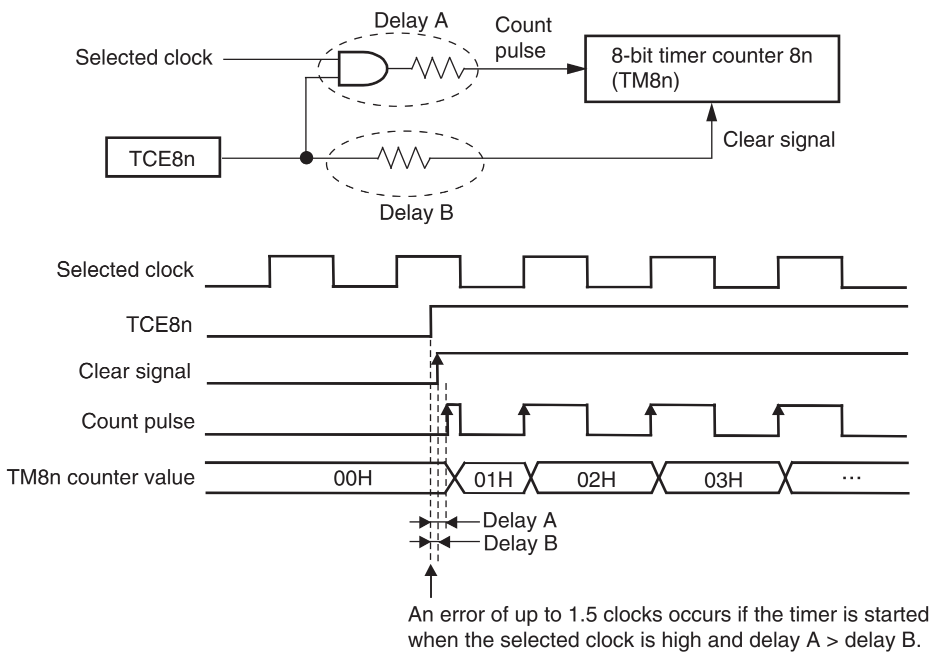
Remark n = 0 to 2

9.5 Notes on Using 8-Bit Timer/Event Counters 80 to 82

(1) Error on starting timer

An error of up to 1.5 clocks is included in the time between when the timer is started and when a match signal is generated. This is because the rising edge is detected and the counter is incremented if the timer is started while the selected clock is high (see **Figure 9-13**).

Figure 9-13. Case of Error Occurrence of up to 1.5 Clocks



Remark n = 0 to 2

(2) Count value if external clock input from TI8n pin is selected

When the rising edge of the external clock signal input from the TI8n pin is selected as the count clock, the count value may start from 01H if the timer is enabled (TCE8n = 0 → 1) while the TI8n pin is high. This is because the input signal of the TI8n pin is internally ANDed with the TCE8n signal. Consequently, the counter is incremented because the rising edge of the count clock is input to the timer immediately when the TCE8n pin is set. Depending on the delay timing, the count value is incremented by one if the rising edge is input after the counter is cleared. Counting is not affected if the rising edge is input before the counter is cleared (the counter operates normally).

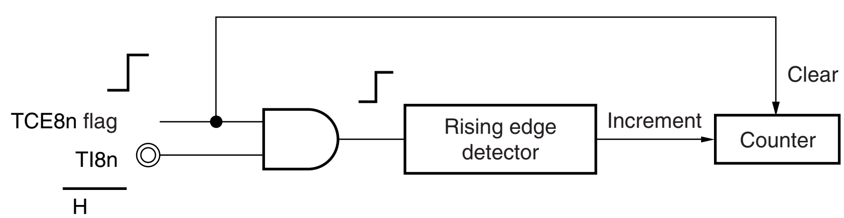
By the same factor as the above, when the falling edge of the external clock signal input from the TI8n pin is selected as the count clock, the count value may start from 01H if the timer is enabled (TCE8n = 0 → 1) while the TI8n pin is low.

Use the timer being aware that it has an error of one count, or take either of the following actions A or B.

<Action A> Always start the timer while the TI8n pin is low if the rising edge is selected.
Always start the timer while the TI8n pin is high if the falling edge is selected

<Action B> Save the count value to a control register when the timer is started, SUB the count value with the count value saved to the control register when reading the count value, and take the result of SUB as the true count value.

Figure 9-14. Counting Operation if Timer Is Started When TI8n Is High (When the rising edge is selected)

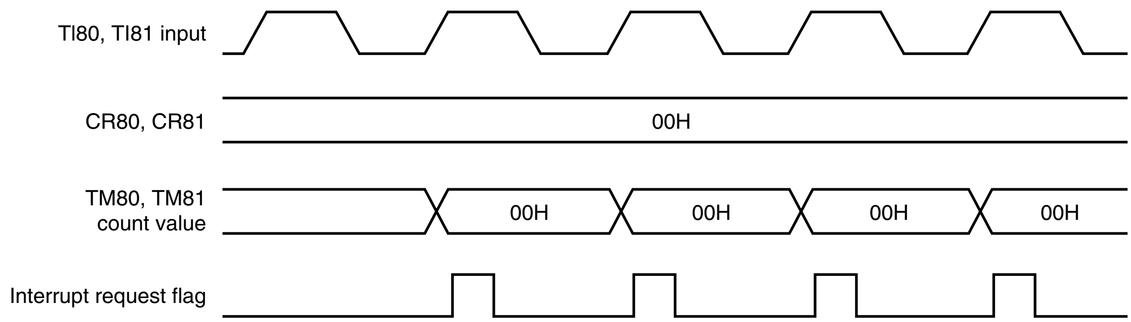


(3) Setting of 8-bit compare register 8n

8-bit compare register 8n (CR8n) can be set to 00H.

Therefore, one pulse can be counted when an 8-bit timer/event counter operates as an event counter.

Figure 9-15. External Event Counter Operation Timing



Cautions 1. When CR8n is rewritten to timer counter operation mode (PWME8n (8-bit timer mode control register 8n (TMC8n)) = 0), be sure to stop the timer operation beforehand. If CR8n is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

2. If CR8n is rewritten during timer operation in the PWM operation mode (PWME8n = 1), pulses may not be generated for one cycle after the rewrite.

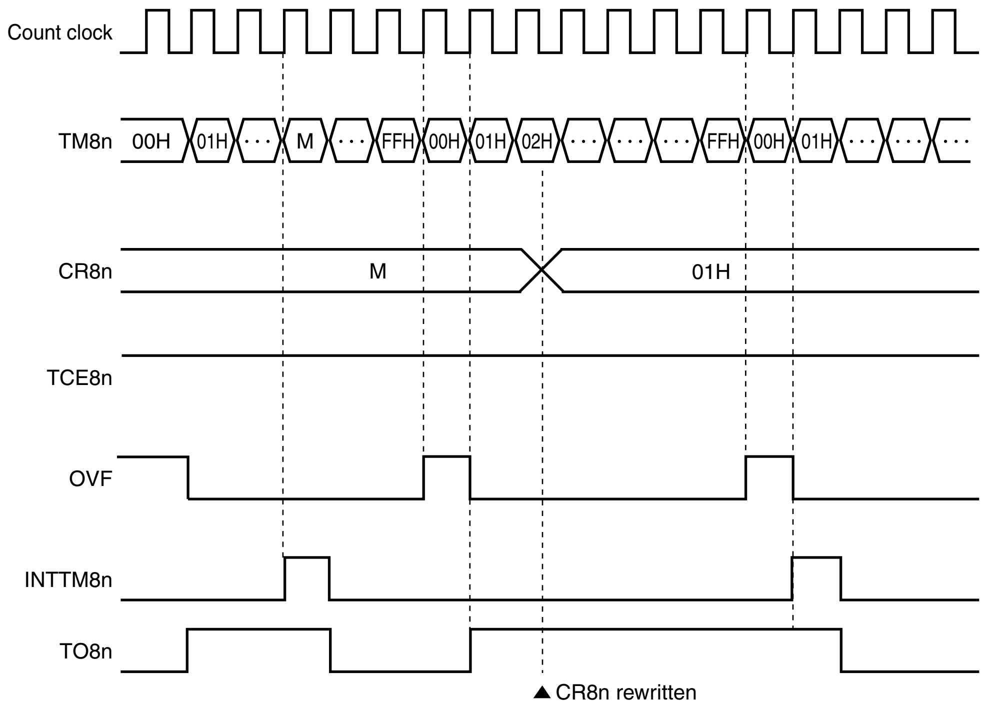
3. Do not set CR8n to 00H in PWM operation mode; otherwise, PWM may not be output normally.

Remark n = 0 to 2

(4) Timer operation after compare register is rewritten during PWM output

When 8-bit compare register 8n (CR8n) is rewritten during PWM output, if the new value is smaller than that of 8-bit timer/counter 8n (TM8n), a high-level signal may be output for the next cycle (256 count pulses) after the CR8n value is rewritten. Figure 9-16 shows the timing at which the high-level signal is output.

Figure 9-16. Operation Timing After Compare Register Is Rewritten During PWM Output



M = 01H to FFH

Remark n = 0 to 2

(5) Cautions when STOP mode is set

Be sure to stop timer operations (TCE8n = 0) before executing the STOP instruction.

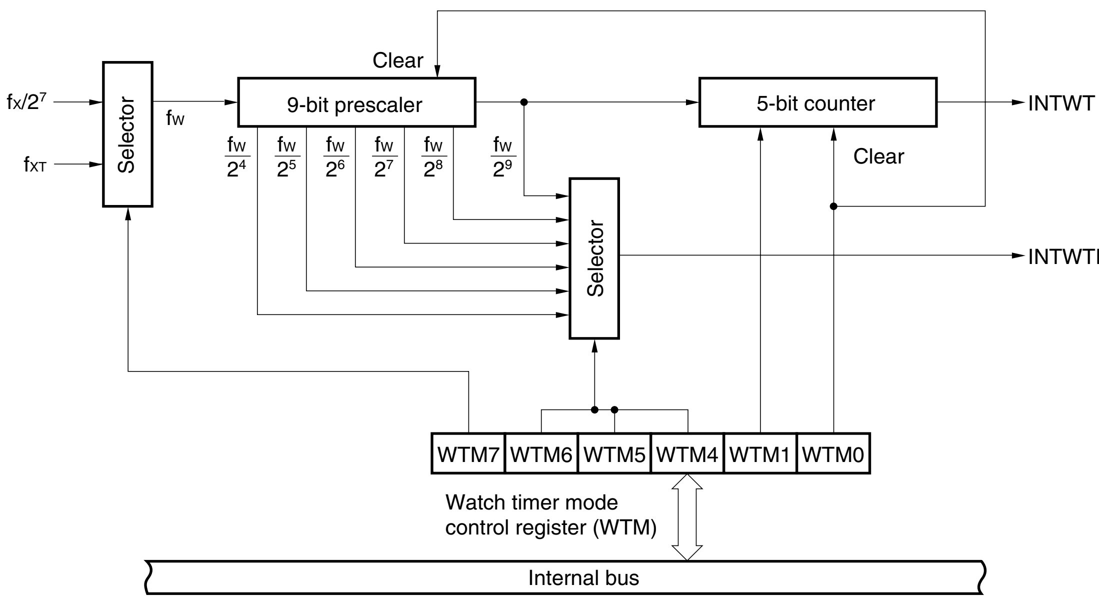
10.1 Watch Timer Functions

The watch timer has the following functions.

- Watch timer
- Interval timer

The watch and interval timers can be used at the same time.
Figure 10-1 is a block diagram of the watch timer.

Figure 10-1. Block Diagram of Watch Timer



(1) Watch timer

The 4.19 MHz main system clock or 32.768 kHz subsystem clock is used to issue an interrupt request (INTWT) at 0.5-second intervals.

Caution When the main system clock is operating at 5.0 MHz, it cannot be used to generate a 0.5-second interval. In this case, the subsystem clock, which operates at 32.768 kHz, should be used instead.

(2) Interval timer

The interval timer is used to generate an interrupt request (INTWTI) at specified intervals.

Table 10-1. Interval Generated Using Interval Timer

Interval	At f_X = 10.0 MHz[Note]	At f_X = 5.0 MHz	At f_X = 4.19 MHz	At f_{XT} = 32.768 kHz
$2^4 \times 1/f_W$	204 μs	409 μs	489 μs	488 μs
$2^5 \times 1/f_W$	409 μs	819 μs	978 μs	977 μs
$2^6 \times 1/f_W$	819 μs	1.64 ms	1.96 ms	1.95 ms
$2^7 \times 1/f_W$	1.64 ms	3.28 ms	3.91 ms	3.91 ms
$2^8 \times 1/f_W$	3.28 ms	6.55 ms	7.82 ms	7.81 ms
$2^9 \times 1/f_W$	6.55 ms	13.1 ms	15.6 ms	15.6 ms

Note Expanded-specification products only.

Remarks 1. f_W: Watch timer clock frequency ($f_X/2^7$ or f_{XT})

2. f_X: Main system clock oscillation frequency

3. f_{XT}: Subsystem clock oscillation frequency

10.2 Watch Timer Configuration

The watch timer consists of the following hardware.

Table 10-2. Watch Timer Configuration

Item	Configuration
Counter	5 bits × 1
Prescaler	9 bits × 1
Control register	Watch timer mode control register (WTM)

10.3 Watch Timer Control Register

The watch timer mode control register (WTM) is used to control the watch timer.

- Watch timer mode control register (WTM)
  WTM selects a count clock for the watch timer and specifies whether to enable operation of the timer. It also specifies the prescaler interval and how the 5-bit counter is controlled.
  WTM is set with a 1-bit or 8-bit memory manipulation instruction.
  $\overline{\text{RESET}}$ input sets WTM to 00H.

Figure 10-2. Format of Watch Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
WTM	WTM7	WTM6	WTM5	WTM4	0	0	WTM1	WTM0	FF4AH	00H	R/W

WTW7		Watch timer count clock (f_W) section	
		At f_X = 10.0 MHz[Note] or f_{XT} = 32.768 kHz operation	At f_X = 5.0 MHz or f_{XT} = 32.768 kHz operation
0	$f_X/2^7$	78.2 kHz	39.1 kHz
1	f_{XT}	32.768 kHz	

WTM6	WTM5	WTM4	Prescaler interval selection
0	0	0	$2^4/f_W$ (488 μs)
0	0	1	$2^5/f_W$ (977 μs)
0	1	0	$2^6/f_W$ (1.95 ms)
0	1	1	$2^7/f_W$ (3.91 ms)
1	0	0	$2^8/f_W$ (7.81 ms)
1	0	1	$2^9/f_W$ (15.6 ms)
Other than above			Setting prohibited

WTM1	Control of 5-bit counter operation
0	Cleared after stop
1	Started

WTM0	Watch timer operation
0	Operation disabled (both prescaler and timer cleared)
1	Operation enabled

Note Expanded-specification products only.

Remarks 1. f_W: Watch timer clock frequency ($f_X/2^7$ or f_{XT})

2. f_X: Main system clock oscillation frequency

3. f_{XT}: Subsystem clock oscillation frequency

4. The values in parentheses apply to operation at f_W = 32.768 kHz.

10.4 Watch Timer Operation

10.4.1 Operation as watch timer

The main system clock (4.19 MHz) or subsystem clock (32.768 kHz) is used to enable the watch timer to operate at 0.5-second intervals.

The watch timer is used to generate an interrupt request at specified intervals.

By setting bits 0 and 1 (WTM0 and WTM1) of the watch timer mode control register (WTM) to 1, the watch timer starts counting. By setting them to 0, the 5-bit counter is cleared and the watch timer stops counting.

Only the watch timer can be started form zero seconds by clearing WTM1 to 0 when the interval timer and watch timer operate at the same time. In this case, however, an error of up to $2^9 \times 1/f_W$ seconds may occur in the overflow (INTWT) after the zero-second start of the watch timer because the 9-bit prescaler is not cleared to 0.

10.4.2 Operation as interval timer

The interval timer is used to repeatedly generate an interrupt request at the interval specified by a count value set in advance.

The interval can be selected by bits 4 to 6 (WTM4 to WTM6) of the watch timer mode control register (WTM).

Table 10-3. Interval Generated Using Interval Timer

WTM6	WTM5	WTM4	Interval	At f_X = 10.0 MHz[Note]	At f_X = 5.0 MHz	At f_X = 4.19 MHz	At f_{XT} = 32.768 kHz
0	0	0	$2^4 \times 1/f_W$	204 μs	409 μs	489 μs	488 μs
0	0	1	$2^5 \times 1/f_W$	409 μs	819 μs	978 μs	977 μs
0	1	0	$2^6 \times 1/f_W$	819 μs	1.64 ms	1.96 ms	1.95 ms
0	1	1	$2^7 \times 1/f_W$	1.64 ms	3.28 ms	3.91 ms	3.91 ms
1	0	0	$2^8 \times 1/f_W$	3.27 ms	6.55 ms	7.82 ms	7.81 ms
1	0	1	$2^9 \times 1/f_W$	6.55 ms	13.1 ms	15.6 ms	15.6 ms
Other than above			Setting prohibited				

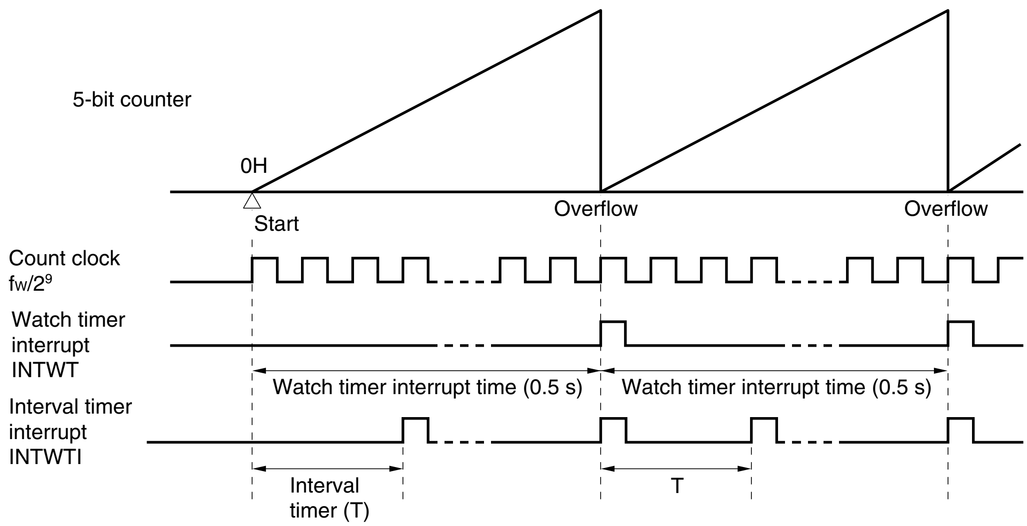
Note Expanded-specification products only.

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

3. f_W: Watch timer clock frequency

Figure 10-3. Watch Timer/Interval Timer Operation Timing



Caution **When operation of the watch timer and 5-bit counter operation is enabled by setting bit 0 (WTM0) of the watch timer mode control register (WTM) to 1, the interval until the first interrupt request (INTWT) is generated after the register is set does not exactly match the watch timer interrupt time (0.5s). This is because there is a delay of one 9-bit prescaler output cycle until the 5-bit counter starts counting. Subsequently, however, the INTWT signal is generated at the specified intervals.**

Remarks 1. fw: Watch timer clock frequency

2. The values in parentheses apply to operation at fw = 32.768 kHz.

CHAPTER 11 WATCHDOG TIMER

11.1 Watchdog Timer Functions

The watchdog timer has the following functions.

- Watchdog timer
- Interval timer

Caution Select the watchdog timer mode or interval timer mode by using the watchdog timer mode register (WDTM).

(1) Watchdog timer

The watchdog timer is used to detect inadvertent program loops. When an inadvertent loop is detected, a non-maskable interrupt or a $\overline{\text{RESET}}$ signal can be generated.

Table 11-1. Inadvertent Loop Detection Time of Watchdog Timer

Inadvertent Loop Detection Time	At fx = 10.0 MHz[Note]	At fx = 5.0 MHz
$2^{11} \times 1/fx$	205 μs	410 μs
$2^{13} \times 1/fx$	819 μs	1.64 ms
$2^{15} \times 1/fx$	3.27 ms	6.55 ms
$2^{17} \times 1/fx$	13.1 ms	26.2 ms

Note Expanded-specification products only.

Remark fx: Main system clock oscillation frequency

(2) Interval timer

The interval timer generates an interrupt at an arbitrary interval set in advance.

Table 11-2. Interval Time

Interval	At fx = 10.0 MHz[Note]	At fx = 5.0 MHz
$2^{11} \times 1/fx$	205 μs	410 μs
$2^{13} \times 1/fx$	819 μs	1.64 ms
$2^{15} \times 1/fx$	3.27 ms	6.55 ms
$2^{17} \times 1/fx$	13.1 ms	26.2 ms

Note Expanded-specification products only.

Remark fx: Main system clock oscillation frequency

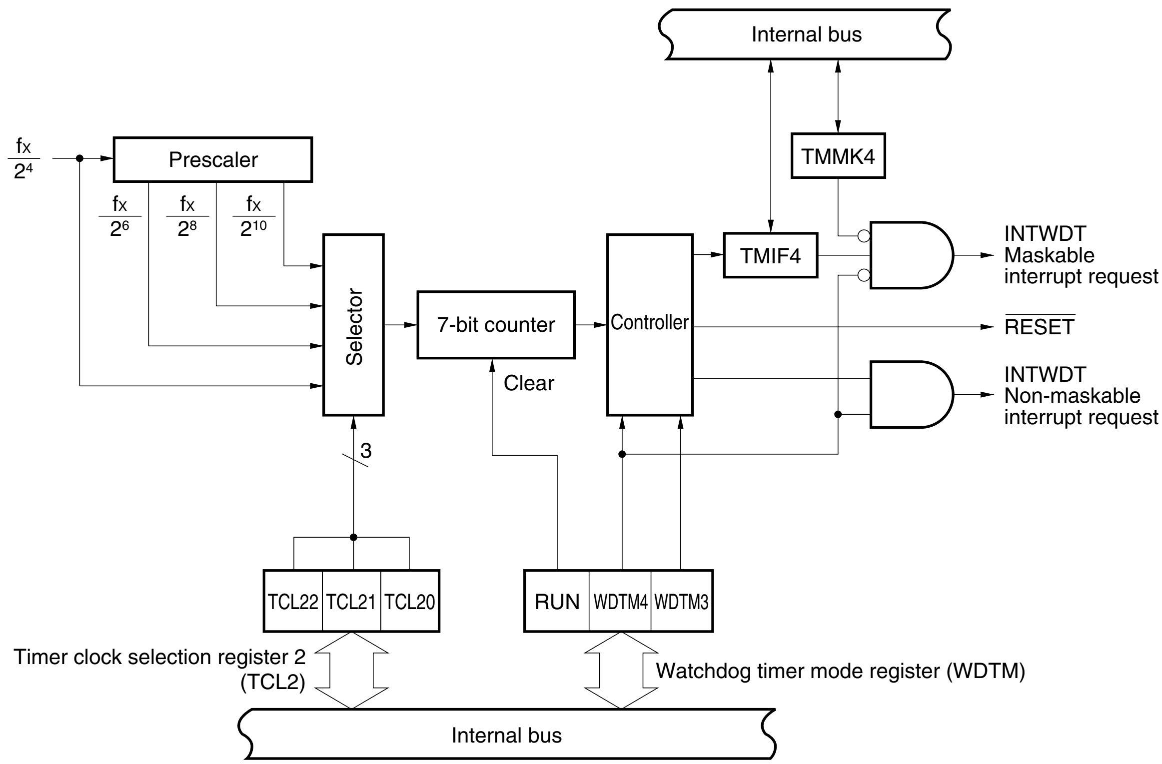
11.2 Watchdog Timer Configuration

The watchdog timer consists of the following hardware.

Table 11-3. Configuration of Watchdog Timer

Item	Configuration
Control registers	Timer clock selection register 2 (TCL2) Watchdog timer mode register (WDTM)

Figure 11-1. Block Diagram of Watchdog Timer



11.3 Watchdog Timer Control Registers

The following two types of registers are used to control the watchdog timer.

- Timer clock selection register 2 (TCL2)
- Watchdog timer mode register (WDTM)

(1) Timer clock selection register 2 (TCL2)

This register sets the watchdog timer count clock.

TCL2 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TCL2 to 00H.

Figure 11-2. Format of Timer Clock Selection Register 2

Symbol	7	6	5	4	3	2	1	0	Address	Address	R/W
TCL2	0	0	0	0	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

TCL22	TCL21	TCL20	Watchdog timer count clock selection			Interval		
				At fx = 10.0 MHz[Note]	At fx = 5.0 MHz		At fx = 10.0 MHz[Note]	At fx = 5.0 MHz
0	0	0	$fx/2^4$	625.0 kHz	312.5 kHz	$2^{11}/fx$	205 μs	410 μs
0	1	0	$fx/2^6$	156.2 kHz	78.1 kHz	$2^{13}/fx$	819 μs	1.64 ms
1	0	0	$fx/2^8$	39.0 kHz	19.5 kHz	$2^{15}/fx$	3.27 ms	6.55 ms
1	1	0	$fx/2^{10}$	9.76 kHz	4.88 kHz	$2^{17}/fx$	13.1 ms	26.2 ms
Other than above			Setting prohibited					

Note Expanded-specification products only.

Remark fx: Main system clock oscillation frequency

(2) Watchdog timer mode register (WDTM)

This register sets an operation mode of the watchdog timer, and enables/disables counting of the watchdog timer.

WDTM is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears WDTM to 00H.

Figure 11-3. Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

RUN	Watchdog timer operation selection[Note 1]
0	Stop counting
1	Clear counter and start counting

WDTM4	WDTM3	Watchdog timer operation mode selection[Note 2]
0	0	Operation stop
0	1	Interval timer mode (generates a maskable interrupt upon overflow occurrence)[Note 3]
1	0	Watchdog timer mode 1 (generates a non-maskable interrupt upon overflow occurrence)
1	1	Watchdog timer mode 2 (starts reset operation upon overflow occurrence.)

Notes 1. Once RUN has been set to 1, it cannot be cleared to 0 by software. Therefore, when counting is started, it cannot be stopped by any means other than $\overline{\text{RESET}}$ input.

2. Once WDTM3 and WDTM4 have been set to 1, they cannot be cleared to 0 by software.

3. The watchdog timer starts operations as an interval timer when RUN is set to 1.

Cautions 1. When the watchdog timer is cleared by setting RUN to 1, the actual overflow time is up to 0.8% shorter than the time set by timer clock selection register 2 (TCL2).

2. To set watchdog timer mode 1 or 2, set WDTM4 to 1 after confirming that TMIF4 (bit 0 of interrupt request flag register 0 (IF0)) is set to 0. When watchdog timer mode 1 or 2 is selected with TMIF4 set to 1, a non-maskable interrupt is generated upon the completion of rewriting WDTM4.

11.4 Watchdog Timer Operation

11.4.1 Operation as watchdog timer

The watchdog timer detects an inadvertent program loop when bit 4 (WDTM4) of the watchdog timer mode register (WDTM) is set to 1.

The count clock (inadvertent loop detection time interval) of the watchdog timer can be selected by bits 0 to 2 (TCL20 to TCL22) of timer clock selection register 2 (TCL2). By setting bit 7 (RUN) of WDTM to 1, the watchdog timer is started. Set RUN to 1 within the set inadvertent loop detection time interval after the watchdog timer has been started. By setting RUN to 1, the watchdog timer can be cleared and start counting. If RUN is not set to 1, and the inadvertent loop detection time is exceeded, a system reset signal or a non-maskable interrupt is generated, depending on the value of bit 3 (WDTM3) of WDTM.

The watchdog timer continues operation in HALT mode, but stops in STOP mode. Therefore, first set RUN to 1 to clear the watchdog timer before executing the STOP instruction.

Cautions 1. The actual inadvertent loop detection time may be up to 0.8% shorter than the set time.

2. When the subsystem clock is selected as the CPU clock, watchdog timer count operation is stopped. Even when the main system clock continues oscillating in this case, the watchdog timer count operation is stopped.

Table 11-4. Inadvertent Loop Detection Time of Watchdog Timer

TCL22	TCL21	TCL20	Inadvertent Loop Detection Time	At fx = 10.0 MHz^Note	At fx = 5.0 MHz
0	0	0	$2^{11} \times 1/f_X$	205 μs	410 μs
0	1	0	$2^{13} \times 1/f_X$	819 μs	1.64 ms
1	0	0	$2^{15} \times 1/f_X$	3.27 ms	6.55 ms
1	1	0	$2^{17} \times 1/f_X$	13.1 ms	26.2 ms

Note Expanded-specification products only.

Remark fx: Main system clock oscillation frequency

11.4.2 Operation as interval timer

When bits 4 and 3 (WDTM4, WDTM3) of the watchdog timer mode register (WDTM) are set to 0 and 1, respectively, the watchdog timer operates as an interval timer that repeatedly generates an interrupt at intervals specified by a count value set in advance.

Select a count clock (or interval) by setting bits 0 to 2 (TCL20 to TCL22) of timer clock selection register 2 (TCL2). The watchdog timer starts operation as an interval timer when the RUN bit (bit 7 of WDTM) is set to 1.

In interval timer mode, the interrupt mask flag (TMMK4) is valid, and a maskable interrupt (INTWDT) can be generated. The priority of INTWDT is set as the highest of all the maskable interrupts.

The interval timer continues operation in HALT mode, but stops in STOP mode. Therefore, first set RUN to 1 to clear the interval timer before executing the STOP instruction.

Cautions 1. Once bit 4 (WDTM4) of WDTM is set to 1 (when watchdog timer mode is selected), interval timer mode is not set unless a $\overline{\text{RESET}}$ signal is input.

2. The interval time may be up to 0.8% shorter than the set time when WDTM has just been set.

Table 11-5. Interval Time of Interval Timer

TCL22	TCL21	TCL20	Interval	At fx = 10.0 MHz[Note]	At fx = 5.0 MHz
0	0	0	$2^{11} \times 1/f_X$	205 μs	410 μs
0	1	0	$2^{13} \times 1/f_X$	819 μs	1.64 ms
1	0	0	$2^{15} \times 1/f_X$	3.27 ms	6.55 ms
1	1	0	$2^{17} \times 1/f_X$	13.1 ms	26.2 ms

Note Expanded-specification products only.

Remark fx: Main system clock oscillation frequency

12.1 8-Bit A/D Converter Functions

The 8-bit A/D converter is an 8-bit resolution converter that converts an analog input to a digital signal. This converter can control eight channels (ANI0 to ANI7) of analog inputs.

A/D conversion can be started only by software.

One of analog inputs ANI0 to ANI7 is selected for A/D conversion. A/D conversion is performed repeatedly, with an interrupt request (INTAD0) being issued each time A/D conversion is completed.

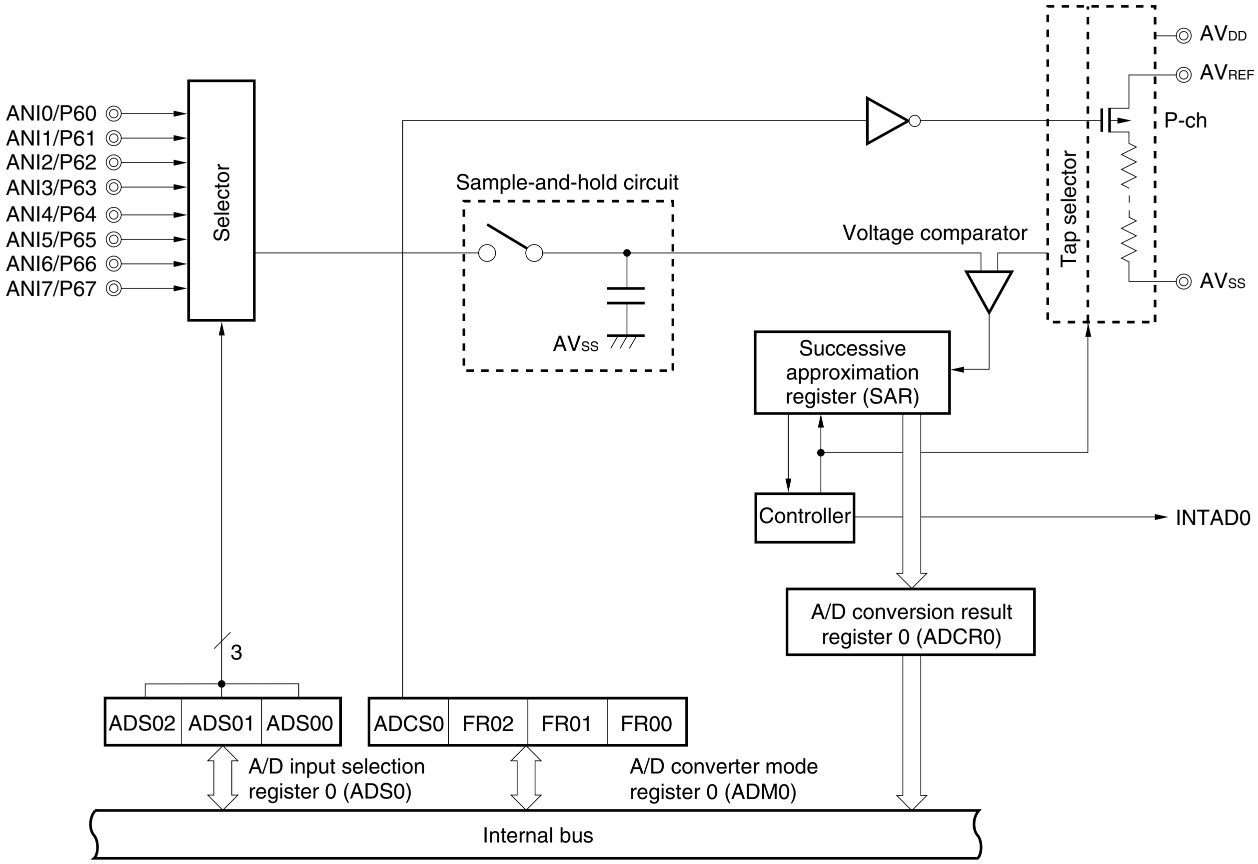
12.2 8-Bit A/D Converter Configuration

The 8-bit A/D converter consists of the following hardware.

Table 12-1. Configuration of 8-Bit A/D Converter

Item	Configuration
Analog input	8 channels (ANI0 to ANI7)
Registers	Successive approximation register (SAR) A/D conversion result register 0 (ADCR0)
Control registers	A/D converter mode register 0 (ADM0) A/D input selection register 0 (ADS0)

Figure 12-1. Block Diagram of 8-Bit A/D Converter



(1) Successive approximation register (SAR)

SAR receives the result of comparing an analog input voltage and a voltage at the voltage tap (comparison voltage), received from the series resistor string, starting from the most significant bit (MSB).

Upon receiving all the bits, down to the least significant bit (LSB), that is, upon the completion of A/D conversion, SAR sends its contents to A/D conversion result register 0 (ADCR0).

(2) A/D conversion result register 0 (ADCR0)

ADCR0 holds the result of A/D conversion. Each time A/D conversion ends, the conversion result in the successive approximation register is loaded into ADCR0, which is an 8-bit register.

ADCR0 can be read with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

(3) Sample-and-hold circuit

The sample-and-hold circuit samples consecutive analog inputs from the input circuit, one by one, and sends them to the voltage comparator. The sampled analog input voltage is held during A/D conversion.

(4) Voltage comparator

The voltage comparator compares an analog input with the voltage output by the series resistor string.

(5) Series resistor string

The series resistor string is configured between AV_{REF} and AV_{SS}. It generates the reference voltages against which analog inputs are compared.

(6) ANI0 to ANI7

The ANI0 to ANI7 pins are the 8-channel analog input pins for the A/D converter. They are used to receive the analog signals for A/D conversion.

Caution Do not supply the ANI0 to ANI7 pins with voltages that fall outside the rated range. If a voltage greater than or equal to AV_{REF} or less than AV_{SS} (even if within the absolute maximum ratings) is supplied to any of these pins, the conversion value for the corresponding channel will be undefined. Furthermore, the conversion values for the other channels may also be affected.

(7) AV_{REF}

This pin inputs the A/D converter reference voltage.
It converts signals input to ANI0 to ANI7 into digital signals according to the voltage applied between AV_{REF} and AV_{SS}.

(8) AV_{SS} pin

The AV_{SS} pin is a ground potential pin for the A/D converter. This pin must be held at the same potential as the V_{SS0} pin, even while the A/D converter is not being used.

(9) AV_{DD} pin

The AV_{DD} pin is an analog power supply pin for the A/D converter. This pin must be held at the same potential as the V_{DD0} pin, even while the A/D converter is not being used.

12.3 8-Bit A/D Converter Control Registers

The following two registers are used to control the 8-bit A/D converter.

- A/D converter mode register 0 (ADM0)
- A/D input selection register 0 (ADS0)

(1) A/D converter mode register 0 (ADM0)

ADM0 specifies the conversion time for analog inputs. It also specifies whether to enable conversion.
ADM0 is set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears ADM0 to 00H.

Figure 12-2. Format of A/D Converter Mode Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
ADM0	ADCS0	0	FR02	FR01	FR00	0	0	0	FF80H	00H	R/W

ADCS0	A/D conversion control
0	Conversion disabled
1	Conversion enabled

FR02	FR01	FR00	A/D conversion time selection[Note 1]		
				At fx = 10.0 MHz operation[Note 2]	At fx = 5.0 MHz operation
0	0	0	144/fx	14.4 μs	28.8 μs
0	0	1	120/fx	12.0 μs	24.0 μs
0	1	0	96/fx	Setting prohibited[Note 3]	19.2 μs
1	0	0	72/fx	Setting prohibited[Note 3]	14.4 μs
1	0	1	60/fx	Setting prohibited[Note 3]	12.0 μs[Note 4]
1	1	0	48/fx	Setting prohibited[Note 3]	
Other than above			Setting prohibited		

Notes 1. Set the A/D conversion time so that it satisfies the following ratings.
<Expanded-specification products>
$4.5 \le AV_{REF} \le AV_{DD} = V_{DD} \le 5.5$ V ..... 12 μs min.
$2.7 \le AV_{REF} \le AV_{DD} = V_{DD} < 4.5$ V ..... 14 μs min.
$1.8 \le AV_{REF} \le AV_{DD} = V_{DD} < 2.7$ V ..... 28 μs min.
<Conventional products>
$2.7 \le AV_{REF} \le AV_{DD} = V_{DD} \le 5.5$ V ..... 14 μs min.
$1.8 \le AV_{REF} \le AV_{DD} = V_{DD} < 2.7$ V ..... 28 μs min.

2. Expanded-specification products only.

3. Setting prohibited because the A/D conversion time cannot satisfy the ratings in **Note 1** during operation under these fx conditions.

4. Can only be set for expanded-specification products under the following conditions:
$4.5 \le AV_{REF} \le AV_{DD} = V_{DD} \le 5.5$ V. Other settings are prohibited.

Cautions 1. The result of conversion performed immediately after bit 7 (ADCS0) is set is undefined.

2. The conversion result may be undefined after ADCS0 has been cleared to 0 (for details, see 12.5 (5) Timing of undefined A/D conversion result).

Remark fx: Main system clock oscillation frequency

(2) A/D input selection register 0 (ADS0)

ADS0 specifies the port used to input the analog voltage to be converted to a digital signal.

ADS0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ADS0 to 00H.

Figure 12-3. Format of A/D Input Selection Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ADS0	0	0	0	0	0	ADS02	ADS01	ADS00	FF84H	00H	R/W

ADS02	ADS01	ADS00	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

Caution Bits 3 to 7 must all be set to 0.

12.4 8-Bit A/D Converter Operation

12.4.1 Basic operation of 8-bit A/D converter

<1> Select a channel for A/D conversion, using A/D input selection register 0 (ADS0).

<2> The voltage supplied to the selected analog input channel is sampled using the sample and hold circuit.

<3> After sampling continues for a certain period of time, the sample and hold circuit is put on hold to keep the input analog voltage until A/D conversion is completed.

<4> Bit 7 of the successive approximation register (SAR) is set. The series resistor string tap voltage at the tap selector is set to half of AV_{REF}.

<5> The series resistor string tap voltage is compared with the analog input voltage using the voltage comparator. If the analog input voltage is higher than half of AV_{REF}, the MSB of SAR is left set. If it is lower than half of AV_{REF}, the MSB is reset.

<6> Bit 6 of SAR is set automatically, and comparison shifts to the next stage. The next tap voltage of the series resistor string is selected according to bit 7, which reflects the previous comparison result, as follows:

- Bit 7 = 1: Three quarters of AV_{REF}
- Bit 7 = 0: One quarter of AV_{REF}

The tap voltage is compared with the analog input voltage. Bit 6 is set or reset according to the result of comparison.

- Analog input voltage ≥ tap voltage: Bit 6 = 1
- Analog input voltage < tap voltage: Bit 6 = 0

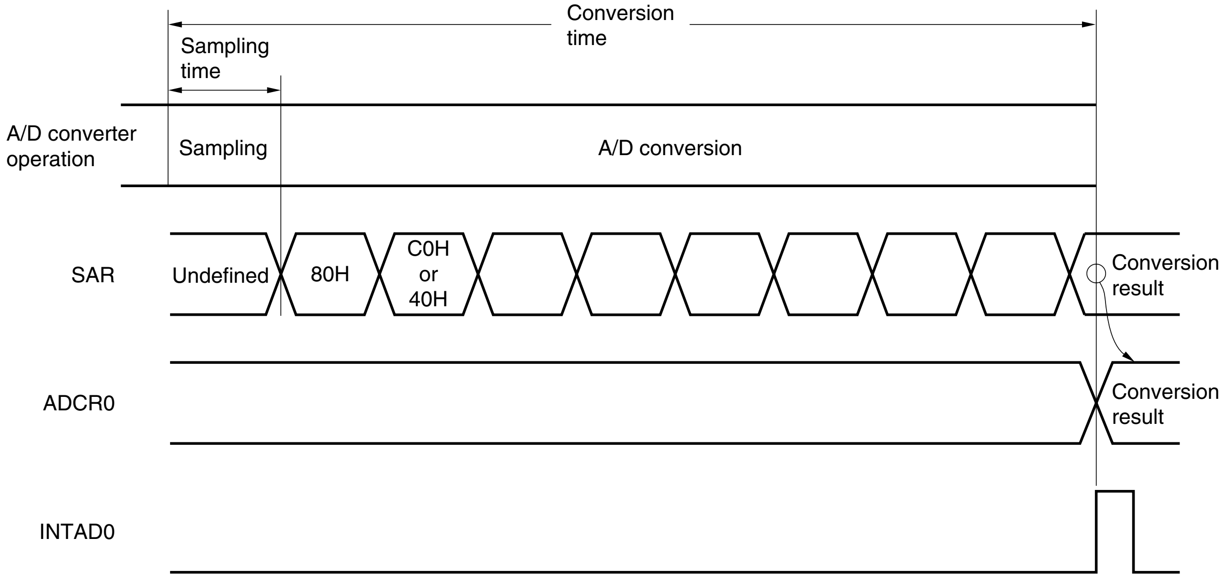
<7> Comparison is repeated until bit 0 of SAR is reached.

<8> When comparison is completed for all of the 8 bits, a significant digital result is left in SAR. This value is sent to and latched in A/D conversion result register 0 (ADCR0). At the same time, it is possible to generate an A/D conversion end interrupt request (INTAD0).

Cautions 1. The first A/D conversion value immediately after A/D conversion has been started may be undefined.

2. In standby mode, A/D converter operation is stopped.

Figure 12-4. Basic Operation of 8-Bit A/D Converter



A/D conversion continues until bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) is reset to 0 by software.

If an attempt is made to write to ADM0 or A/D input selection register 0 (ADS0) during A/D conversion, the ongoing A/D conversion is canceled. In this case, A/D conversion is restarted from the beginning, if ADCS0 is set to 1.

$\overline{\text{RESET}}$ input makes A/D conversion result register 0 (ADCR0) undefined.

12.4.2 Input voltage and conversion result

The relationships between the analog input voltage at the analog input pins (ANI0 to ANI7) and the A/D conversion result (A/D conversion result register 0 (ADCR0)) are represented by:

$$ADCR0 = INT\left(\frac{V_{IN}}{AV_{REF}} \times 256 + 0.5\right)$$

or

$$(ADCR0 - 0.5) \times \frac{AV_{REF}}{256} \leq V_{IN} < (ADCR0 + 0.5) \times \frac{AV_{REF}}{256}$$

INT( ): Function that returns the integer part of a parenthesized value

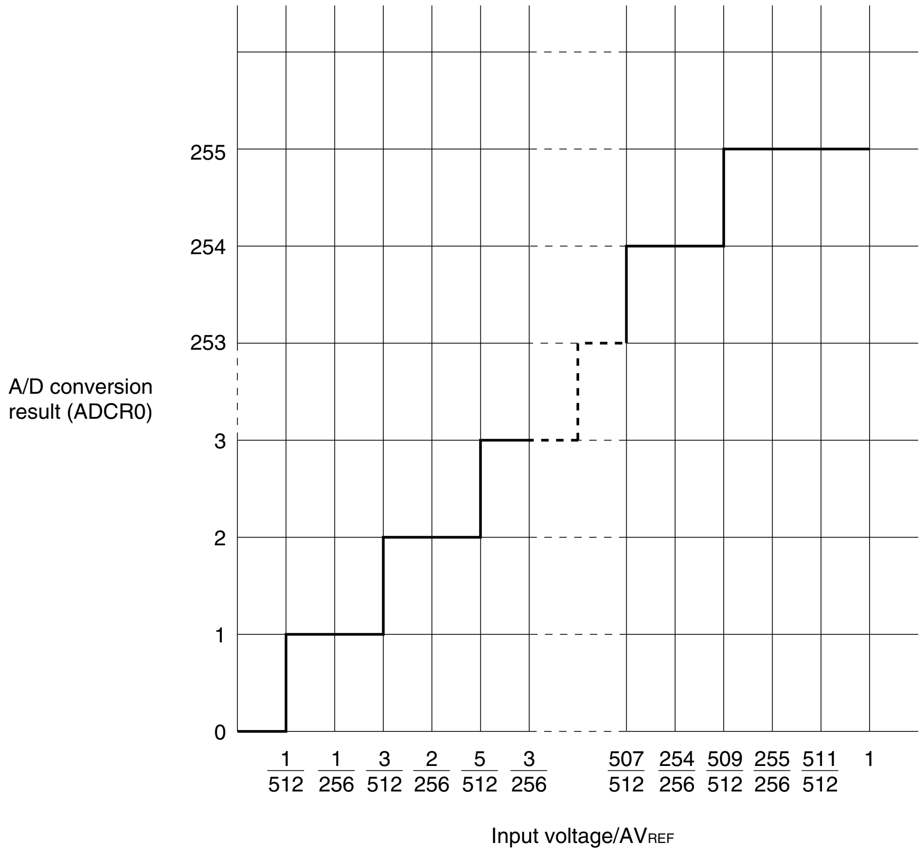
V_{IN}: Analog input voltage

AV_{REF}: Voltage of AV_{REF} pin

ADCR0: Value in A/D conversion result register 0 (ADCR0)

Figure 12-5 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 12-5. Relationship Between Analog Input Voltage and A/D Conversion Result



12.4.3 Operation mode of 8-bit A/D converter

The A/D converter is initially in select mode. In this mode, A/D input selection register 0 (ADS0) is used to select an analog input channel from ANI0 to ANI7 for A/D conversion.

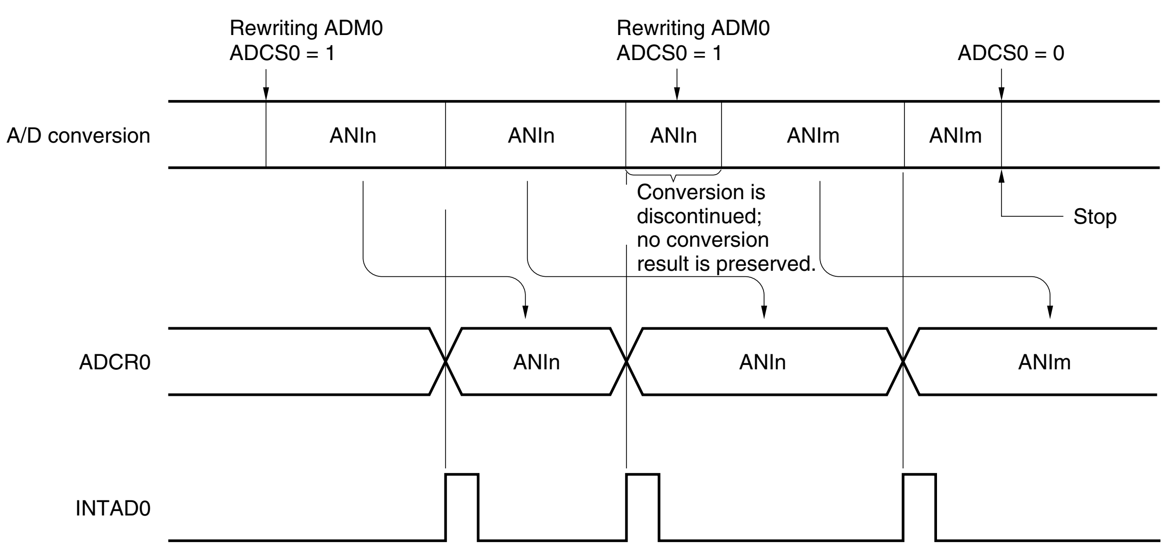
A/D conversion can be started only by software; that is, by setting A/D converter mode register 0 (ADM0).

The A/D conversion result is saved to A/D conversion result register 0 (ADCR0). At the same time, an interrupt request signal (INTAD0) is generated.

- **Software-started A/D conversion**

  Setting bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) to 1 triggers A/D conversion for the voltage applied to the analog input pin specified in A/D input selection register 0 (ADS0). Upon completion of A/D conversion, the conversion result is saved to A/D conversion result register 0 (ADCR0). At the same time, an interrupt request signal (INTAD0) is generated. Once A/D conversion is activated, and completed, another session of A/D conversion is started. A/D conversion is repeated until new data is written to ADM0. If data where ADCS0 is 1 is written to ADM0 again during A/D conversion, the ongoing session of A/D conversion is discontinued, and a new session of A/D conversion begins for the new data. If data where ADCS0 is 0 is written to ADM0 again during A/D conversion, A/D conversion is stopped immediately.

Figure 12-6. Software-Started A/D Conversion



Remarks 1. n = 0 to 7

2. m = 0 to 7

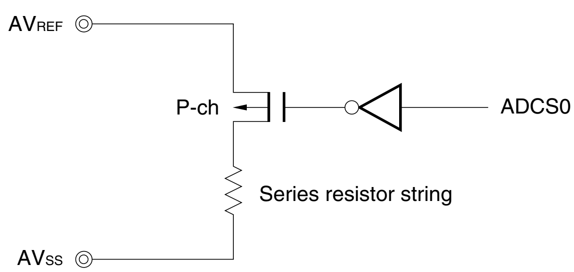
12.5 Cautions Related to 8-Bit A/D Converter

(1) Current consumption in standby mode

In standby mode, the A/D converter stops operating. Setting bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) to 0 can reduce the current consumption.

Figure 12-7 shows how to reduce the current consumption in standby mode.

Figure 12-7. How to Reduce Current Consumption in Standby Mode



(2) Input range for ANI0 to ANI7 pins

Be sure to keep the input voltage at ANI0 to ANI7 within its rating. If a voltage greater than or equal to AV_{REF} or less than or equal to AV_{SS} (even within the absolute maximum ratings) is input into a conversion channel, the conversion output of the channel becomes undefined, and the conversion output of the other channels may also be affected.

(3) Conflict

<1> Conflict between writing to A/D conversion result register 0 (ADCR0) at the end of conversion and reading from ADCR0 using instruction

Reading from ADCR0 takes precedence. After reading, the new conversion result is written to ADCR0.

<2> Conflict between writing to ADCR0 at the end of conversion and writing to A/D converter mode register 0 (ADM0) or A/D input selection register 0 (ADS0)

Writing to ADM0 or ADS0 takes precedence. ADCR0 is not written to. No A/D conversion end interrupt request signal (INTAD0) is generated.

(4) Conversion result immediately after start of A/D conversion

The first A/D conversion value immediately after A/D conversion has been started is undefined. Poll the A/D conversion end interrupt request (INTAD0) and drop the first conversion result.

(5) Timing of undefined A/D conversion result

The A/D conversion value may become undefined if the timing of the completion of A/D conversion and that to stop the A/D conversion operation conflict. Therefore, read the A/D conversion result while the A/D conversion operation is in progress. To read the A/D conversion result after the A/D conversion operation has been stopped, stop the A/D conversion operation before the next conversion operation is completed. Figures 12-8 and 12-9 show the timing at which the conversion result is read.

Figure 12-8. Conversion Result Read Timing (If Conversion Result Is Undefined)

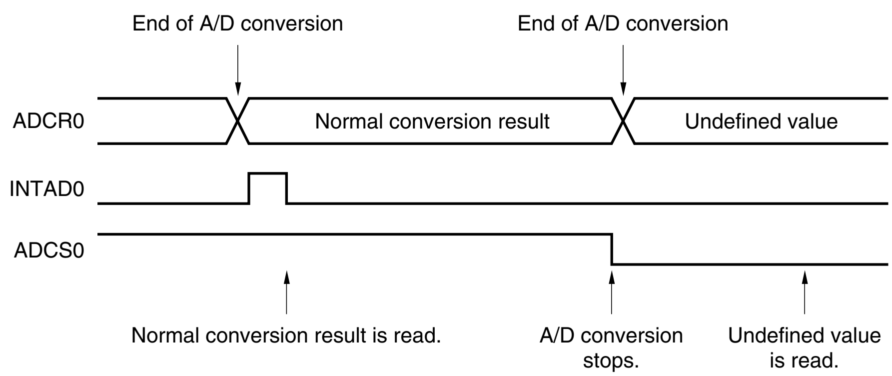
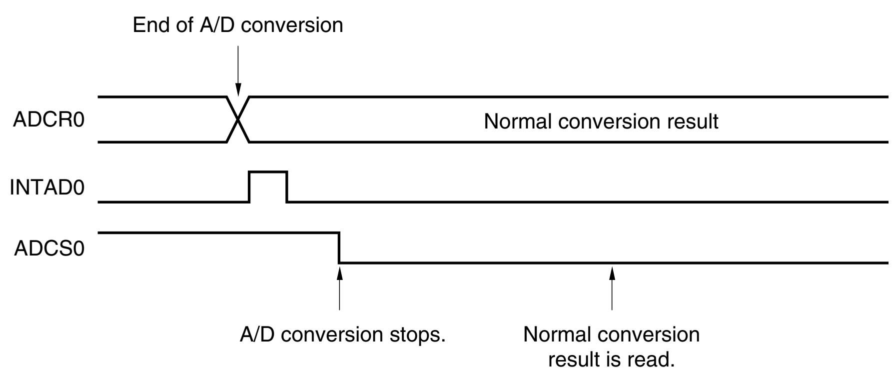


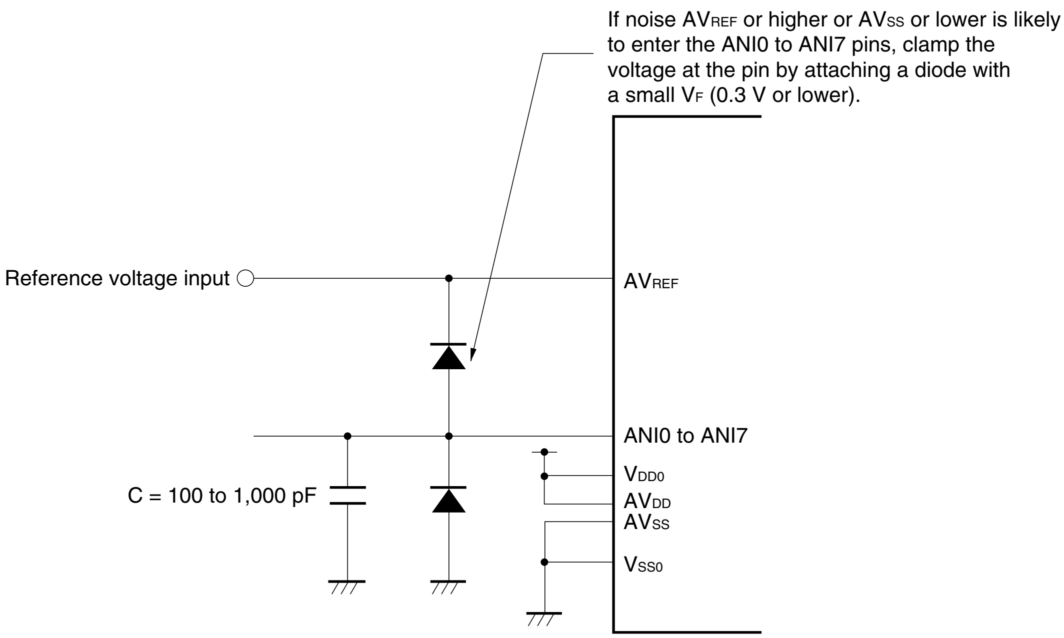
Figure 12-9. Conversion Result Read Timing (If Conversion Result Is Normal)



(6) Noise prevention

To maintain a resolution of 8 bits, watch out for noise on the AV_{REF} and ANI0 to ANI7 pins. The higher the output impedance of the analog input source, the larger the effect from noise. To reduce noise, attach an external capacitor to the relevant pins as shown in Figure 12-10.

Figure 12-10. Analog Input Pin Handling



(7) ANI0 to ANI7

The analog input pins (ANI0 to ANI7) are alternate-function pins. They are used also as port pins (P60 to P67).

If any of ANI0 to ANI7 has been selected for A/D conversion, do not execute input instructions for the ports. Otherwise, the conversion resolution may become lower.

If a digital pulse is applied to a pin adjacent to the analog input pins during A/D conversion, coupling noise may occur which prevents an A/D conversion result from being obtained as expected. Avoid applying a digital pulse to pins adjacent to the analog input pins during A/D conversion.

(8) Input impedance of ANI0 to ANI7 pins

This A/D converter charges the internal sampling capacitor for about 1/10 of the conversion time, and performs sampling.

Therefore at times other than sampling, only the leak current is output. During sampling, the current for charging the capacitor is also output, so the input impedance fluctuates and has no meaning.

However, to ensure adequate sampling, it is recommended that the output impedance of the analog input source be set to below 10 kΩ, or a 100 pF capacitor be connected to the ANI0 to ANI7 pins (see Figure 12-10).

(9) Input impedance of the AV_{REF} pin

A series resistor string of several 10 kΩ is connected across the AV_{REF} and AV_{SS} pins.

If the output impedance of the reference voltage source is high, this high impedance is eventually connected in series with the series resistor string across the AV_{REF} and AV_{SS} pins, leading to a higher reference voltage error.

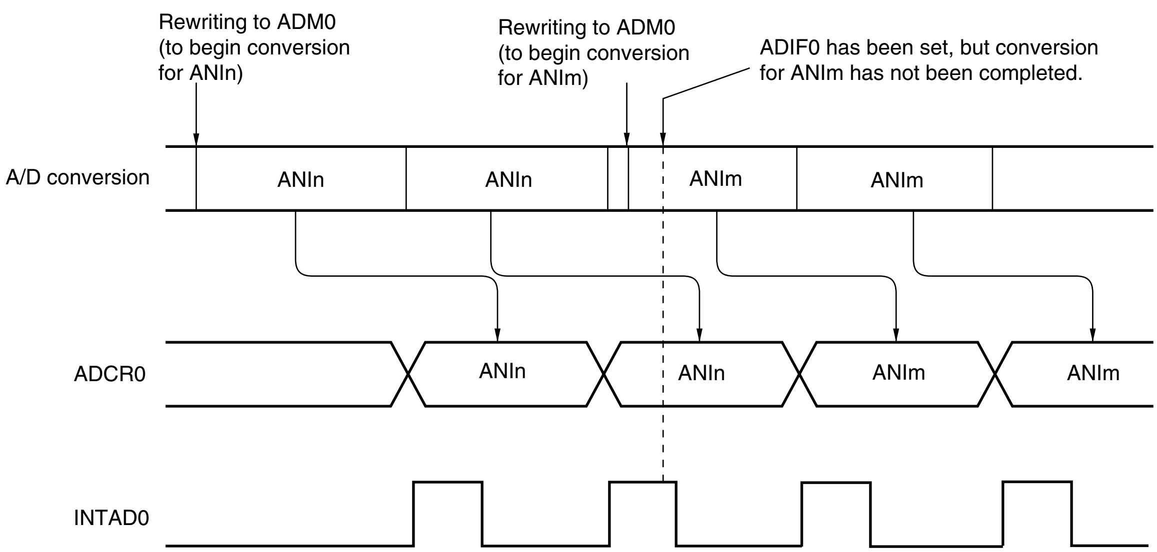
(10) Interrupt request flag (ADIF0)

Changing the content of A/D converter mode register 0 (ADM0) does not clear the interrupt request flag (ADIF0).

If the analog input pins are changed during A/D conversion, therefore, the A/D conversion result and the conversion end interrupt request flag may reflect the previous analog input immediately before writing to ADM0 occurs. In this case, ADIF0 may already be set if it is read-accessed immediately after ADM0 is write-accessed, even when A/D conversion has not been completed for the new analog input.

In addition, when A/D conversion is restarted, ADIF0 must be cleared beforehand.

Figure 12-11. A/D Conversion End Interrupt Request Generation Timing



Remarks 1. n = 0 to 7

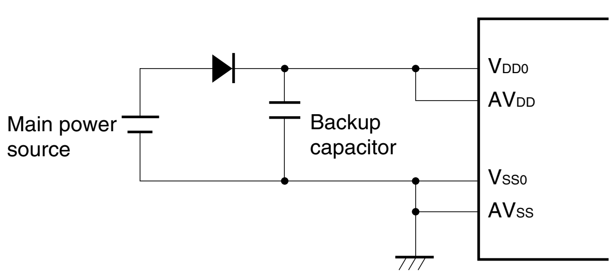
2. m = 0 to 7

(11) AV$_{DD}$ pin

The AV$_{DD}$ pin is used to supply power to the analog circuit. It is also used to supply power to the ANI0 to ANI7 input circuit.

If your application is designed to be changed to backup power, the AV$_{DD}$ pin must be supplied with the same voltage level as for the V$_{DD0}$ pin, as shown in Figure 12-12.

Figure 12-12. AV$_{DD}$ Pin Handling



13.1 10-Bit A/D Converter Functions

The 10-bit A/D converter is a 10-bit resolution converter that converts an analog input to a digital signal. This converter can control eight channels (ANI0 to ANI7) of analog inputs.

A/D conversion can be started only by software.

One of analog inputs ANI0 to ANI7 is selected for A/D conversion. A/D conversion is performed repeatedly, with an interrupt request (INTAD0) being issued each time A/D conversion is completed.

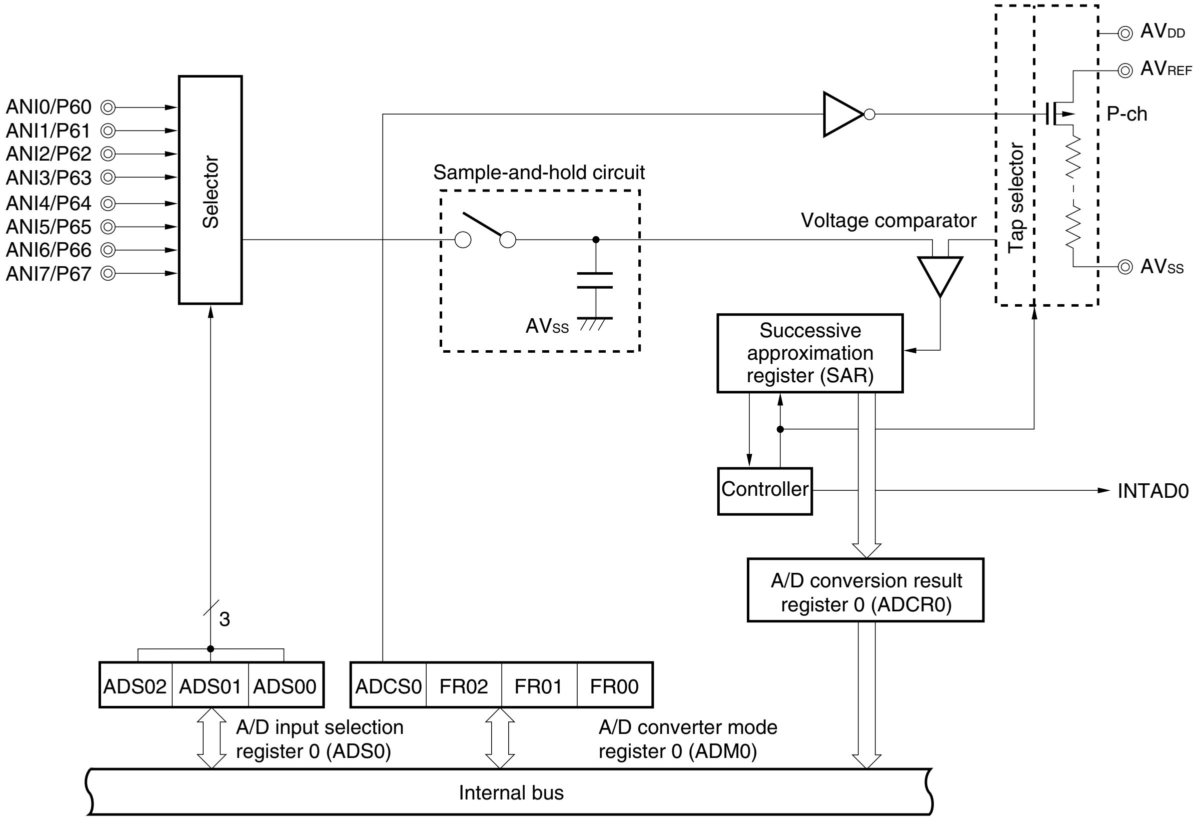
13.2 10-Bit A/D Converter Configuration

The 10-bit A/D converter consists of the following hardware.

Table 13-1. Configuration of 10-Bit A/D Converter

Item	Configuration
Analog input	8 channels (ANI0 to ANI7)
Registers	Successive approximation register (SAR) A/D conversion result register 0 (ADCR0)
Control registers	A/D converter mode register 0 (ADM0) A/D input selection register 0 (ADS0)

Figure 13-1. Block Diagram of 10-Bit A/D Converter



(1) Successive approximation register (SAR)

SAR receives the result of comparing an analog input voltage and a voltage at a voltage tap (comparison voltage), received from the series resistor string, starting from the most significant bit (MSB).

Upon receiving all the bits, down to the least significant bit (LSB), that is, upon the completion of A/D conversion, SAR sends its contents to A/D conversion result register 0 (ADCR0).

(2) A/D conversion result register 0 (ADCR0)

ADCR0 is a 16-bit register that holds the result of A/D conversion. The lower 6 bits are fixed to 0. Each time A/D conversion ends, the conversion result in the successive approximation register is loaded into ADCR0. The results are stored in ADCR0 from the most significant bit (MSB).

ADCR0 can be read with a 16-bit memory manipulation instruction.

RESET input sets ADCR0 to 0000H.

Symbol	FF15H								FF14H								Address	After reset	R/W
ADCR0											0	0	0	0	0	0	FF14H, FF15H	0000H	R

Caution When the μPD78F9177, the flash memory counterpart of the μPD789166 or μPD789167, is used, the register can be accessed in 8-bit units. However, only an object file assembled with the μPD789166 or μPD789167 can be used. The same is also true for the μPD78F9177Y, the flash memory counterpart of the μPD789166Y or μPD789167Y. When the μPD78F9177Y is used, the register can be accessed in 8-bit units. However, only an object file assembled with the μPD789166Y or μPD789167Y can be used.

(3) Sample-and-hold circuit

The sample-and-hold circuit samples consecutive analog inputs from the input circuit, one by one, and sends them to the voltage comparator. The sampled analog input voltage is held during A/D conversion.

(4) Voltage comparator

The voltage comparator compares an analog input with the voltage output by the series resistor string.

(5) Series resistor string

The series resistor string is configured between AV_{REF} and AV_{SS}. It generates the reference voltages against which analog inputs are compared.

(6) ANI0 to ANI7

The ANI0 to ANI7 pins are the 8-channel analog input pins for the A/D converter. They are used to receive the analog signals for A/D conversion.

Caution Do not supply the ANI0 to ANI7 pins with voltages that fall outside the rated range. If a voltage greater than or equal to AV_{REF} or less than or equal to AV_{SS} (even if within the absolute maximum ratings) is supplied to any of these pins, the conversion value for the corresponding channel will be undefined. Furthermore, the conversion values for the other channels may also be affected.

(7) AV_{REF} pin

This pin inputs the A/D converter reference voltage.

It converts signals input to ANI0 to ANI7 into digital signals according to the voltage applied between AV_{REF} and AV_{SS}.

(8) AV_{SS} pin

The AV_{SS} pin is a ground potential pin for the A/D converter. This pin must be held at the same potential as the V_{SS0} pin, even while the A/D converter is not being used.

(9) AV_{DD} pin

The AV_{DD} pin is an analog power supply pin for the A/D converter. This pin must be held at the same potential as the V_{DD0} pin, even while the A/D converter is not being used.

13.3 10-Bit A/D Converter Control Registers

The following two registers are used to control the 10-bit A/D converter.

- A/D converter mode register 0 (ADM0)
- A/D input selection register 0 (ADS0)

(1) A/D converter mode register 0 (ADM0)

ADM0 specifies the conversion time for analog inputs. It also specifies whether to enable conversion.
ADM0 is set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears ADM0 to 00H.

Figure 13-2. Format of A/D Converter Mode Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
ADM0	ADCS0	0	FR02	FR01	FR00	0	0	0	FF80H	00H	R/W

ADCS0	A/D conversion control
0	Conversion disabled
1	Conversion enabled

FR02	FR01	FR00	A/D conversion time selection[Note 1]		
				At fx = 10.0 MHz operation[Note 2]	At fx = 5.0 MHz operation
0	0	0	144/fx	14.4 μs	28.8 μs
0	0	1	120/fx	12.0 μs	24.0 μs
0	1	0	96/fx	Setting prohibited[Note 3]	19.2 μs
1	0	0	72/fx	Setting prohibited[Note 3]	14.4 μs
1	0	1	60/fx	Setting prohibited[Note 3]	12.0 μs[Note 4]
1	1	0	48/fx	Setting prohibited[Note 3]	
Other than above			Setting prohibited		

Notes 1. Set the A/D conversion time so that it satisfies the following ratings.
<Expanded-specification products>
$4.5 \leq AV_{REF} \leq AV_{DD} = V_{DD} \leq 5.5$ V ..... 12 μs min.
$2.7 \leq AV_{REF} \leq AV_{DD} = V_{DD} < 4.5$ V ..... 14 μs min.
$1.8 \leq AV_{REF} \leq AV_{DD} = V_{DD} < 2.7$ V ..... 28 μs min.
<Conventional products>
$2.7 \leq AV_{REF} \leq AV_{DD} = V_{DD} \leq 5.5$ V ..... 14 μs min.
$1.8 \leq AV_{REF} \leq AV_{DD} = V_{DD} < 2.7$ V ..... 28 μs min.

2. Expanded-specification products only.

3. Setting prohibited because the A/D conversion time cannot satisfy the ratings in **Note 1** during operation under these fx conditions.

4. Can only be set for expanded-specification products under the following conditions:
$4.5 \leq AV_{REF} \leq AV_{DD} = V_{DD} \leq 5.5$ V. Other settings are prohibited.

Cautions 1. The result of conversion performed immediately after bit 7 (ADCS0) is set is undefined.

2. The conversion result may be undefined after ADCS0 has been cleared to 0 (For details, see 13.5 (5) Timing of undefined A/D conversion result).

Remark fx: Main system clock oscillation frequency

(2) A/D input selection register 0 (ADS0)

ADS0 specifies the port used to input the analog voltage to be converted to a digital signal.

ADS0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ADS0 to 00H.

Figure 13-3. Format of A/D Input Selection Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ADS0	0	0	0	0	0	ADS02	ADS01	ADS00	FF84H	00H	R/W

ADS02	ADS01	ADS00	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

Caution Bits 3 to 7 must all be set to 0.

13.4 10-Bit A/D Converter Operation

13.4.1 Basic operation of 10-bit A/D converter

<1> Select a channel for A/D conversion, using A/D input selection register 0 (ADS0).

<2> The voltage supplied to the selected analog input channel is sampled using the sample and hold circuit.

<3> After sampling continues for a certain period of time, the sample and hold circuit is put on hold to keep the input analog voltage until A/D conversion is completed.

<4> Bit 9 of the successive approximation register (SAR) is set. The series resistor string tap voltage at the tap selector is set to half of AV_{REF}.

<5> The series resistor string tap voltage is compared with the analog input voltage using the voltage comparator. If the analog input voltage is higher than half of AV_{REF}, the MSB of SAR is left set. If it is lower than half of AV_{REF}, the MSB is reset.

<6> Bit 8 of SAR is set automatically, and comparison shifts to the next stage. The next tap voltage of the series resistor string is selected according to bit 9, which reflects the previous comparison result, as follows:

- Bit 9 = 1: Three quarters of AV_{REF}
- Bit 9 = 0: One quarter of AV_{REF}

The tap voltage is compared with the analog input voltage. Bit 8 is set or reset according to the result of comparison.

- Analog input voltage ≥ tap voltage: Bit 8 = 1
- Analog input voltage < tap voltage: Bit 8 = 0

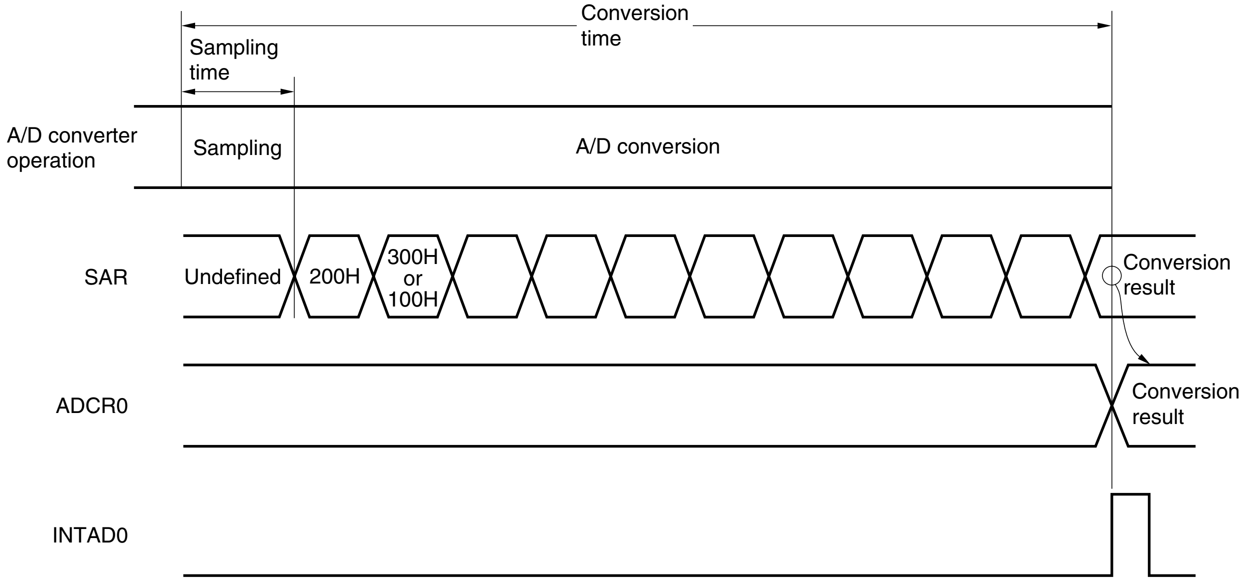
<7> Comparison is repeated until bit 0 of SAR is reached.

<8> When comparison is completed for all of the 10 bits, a significant digital result is left in SAR. This value is sent to and latched in A/D conversion result register 0 (ADCR0). At the same time, it is possible to generate an A/D conversion end interrupt request (INTAD0).

Cautions 1. The first A/D conversion value immediately after A/D conversion has been started may be undefined.

2. In standby mode, A/D converter operation is stopped.

Figure 13-4. Basic Operation of 10-Bit A/D Converter



A/D conversion continues until bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) is reset to 0 by software.

If an attempt is made to write to ADM0 or A/D input selection register 0 (ADS0) during A/D conversion, the ongoing A/D conversion is canceled. In this case, A/D conversion is restarted from the beginning, if ADCS0 is set to 1.

$\overline{\text{RESET}}$ input makes A/D conversion result register 0 (ADCR0) undefined.

13.4.2 Input voltage and conversion result

The relationships between the analog input voltage at the analog input pins (ANI0 to ANI7) and the A/D conversion result (A/D conversion result register 0 (ADCR0)) are represented by:

$$\text{ADCR0} = \text{INT}\left(\frac{V_{IN}}{AV_{REF}} \times 1{,}024 + 0.5\right)$$

or

$$(\text{ADCR0} - 0.5) \times \frac{AV_{REF}}{1{,}024} \leq V_{IN} < (\text{ADCR0} + 0.5) \times \frac{AV_{REF}}{1{,}024}$$

INT( ): Function that returns the integer part of a parenthesized value

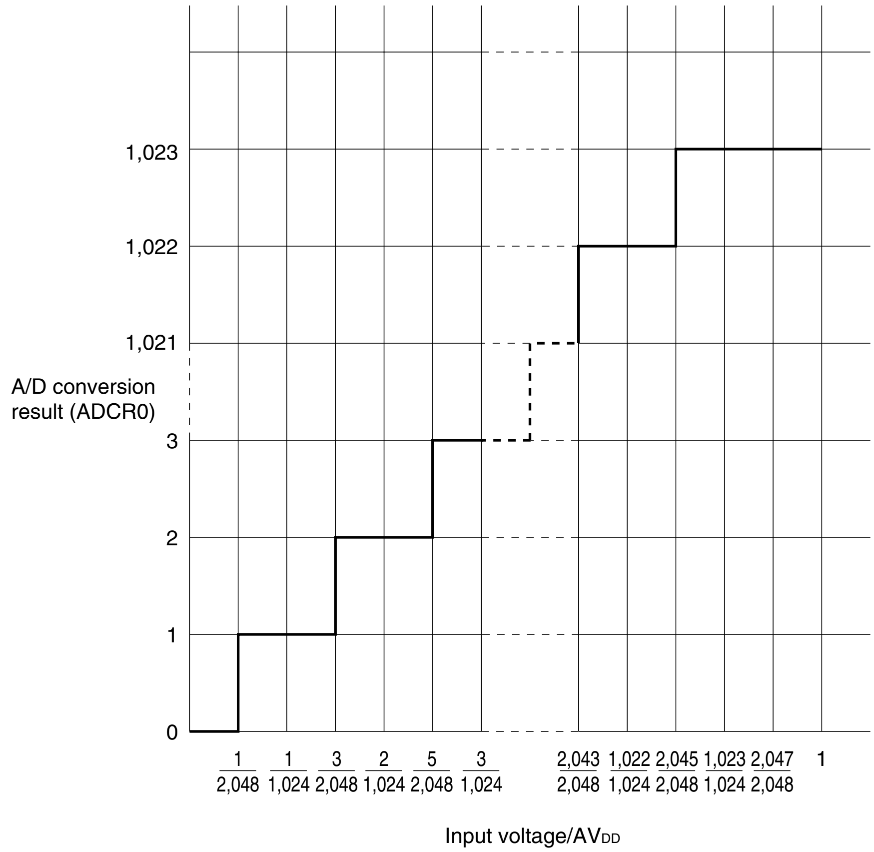
V_{IN}: Analog input voltage

AV_{REF}: Voltage of AV_{REF} pin

ADCR0: Value in A/D conversion result register 0 (ADCR0)

Figure 13-5 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 13-5. Relationship Between Analog Input Voltage and A/D Conversion Result



13.4.3 Operation mode of 10-bit A/D converter

The A/D converter is initially in select mode. In this mode, A/D input selection register 0 (ADS0) is used to select an analog input channel from ANI0 to ANI7 for A/D conversion.

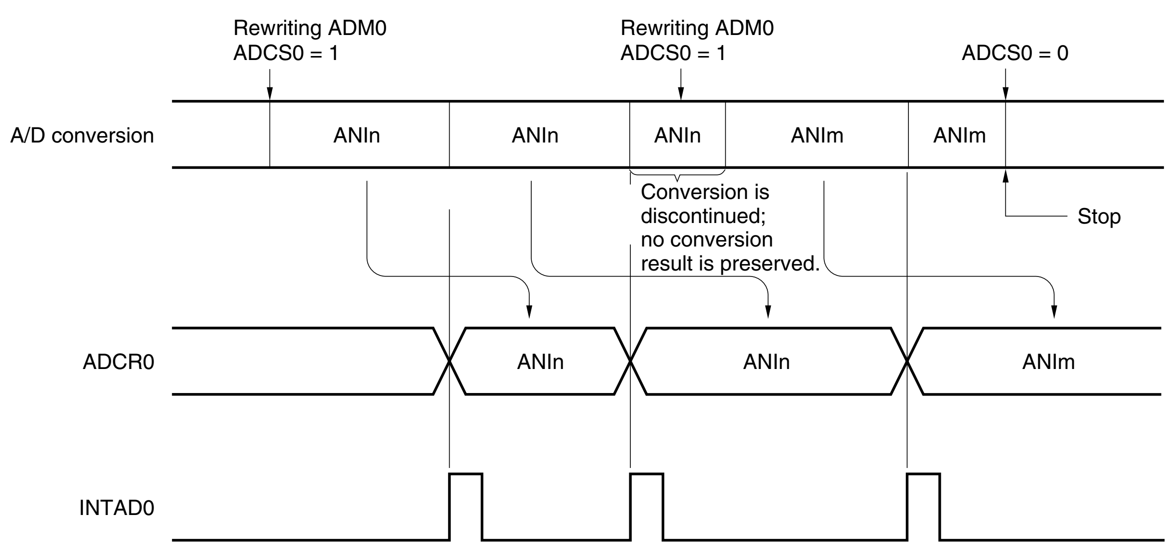
A/D conversion can be started only by software; that is, by setting A/D converter mode register 0 (ADM0).

The A/D conversion result is saved to A/D conversion result register 0 (ADCR0). At the same time, an interrupt request signal (INTAD0) is generated.

- **Software-started A/D conversion**

  Setting bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) to 1 triggers A/D conversion for the voltage applied to the analog input pin specified in A/D input selection register 0 (ADS0). Upon completion of A/D conversion, the conversion result is saved to A/D conversion result register 0 (ADCR0). At the same time, an interrupt request signal (INTAD0) is generated. Once A/D conversion is activated, and completed, another session of A/D conversion is started. A/D conversion is repeated until new data is written to ADM0. If data where ADCS0 is 1 is written to ADM0 again during A/D conversion, the ongoing session of A/D conversion is discontinued, and a new session of A/D conversion begins for the new data. If data where ADCS0 is 0 is written to ADM0 again during A/D conversion, A/D conversion is stopped immediately.

Figure 13-6. Software-Started A/D Conversion



Remarks 1. n = 0 to 7

2. m = 0 to 7

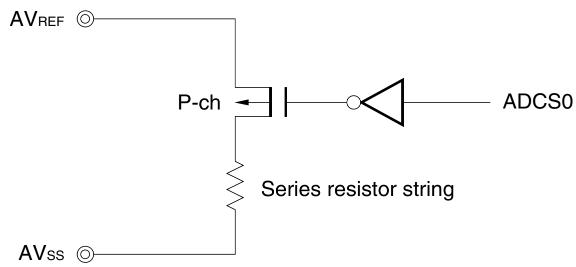
13.5 Cautions Related to 10-Bit A/D Converter

(1) Current consumption in standby mode

In standby mode, the A/D converter stops operating. Stopping conversion (bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) = 0) can reduce the current consumption.

Figure 13-7 shows how to reduce the current drain in standby mode.

Figure 13-7. How to Reduce Current Consumption in Standby Mode



(2) Input range for ANI0 to ANI7 pins

Be sure to keep the input voltage at ANI0 to ANI7 within its rating. If a voltage greater than or equal to AV_{REF} or less than or equal to AV_{SS} (even within the absolute maximum rating) is input into a conversion channel, the conversion output of the channel becomes undefined, and the conversion output of the other channels may also be affected.

(3) Conflict

<1> Conflict between writing to A/D conversion result register 0 (ADCR0) at the end of conversion and reading from ADCR0 using instruction

Reading from ADCR0 takes precedence. After reading, the new conversion result is written to ADCR0.

<2> Conflict between writing to ADCR0 at the end of conversion and writing to A/D converter mode register 0 (ADM0) or A/D input selection register 0 (ADS0)

Writing to ADM0 or ADS0 takes precedence. ADCR0 is not written to. No A/D conversion end interrupt request signal (INTAD0) is generated.

(4) Conversion result immediately after start of A/D conversion

The first A/D conversion value immediately after A/D conversion has been started is undefined. Poll the A/D conversion end interrupt request (INTAD0) and drop the first conversion result.

(5) Timing of undefined A/D conversion result

The A/D conversion value may become undefined if the timing of the completion of A/D conversion and that to stop the A/D conversion operation conflict. Therefore, read the A/D conversion result while the A/D conversion operation is in progress. To read the A/D conversion result after the A/D conversion operation has been stopped, stop the A/D conversion operation before the next conversion operation is completed. Figures 13-8 and 13-9 show the timing at which the conversion result is read.

Figure 13-8. Conversion Result Read Timing (If Conversion Result Is Undefined)

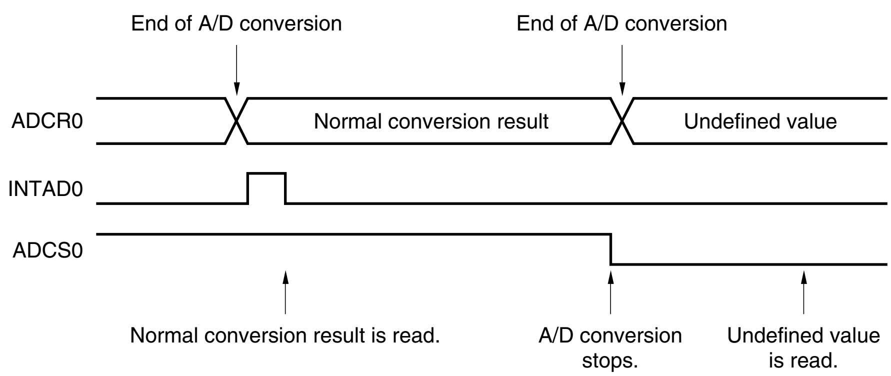
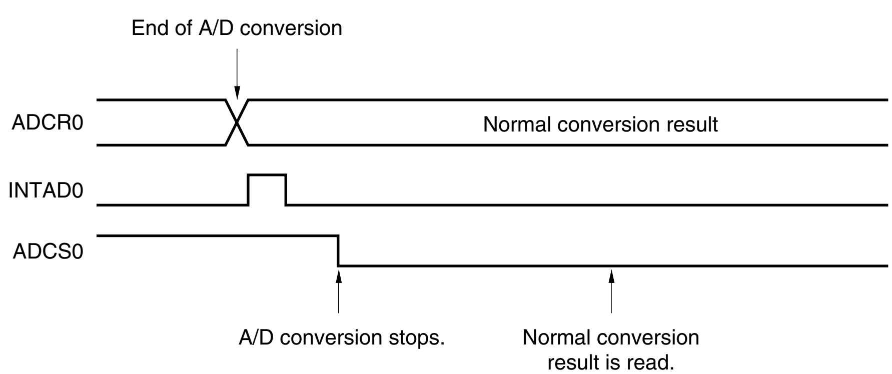


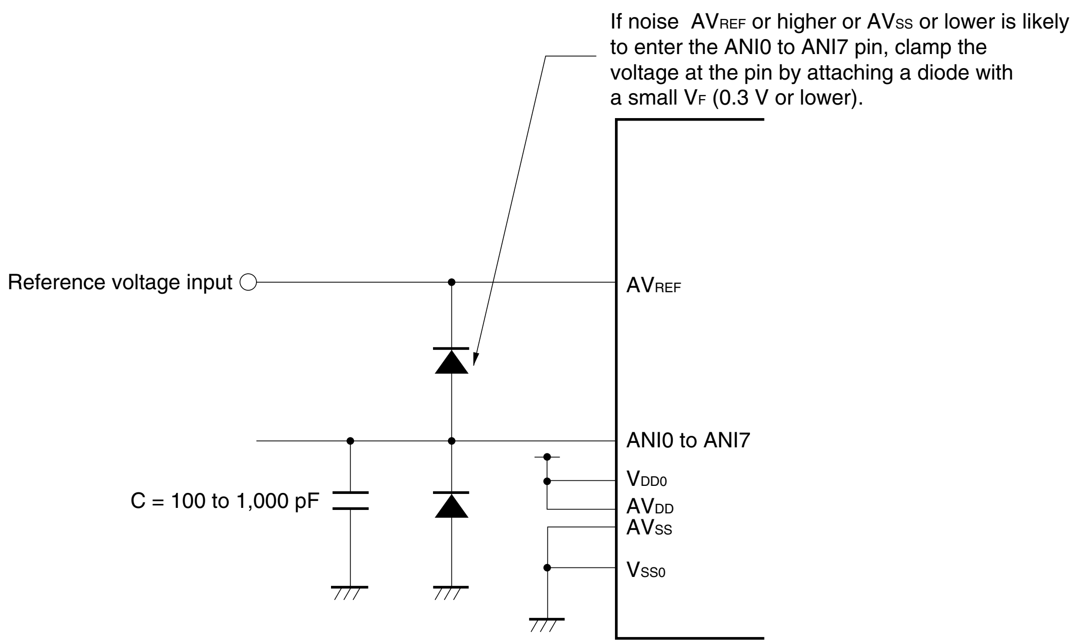
Figure 13-9. Conversion Result Read Timing (If Conversion Result Is Normal)



(6) Noise prevention

To maintain a resolution of 10 bits, watch out for noise on the AV_{REF} and ANI0 to ANI7 pins. The higher the output impedance of the analog input source, the larger the effect from noise. To reduce noise, attach an external capacitor to the relevant pins as shown in Figure 13-10.

Figure 13-10. Analog Input Pin Handling



(7) ANI0 to ANI7

The analog input pins (ANI0 to ANI7) are alternate-function pins. They are used also as port pins (P60 to P67).

If any of ANI0 to ANI7 has been selected for A/D conversion, do not execute input instructions for the ports. Otherwise, the conversion resolution may become lower.

If a digital pulse is applied to a pin adjacent to the analog input pins during A/D conversion, coupling noise may occur which prevents an A/D conversion result from being obtained as expected. Avoid applying a digital pulse to pins adjacent to the analog input pins during A/D conversion.

(8) Input impedance of ANI0 to ANI7 pins

This A/D converter charges the internal sampling capacitor for about 1/10 of the conversion time, and performs sampling.

Therefore at times other than sampling, only the leak current is output. During sampling, the current for charging the capacitor is also output, so the input impedance fluctuates and has no meaning.

However, to ensure adequate sampling, it is recommended that the output impedance of the analog input source be set to below 10 kΩ, or a 100 pF capacitor be connected to the ANI0 to ANI7 pins (see Figure 13-10).

(9) Input impedance of the AV_{REF} pin

A series resistor string of several 10 kΩ is connected across the AV_{REF} and AV_{SS} pins.

If the output impedance of the reference voltage source is high, this high impedance is eventually connected in series with the series resistor string across the AV_{REF} and AV_{SS} pins, leading to a higher reference voltage error.

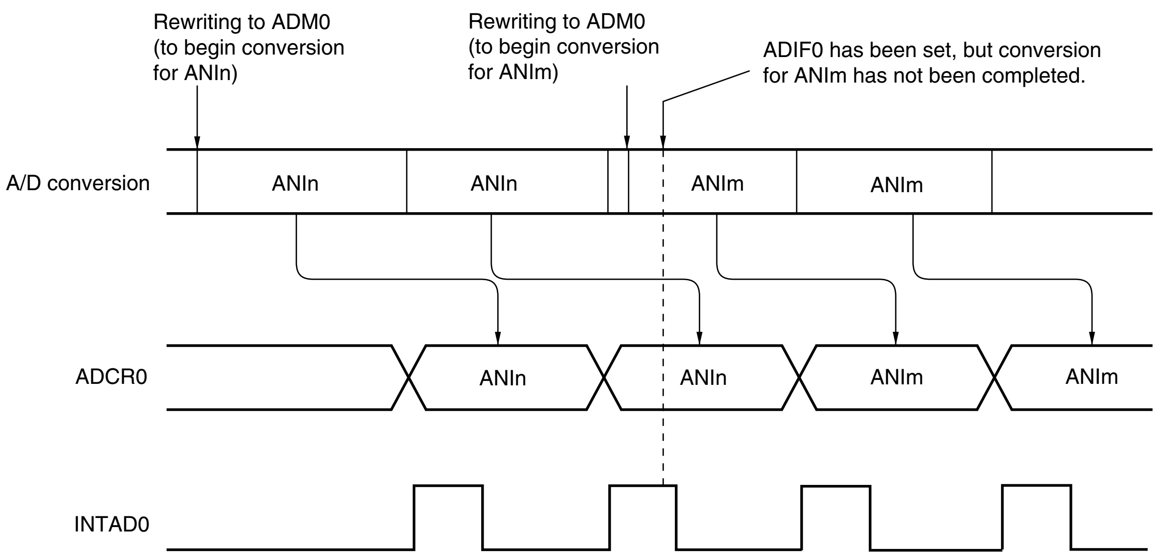
(10) Interrupt request flag (ADIF0)

Changing the content of A/D converter mode register 0 (ADM0) does not clear the interrupt request flag (ADIF0).

If the analog input pins are changed during A/D conversion, therefore, the A/D conversion result and the conversion end interrupt request flag may reflect the previous analog input immediately before writing to ADM0 occurs. In this case, ADIF0 may already be set if it is read-accessed immediately after ADM0 is write-accessed, even when A/D conversion has not been completed for the new analog input.

In addition, when A/D conversion is restarted, ADIF0 must be cleared beforehand.

Figure 13-11. A/D Conversion End Interrupt Request Generation Timing



Remarks 1. n = 0 to 7

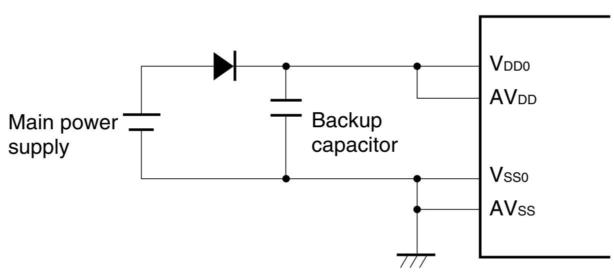
2. m = 0 to 7

(11) AV$_{DD}$ pin

The AV$_{DD}$ pin is used to supply power to the analog circuit. It is also used to supply power to the ANI0 to ANI7 input circuit.

If your application is designed to be changed to backup power, the AV$_{DD}$ pin must be supplied with the same voltage level as for the V$_{DD0}$ pin, as shown in Figure 13-12.

Figure 13-12. AV$_{DD}$ Pin Treatment



CHAPTER 14 SERIAL INTERFACE 20

14.1 Functions of Serial Interface 20

Serial interface 20 has the following three modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode
- 3-wire serial I/O mode

(1) Operation stop mode

This mode is used when serial transfer is not performed. Power consumption is minimized in this mode.

(2) Asynchronous serial interface (UART) mode

This mode is used to send and receive the one byte of data that follows a start bit. It supports full-duplex communication.

Serial interface 20 contains an UART-dedicated baud rate generator, enabling communication over a wide range of baud rates. It is also possible to define baud rates by dividing the frequency of the clock input to the ASCK20 pin.

(3) 3-wire serial I/O mode (switchable between MSB-first and LSB-first transmission)

This mode is used to transmit 8-bit data, using three lines: a serial clock ($\overline{\text{SCK20}}$) line and two serial data lines (SI20 and SO20).

As it supports simultaneous transmission and reception, 3-wire serial I/O mode requires less processing time for data transmission than asynchronous serial interface mode.

Because, in 3-wire serial I/O mode, it is possible to select whether 8-bit data transmission begins with the MSB or LSB, serial interface 20 can be connected to any device regardless of whether that device is designed for MSB-first or LSB-first transmission.

3-wire serial I/O mode is useful for connecting peripheral I/O circuits and display controllers having conventional synchronous serial interfaces, such as those of the 75XL, 78K, and 17K Series devices.

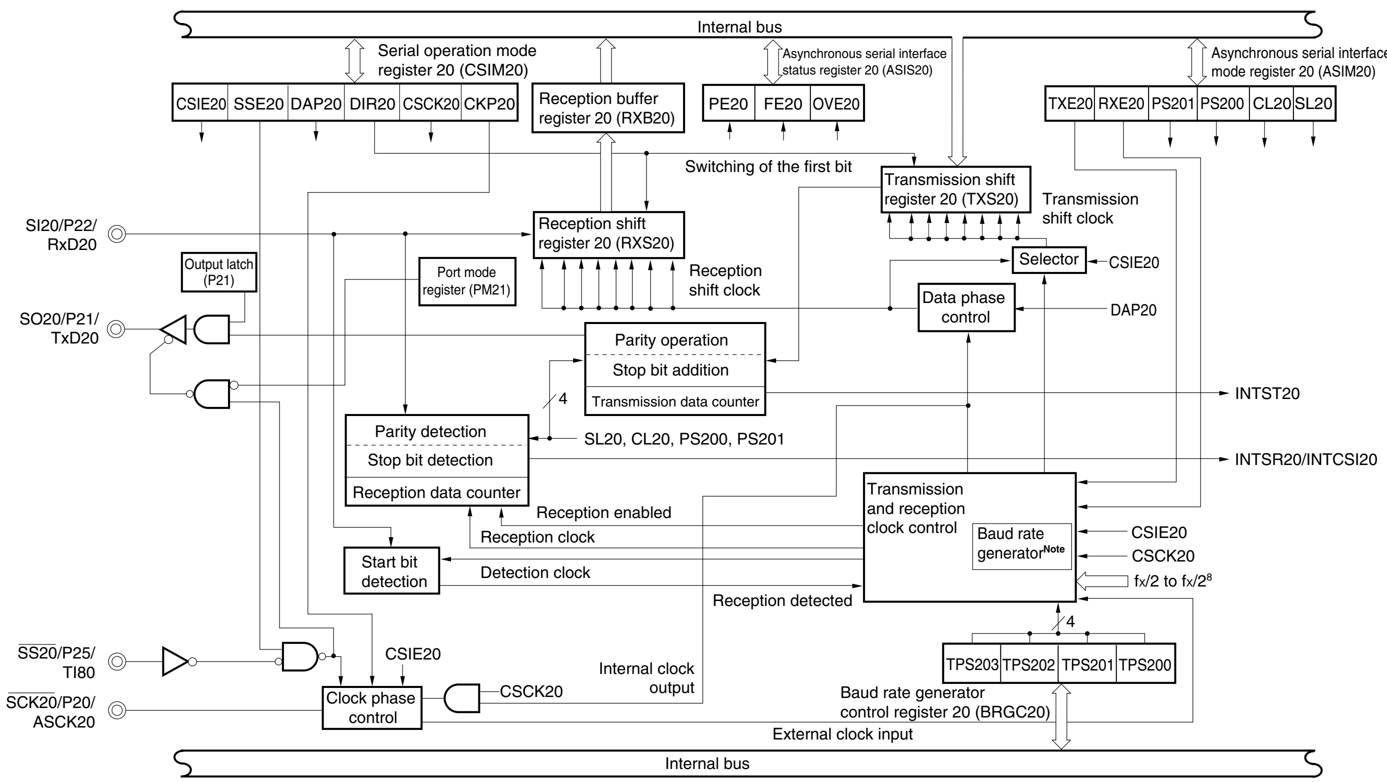
14.2 Configuration of Serial Interface 20

Serial interface 20 consists of the following hardware.

Table 14-1. Configuration of Serial Interface 20

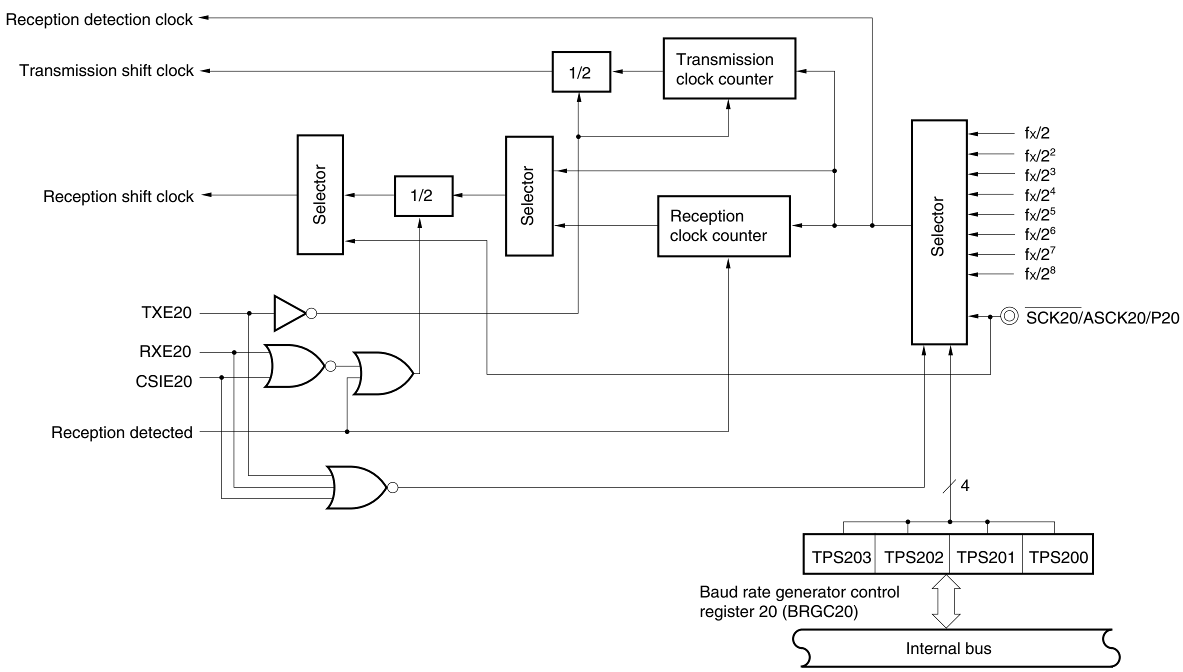
Item	Configuration
Registers	Transmission shift register 20 (TXS20) Reception shift register 20 (RXS20) Reception buffer register 20 (RXB20)
Control registers	Serial operation mode register 20 (CSIM20) Asynchronous serial interface mode register 20 (ASIM20) Asynchronous serial interface status register 20 (ASIS20) Baud rate generator control register 20 (BRGC20) Port mode register 2 (PM2) Port 2 (P2)

Figure 14-1. Block Diagram of Serial Interface 20



Note See **Figure 14-2** for the configuration of the baud rate generator.

Figure 14-2. Block Diagram of Baud Rate Generator 20



(1) Transmission shift register 20 (TXS20)

TXS20 is a register in which transmission data is prepared. The transmission data is output from TXS20 bit serially.

When the data length is seven bits, bits 0 to 6 of the data in TXS20 will be transmission data. Writing data to TXS20 triggers transmission.

TXS20 can be written with an 8-bit memory manipulation instruction, but cannot be read.

$\overline{\text{RESET}}$ input sets TXS20 to FFH.

Caution Do not write to TXS20 during transmission.
TXS20 and reception buffer register 20 (RXB20) are mapped at the same address, so any attempt to read from TXS20 results in a value being read from RXB20.

(2) Reception shift register 20 (RXS20)

RXS20 is a register in which serial data, received at the RxD20 pin, is converted to parallel data. Once one entire byte has been received, RXS20 feeds the reception data to reception buffer register 20 (RXB20).

RXS20 cannot be manipulated directly by a program.

(3) Reception buffer register 20 (RXB20)

RXB20 holds reception data. A new reception data is transferred from reception shift register 20 (RXS20) every 1-byte data reception.

When the data length is seven bits, the reception data is sent to bits 0 to 6 of RXB20, in which the MSB is always fixed to 0.

RXB20 can be read with an 8-bit memory manipulation instruction, but cannot be written.

$\overline{\text{RESET}}$ input makes RXB20 undefined.

Caution RXB20 and transmission shift register 20 (TXS20) are mapped at the same address, so any attempt to write to RXB20 results in a value being written to TXS20.

(4) Transmission controller

The transmission controller controls transmission. For example, it adds start, parity, and stop bits to the data in transmission shift register 20 (TXS20), according to the setting of asynchronous serial interface mode register 20 (ASIM20).

(5) Reception controller

The reception controller controls reception according to the setting of asynchronous serial interface mode register 20 (ASIM20). It also checks for errors, such as parity errors, during reception. If an error is detected, asynchronous serial interface status register 20 (ASIS20) is set according to the status of the error.

14.3 Control Registers of Serial Interface 20

Serial interface 20 is controlled by the following registers.

- Serial operation mode register 20 (CSIM20)
- Asynchronous serial interface mode register 20 (ASIM20)
- Asynchronous serial interface status register 20 (ASIS20)
- Baud rate generator control register 20 (BRGC20)
- Port mode register 2 (PM2)
- Port 2 (P2)

(1) Serial operation mode register 20 (CSIM20)

CSIM20 is used to make the settings related to 3-wire serial I/O mode.
CSIM20 is set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears CSIM20 to 00H.

Figure 14-3. Format of Serial Operation Mode Register 20

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM20	CSIE20	SSE20	0	0	DAP20	DIR20	CSCK20	CKP20	FF72H	00H	R/W

CSIE20	3-wire serial I/O mode operation control
0	Operation disabled
1	Operation enabled

SSE20	$\overline{\text{SS20}}$-pin selection	Function of $\overline{\text{SS20}}$/P25 pin	Communication status
0	Not used	Port function	Communication enabled
1	Used	0	Communication enabled
		1	Communication disabled

DAP20	3-wire serial I/O mode data phase selection
0	Output at the falling edge of $\overline{\text{SCK20}}$.
1	Output at the rising edge of $\overline{\text{SCK20}}$.

DIR20	First-bit specification
0	MSB
1	LSB

CSCK20	3-wire serial I/O mode clock selection
0	External clock input to the $\overline{\text{SCK20}}$ pin
1	Output of the dedicated baud rate generator

CKP20	3-wire serial I/O mode clock phase selection
0	Clock is active-low , and $\overline{\text{SCK20}}$ is high level in the idle state.
1	Clock is active-high , and $\overline{\text{SCK20}}$ is low level in the idle state.

Cautions 1. Bits 4 and 5 must be set to 0.

2. CSIM20 must be cleared to 00H, if UART mode is selected.

3. Switch operating modes after halting the serial transmit/receive operation.

4. When the external input clock is selected in 3-wire serial I/O mode, set input mode by setting bit 0 of port mode register 2 (PM2) to 1.

(2) Asynchronous serial interface mode register 20 (ASIM20)

ASIM20 is used to make the settings related to the asynchronous serial interface mode.
ASIM20 is set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears ASIM20 to 00H.

Figure 14-4. Format of Asynchronous Serial Interface Mode Register 20

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
ASIM20	TXE20	RXE20	PS201	PS200	CL20	SL20	0	0	FF70H	00H	R/W

TXE20	Transmit operation control
0	Transmit operation stop
1	Transmit operation enable

RXE20	Receive operation control
0	Receive operation stop
1	Receive operation enable

PS201	PS200	Parity bit specification
0	0	No parity
0	1	Always add 0 parity at transmission. Parity check is not performed at reception (No parity error is generated).
1	0	Odd parity
1	1	Even parity

CL20	Transmit data character length specification
0	7 bits
1	8 bits

SL20	Transmit data stop bit length
0	1 bit
1	2 bits

Cautions 1. Bits 0 and 1 must be set to 0.

2. If 3-wire serial I/O mode is selected, ASIM20 must be cleared to 00H.

3. Switch operating modes after halting serial transmit/receive operation.

Table 14-2. Operating Mode Settings of Serial Interface 20

(1) Operation stop mode

ASIM20		CSIM20			PM22	P22	PM21	P21	PM20	P20	First Bit	Shift Clock	P22/SI20/ RxD20 Pin Function	P21/SO20/ TxD20 Pin Function	P20/$\overline{SCK20}$/ ASCK20 Pin Function
TXE20	RXE20	CSIE20	DIR20	CSCK20											
0	0	0	×	×	× [Note 1]	× [Note 1]	× [Note 1]	× [Note 1]	× [Note 1]	× [Note 1]	–	–	P22	P21	P20
Other than above											Setting prohibited				

(2) 3-wire serial I/O mode

ASIM20		CSIM20			PM22	P22	PM21	P21	PM20	P20	First Bit	Shift Clock	P22/SI20/ RxD20 Pin Function	P21/SO20/ TxD20 Pin Function	P20/$\overline{SCK20}$/ ASCK20 Pin Function
TXE20	RXE20	CSIE20	DIR20	CSCK20											
0	0	1	0	0	× [Note 2]	× [Note 2]	0	1	1	×	MSB	External clock	SI20 [Note 2]	SO20 (CMOS output)	$\overline{SCK20}$ input
				1					0	1		Internal clock			$\overline{SCK20}$ output
		1	1	0					1	×	LSB	External clock			$\overline{SCK20}$ input
				1					0	1		Internal clock			$\overline{SCK20}$ output
Other than above											Setting prohibited				

(3) Asynchronous serial interface mode

ASIM20		CSIM20			PM22	P22	PM21	P21	PM20	P20	First Bit	Shift Clock	P22/SI20/ RxD20 Pin Function	P21/SO20/ TxD20 Pin Function	P20/$\overline{SCK20}$/ ASCK20 Pin Function
TXE20	RXE20	CSIE20	DIR20	CSCK20											
1	0	0	0	0	× [Note 1]	× [Note 1]	0	1	1	×	LSB	External clock	P22	TxD20 (CMOS output)	ASCK20 input
									× [Note 1]	× [Note 1]		Internal clock			P20
0	1	0	0	0	1	×	× [Note 1]	× [Note 1]	1	×		External clock	RxD20	P21	ASCK20 input
									× [Note 1]	× [Note 1]		Internal clock			P20
1	1	0	0	0	1	×	0	1	1	×		External clock		TxD20 (CMOS output)	ASCK20 input
									× [Note 1]	× [Note 1]		Internal clock			P20
Other than above											Setting prohibited				

Notes 1. These pins can be used for port functions.

2. When only transmission is used, this pin can be used as P22 (CMOS I/O).

Remark ×: Don't care.

(3) Asynchronous serial interface status register 20 (ASIS20)

ASIS20 indicates the type of a reception error, if an error occurs while asynchronous serial interface mode is set.

ASIS20 is set with a 1-bit or 8-bit memory manipulation instruction.

The contents of ASIS20 are undefined in 3-wire serial I/O mode.

$\overline{\text{RESET}}$ input clears ASIS20 to 00H.

Figure 14-5. Format of Asynchronous Serial Interface Status Register 20

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ASIS20	0	0	0	0	0	PE20	FE20	OVE20	FF71H	00H	R

PE20	Parity error flag
0	No parity error has occurred.
1	A parity error has occurred (when the transmit parity and receive parity do not match).

FE20	Flaming error flag
0	No framing error has occurred.
1	A framing error has occurred (when stop bit is not detected).Note 1

OVE20	Overrun error flag
0	No overrun error has occurred.
1	An overrun error has occurred.Note 2 (when the next receive operation is completed before the data is read from reception buffer register 20)

Notes 1. Even when the stop bit length is set to 2 bits by setting bit 2 (SL20) of asynchronous serial interface mode register 20 (ASIM20), the stop bit detection at reception is performed with 1 bit.

2. Be sure to read reception buffer register 20 (RXB20) when an overrun error occurs. If not, every time the data is received an overrun error occurs.

(4) Baud rate generator control register 20 (BRGC20)

BRGC20 is used to specify the serial clock for serial interface 20.

BRGC20 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears BRGC20 to 00H.

Figure 14-6. Format of Baud Rate Generator Control Register 20

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
BRGC20	TPS203	TPS202	TPS201	TPS200	0	0	0	0	FF73H	00H	R/W

TPS203	TPS202	TPS201	TPS200	3-bit counter source clock selection			n
					At fx = 10.0 MHz operation[Note 1]	At fX = 5.0 MHz operation	
0	0	0	0	fx/2	5.00 MHz	2.50 MHz	1
0	0	0	1	$f_X/2^2$	2.50 MHz	1.25 MHz	2
0	0	1	0	$f_X/2^3$	1.25 MHz	625 kHz	3
0	0	1	1	$f_X/2^4$	625 kHz	313 kHz	4
0	1	0	0	$f_X/2^5$	313 kHz	156 kHz	5
0	1	0	1	$f_X/2^6$	156 kHz	78.1 kHz	6
0	1	1	0	$f_X/2^7$	78.1 kHz	39.1 kHz	7
0	1	1	1	$f_X/2^8$	39.1 kHz	19.5 kHz	8
1	0	0	0	External clock input to the ASCK20 pin[Note 2]			–
Other than above				Setting prohibited			

Notes 1. Expanded-specification products only.

2. An external clock can be used only in UART mode.

Cautions 1. When writing to BRGC00 is performed during a communication operation, the output of baud rate generator is disrupted and communications cannot be performed normally. Be sure not to write to BRGC00 during communication operations.

2. Be sure not to select n = 1 in UART mode when fx > 2.5 MHz because the baud rate will exceed the rated range.

3. Be sure not to select n = 2 in UART mode when fx > 5.0 MHz because the baud rate will exceed the rated range.

4. Be sure not to select n = 1 in 3-wire serial I/O mode when fx > 5.0 MHz because the serial clock specification will be exceeded.

5. When the external input clock is selected, set input mode by setting bit 0 of port mode register 2 (PM2) to 1.

Remarks 1. fx: Main system clock oscillation frequency

2. n: Values determined by the settings of TPS200 to TPS203 ($1 \leq n \leq 8$)

The baud rate transmit/receive clock to be generated is either a signal scaled from the system clock, or a signal scaled from the clock input to the ASCK20 pin.

(a) Generation of baud rate transmit/receive clock from system clock

The transmit/receive clock is generated by scaling the system clock. The baud rate of a clock generated from the system clock is estimated by using the following expression.

$$[\text{Baud rate}] = \frac{f_X}{2^{n+1} \times 8} [\text{bps}]$$

f_X: Main system clock oscillation frequency

n: Values in Figure 14-6, determined by the values of TPS200 to TPS203 ($2 \leq n \leq 8$)

Table 14-3. Example of Relationship Between System Clock and Baud Rate

Baud Rate (bps)	At f_X = 10.0 MHz[Note]			At f_X = 5.0 MHz			At f_X = 4.9152 MHz		
	n	BRGC20 Set Value	Error (%)	n	BRGC20 Set Value	Error (%)	n	BRGC20 Set Value	Error (%)
1,200	–	–	1.73	8	70H	1.73	8	70H	0
2,400	8	70H		7	60H		7	60H	
4,800	7	60H		6	50H		6	50H	
9,600	6	50H		5	40H		5	40H	
19,200	5	40H		4	30H		4	30H	
38,400	4	30H		3	20H		3	20H	
76,800	3	20H		2	10H		2	10H	

Note Expanded-specification products only.

Cautions 1. Be sure not to select n = 1 during operation at f_X > 2.5 MHz because the baud rate will exceed the rated range.

2. Be sure not to select n = 2 during operation at f_X > 5.0 MHz because the baud rate will exceed the rated range.

(b) Generation of baud rate transmit/receive clock from external clock input to ASCK20 pin

The transmit/receive clock is generated by scaling the clock input from the ASCK20 pin. The baud rate of a clock generated from the clock input to the ASCK20 pin is calculated by using the following expression.

$$[\text{Baud rate}] = \frac{f_{ASCK}}{16}\ [\text{bps}]$$

f_{ASCK}: Frequency of clock input to the ASCK20 pin

Table 14-4. Relationship Between ASCK20 Pin Input Frequency and Baud Rate (When BRGC20 Is Set to 80H)

Baud Rate (bps)	ASCK20 Pin Input Frequency (kHz)
75	1.2
150	2.4
300	4.8
600	9.6
1,200	19.2
2,400	38.4
4,800	76.8
9,600	153.6
19,200	307.2
31,250	500.0
38,400	614.4

(c) Generation of 3-wire serial I/O mode serial clock from system clock

The serial clock is generated by scaling the system clock. The serial clock frequency is calculated by using the following expression. BRGC20 does not have to be set when the serial clock is input to the $\overline{\text{SCK20}}$ pin externally.

$$\text{Serial clock frequency} = \frac{f_X}{2^{n+1}}\ [\text{Hz}]$$

f_X: System clock oscillation frequency

n: Value determined by settings of TPS200 to TPS203 in Fig. 14-6.

14.4 Operation of Serial Interface 20

Serial interface 20 provides the following three modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode
- 3-wire serial I/O mode

14.4.1 Operation stop mode

In operation stop mode, serial transfer is not executed; therefore, the power consumption can be reduced. The P20/$\overline{\text{SCK20}}$/ASCK20, P21/SO20/TxD20, and P22/SI20/RxD20 pins can be used as normal I/O ports.

(1) Register setting

Operation stop mode is set by serial operation mode register 20 (CSIM20) and asynchronous serial interface mode register 20 (ASIM20).

(a) Serial operation mode register 20 (CSIM20)

CSIM20 is set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears CSIM20 to 00H.

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM20	CSIE20	SSE20	0	0	DAP20	DIR20	CSCK20	CKP20	FF72H	00H	R/W

CSIE20	Operation control in 3-wire serial I/O mode
0	Operation disabled
1	Operation enabled

Caution Bits 4 and 5 must be set to 0.

(b) Asynchronous serial interface mode register 20 (ASIM20)

ASIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ASIM20 to 00H.

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
ASIM20	TXE20	RXE20	PS201	PS200	CL20	SL20	0	0	FF70H	00H	R/W

TXE20	Transmit operation control
0	Transmit operation stopped
1	Transmit operation enabled

RXE20	Receive operation control
0	Receive operation stopped
1	Receive operation enabled

Caution Bits 0 and 1 must be set to 0.

14.4.2 Asynchronous serial interface (UART) mode

In this mode, the one-byte data following the start bit is transmitted/received and thus full-duplex communication is possible.

This device incorporates an UART-dedicated baud rate generator that enables communications at the desired baud rate from many options. In addition, the baud rate can also be defined by dividing the clock input to the ASCK20 pin.

The UART-dedicated baud rate generator also can output the 31.25 kbps baud rate that complies with the MIDI standard.

(1) Register setting

UART mode is set by serial operation mode register 20 (CSIM20), asynchronous serial interface mode register 20 (ASIM20), asynchronous serial interface status register 20 (ASIS20), baud rate generator control register 20 (BRGC20), port mode register 2 (PM2), and port 2 (P2).

(a) Serial operation mode register 20 (CSIM20)

CSIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSIM20 to 00H.

Set CSIM20 to 00H when UART mode is selected.

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM20	CSIE20	SSE20	0	0	DAP20	DIR20	CSCK20	CKP20	FF72H	00H	R/W

CSIE20	3-wire serial I/O mode operation control
0	Operation disabled
1	Operation enabled

SSE20	$\overline{\text{SS20}}$-pin selection	Function of $\overline{\text{SS20}}$/P25 pin	Communication status
0	Not used	Port function	Communication enabled
1	Used	0	Communication enabled
		1	Communication disabled

DAP20	3-wire serial I/O mode data phase selection
0	Outputs at the falling edge of $\overline{\text{SCK20}}$.
1	Outputs at the rising edge of $\overline{\text{SCK20}}$.

DIR20	First-bit specification
0	MSB
1	LSB

CSCK20	3-wire serial I/O mode clock selection
0	External clock input to the $\overline{\text{SCK20}}$ pin
1	Output of the dedicated baud rate generator

CKP20	3-wire serial I/O mode clock phase selection
0	Clock is active-low, and $\overline{\text{SCK20}}$ is high level in the idle state.
1	Clock is active-high, and $\overline{\text{SCK20}}$ is low level in the idle state.

Cautions 1. Bits 4 and 5 must be set to 0.

2. CSIM20 must be cleared to 00H, if UART mode is selected.

3. Switch operating modes after halting serial transmit/receive operation.

(b) Asynchronous serial interface mode register 20 (ASIM20)

ASIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ASIM20 to 00H.

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
ASIM20	TXE20	RXE20	PS201	PS200	CL20	SL20	0	0	FF70H	00H	R/W

TXE20	Transmit operation control
0	Transmit operation stop
1	Transmit operation enable

RXE20	Receive operation control
0	Receive operation stop
1	Receive operation enable

PS201	PS200	Parity bit specification
0	0	No parity
0	1	Always add 0 parity at transmission. Parity check is not performed at reception (no parity error is generated).
1	0	Odd parity
1	1	Even parity

CL20	Character length specification
0	7 bits
1	8 bits

SL20	Transmit data stop bit length specification
0	1 bit
1	2 bits

Cautions 1. Bits 0 and 1 must be set to 0.

2. Switch operating modes after halting the serial transmit/receive operation.

(c) Asynchronous serial interface status register 20 (ASIS20)

ASIS20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ASIS20 to 00H.

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ASIS20	0	0	0	0	0	PE20	FE20	OVE20	FF71H	00H	R

PE20	Parity error flag
0	Parity error not generated
1	Parity error generated (when the parity of transmit data does not match)

FE20	Framing error flag
0	Framing error not generated
1	Framing error generated (when stop bit is not detected)Note 1

OVE20	Overrun error flag
0	Overrun error not generated
1	Overrun error generatedNote 2 (when the next receive operation is completed before data is read from reception buffer register 20)

Notes 1. Even when the stop bit length is set to 2 bits by setting bit 2 (SL20) of asynchronous serial interface mode register 20 (ASIM20), the stop bit detection at reception is performed with 1 bit.

2. Be sure to read reception buffer register 20 (RXB20) when an overrun error occurs. If not, every time the data is received an overrun error is generated.

(d) Baud rate generator control register 20 (BRGC20)

BRGC20 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears BRGC20 to 00H.

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
BRGC20	TPS203	TPS202	TPS201	TPS200	0	0	0	0	FF73H	00H	R/W

TPS203	TPS202	TPS201	TPS200	3-bit counter source clock selection			n
					At fx = 10.0 MHz operation[Note]	At fx = 5.0 MHz operation	
0	0	0	0	fx/2	5.00 MHz	2.50 MHz	1
0	0	0	1	$f_X/2^2$	2.50 MHz	1.25 MHz	2
0	0	1	0	$f_X/2^3$	1.25 MHz	625 kHz	3
0	0	1	1	$f_X/2^4$	625 kHz	313 kHz	4
0	1	0	0	$f_X/2^5$	313 kHz	156 kHz	5
0	1	0	1	$f_X/2^6$	156 kHz	78.1 kHz	6
0	1	1	0	$f_X/2^7$	78.1 kHz	39.1 kHz	7
0	1	1	1	$f_X/2^8$	39.1 kHz	19.5 kHz	8
1	0	0	0	External clock input to the ASCK20 pin			–
Other than above				Setting prohibited			

Note Expanded-specification products only.

Cautions 1. When writing to BRGC20 is performed during a communication operation, the output of the baud rate generator is disrupted and communications cannot be performed normally. Be sure not to write to BRGC20 during a communication operation.

2. Be sure not to select n = 1 during operation at fx > 2.5 MHz because the baud rate will exceed the rated range.

3. Be sure not to select n = 2 during operation at fx > 5.0 MHz because the baud rate will exceed the rated range.

4. When the external input clock is selected, set input mode by setting bit 0 of port mode register 2 (PM2) to 1.

Remarks 1. fx: Main system clock oscillation frequency

2. n: Values determined by the settings of TPS200 to TPS203 ($1 \le n \le 8$)

The baud rate transmit/receive clock to be generated is either a signal scaled from the system clock, or a signal scaled from the clock input to the ASCK20 pin.

(i) Generation of baud rate transmit/receive clock from system clock

The transmit/receive clock is generated by scaling the system clock. The baud rate of a clock generated from the system clock is estimated by using the following expression.

$$[\text{Baud rate}] = \frac{f_X}{2^{n+1} \times 8} \text{ [bps]}$$

f_X: Main system clock oscillation frequency

n: Values in the above table determined by the settings of TPS200 to TPS203 ($2 \leq n \leq 8$)

Table 14-5. Example of Relationship Between System Clock and Baud Rate

Baud Rate (bps)	At f_X = 10.0 MHz[Note]			At f_X = 5.0 MHz			At f_X = 4.9152 MHz		
	n	BRGC20 Set Value	Error (%)	n	BRGC20 Set Value	Error (%)	n	BRGC20 Set Value	Error (%)
1,200	–	–	1.73	8	70H	1.73	8	70H	0
2,400	8	70H		7	60H		7	60H	
4,800	7	60H		6	50H		6	50H	
9,600	6	50H		5	40H		5	40H	
19,200	5	40H		4	30H		4	30H	
38,400	4	30H		3	20H		3	20H	
76,800	3	20H		2	10H		2	10H	

Note Expanded-specification products only.

Cautions 1. Be sure not to select n = 1 during operation at f_X > 2.5 MHz because the baud rate will exceed the rated range.

2. Be sure not to select n = 2 during operation at f_X > 5.0 MHz because the baud rate will exceed the rated range.

(ii) Generation of baud rate transmit/receive clock from external clock input to ASCK20 pin

The transmit/receive clock is generated by scaling the clock input from the ASCK20 pin. The baud rate of a clock generated from the clock input to the ASCK20 pin is estimated by using the following expression.

$$[\text{Baud rate}] = \frac{f_{ASCK}}{16} \text{ [bps]}$$

f_{ASCK}: Frequency of clock input to ASCK20 pin

Table 14-6. Relationship Between ASCK20 Pin Input Frequency and Baud Rate (When BRGC20 Is Set to 80H)

Baud Rate (bps)	ASCK20 Pin Input Frequency (kHz)
75	1.2
150	2.4
300	4.8
600	9.6
1,200	19.2
2,400	38.4
4,800	76.8
9,600	153.6
19,200	307.2
31,250	500.0
38,400	614.4

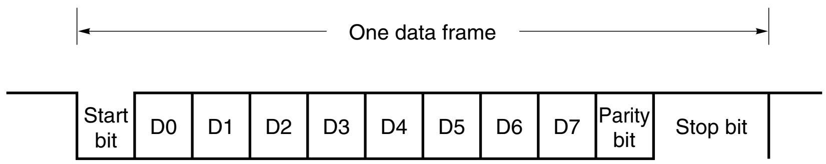
(2) Communication operation

(a) Data format

The transmit/receive data format is as shown in Figure 14-7. One data frame consists of a start bit, character bits, parity bit, and stop bit(s).

The specification of character bit length in one data frame, parity selection, and specification of stop bit length is carried out with asynchronous serial interface mode register 20 (ASIM20).

Figure 14-7. Asynchronous Serial Interface Transmit/Receive Data Format



- Start bits .... 1 bit
- Character bits............ 7 bits/8 bits
- Parity bits .... Even parity/odd parity/0 parity/no parity
- Stop bit(s) .... 1 bit/2 bits

When 7 bits are selected as the number of character bits, only the lower 7 bits (bits 0 to 6) are valid; in transmission the most significant bit (bit 7) is ignored, and in reception the most significant bit (bit 7) is always “0”.

The serial transfer rate is selected by baud rate generator control register 20 (BRGC20).

If a serial data receive error is generated, the receive error contents can be determined by reading the status of asynchronous serial interface status register 20 (ASIS20).

(b) Parity types and operation

The parity bit is used to detect a bit error in the communication data. Normally, the same kind of parity bit is used on the transmitting side and the receiving side. With even parity and odd parity, a one-bit (odd number) error can be detected. With 0 parity and no parity, an error cannot be detected.

(i) Even parity

- **At transmission**

  The parity bit is determined so that the number of bits with a value of "1" in the transmit data including the parity bit is even. The parity bit value should be as follows.

  The number of bits with a value of "1" is an odd number in transmit data: 1
  The number of bits with a value of "1" is an even number in transmit data: 0

- **At reception**

  The number of bits with a value of "1" in the receive data including parity bit is counted, and if the number is odd, a parity error is generated.

(ii) Odd parity

- **At transmission**

  Conversely to even parity, the parity bit is determined so that the number of bits with a value of "1" in the transmit data including parity bit is odd. The parity bit value should be as follows.

  The number of bits with a value of "1" is an odd number in transmit data: 0
  The number of bits with a value of "1" is an even number in transmit data: 1

- **At reception**

  The number of bits with a value of "1" in the receive data including parity bit is counted, and if the number is even, a parity error is generated.

(iii) 0 parity

When transmitting, the parity bit is set to "0" irrespective of the transmit data.
At reception, a parity bit check is not performed. Therefore, a parity error is not generated, irrespective of whether the parity bit is set to "0" or "1".

(iv) No parity

A parity bit is not added to the transmit data. At reception, data is received assuming that there is no parity bit. Since there is no parity bit, a parity error is not generated.

(c) Transmission

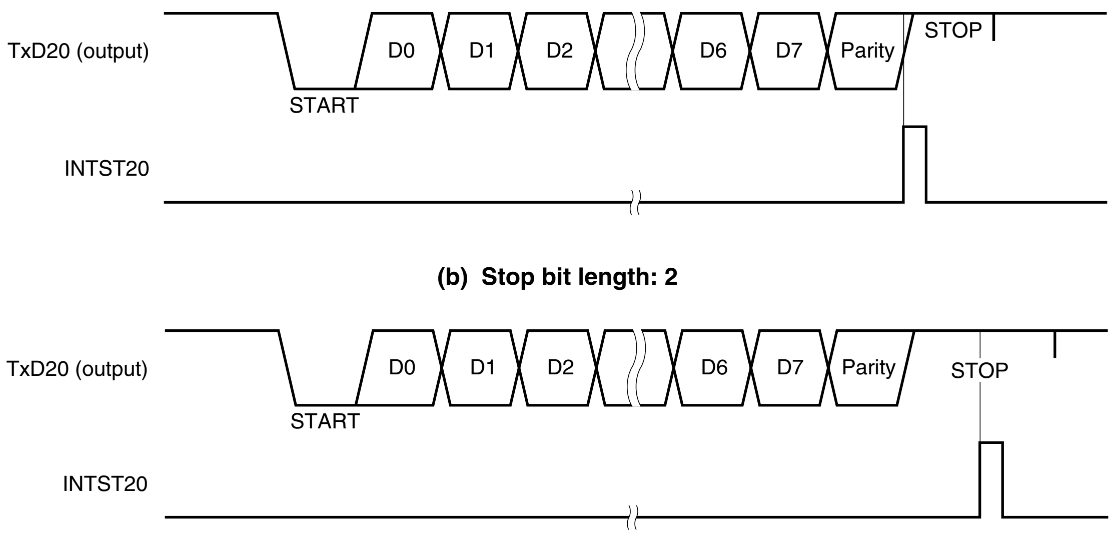
A transmit operation is started by writing transmit data to transmission shift register 20 (TXS20). The start bit, parity bit, and stop bit(s) are added automatically.

When the transmit operation starts, the data in TXS20 is shifted out, and when TXS20 is empty, a transmission completion interrupt (INTST20) is generated.

Figure 14-8. Asynchronous Serial Interface Transmission Completion Interrupt Timing

(a) Stop bit length: 1

(b) Stop bit length: 2



Caution Do not rewrite asynchronous serial interface mode register 20 (ASIM20) during a transmit operation. If the ASIM20 register is rewritten to during transmission, subsequent transmission may not be performed (the normal state is restored by $\overline{\text{RESET}}$ input).

It is possible to determine whether transmission is in progress by software by using a transmission completion interrupt (INTST20) or the interrupt request flag (STIF20) set by INTST20.

(d) Reception

When bit 6 (RXE20) of asynchronous serial interface mode register 20 (ASIM20) is set to 1, a receive operation is enabled and sampling of the RxD20 pin input is performed.

RxD20 pin input sampling is performed using the serial clock specified by BRGC20.

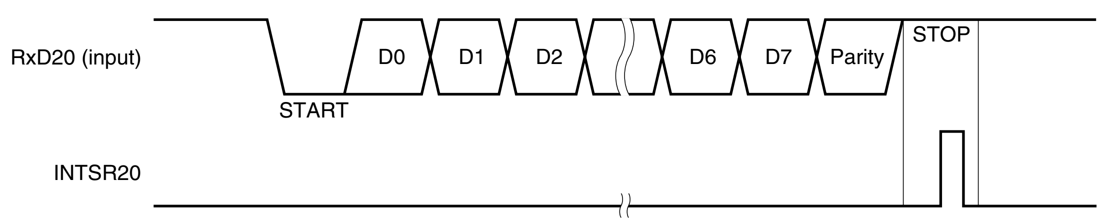
When the RxD20 pin input becomes low, the 3-bit counter starts counting, and at the time when half the time determined by the specified baud rate has passed, the data sampling start timing signal is output. If the RxD20 pin input sampled again as a result of this start timing signal is low, it is identified as a start bit, the 3-bit counter is initialized and starts counting, and data sampling is performed. When character data, a parity bit, and one stop bit are detected after the start bit, reception of one frame of data ends.

When one frame of data has been received, the receive data in the shift register is transferred to reception buffer register 20 (RXB20), and a reception completion interrupt (INTSR20) is generated.

If an error is generated, the receive data in which the error was generated is still transferred to RXB20, and INTSR20 is generated.

If the RXE20 bit is reset to 0 during the receive operation, the receive operation is stopped immediately. In this case, the contents of RXB20 and asynchronous serial interface status register 20 (ASIS20) are not changed, and INTSR20 is not generated.

Figure 14-9. Asynchronous Serial Interface Reception Completion Interrupt Timing



Caution Be sure to read reception buffer register 20 (RXB20) even if a receive error occurs. If RXB20 is not read, an overrun error will be generated when the next data is received, and the receive error state will continue indefinitely.

(e) Receive errors

The following three errors may occur during a receive operation: a parity error, framing error, and overrun error. After data reception, an error flag is set in asynchronous serial interface status register 20 (ASIS20). Receive error causes are shown in Table 14-7.

It is possible to determine what kind of error occurred during reception by reading the contents of ASIS20 in the reception error interrupt servicing (see **Figures 14-9** and **14-10**).

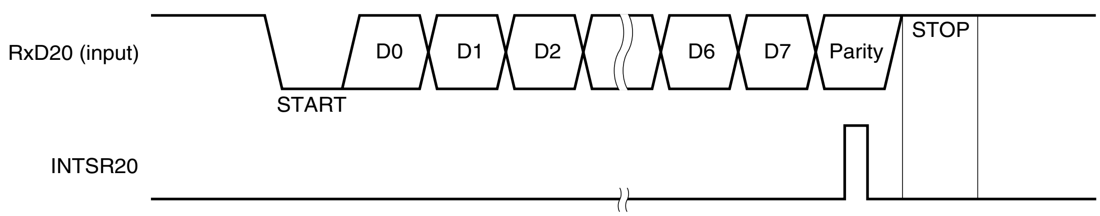
The contents of ASIS20 are reset to 0 by reading reception buffer register 20 (RXB20) or receiving the next data (if there is an error in the next data, the corresponding error flag is set).

Table 14-7. Receive Error Causes

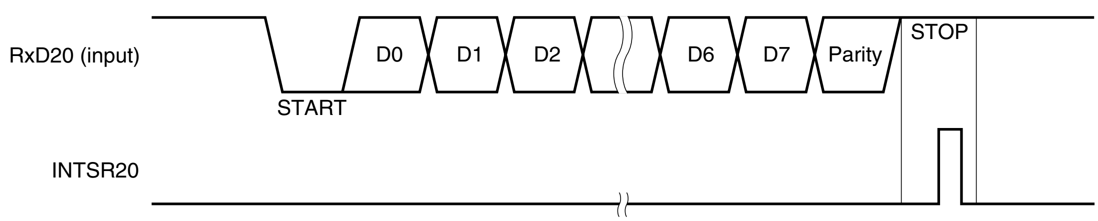
Receive Errors	Cause
Parity error	Transmission-time parity and reception data parity do not match
Framing error	Stop bit not detected
Overrun error	Reception of next data is completed before data is read from reception buffer register

Figure 14-10. Receive Error Timing

(a) Parity error occurred



(b) Framing error or overrun error occurred



Cautions 1. The contents of the ASIS20 register are reset to 0 by reading reception buffer register 20 (RXB20) or receiving the next data. To ascertain the error contents, read ASIS20 before reading RXB20.

2. Be sure to read reception buffer register 20 (RXB20) even if a receive error occurred. If RXB20 is not read, an overrun error will occur when the next data is received, and the receive error state will continue indefinitely.

(f) Reading receive data

When the reception completion interrupt (INTSR20) occurs, receive data can be read by reading the value of reception buffer register 20 (RXB20).

To read the receive data stored in reception buffer register 20 (RXB20), read while reception is enabled (RXE20 = 1).

Remark However, if it is necessary to read receive data after reception has stopped (RXE20 = 0), read using either of the following methods.

(a) Read after setting RXE20 = 0 after waiting for one cycle or more of the source clock selected by BRGC20.

(b) Read after bit 2 (DIR20) of serial operation mode register 20 (CSIM20) is set (1).

Program example of (a) (BRGC20 = 00H (source clock = fx/2))

```
INTREX:                   ;<Reception completion interrupt routine>
        NOP               ;2 clocks
        CLR1 RXE20        ;Reception stopped
        MOV  A, RXB20     ;Read receive data
```

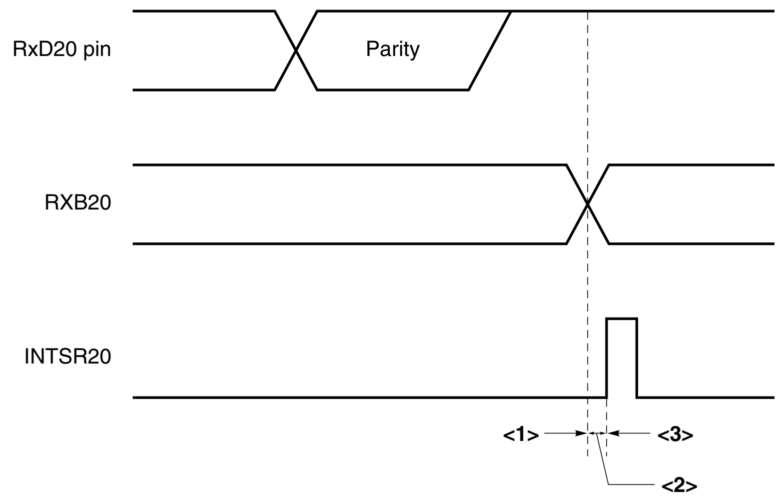
Program example of (b)

```
INTRXE:                   ;<Reception completion interrupt routine>
        SET1 CSIM20.2     ;DIR20 flag is set to LSB first
        CLR1 RXE20        ;Reception stopped
        MOV  A, RXB20     ;Read receive data
```

(3) Cautions related to UART mode

(a) When bit 7 (TXE20) of asynchronous serial interface mode register 20 (ASIM20) is cleared during transmission, be sure to set transmission shift register 20 (TXS20) to FFH, then set TXE20 to 1 before executing the next transmission.

(b) When bit 6 (RXE20) of asynchronous serial interface mode register 20 (ASIM20) is cleared during reception, reception buffer register 20 (RXB20) and the reception completion interrupt (INTSR20) are as follows.



When RXE20 is set to 0 at the time indicated by **<1>**, RXB20 holds the previous data and INTSR20 is not generated.
When RXE20 is set to 0 at the time indicated by **<2>**, RXB20 renews the data and INTSR20 is not generated.
When RXE20 is set to 0 at the time indicated by **<3>**, RXB20 renews the data and INTSR20 is generated.

14.4.3 3-wire serial I/O mode

The 3-wire serial I/O mode is useful for connection of peripheral I/Os and display controllers, etc., which incorporate a conventional synchronous serial interface, such as the 75XL Series, 78K Series, 17K Series, etc.

Communication is performed using three lines: the serial clock (SCK20), serial output (SO20), and serial input (SI20).

(1) Register setting

3-wire serial I/O mode settings are performed using serial operation mode register 20 (CSIM20), asynchronous serial interface mode register 20 (ASIM20), baud rate generator control register 20 (BRGC20), port mode register 2 (PM2), and port 2 (P2).

(a) Serial operation mode register 20 (CSIM20)

CSIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

RESET input clears CSIM20 to 00H.

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM20	CSIE20	SSE20	0	0	DAP20	DIR20	CSCK20	CKP20	FF72H	00H	R/W

CSIE20	3-wire serial I/O mode operation control
0	Operation disabled
1	Operation enabled

SSE20	SS20-pin selection	Function of SS20/P25 pin	Communication status
0	Not used	Port function	Communication enabled
1	Used	0	Communication enabled
		1	Communication disabled

DAP20	3-wire serial I/O mode data phase selection
0	Outputs at the falling edge of SCK20.
1	Outputs at the rising edge of SCK20.

DIR20	First-bit specification
0	MSB
1	LSB

CSCK20	3-wire serial I/O mode clock selection
0	External clock input to the SCK20 pin
1	Output of the dedicated baud rate generator

CKP20	3-wire serial I/O mode clock phase selection
0	Clock is active-low , and SCK20 is at high level in the idle state.
1	Clock is active-high , and SCK20 is at low level in the idle state.

Cautions 1. Bits 4 and 5 must be set to 0.

2. Switch operating modes after halting the serial transmit/receive operation.

3. When the external input clock is selected in 3-wire serial I/O mode, set input mode by setting bit 0 of port mode register 2 (PM2) to 1.

(b) Asynchronous serial interface mode register 20 (ASIM20)

ASIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ASIM20 to 00H.

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
ASIM20	TXE20	RXE20	PS201	PS200	CL20	SL20	0	0	FF70H	00H	R/W

TXE20	Transmit operation control
0	Transmit operation stop
1	Transmit operation enable

RXE20	Receive operation control
0	Receive operation stop
1	Receive operation enable

PS201	PS200	Parity bit specification
0	0	No parity
0	1	Always add 0 parity at transmission. Parity check is not performed at reception (no parity error is generated).
1	0	Odd parity
1	1	Even parity

CL20	Character length specification
0	7 bits
1	8 bits

SL20	Transmit data stop bit length specification
0	1 bit
1	2 bits

Cautions 1. Bits 0 and 1 must be set to 0.

2. ASIM20 must be cleared to 00H if 3-wire serial I/O mode is selected.

3. Switch operating modes after halting serial transmit/receive operation.

(c) Baud rate generator control register 20 (BRGC20)

BRGC20 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears BRGC20 to 00H.

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
BRGC20	TPS203	TPS202	TPS201	TPS200	0	0	0	0	FF73H	00H	R/W

TPS203	TPS202	TPS201	TPS200	3-bit counter source clock selection			n
					At fx = 10.0 MHz operation[Note]	At fx = 5.0 MHz operation	
0	0	0	0	fx/2	5.00 MHz	2.50 MHz	1
0	0	0	1	$fx/2^2$	2.50 MHz	1.25 MHz	2
0	0	1	0	$fx/2^3$	1.25 MHz	625 kHz	3
0	0	1	1	$fx/2^4$	625 kHz	313 kHz	4
0	1	0	0	$fx/2^5$	313 kHz	156 kHz	5
0	1	0	1	$fx/2^6$	156 kHz	78.1 kHz	6
0	1	1	0	$fx/2^7$	78.1 kHz	39.1 kHz	7
0	1	1	1	$fx/2^8$	39.1 kHz	19.5 kHz	8
Other than above				Setting prohibited			

Note Expanded-specification products only.

Cautions 1. When writing to BRGC20 is performed during a communication operation, the baud rate generator output is disrupted and communications cannot be performed normally. Be sure not to write to BRGC20 during a communication operation.

2. If fx > 5.0 MHz in the 3-wire serial I/O mode, this setting is prohibited because n = 1 exceeds the rated range of the serial clock.

Remarks 1. fx: Main system clock oscillation frequency

2. n: Values determined by the settings of TPS200 to TPS203 ($1 \le n \le 8$)

If the internal clock is used as the serial clock for 3-wire serial I/O mode, set the TPS200 to TPS203 bits to set the frequency of the serial clock. To obtain the frequency to be set, use the following expression. When an external clock is used, setting BRGC20 is not necessary.

$$\text{Serial clock frequency} = \frac{fx}{2^{n+1}} \text{ [Hz]}$$

fx: Main system clock oscillation frequency

n: Values in the above table determined by the settings of TPS200 to TPS203 ($1 \le n \le 8$)

(2) Communication operation

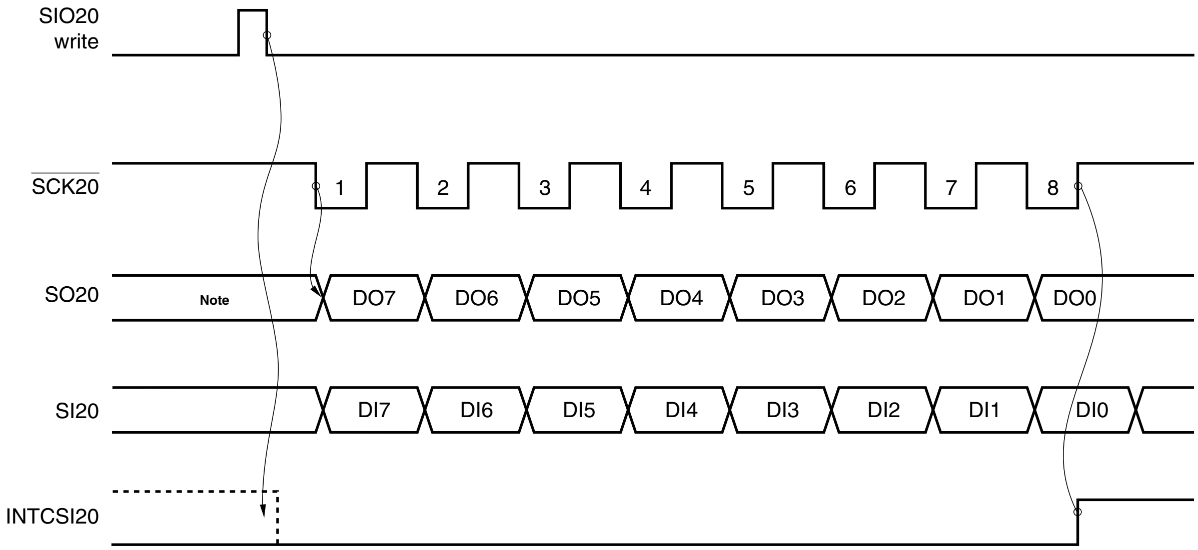
In 3-wire serial I/O mode, data transmission/reception is performed in 8-bit units. Data is transmitted/received bit by bit in synchronization with the serial clock.

Transmission shift register (TXS20/SIO20) and reception shift register (RXS20) shift operations are performed in synchronization with the fall of the serial clock ($\overline{SCK20}$). Then transmit data is held in the SO20 latch and output from the SO20 pin. Also, receive data input to the SI20 pin is latched in the reception buffer register (RXB20/SIO20) on the rise of $\overline{SCK20}$.

At the end of an 8-bit transfer, the operation of TXS20/SIO20 and RXS20 stops automatically, and the interrupt request signal (INTCSI20) is generated.

Figure 14-11. 3-Wire Serial I/O Mode Timing (1/7)

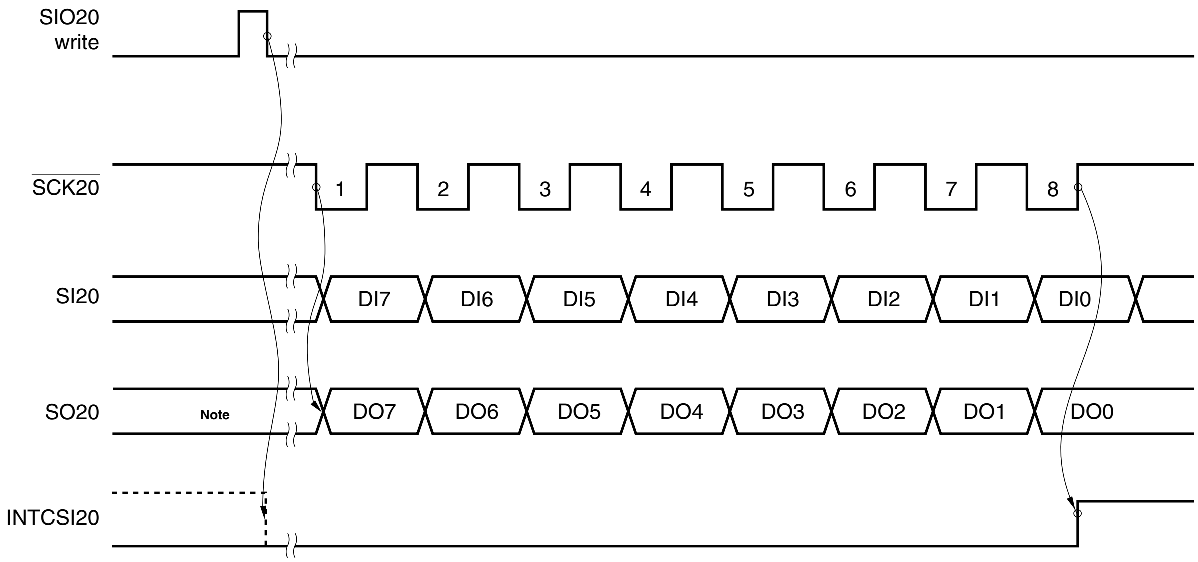
(i) Master operation timing (when DAP20 = 0, CKP20 = 0, SSE20 = 0)



Note The value of the last bit previously output is output.

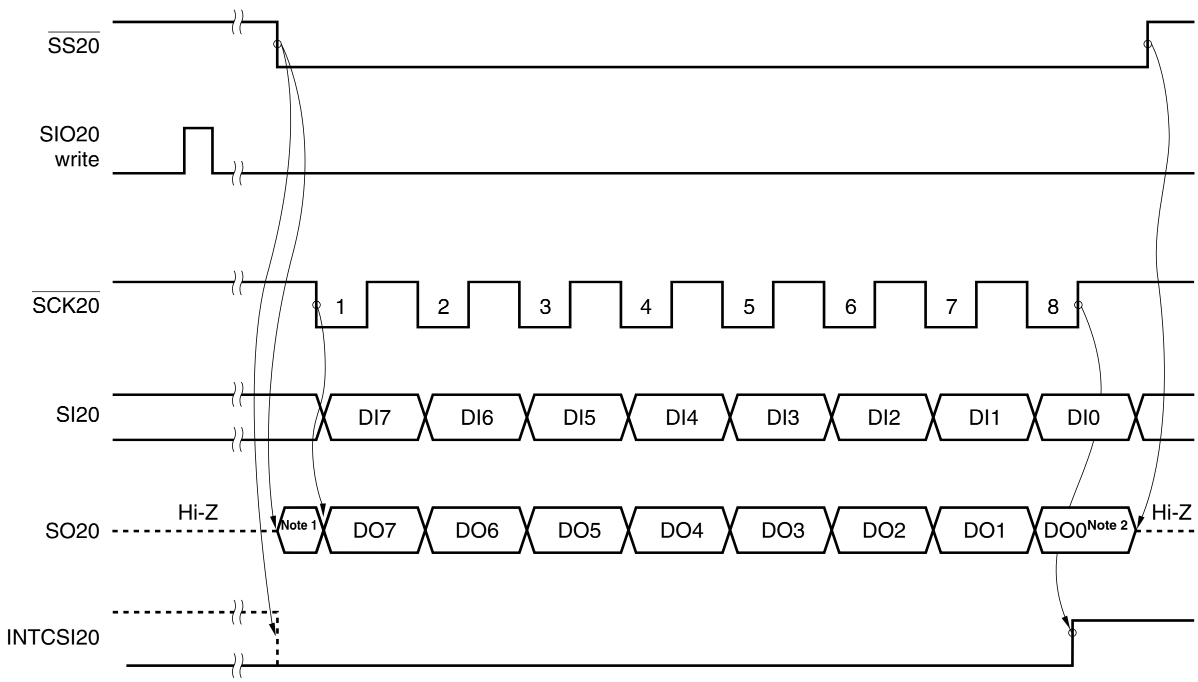
Figure 14-11. 3-Wire Serial I/O Mode Timing (2/7)

(ii) Slave operation timing (when DAP20 = 0, CKP20 = 0, SSE20 = 0)



Note The value of the last bit previously output is output.

(iii) Slave operation (when DAP20 = 0, CKP20 = 0, SSE20 = 1)

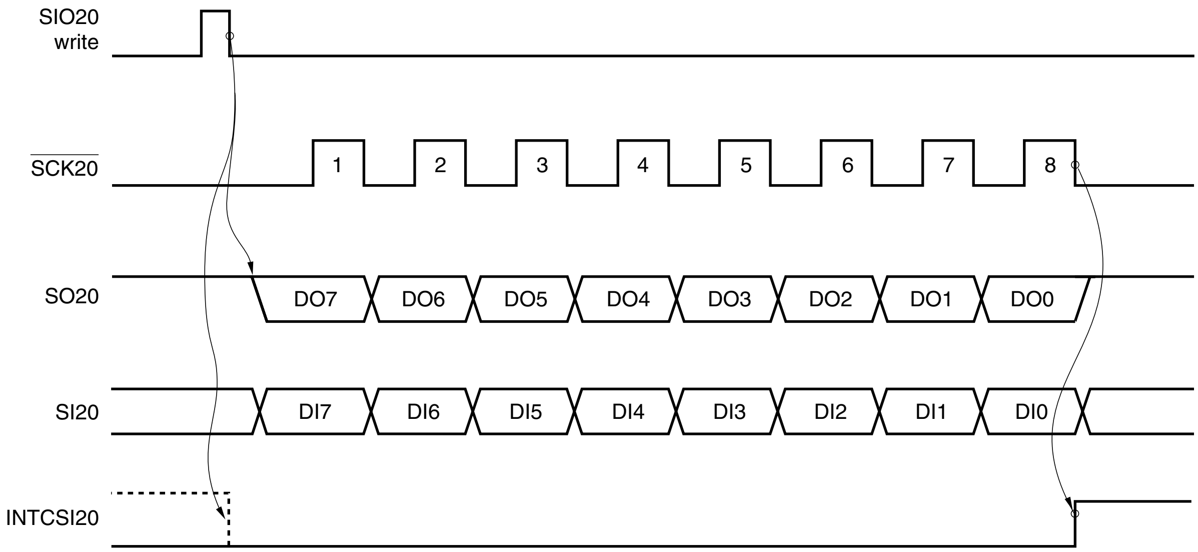


Notes 1. The value of the last bit previously output is output.

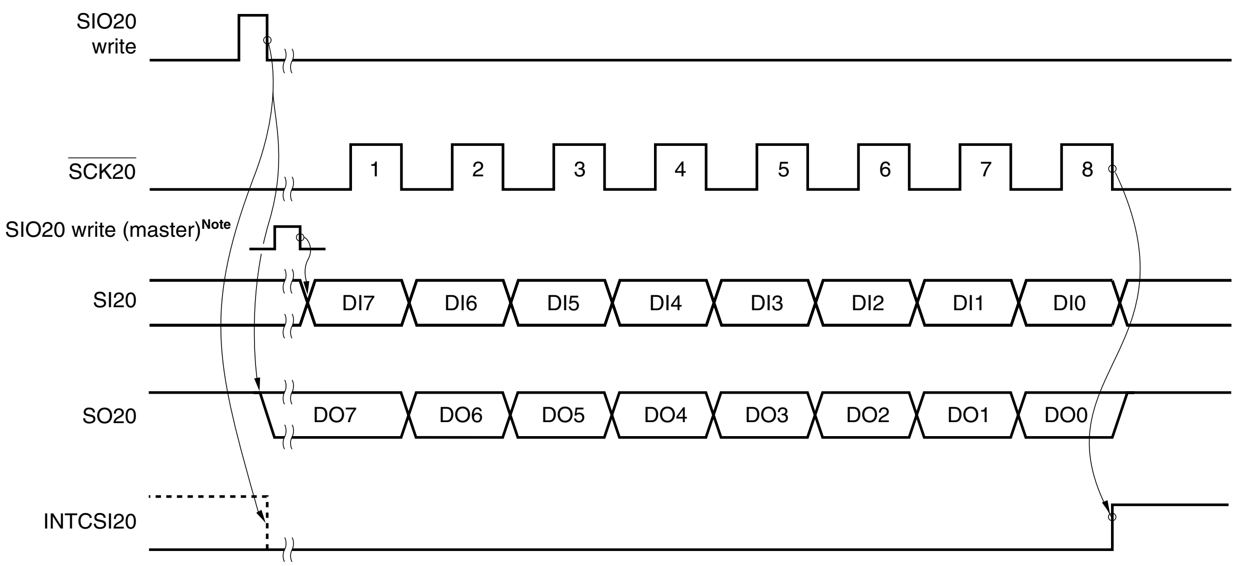
2. DO0 is output until SS20 rises.
When SS20 is high, SO20 is in a high-impedance state.

Figure 14-11. 3-Wire Serial I/O Mode Timing (3/7)

(iv) Master operation (when DAP20 = 0, CKP20 = 1, SSE20 = 0)



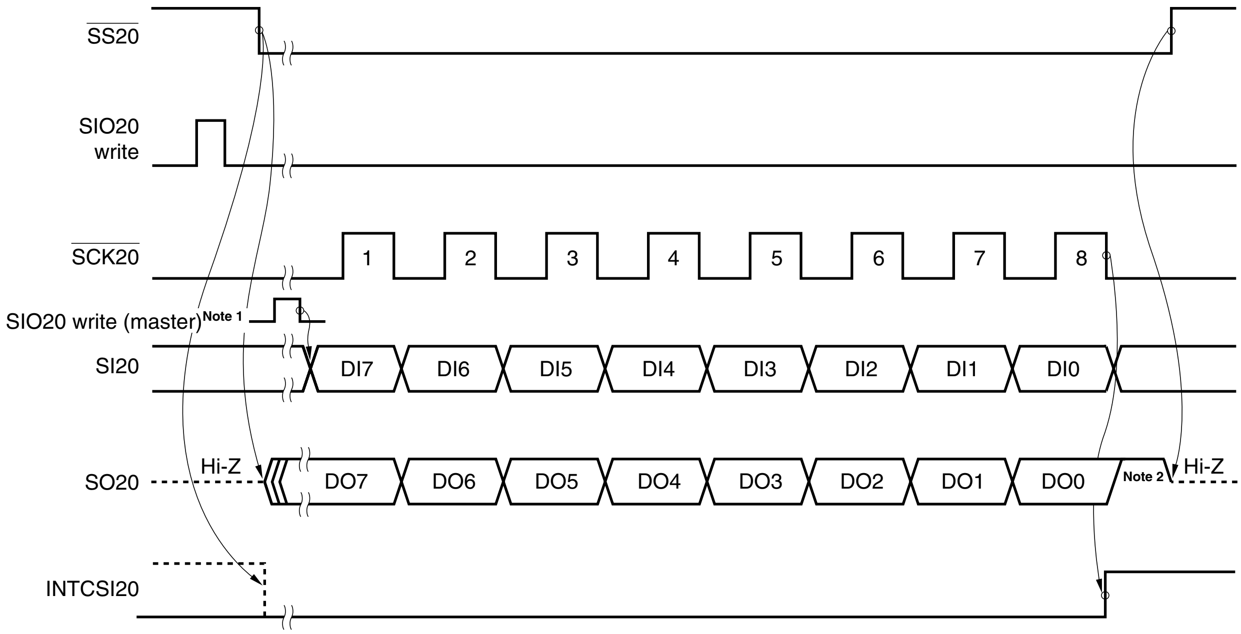
(v) Slave operation (when DAP20 = 0, CKP20 = 1, SSE20 = 0)



Note The data of SI20 is loaded at the first rising edge of $\overline{\text{SCK20}}$. Make sure that the master outputs the first bit before the first rising of $\overline{\text{SCK20}}$.

Figure 14-11. 3-Wire Serial I/O Mode Timing (4/7)

(vi) Slave operation (when DAP20 = 0, CKP20 = 1, SSE20 = 1)



Notes 1. The data of SI20 is loaded at the first rising edge of $\overline{\text{SCK20}}$. Make sure that the master outputs the first bit before the first rising of $\overline{\text{SCK20}}$.

2. SO20 is high until $\overline{\text{SS20}}$ rises after completion of DO0 output. When $\overline{\text{SS20}}$ is high, SO20 is in a high-impedance state.

(vii) Master operation (when DAP20 = 1, CKP20 = 0, SSE20 = 0)

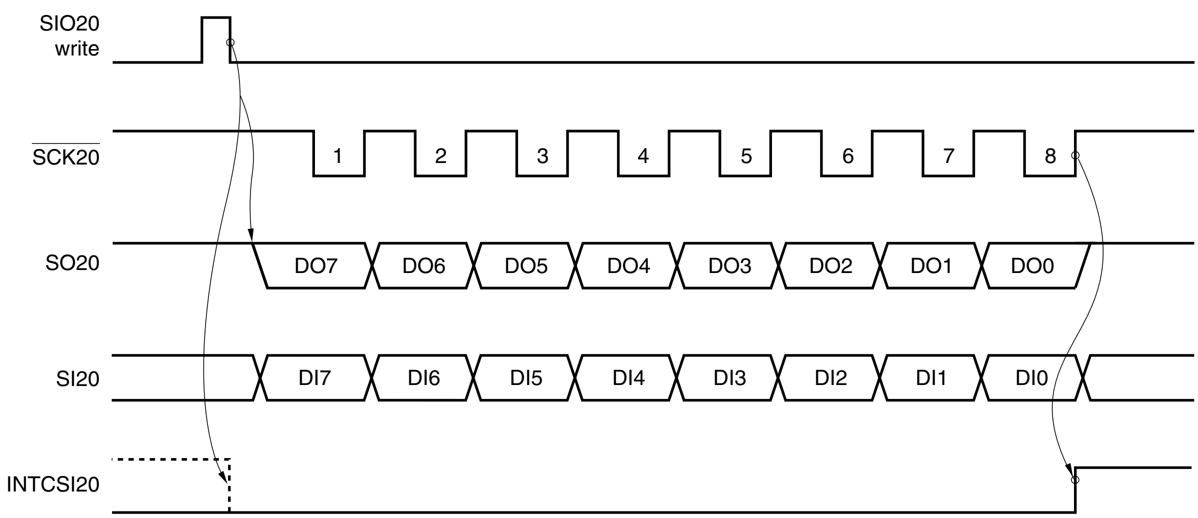
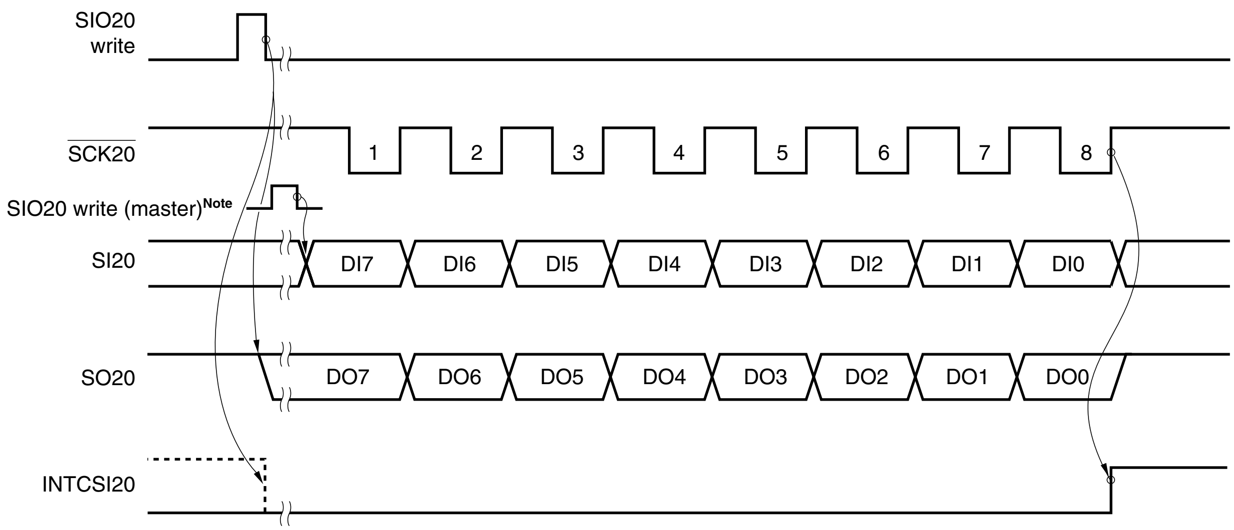


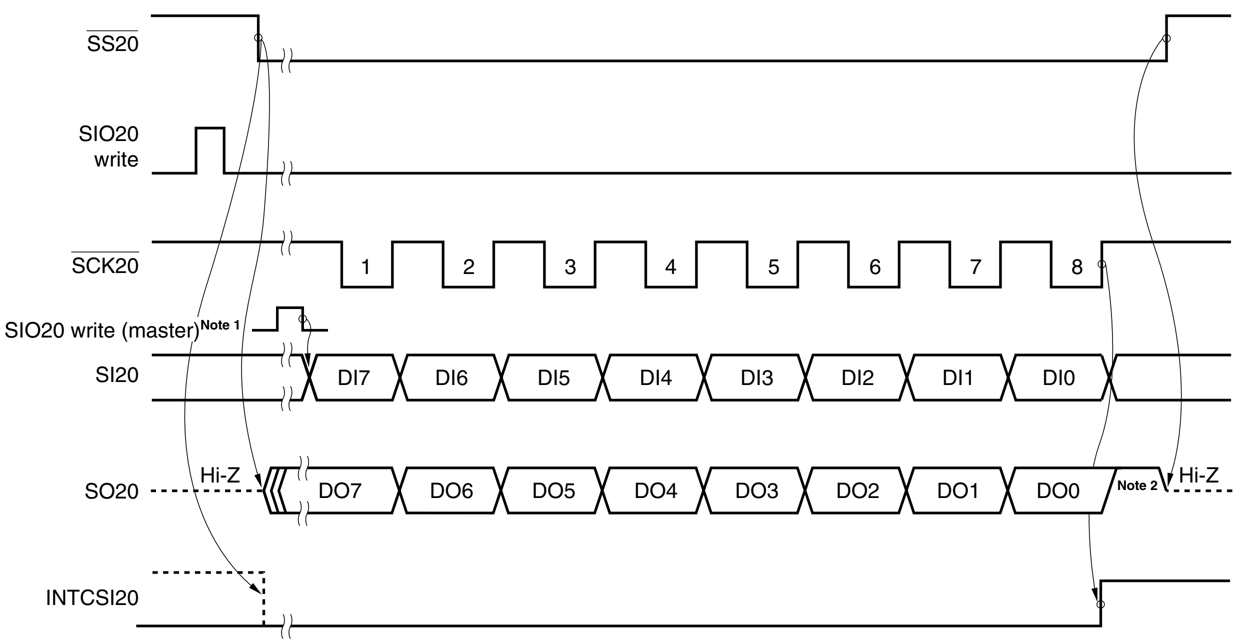
Figure 14-11. 3-Wire Serial I/O Mode Timing (5/7)

(viii) Slave operation (when DAP20 = 1, CKP20 = 0, SSE20 = 0)



Note The data of SI20 is loaded at the first falling edge of $\overline{SCK20}$. Make sure that the master outputs the first bit before the first falling of $\overline{SCK20}$.

(ix) Slave operation (when DAP20 = 1, CKP20 = 0, SSE20 = 1)

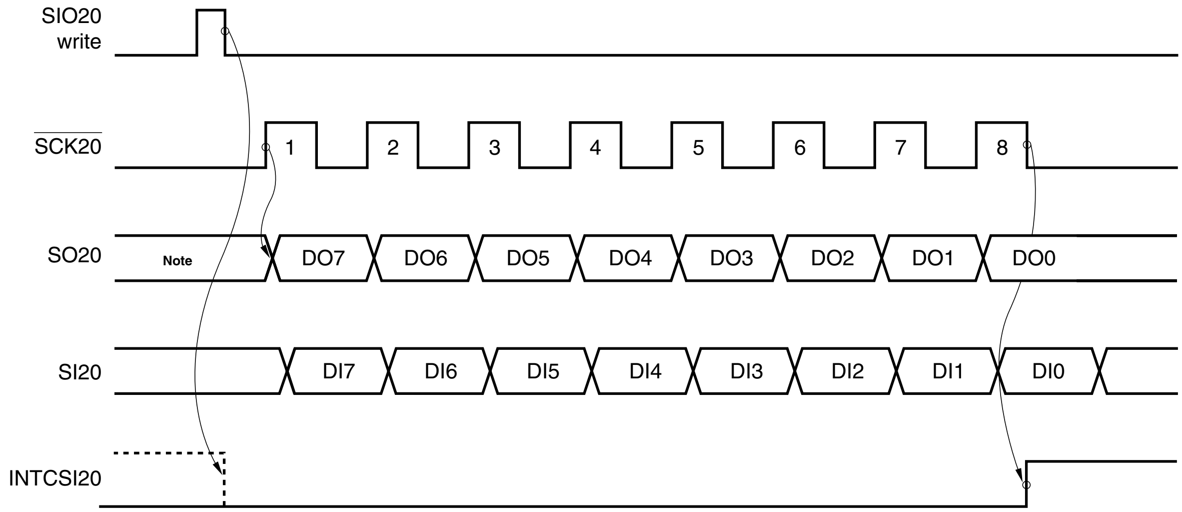


Notes 1. The data of SI20 is loaded at the first falling edge of $\overline{SCK20}$. Make sure that the master outputs the first bit before the first falling of $\overline{SCK20}$.

2. SO20 is high until $\overline{SS20}$ rises after completion of DO0 output. When $\overline{SS20}$ is high, SO20 is in a high-impedance state.

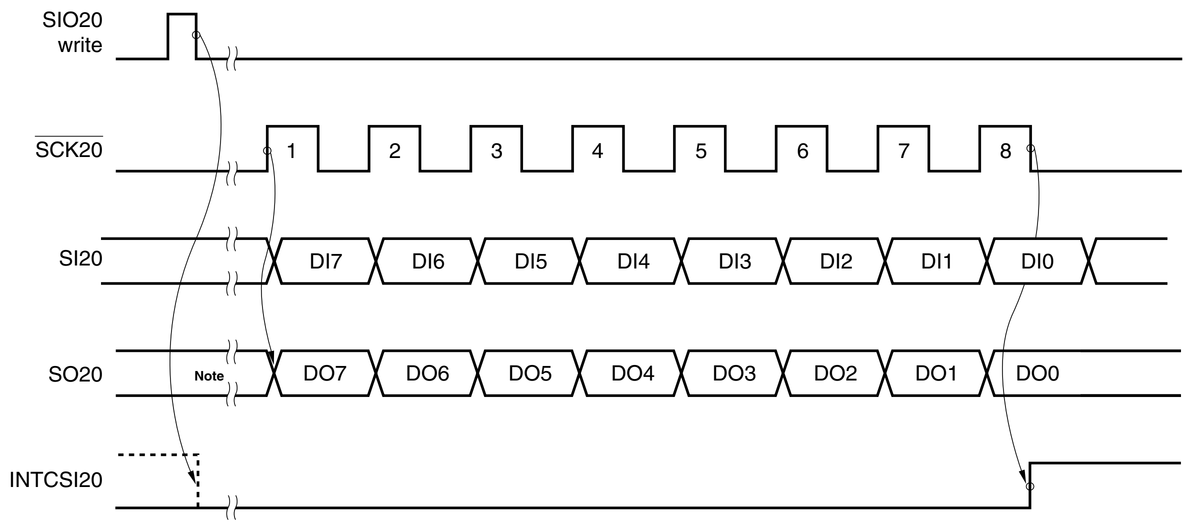
Figure 14-11. 3-Wire Serial I/O Mode Timing (6/7)

(x) Master operation (when DAP20 = 1, CKP20 = 1, SSE20 = 0)



Note The value of the last bit previously output is output.

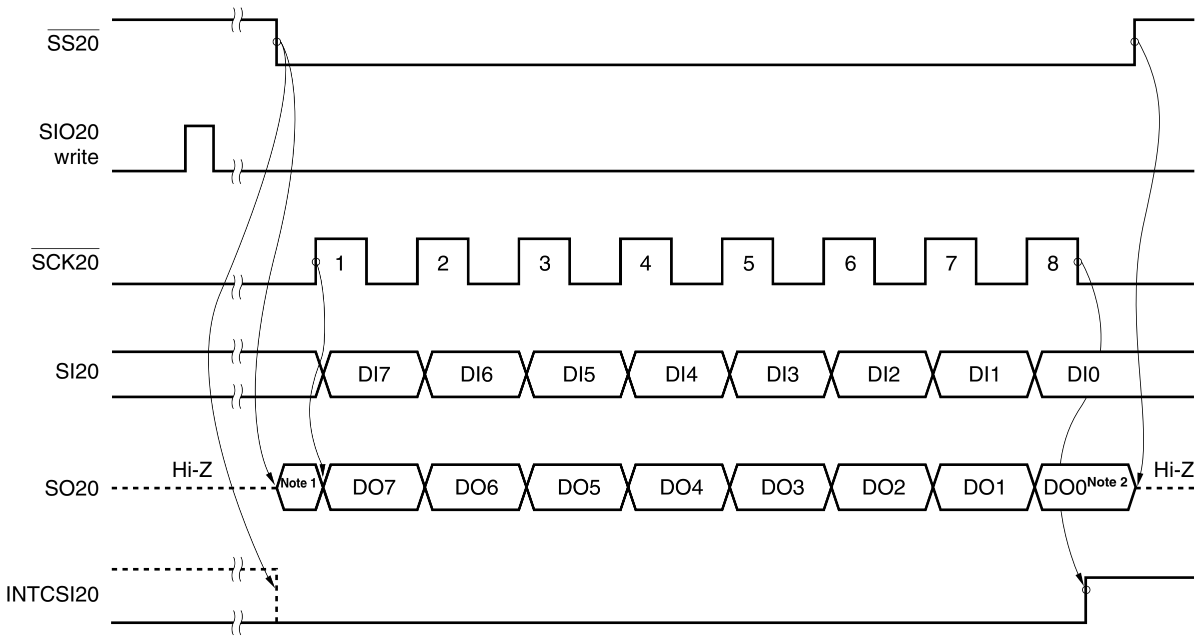
(xi) Slave operation (when DAP20 = 1, CKP20 = 1, SSE20 = 0)



Note The value of the last bit previously output is output.

Figure 14-11. 3-Wire Serial I/O Mode Timing (7/7)

(xii) Slave operation (when DAP20 = 1, CKP20 = 1, SSE20 = 1)



Notes 1. The value of the last bit previously output is output.

2. DO0 is output until $\overline{\text{SS20}}$ rises.

When $\overline{\text{SS20}}$ is high, SO20 is in a high-impedance state.

(3) Transfer start

Serial transfer is started by setting transfer data to the transmission shift register (TXS20/SIO20) when the following two conditions are satisfied.

- Serial operation mode register 20 (CSIM20) bit 7 (CSIE20) = 1
- Internal serial clock is stopped or $\overline{\text{SCK20}}$ is high after 8-bit serial transfer.

Caution If CSIE20 is set to 1 after data is written to TXS20/SIO20, transfer does not start.

A termination of 8-bit transfer stops the serial transfer automatically and generates the interrupt request signal (INTCSI20).

15.1 SMB0 Functions

SMB0 (system management bus) has the following two types of modes.

- Operation stop mode
- SMB mode (supporting multiple masters)

(a) Operation stop mode

This mode is used when serial transfer is not performed. Power consumption is minimized in this mode.

(b) SMB mode (supporting multiple masters)

This mode is used for performing 8-bit data transmission to several devices, using a serial clock (SCL0) line and a serial data bus (SDA0) line.

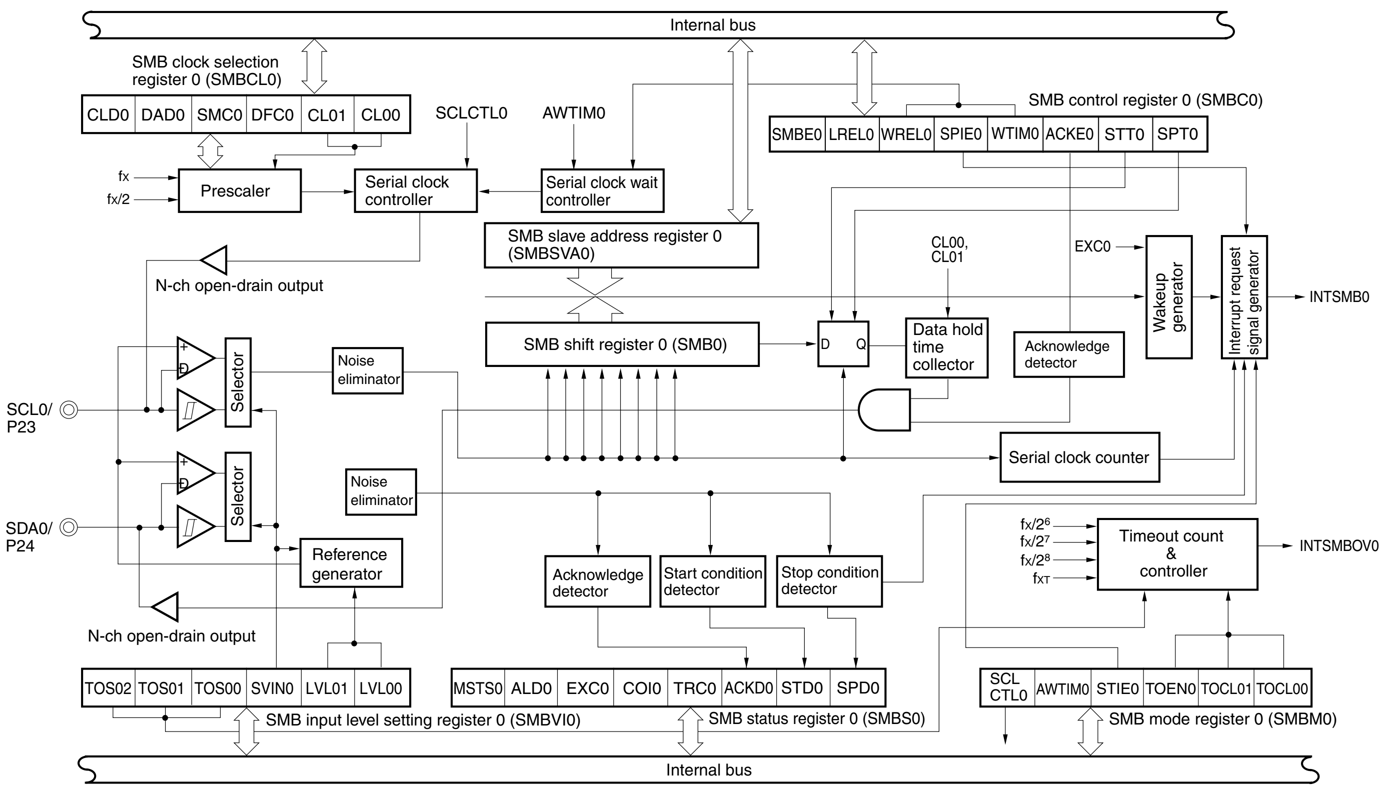
In this mode, which conforms to the SMB format, start conditions, data, and stop conditions can be output on the serial data bus during transmission. Moreover, these data can be automatically detected by hardware during reception.

In SMB0, SCL0 and SDA0 are open-drain outputs, and therefore a pull-up resistor is required for the serial clock line and serial data bus line.

I^2C (Inter IC) bus standard mode or high-speed mode can be specified by software in SMB mode.

Figure 15-1 shows the block diagram of SMB0.

Figure 15-1. Block Diagram of SMB0



15.2 SMB0 Configuration

SMB0 consists of the following hardware.

Table 15-1. Configuration of SMB0

Item	Configuration
Registers	SMB shift register 0 (SMB0) SMB slave address register 0 (SMBSVA0)
Control registers	SMB control register 0 (SMBC0) SMB status register 0 (SMBS0) SMB clock selection register 0 (SMBCL0) SMB mode register 0 (SMBM0) SMB input level setting register 0 (SMBVI0) Port mode register 2 (PM2) Port 2 (P2)

(1) SMB shift register 0 (SMB0)

SMB0 is a register that converts 8-bit serial data to 8-bit parallel data, and vice-versa. SMB0 is used both for transmitting and receiving data.

Write and read operations for SMB0 control actual send and receive operations.

SMB0 is manipulated with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears SMB0 to 00H.

(2) SMB slave address register 0 (SMBSVA0)

This register is used to set a local address when used as a slave.

SMBSVA0 is manipulated with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears SMBSVA0 to 00H.

(3) SO latch

The SO latch is a latch that holds the SDA0 pin output level.

(4) Wakeup controller

This circuit generates an interrupt request when the address value set in SMB slave address register 0 (SMBSVA0) and the received address match, or when an extension code is received.

(5) Clock selector

Selects the sampling clock to be used.

(6) Serial clock counter

Counts the serial clock output/input during send/receive operations, to check if 8-bit data has been sent or received.

(7) Interrupt request signal generator

Controls the generation of interrupt request signals.

SMB interrupts are generated with the following two triggers.

- 8th clock or 9th clock of serial clock (set with WTIM0 bit[Note])
- Generation of interrupt request at detection of stop condition (set with bit SPIE0[Note])

Note WTIM0 bit: SMB control register 0 (SMBC0) bit 3
SPIE0 bit: SMB control register 0 (SMBC0) bit 4

(8) Serial clock controller

In master mode, generates the clock to be output to the SCL0 pin from the sampling clock.

(9) Serial clock wait controller

Controls the wait timing.

(10) Acknowledge output circuit, stop condition detector, start condition detector, acknowledge detector

Perform output and detection of control signals.

(11) Data hold time corrector

Generates the data hold time from the falling edge of the serial clock.

15.3 SMB0 Control Registers

The following five registers are used to control SMB0.

- SMB control register 0 (SMBC0)
- SMB status register 0 (SMBS0)
- SMB clock selection register 0 (SMBCL0)
- SMB mode register 0 (SMBM0)
- SMB input level setting register 0 (SMBVI0)

The following registers are also used.

- SMB shift register 0 (SMB0)
- SMB slave address register 0 (SMBSVA0)

(1) SMB control register 0 (SMBC0)

This register sets SMB operation enable/disable, the wait timing, and other SMB operations.
SMBC0 is manipulated with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears SMBC0 to 00H.

Caution Set port mode register 2 (PM2×) as follows in SMB mode.
Reset the output latch to 0.

- **Set P23 (SCL0) in output mode (PM23 = 0).**
- **Set P24 (SDA0) in output mode (PM24 = 0).**

Figure 15-2. Format of SMB Control Register 0 (1/4)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
SMBC0	SMBE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0	FF78H	00H	R/W

SMBE0	SMB operation[Note 1]
0	Operation disabled. Presets SMB status register 0 (SMBS0). Internal operation also disabled.
1	Operation enabled

Clear conditions (SMBE0 = 0)	Set conditions (SMBE0 = 1)
• Cleared with instruction • Cleared by $\overline{RESET}$ input	• Set with instruction

LREL0	Escape from transmission
0	Normal operation
1	Escape from the current transmission and enter the standby status. Automatically cleared after execution. This bit is used when extension codes not relevant to the local station are received. The SCL0 and SDA0 lines enter the high impedance status. The following flags are cleared. • STD0 • STT0 • SPT0 • ACKD0 • TRC0 • COI0 • EXC0 • MSTS0

The standby status continues until the following communication participation conditions are met.
- Startup as master after detection of stop condition
- Matching addresses or extension code reception after start condition

Clear conditions (LREL0 = 0)[Note 2]	Set conditions (LREL0 = 1)
• Automatically cleared after execution • Cleared by $\overline{RESET}$ input	• Set with instruction

WREL0	Wait cancel
0	Do not cancel wait.
1	Cancel wait. Automatically cleared after wait cancellation.

Clear conditions (WREL0 = 0)[Note 2]	Set conditions (WREL0 = 1)
• Automatically cleared after execution • Cleared by $\overline{RESET}$ input	• Set with instruction

SPIE0	Interrupt request generation at stop condition detection
0	Disabled
1	Enabled

Clear conditions (SPIE0 = 0)[Note 2]	Set conditions (SPIE0 = 1)
• Cleared with instruction • Cleared by $\overline{RESET}$ input	• Set with instruction

Notes 1. Before setting SMBE0 to 1, fix the value of SMB clock selection register 0 (SMBCL0). To change the communication clock, clear SMBE0 to 0 first before rewriting SMBCL0.

2. This flag's signals are made invalid by setting SMBE0 = 0.

Figure 15-2. Format of SMB Control Register 0 (2/4)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
SMBC0	SMBE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0	FF78H	00H	R/W

WTIM0	Wait and interrupt request generation control
0	Generate interrupt request at falling edge of 8th clock. In case of master: Wait with clock output at low level after 8 clocks have been output. In case of slave: Wait master with clock set to low level after 8 clocks have been input.
1	Generate interrupt request at falling edge of 9th clock. In case of master: Wait with clock at low level after 9 clocks have been output. In case of slave: Wait master with clock set to low level after 9 clocks have been input.
The setting of this bit becomes invalid during address transmission, and becomes effective at the end of transmission. During operation as master, a wait is inserted at the falling edge of the 9th clock during address transmission. A slave that receives a local address enters the wait status at the falling edge of the 8th or 9th clock according to the setting of AWTIM0. A slave that receives an extension code enters the wait status at the falling edge of the 8th clock.	

Clear conditions (WTIM0 = 0)Note	Set conditions (WTIM0 = 1)
• Cleared with instruction • Cleared by $\overline{\text{RESET}}$ input	• Set with instruction

ACKE0	Acknowledge control
0	Acknowledge disabled
1	Acknowledge enabled. SDA0 line set to low level during 9 clocks. However, invalid during address transmission, and valid when EXC0 = 1.

Clear conditions (ACKE0 = 0)Note	Set conditions (ACKE0 = 1)
• Cleared with instruction • Cleared by $\overline{\text{RESET}}$ input	• Set with instruction

Note This flag's signals are made invalid by setting SMBE0 = 0.

Figure 15-2. Format of SMB Control Register 0 (3/4)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
SMBC0	SMBE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0	FF78H	00H	R/W

STT0	Start condition trigger
0	Do not generate start condition.
1	When bus is released (stop status): Generate start conditions (activation as master). Change SDA0 line from high level to low level and generate start condition. Then secure rated time and sets SCL0 to low level. When not participating on bus: Functions as start condition reservation flag. When set, automatically generate start condition after bus is released.

Cautions regarding set timing

- Master receive operation: Setting during transmission is prohibited.
  Set ACKE0 = 0; Can be set only after end of receive operation has been reported to slave.
- Master transmit operation: Note that start condition may not be generated normally during $\overline{\text{ACK}}$ period.
- Setting at the same time as SPT0 is prohibited.
- After setting STT0, resetting is prohibited if the clear conditions have not been met.

Clear conditions (STT0 = 0)[Note]	Set conditions (STT0 = 1)
• Cleared with instruction • Cleared upon defeat in arbitration • Cleared after generation of start condition by master • Cleared when LREL0 = 1 • Cleared when SMBE0 = 0 • Cleared by $\overline{\text{RESET}}$ input	• Set with instruction

Note This flag's signals are made invalid by setting SMBE0 = 0.

Figure 15-2. Format of SMB Control Register 0 (4/4)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
SMBC0	SMBE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0	FF78H	00H	R/W

<table>
<tr><th>SPT0</th><th colspan="2">Stop condition trigger</th></tr>
<tr><td>0</td><td colspan="2">Do not generate stop condition.</td></tr>
<tr><td>1</td><td colspan="2">Generate stop condition (end transmission as master).
After setting SDA0 line to low level, set SCL0 line to high level, or maintain SCL0 line at high level.
Then, secure rated time, change SDA0 line from low level to high level, and generate stop condition.</td></tr>
<tr><td colspan="3">Cautions regarding set timing
• Master receive operation: Setting during transmission is prohibited.
Set ACKE0 = 0; Can be set only after end of receive operation has been notified to slave.
• Master send operation: Note that stop condition may not be generated normally during $\overline{\text{ACK}}$ period.
• Setting at the same time as STT0 is prohibited.
• Set SPT0 only during operation as master.[Note 1]
• After setting SPT0, resetting is prohibited if the clear conditions have not been met.
• Note that when WTIM0 = 0, if SPT0 is set during the wait period after 8-clock output, a stop condition is generated during the high-level period of the 9th clock following wait release.
If it is necessary to output a 9th clock, change the setting of WTIM0 from 0 to 1 during the wait period following 8-clock output, and set SPT0 during the wait period following the 9th clock output.</td></tr>
<tr><td colspan="2">Clear conditions (SPT0 = 0)[Note 2]</td><td>Set conditions (SPT0 = 1)</td></tr>
<tr><td colspan="2">• Cleared with instruction
• Cleared upon defeat in arbitration
• Cleared automatically after detection of stop condition
• Cleared when LREL0 = 1
• Cleared when SMBE0 = 0
• Cleared by $\overline{\text{RESET}}$ input</td><td>• Set with instruction</td></tr>
</table>

Notes 1. Set SPT0 only during operation as master. However, for master operation by the time a stop condition is detected for the first time following operation enable, SPT0 must be set once to generate a stop condition.

2. This flag's signals are made invalid by setting SMBE0 = 0.

Caution While SMB status register 0 (SMBS0) bit 3 (TRC0) = 1, when WREL0 is set at the 9th clock and wait is released, TRC0 is cleared and the SDA0 line is set to high impedance.

Remarks 1. STD0: SMB status register 0 (SMBS0) bit 1
ACKD0: SMB status register 0 (SMBS0) bit 2
TRC0: SMB status register 0 (SMBS0) bit 3
COI0: SMB status register 0 (SMBS0) bit 4
EXC0: SMB status register 0 (SMBS0) bit 5
MSTS0: SMB status register 0 (SMBS0) bit 7

2. Bits 0 and 1 (SPT0, STT0) are 0 if read after data setting.

(2) SMB status register 0 (SMBS0)

This register indicates the SMB status.

SMBS0 is manipulated with a 1-bit or 8-bit memory manipulation instruction. SMBS0 is a read-only register.

RESET input clears SMBS0 to 00H.

Figure 15-3. Format of SMB Status Register 0 (1/3)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
SMBS0	MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0	FF79H	00H	R

MSTS0	Master status
0	Slave status or communication wait status
1	Master transmission status

Clear conditions (MSTS0 = 0)	Set conditions (MSTS0 = 1)
• Cleared upon detection of stop condition • Cleared when ALD0 = 1 • Cleared when LREL0 = 1 • Cleared when SMBE0 changes from 1 to 0 • Cleared by RESET input	• Set during generation of start condition

ALD0	Arbitration defeat detection
0	No arbitration, or won in arbitration.
1	Defeated in arbitration. MSTS0 cleared.

Clear conditions (ALD0 = 0)	Set conditions (ALD0 = 1)
• Automatically cleared after reading SMBS0[Note] • Cleared when SMBE0 changes from 1 to 0 • Cleared by RESET input	• Set upon defeat in arbitration

EXC0	Extension code receive detection
0	Do not receive extension code.
1	Receive extension code.

Clear conditions (EXC0 = 0)	Set conditions (EXC0 = 1)
• Cleared upon detection of start condition • Cleared upon detection of stop condition • Cleared when LREL0 = 1 • Cleared when SMBE0 changes from 1 to 0 • Cleared by RESET input	• Set when high 4 bits of received address are 0000 or 1111 (set at rising edge of 8th clock)

Note The bit is also cleared when a bit manipulation instruction is executed for any other bit SMBS0.

Figure 15-3. Format of SMB Status Register 0 (2/3)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
SMBS0	MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0	FF79H	00H	R

COI0	Matching address detection
0	Address does not match.
1	Address matches.

Clear conditions (COI0 = 0)	Set conditions (COI0 = 1)
• Cleared upon detection of start condition • Cleared upon detection of stop condition • Cleared when LREL0 = 1 • Cleared when SMBE0 changes from 1 to 0 • Cleared by $\overline{RESET}$ input	• Set when received address matches local address (SVA0) (set at rising edge of 8th clock)

TRC0	Receive/send status detection
0	Receive status (when not in send status). Sets SDA0 line to high impedance.
1	Send status. Sets so that SO latch value can be output to SDA0 line (valid from falling edge of 9th clock of 1st byte).

Clear conditions (TRC0 = 0)	Set conditions (TRC0 = 1)
• Cleared upon detection of stop condition • Cleared when LREL0 = 1 • Cleared SMBE0 changes from 1 to 0 • Cleared when WREL0 = 1[Note] • Cleared when ALD0 changes from 0 to 1 • Cleared by $\overline{RESET}$ input In case of master: • When "1" is output to 1st byte LSB (transmission direction specification bit) In case of slave: • Upon detection of start condition In case of non-participation in communication	In case of master: • Upon generation of start condition In case of slave: • When "1" is input to 1st byte LSB (transmission direction specification bit)

ACKD0	Acknowledge output
0	Do not detect acknowledge.
1	Detect acknowledge.

Clear conditions (ACKD0 = 0)	Set conditions (ACKD0 = 1)
• Cleared upon detection of stop condition • Cleared at rising edge of 1st clock of following byte • Cleared when LREL0 = 1 • Cleared when SMBE0 changes from 1 to 0 • Cleared by $\overline{RESET}$ input	• Set when SDA0 line is low level at rising edge of 9th clock of SCL0

Note When bit 3 (TRC0) of SMB status register 0 (SMBS0) is set to 1, bit 5 (WREL0) of SMB control register 0 (SMBC0) is set during the ninth clock and wait is canceled, after which TRC0 is cleared and the SDA0 line is set to high impedance.

Figure 15-3. Format of SMB Status Register 0 (3/3)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
SMBS0	MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0	FF79H	00H	R

STD0	Start condition detection
0	Do not detect start condition.
1	Detect start condition. Indicates that address transmission is in progress.

Clear conditions (STD0 = 0)	Set conditions (STD0 = 1)
• Cleared upon detection of stop condition • Cleared at rising edge of 1st clock of byte following address transmission • Cleared when LREL0 = 1 • Cleared when SMBE0 changes from 1 to 0 • Cleared by $\overline{\text{RESET}}$ input	• Set upon detection of start condition

SPD0	Stop condition detection
0	Do not detect stop condition.
1	Detect stop condition. Transmission by master is completed and bus is released.

Clear conditions (SPD0 = 0)	Set conditions (SPD0 = 1)
• Cleared at rising edge of 1st clock of address transfer byte following detection of start condition after this bit has been set • Cleared when SMBE0 changes from 1 to 0 • Cleared by $\overline{\text{RESET}}$ input	• Set upon detection of stop condition

Remark LREL0: SMB control register 0 (SMBC0) bit 6
SMBE0: SMB control register 0 (SMBC0) bit 7

(3) SMB clock selection register 0 (SMBCL0)

This register sets the SMB transmission clock.

SMBCL0 is manipulated with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears SMBCL0 to 00H. Table 15-2 shows the SMB communication clocks.

Figure 15-4. Format of SMB Clock Selection Register 0 (1/2)

Symbol	7	6	<5>	<4>	3	2	1	0	Address	After reset	R/W
SMBCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00	FF7AH	00H	R/W[Note 1]

CLD0	SCL0 line level detection (valid only when SMBE0 = 1)	
0	Detect that SCL0 line is low level.	
1	Detect that SCL0 line is high level.	
Clear conditions (CLD0 = 0)		Set conditions (CLD0 = 1)
• Cleared when SCL0 line is low level • Cleared when SMBE0 = 0 • Cleared by $\overline{\text{RESET}}$ input		• Set when SCL0 line is high level

DAD0	SDA0 line level detection (valid only when SMBE0 = 1)	
0	Detect that SDA0 line is low level.	
1	Detect that SDA0 line is high level.	
Clear conditions (DAD0 = 0)		Set conditions (DAD0 = 1)
• Cleared when SDA0 line is low level • Cleared when SMBE0 = 0 • Cleared by $\overline{\text{RESET}}$ input		• Set when SDA0 line is high level

SMC0	Operating mode switching	
0	IIC standard mode or SMB mode operation	
1	IIC high-speed mode	
Clear conditions (SMC0 = 0)		Set conditions (SMC0 = 1)
• Cleared with instruction • Cleared by $\overline{\text{RESET}}$ input		• Set with instruction

DFC0	Digital filter operation control[Note 2]
0	Digital filter off
1	Digital filter on

Notes 1. Bits 4 and 5 are read-only.

2. The digital filter can be used in high-speed mode. When used in high-speed mode, the digital filter provides a slower response.

Caution Bits 6 and 7 must be set to 0.

Figure 15-4. Format of SMB Clock Selection Register 0 (2/2)

Symbol	7	6	<5>	<4>	3	2	1	0	Address	After reset	R/W
SMBCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00	FF7AH	00H	R/W[Note]

CL01	CL00	Communication clock	
		SMB/IIC standard mode (SMC0 = 0)	IIC high-speed mode (SMC0 = 1)
0	0	fx/44	fx/24
0	1	fx/86	
1	0	fx/172	fx/48
1	1	Setting prohibited	

Note Bits 4 and 5 are read-only.

Caution To change the communication clock, stop operations (SMBE0 = 0) first before rewriting SMBCL0.

Remark fx: Main system clock oscillation frequency

Table 15-2. SMB0 Communication Clock

SMC0	CL01	CL00	Communication Clock		Digital Filter Input Delay
			At fx = 10.0 MHz operation[Note 1]	At fx = 5.0 MHz operation	
0	0	0	227.2 kHz[Note 2]	113.6 kHz[Note 2]	250 ns
0	0	1	116.2 kHz[Note 2]	58.13 kHz	250 ns
0	1	0	58.13 kHz	29.06 kHz	500 ns
1	0	0	416.6 kHz[Note 3]	208.3 kHz	250 ns
1	0	1	416.6 kHz[Note 3]	208.3 kHz	250 ns
1	1	0	208.3 kHz	104.1 kHz	500 ns
Other than above			Setting prohibited		

Notes 1. Expanded-specification products only.

2. Since the SMB/IIC standard mode standards specify a range of 10 to 100 kHz, this communication clock falls outside the specifications.

3. Since the standards of the IIC high-speed mode specify a range of 0 to 400 kHz, this communication clock falls outside the specifications.

(4) SMB mode register 0 (SMBM0)

SMBM0 is used to specify SCL0 level control and interrupt control.

SMBM0 is manipulated with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets SMBM0 to 20H.

Figure 15-5. Format of SMB Mode Register 0 (1/2)

Symbol	7	6	<5>	<4>	<3>	<2>	1	0	Address	After reset	R/W
SMBM0	0	0	SCLCTL0	AWTIM0	STIE0	TOEN0	TOCL01	TOCL00	FF7CH	20H	R/W

SCLCTL0	SCL level control[Note 1]
0	SCL0 is held low. When SCL0 is high, SCL0 is held low after waiting until SCL0 is made low.
1	Normal operation

AWTIM0	Wait and interrupt control when an address match is found[Notes 2, 3]
0	At the slave, an interrupt request is generated on the falling edge of the 9th clock period when an address match (COI0 = 1) is found during address data reception. The clock is pulled low to cause the master to wait.
1	At the slave, an interrupt request is generated on the falling edge of the 8th clock period when an address match (COI0 = 1) is found during address data reception. The clock is pulled low to cause the master to wait.

STIE0	Start condition interrupt enable
0	Start condition interrupt generation is disabled.
1	Normal operation

TOEN0	Time out count enable bit[Note 4]
0	The time out count is cleared to 0, then count operation is disabled.
1	Time out count operation is enabled.

Notes 1. If SCL0 is made low by SCLCTL0, the wait state cannot be released by WREL0.

2. When an extension code is received (EXC0 = 1), a wait state is forcibly set in the 8th clock period.

3. During address transfer, the master waits in the 9th clock period.

4. An interrupt (INTSMBOV0) is generated when the time out counter overflows. The hardware does not reset the SMB operation. Ensure that SMB operation is reset by software after INTSMBOV0 generation.

Caution Bits 6 and 7 must be set to 0.

Figure 15-5. Format of SMB Mode Register 0 (2/2)

Symbol	7	6	<5>	<4>	<3>	<2>	1	0	Address	After reset	R/W
SMBM0	0	0	SCLCTL0	AWTIM0	STIE0	TOEN0	TOCL01	TOCL00	FF7CH	20H	R/W

TOCL01	TOCL00	Time out clock f_{TO} selection bits
0	0	$f_X/2^6$ (78.1 kHz)
0	1	$f_X/2^7$ (39.1 kHz)
1	0	$f_X/2^8$ (19.5 kHz)
1	1	f_{XT} (32.768 kHz)

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

(5) SMB input level setting register 0 (SMBVI0)

SMBVI0 is manipulated with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears SMBVI0 to 00H.

Figure 15-6. Format of SMB Input Level Setting Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
SMBVI0	0	TOS02	TOS01	TOS00	SVIN0	0	LVL01	LVL00	FF7DH	00H	R/W

TOS02	TOS01	TOS00	Time out time selection bits							
				At f_X = 10.0 MHz operation[Note 1]			At f_X = 5.0 MHz operation			At f_{XT} = 32.768 kHz operation
				$f_{TO} = f_X/2^6$	$f_{TO} = f_X/2^7$	$f_{TO} = f_X/2^8$	$f_{TO} = f_X/2^6$	$f_{TO} = f_X/2^7$	$f_{TO} = f_X/2^8$	$f_{TO} = f_{XT}$
0	0	0	1024/f_{TO}	6.55 ms	13.1 ms	26.2 ms	13.1 ms	26.2 ms	52.4 ms	31.2 ms
0	0	1	896/f_{TO}	5.73 ms	11.4 ms	22.9 ms	11.4 ms	22.9 ms	45.8 ms	27.3 ms
0	1	0	768/f_{TO}	4.91 ms	9.83 ms	19.6 ms	9.83 ms	19.6 ms	39.3 ms	23.4 ms
0	1	1	640/f_{TO}	4.09 ms	8.19 ms	16.3 ms	8.19 ms	16.3 ms	32.7 ms	19.5 ms
1	0	0	512/f_{TO}	3.27 ms	6.55 ms	13.1 ms	6.55 ms	13.1 ms	26.2 ms	15.6 ms
1	0	1	384/f_{TO}	2.45 ms	4.91 ms	9.83 ms	4.91 ms	9.83 ms	19.6 ms	11.7 ms
1	1	0	256/f_{TO}	1.63 ms	3.27 ms	6.55 ms	3.27 ms	6.55 ms	13.1 ms	7.81 ms
1	1	1	128/f_{TO}	819 μs	1.63 ms	3.27 ms	1.63 ms	3.27 ms	6.55 ms	3.90 ms

SVIN0	Input level selection bit
0	Same input level as the ordinary hysteresis
1	The voltage set with LVL01 and LVL00I is used as the SCL0 and SDA0 input level threshold

LVL01	LVL00	Input level selection bits[Note 2]
0	0	The input level is 0.1875 × V_{DD}.
0	1	The input level is 0.25 × V_{DD}.
1	0	The input level is 0.375 × V_{DD}.
1	1	The input level is 0.5× V_{DD}.

Notes 1. Expanded-specification products only.

2. Set an input level from 0.75 to 1.25 V.

Caution Bits 2 and 7 must be set to 0.

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

3. f_{TO}: Clock selected using bits 0 and 1 (TOCL00, TOCL01) of SMB mode register 0 (SMBM0)

(6) SMB shift register 0 (SMB0)

This register is used to perform serial transmit/receive (shift operation) in synchronization with the serial clock.

Read/write operations can be performed in 8-bit units, but do not write data to SMB0 during transmission.

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
SMB0									FF7EH	00H	R/W

(7) SMB slave address register 0 (SMBSVA0)

This register stores the SMB slave address.

It can be read/written in 8-bit units, but bit 0 is fixed to 0.

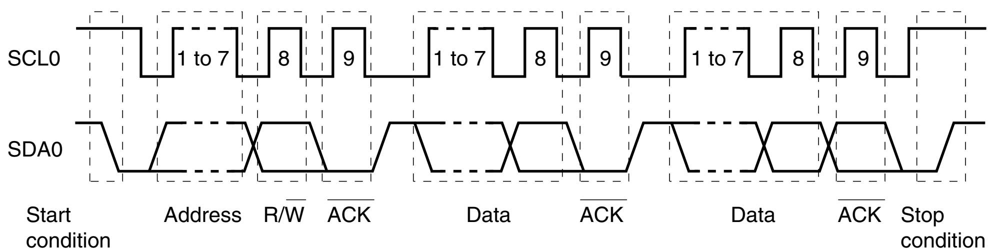
Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
SMBSVA0								0	FF7BH	00H	R/W

15.4 SMB0 Definition and Control Methods

The SMB0 serial data transmission format and the meanings of the signals used are described below.

The transmission timing of the start condition, data, and stop condition output to the serial data bus of the SMB0 is shown in Figure 15-7.

Figure 15-7. SMB0 Serial Data Transmission Timing



The start condition, slave address, and stop condition are output by the master.

SDA0 of only the start condition and stop condition can be changed when SCL0 is high.

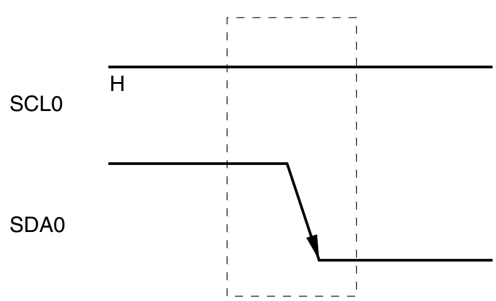
The acknowledge signal ($\overline{ACK}$) can be output by either the master or slave (the slave outputs $\overline{ACK}$ when an address is transferred. The receiver of the data outputs $\overline{ACK}$ when 8-bit data is transferred).

The master continuously outputs the serial clock (SCL0). However, it is possible to prolong the low-level period of the SCL0 and insert a wait in the case of the slave.

15.4.1 Start condition

A start condition is generated when the SDA0 pin changes from high level to low level while the SCL0 pin is high level (serial clock is not output). The start condition of the SCL0 and SDA0 pins is output at the start of serial transmission from the master to the slave. The slave incorporates hardware that detects the start condition.

Figure 15-8. Start Condition



The start condition is output when SMB control register 0 (SMBC0) bit 1 (STT0) is set to 1 in the stop condition detection status (STD0: SMB status register 0 (SMBS0) bit 1 = 1). Moreover, when the start condition is detected, SMBS0 bit 1 (STD0) is set to 1, and when bit 3 (STIE0) of SMBM0 is set to 1, INTSMB0 is generated.

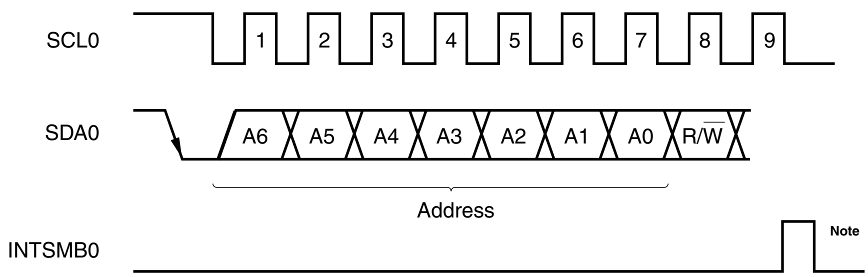
15.4.2 Address

The 7-bit data following the start condition is defined as an address.

An address consists of 7 bits of data output to select a particular slave among several slaves connected to the master via the bus line. Therefore, slaves on the bus line must each have a different address.

Slaves detect start conditions via hardware and check if the 7-bit data matches the value of SMB slave address register 0 (SMBSVA0). If the 7-bit data and the SMBSVA0 value match, that slave is selected, and communication between the master and that slave is performed until the master issues a start condition or a stop condition.

Figure 15-9. Address



Note If other than a local address or extension code is received during slave operation, INTSMB0 is not issued.

Addresses are written and output to SMB shift register 0 (SMB0) as 8 bits consisting of the slave address and the transmission direction (see **15.4.3**). Moreover, received addresses are written to SMB0.

Slave addresses are allocated to the high 7 bits of SMB0.

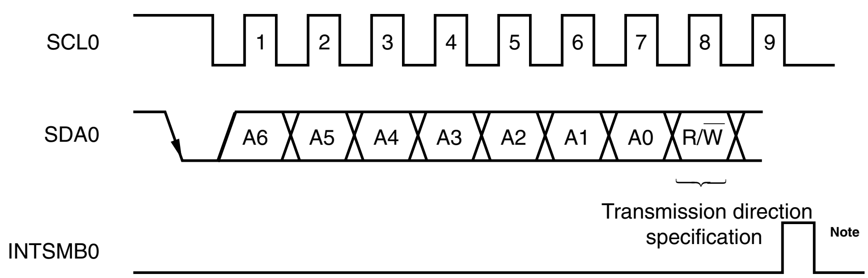
15.4.3 Specification of transmission direction

The master sends a 1-bit data following the 7-bit address to specify the transmission direction.

When this transmission direction bit is 0, the master sends data to the slave.

When this bit is 1, the slave sends data to the master.

Figure 15-10. Specification of Transmission Direction



Note If other than a local address or extension code is received during slave operation, INTSMB0 is not issued.

15.4.4 Acknowledge signal ($\overline{\text{ACK}}$)

The acknowledge signal ($\overline{\text{ACK}}$) is used to confirm reception of serial data on the transmitting and receiving sides.

On the receiving side, an acknowledge signal is returned each time 8 bits of data are received. On the sending side, an acknowledge signal is normally received following transmission of 8 bits of data. However, when the master is receiving, no acknowledge signal is output after the final data has been received. The transmitting side detects whether an acknowledge signal is returned following transmission of 8 bits of data. If an acknowledge signal is returned, processing is continued assuming that the data was successfully received. If no acknowledge signal is returned by the slave, the master outputs a stop condition or a restart condition, and stops transmission. An acknowledge signal is not returned for the following two reasons.

<1> Reception was not performed normally.
<2> The final data was received.

If the receiving side sets the SDA0 line to low level at the 9th clock, the acknowledge signal becomes active (normal reception response).

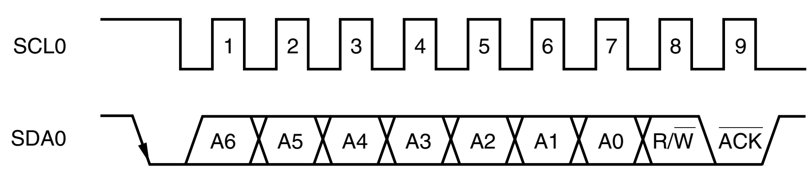
When SMB control register 0 (SMBC0) bit 2 (ACKE0) = 1, the acknowledge signal automatic generation enable state is entered.

SMB status register 0 (SMBS0) bit 3 (TRC0) is set by the 8th bit following the 7-bit address. However, when the TRC0 bit value is 0, receive status is selected, therefore set ACKE0 to 1.

During a slave receive operation (TRC0 = 0), if the slave side receives several bytes and does not require subsequent data, ACKE0 can be set to 0 so that the master does not start the next transmission.

In the same way, if, during a master receive operation (TRC0 = 0), subsequent data is not required and you want to output a restart condition or a stop condition, set ACKE0 to 0 so that no $\overline{\text{ACK}}$ signal is output. This must be done so that the data's MSB is not output to the SDA0 line during the slave transmission operation (transmission stop).

Figure 15-11. Acknowledge Signal



When a slave receives a local address, it automatically outputs an acknowledge signal in synchronization with the falling edge of the 8th clock of SCL0, regardless of the value of ACKE0. If a slave receives other than a local address, no acknowledge signal is output.

The acknowledge signal output method during data reception depends on the wait timing setting, as follows.

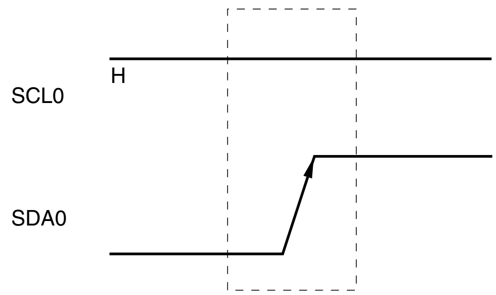
- 8-clock wait: Acknowledge signal is output when the value of ACKE0 becomes 1 before wait cancellation is performed.
- 9-clock wait: Acknowledge signal is automatically output in synchronization with the falling edge of the 8th clock of SCL0 by setting ACKE0 to 1 beforehand.

15.4.5 Stop condition

When the SDA0 pin changes from low level to high level while the SCL0 pin is at high level, a stop condition is generated.

A stop condition is the signal that is output when serial transfer from the master to a slave is completed. Slaves incorporate hardware for the detection of stop conditions.

Figure 15-12. Stop Condition



A stop condition is generated when bit 0 (SPT0) of SMB control register 0 (SMBC0) is set to 1. If, when a stop condition is detected, bit 0 (SPD0) of SMB status register 0 (SMBS0) and bit 4 (SPIE0) of SMBC0 are set to 1, INTSMB0 is generated.

15.4.6 Wait signal ($\overline{\text{WAIT}}$)

A wait signal ($\overline{\text{WAIT}}$) indicates to the other party that the master or slave is getting ready (wait status) to send or receive data.

A wait status is notified by making the SCL0 pin low level. When the wait status of both the master and slave is canceled, the next transmission starts.

Figure 15-13. Wait Signal (1/2)

(1) When master = 9-clock wait, slave = 8-clock wait (Master: send, Slave: receive, ACKE0 = 1)

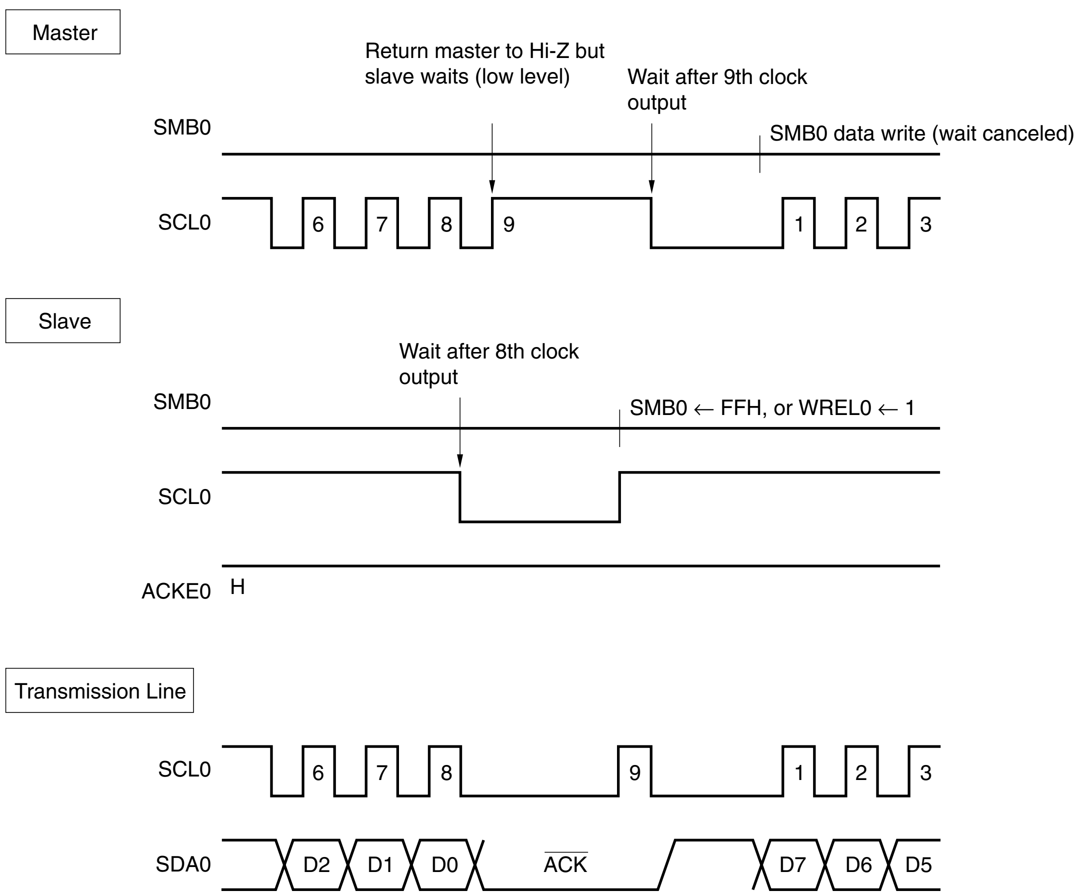
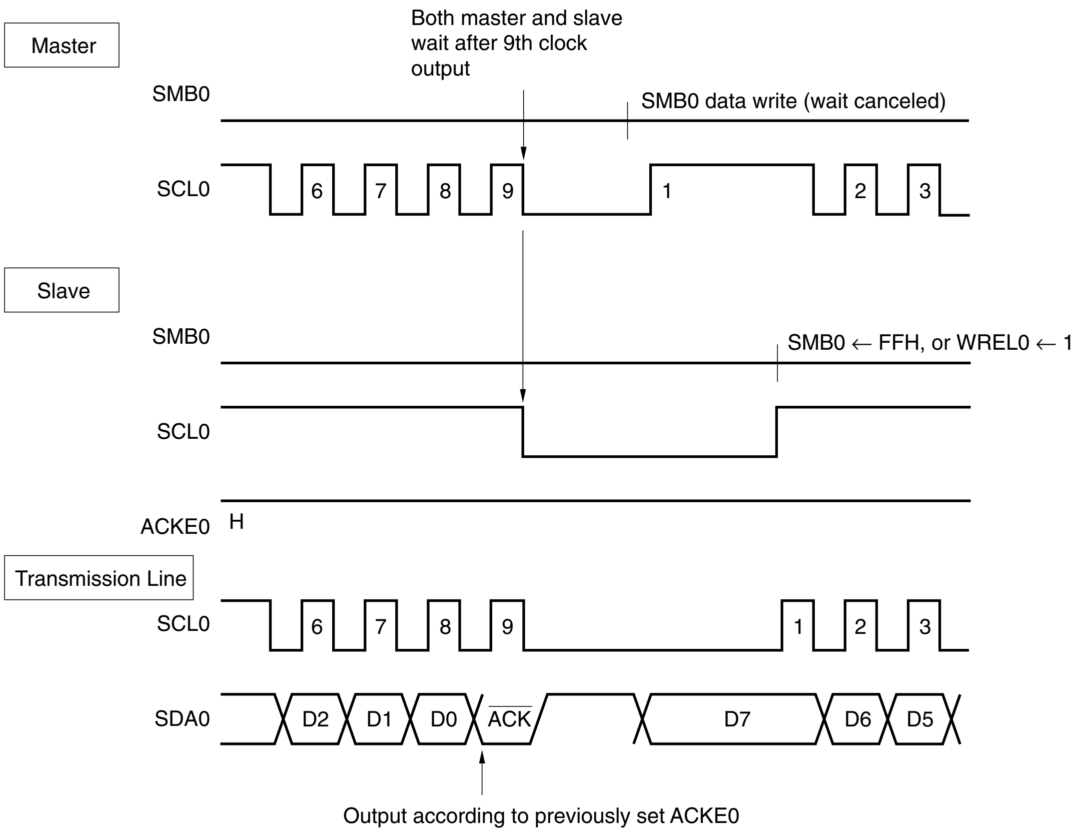


Figure 15-13. Wait Signal (2/2)

(2) Master, slave = 9-clock wait
(Master: send, Slave: receive, ACKE0 = 1)



Remark ACKE0: SMB control register 0 (SMBC0) bit 2
WREL0: SMB control register 0 (SMBC0) bit 5

Waits are automatically generated by setting bit 3 (WTIM0) of SMB control register 0 (SMBC0).
Normally, the receive side cancels the wait status when SMBC0 bit 5 (WREL0) = 1 or SMB shift register (SMB0) ← FFH write, and the transmit side cancels the wait status when data is written to SMB0.
In the case of the master, wait status can be canceled by the following methods.

- Setting SMBC0 bit 1 (STT0) to 1
- Setting SMBC0 bit 0 (SPT0) to 1

15.4.7 SMB0 interrupt (INTSMB0)

The following section shows the values of SMB status register 0 (SMBS0) using the INTSMB0 interrupt request generation timing and INTSMB0 interrupt timing.

Caution The case when AWTIM0 = 0 is described here.

(1) Master operation

(a) Start — Address — Data — Data — Stop (normal send/receive)

<1> When WTIM0 = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 ▲3 ▲4 △5

◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 1000×000B
▲ 3: SMBS0 = 1000×000B
▲ 4: SMBS0 = 1000××00B
△ 5: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 ▲3 △4

◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 1000×100B
▲ 3: SMBS0 = 1000××00B
△ 4: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(b) Start — Address — Data — Start — Address — Data — Stop (restart)

<1> When WTIM0 = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP
◇0			▲1	▲2				▲3		▲4	▲5	△6

◇ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 1000×000B
▲ 3: SMBS0 = 1000×110B
▲ 4: SMBS0 = 1000×000B
▲ 5: SMBS0 = 1000××00B
△ 6: SMBS0 = 00000001B

Remark ◇ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP
◇0			▲1		▲2				▲3		▲4	△5

◇ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 1000××00B
▲ 3: SMBS0 = 1000×110B
▲ 4: SMBS0 = 1000××00B
△ 5: SMBS0 = 00000001B

Remark ◇ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(c) Start — Code — Data — Data — Stop (extension code transmission)

<1> When WTIM0 = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 ▲3 ▲4 △5

◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1010××10B
▲ 2: SMBS0 = 1010×000B
▲ 3: SMBS0 = 1010×000B
▲ 4: SMBS0 = 1010××00B
△ 5: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 ▲3 △4

◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 0010×110B
▲ 2: SMBS0 = 0010×100B
▲ 3: SMBS0 = 0010××00B
△ 4: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(2) Slave operation (during slave address data reception (matching SVA0))

(a) Start — Address — Data — Data — Stop

<1> When WTIM0 = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP
	◊0			▲1	▲2		▲3	△4

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0001×110B
▲ 2: SMBS0 = 0001×000B
▲ 3: SMBS0 = 0001×000B
△ 4: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP
	◊0			▲1		▲2		▲3 △4

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0001×110B
▲ 2: SMBS0 = 0001×100B
▲ 3: SMBS0 = 0001××00B
△ 4: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(b) Start — Address — Data — Start — Address — Data — Stop

<1> When WTIM0 = 0 (matching SVA0 after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 ▲3 ▲4 △5

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0001×110B
▲ 2: SMBS0 = 0001×000B
▲ 3: SMBS0 = 0001×110B
▲ 4: SMBS0 = 0001×000B
△ 5: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1 (matching SVA0 after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 ▲3 ▲4 △5

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0001×110B
▲ 2: SMBS0 = 0001××00B
▲ 3: SMBS0 = 0001×110B
▲ 4: SMBS0 = 0001××00B
△ 5: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(c) Start — Address — Data — Start — Code — Data — Stop

<1> When WTIM0 = 0 (extension code reception after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP
◊0			▲1	▲2				▲3		▲4		△5

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0001×110B
▲ 2: SMBS0 = 0001×000B
▲ 3: SMBS0 = 0010×010B
▲ 4: SMBS0 = 0010×000B
△ 5: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1 (extension code reception after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP
◊0			▲1		▲2			▲3	▲4		▲5	△6

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0001×110B
▲ 2: SMBS0 = 0001××00B
▲ 3: SMBS0 = 0010×010B
▲ 4: SMBS0 = 00100110B
▲ 5: SMBS0 = 0010××00B
△ 6: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(d) Start — Address — Data — Start — Address — Data — Stop

<1> When WTIM0 = 0 (unmatching address (except extension code) after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP
◊0			▲1	▲2					▲3			△4

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0001×110B
▲ 2: SMBS0 = 0001×000B
▲ 3: SMBS0 = 0000××10B
△ 4: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1 (unmatching address (except extension code) after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP
◊0			▲1		▲2				▲3			△4

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0001×110B
▲ 2: SMBS0 = 0001××00B
▲ 3: SMBS0 = 0000××10B
△ 4: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(3) Slave operation (during extension code reception)

(a) Start — Code — Data — Data — Stop

<1> When WTIM0 = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◇0 ▲1 ▲2 ▲3 △4

◇ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0010×010B
▲ 2: SMBS0 = 0010×000B
▲ 3: SMBS0 = 0010×000B
△ 4: SMBS0 = 00000001B

Remark ◇ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◇0 ▲1 ▲2 ▲3 ▲4 △5

◇ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0010×010B
▲ 2: SMBS0 = 0010×110B
▲ 3: SMBS0 = 0010××00B
▲ 4: SMBS0 = 0010××00B
△ 5: SMBS0 = 00000001B

Remark ◇ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(b) Start — Code — Data — Start — Address — Data — Stop

<1> When WTIM0 = 0 (matching SVA0 after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 ▲3 ▲4 △5

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0010×010B
▲ 2: SMBS0 = 0010×000B
▲ 3: SMBS0 = 0001×110B
▲ 4: SMBS0 = 0001×000B
△ 5: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1 (matching SVA0 after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 ▲3 ▲4 ▲5 △6

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0010×010B
▲ 2: SMBS0 = 0010×110B
▲ 3: SMBS0 = 0010××00B
▲ 4: SMBS0 = 0001×110B
▲ 5: SMBS0 = 0001××00B
△ 6: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(c) Start — Code — Data — Start — Code — Data — Stop

<1> When WTIM0 = 0 (extension code reception after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP
◊0		▲1		▲2					▲3	▲4		△5

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0010×010B
▲ 2: SMBS0 = 0010×000B
▲ 3: SMBS0 = 0010×010B
▲ 4: SMBS0 = 0010×000B
△ 5: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1 (extension code reception after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP
◊0		▲1	▲2		▲3			▲4	▲5		▲6	△7

◊ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0010×010B
▲ 2: SMBS0 = 0010×110B
▲ 3: SMBS0 = 0010××00B
▲ 4: SMBS0 = 0010×010B
▲ 5: SMBS0 = 0010×110B
▲ 6: SMBS0 = 0010××00B
△ 7: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(d) Start — Code — Data — Start — Address — Data — Stop

<1> When WTIM0 = 0 (unmatching address (except extension code) after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP

◇0 ▲1 ▲2 ▲3 △4

◇ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0010×010B
▲ 2: SMBS0 = 0010×000B
▲ 3: SMBS0 = 00000×10B
△ 4: SMBS0 = 00000001B

Remark ◇ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1 (unmatching address (except extension code) after restart)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP

◇0 ▲1 ▲2 ▲3 ▲4 △5

◇ 0: SMBS0 = 00000010B
▲ 1: SMBS0 = 0010×010B
▲ 2: SMBS0 = 0010×110B
▲ 3: SMBS0 = 0010××00B
▲ 4: SMBS0 = 00000×10B
△ 5: SMBS0 = 00000001B

Remark ◇ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(4) Non-participation in communication

(a) Start — Code — Data — Data — Stop

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◇0 △1

◇ 0: SMBS0 = 00000010B
△ 1: SMBS0 = 00000001B

Remark ◇ Generate only when STIE0 = 1
△ Generate only when SPIE0 = 1

(5) Arbitration defeat operation (operation as slave after arbitration defeat)

(a) In case of arbitration defeat during slave address data transmission

<1> When WTIM0 = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP	
	◇0			▲1	▲2		▲3		△4

◇ 0: SMBS0 = 10001010B

▲ 1: SMBS0 = 0101×110B (Example: Read ALD0 during interrupt processing)

▲ 2: SMBS0 = 0001×000B

▲ 3: SMBS0 = 0001×000B

△ 4: SMBS0 = 00000001B

Remark
◇ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP	
	◇0			▲1		▲2		▲3	△4

◇ 0: SMBS0 = 10001010B

▲ 1: SMBS0 = 0101×110B (Example: Read ALD0 during interrupt processing)

▲ 2: SMBS0 = 0001×100B

▲ 3: SMBS0 = 0001××00B

△ 4: SMBS0 = 00000001B

Remark
◇ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(b) In case of arbitration defeat during extension code transmission

<1> When WTIM0 = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 ▲3 △4

◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 0110×010B (Example: Read ALD0 during interrupt processing)
▲ 2: SMBS0 = 0010×000B
▲ 3: SMBS0 = 0010×000B
△ 4: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 ▲3 ▲4 △5

◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 0110×010B (Example: Read ALD0 during interrupt processing)
▲ 2: SMBS0 = 0010×110B
▲ 3: SMBS0 = 0010×100B
▲ 4: SMBS0 = 0010××00B
△ 5: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(6) Arbitration defeat operation (non-participation after arbitration defeat)

(a) In case of arbitration defeat during slave address data transmission

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◊0 ▲1 △2

◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 01000110B (Example: Read ALD0 during interrupt processing)
△ 2: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1

(b) In case of arbitration defeat during extension code transmission

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

◊0 ▲1 △2

◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 0110×010B (Example: Read ALD0 during interrupt processing, LREL0 = 1 set by software)
△ 2: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(c) In case of arbitration defeat during data transmission

<1> When WTIM0 = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP	
	◊0			▲1	▲2				△3

◊ 0: SMBS0 = 10001010B

▲ 1: SMBS0 = 10001110B

▲ 2: SMBS0 = 01000000B (Example: Read ALD0 during interrupt processing)

△ 3: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1

▲ Always generate

△ Generate only when SPIE0 = 1

<2> When WTIM0 = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP	
	◊0			▲1		▲2			△3

◊ 0: SMBS0 = 10001010B

▲ 1: SMBS0 = 10001110B

▲ 2: SMBS0 = 01000100B (Example: Read ALD0 during interrupt processing)

△ 3: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1

▲ Always generate

△ Generate only when SPIE0 = 1

(d) In case of defeat by restart condition during data transmission

<1> Other than extension code (Example: Matching SVA0)

ST	AD6 to AD0	RW	AK	D7 to Dn	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 △3

◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 01000110B (Example: Read ALD0 during interrupt processing)
△ 3: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care
Dn = D6 to D0

<2> Extension code

ST	AD6 to AD0	RW	AK	D7 to Dn	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP

◊0 ▲1 ▲2 △3

◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 0110×010B (Example: Read ALD0 during interrupt processing,
SMBC0: LREL0 = 1 set by software)
△ 3: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care
Dn = D6 to D0

(e) In case of defeat by stop condition during data transmission

ST	AD6 to AD0	RW	AK	D7 to Dn	SP

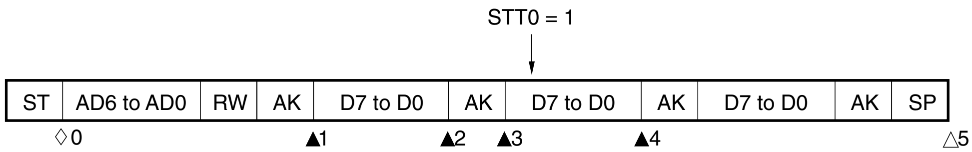
◇0 ▲1 △2

◇ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
△ 2: SMBS0 = 01000001B

Remark ◇ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care
Dn = D6 to D0

(f) In case of arbitration defeat by data low level while attempting to generate restart condition

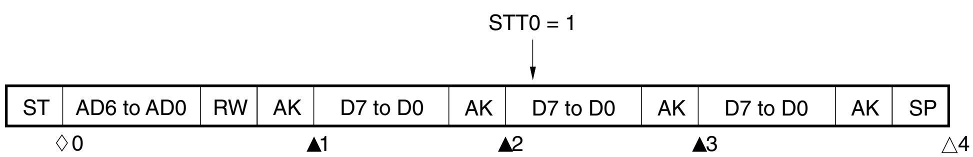
<1> When WTIM0 = 0



◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 1000×000B
▲ 3: SMBS0 = 1000××00B
▲ 4: SMBS0 = 10000000B (Example: Read ALD0 during interrupt processing)
△ 5: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1

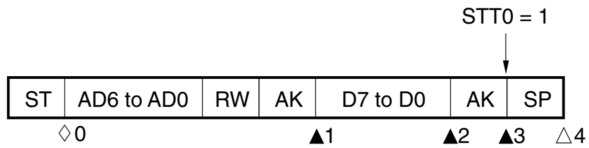


◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 1000××00B
▲ 3: SMBS0 = 01000100B (Example: Read ALD0 during interrupt processing)
△ 4: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(g) In case of arbitration defeat by stop condition while attempting to generate restart condition

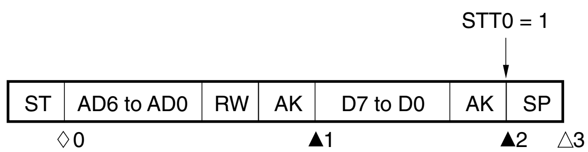
<1> When WTIM0 = 0



◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 1000×000B
▲ 3: SMBS0 = 1000××00B
△ 4: SMBS0 = 01000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1

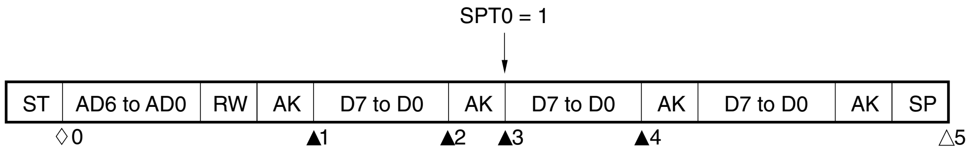


◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 1000××00B
△ 3: SMBS0 = 01000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(h) In case of arbitration defeat by data low level while attempting to generate a stop condition

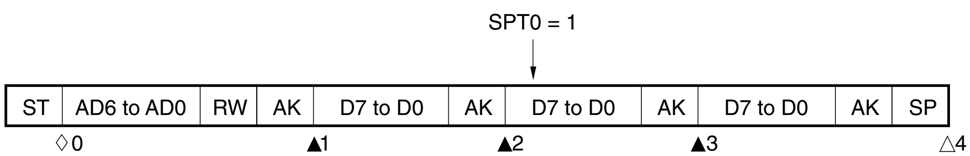
<1> When WTIM0 = 0



◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 1000×000B
▲ 3: SMBS0 = 1000××00B
▲ 4: SMBS0 = 01000000B (Example: Read ALD0 during interrupt processing)
△ 5: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

<2> When WTIM0 = 1



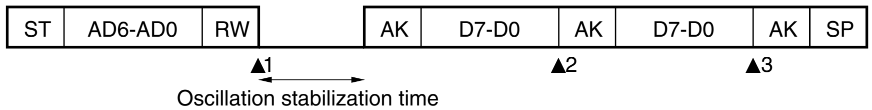
◊ 0: SMBS0 = 10001010B
▲ 1: SMBS0 = 1000×110B
▲ 2: SMBS0 = 1000××00B
▲ 3: SMBS0 = 01000000B (Example: Read ALD0 during interrupt processing)
△ 4: SMBS0 = 00000001B

Remark ◊ Generate only when STIE0 = 1
▲ Always generate
△ Generate only when SPIE0 = 1
× Don't care

(7) Slave operation (after STOP mode is released)

(a) Start — Address — Data — Data — Stop

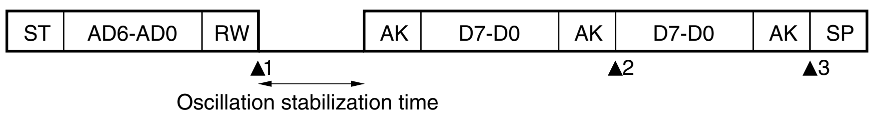
<1> When WTIM0 = 0



▲1: SMBS0 = 0001X010B
▲2: SMBS0 = 0001X000B
▲3: SMBS0 = 0001X000B

Remark ▲ Always generate
× Don't care

<2> When WTIM0 = 1



▲1: SMBS0 = 0001X010B
▲2: SMBS0 = 0001X100B
▲3: SMBS0 = 0001XX00B

Remark ▲ Always generate
× Don't care

Cautions 1. Be sure to set STIE0 = SPIE0 = 0 when releasing STOP mode upon address match. In this case however, the timeout count operation or stop operation cannot be controlled, because an interrupt is not generated even if a start or stop condition is output by another device during STOP mode operation.

2. When releasing STOP mode, the timeout count operation cannot be performed in the period from the start condition to oscillation stabilization, because an interrupt is not generated when a start condition is generated.

15.4.8 Interrupt request (INTSMB0) generation timing and wait control

INTSMB0 generation and wait control can be performed at the timing indicated in Table 15-3 by setting bit 3 (WTIM0) of SMB control register 0 (SMBC0).

Table 15-3. INTSMB0 Generation Timing and Wait Control

WTIM0	AWTIM0	During Slave Operation			During Master Operation		
		Address	Data Receive	Data Transmit	Address	Data Receive	Data Transmit
0	0	9 Notes 1, 2	8 Note 2	8 Note 2	9	8	8
	1	8 Notes 1, 2					
1	0	9 Notes 1, 2	9 Note 2	9 Note 2	9	9	9
	1	8 Notes 1, 2					

Notes 1. INTSMB0 and wait signals are generated by a slave at the falling edge of the 8th or 9th clock according to the setting of AWTIM0 only when matching with the address of the SMB slave address register (SMBSVA0) occurs.
Moreover, at this time, an $\overline{ACK}$ signal is output regardless of the setting of bit 2 (ACKE0) of SMBC0. A slave that receives an extension code generates INTSMB0 at the falling edge of the 8th clock.

2. If the address received does not match the address set in SMB slave address register 0 (SMBSVA0), the slave does not generate INTSMB0 and wait signals.

Remark Figures listed in Table 15-3 above indicate the number of serial clocks. Interrupt requests and wait control are synchronized with the falling edge of the serial clock.

(1) During address transmission/reception

- During slave operation: Interrupt and wait timing is set based on the conditions described in notes 1 and 2 above regardless of the WTIM0 bit setting.
- During master operation: Interrupt and wait signals are generated at the falling edge of the 9th clock regardless of the WTIM0 bit setting.

(2) During data reception

- During master/slave operation: Interrupt and wait timing is set by the WTIM0 bit.

(3) During data transmission

- During master/slave operation: Interrupt and wait timing is set by the WTIM0 bit.

(4) Wait cancellation method

Waits can be canceled by one of the following four methods.

- Setting SMB control register 0 (SMBC0) bit 5 (WREL0) to 1
- Performing SMB shift register 0 (SMB0) write operation
- Setting a start condition (by setting SMBC0 bit 1 (STT0) to 1)
- Setting a stop condition (by setting SMBC0 bit 0 (SPT0) to 1)

When 8-clock wait is selected (WTIM0 = 0), the $\overline{ACK}$ output level must be determined before the wait status is released.

(5) Stop condition detection

An INTSMB0 signal is output when a stop condition is detected (only when SPIE0 = 1).

(6) Start condition detection

An INTSMB0 signal is output when a start condition is detected (only when STIE0 = 1).

15.4.9 Matching address detection method

In SMB mode, a particular slave device can be selected by sending that slave address to the master.

The detection of matching addresses is performed automatically by hardware. If a local address has been set in SMB slave address register 0 (SMBSVA0), and the slave address sent from the master matches the address set in SMBSVA0, or if the extension code is received, an INTSMB0 interrupt request is generated.

15.4.10 Error detection

In SMB mode, because the status of the serial data bus (SDA0) during transmission is also input to SMB shift register 0 (SMB0), transmission errors can be detected by comparing the SMB0 data before transmission start and at transmission end. If the two data do not match, a transmission error is considered to have occurred.

15.4.11 Extension code

(1) An extension code is considered to have been received when the high four bits of the receive address are 0000 or 1111, and in this case the extension code receive flag (EXC0) is set and an interrupt request (INTSMB0) is generated at the falling edge of the 8th clock.
The local address stored in SMB slave address register 0 (SMBSVA0) is not affected.

(2) When 111110×× is set to SMBSVA0 and 111110××0 is transferred from the master during transfer of a 10-bit address, the following occurs. However, INTSMB0 is generated at the falling edge of the 8th clock.

- Matching high 4 bits: EXC0 = 1[Note]
- Matching 7-bit data: COI0 = 1[Note]

Note EXC0: SMB status register 0 (SMBS0) bit 5
COI0: SMB status register 0 (SMBS0) bit 4

(3) Because the processing after an interrupt request is generated differs depending on the data that follows the extension code, it is performed by software. For instance, if operation as a slave is not desired following the reception of an extension code, set LREL0 to 1, in which case the following communication standby status is entered.

Table 15-4. Extension Code Bit Definition

Slave Address	R/W Bit	Description
0000 000	0	General call address
0000 000	1	Start byte
0000 001	×	CBUS address
0000 010	×	Address reserved for different bus format
1111 0××	×	10-bit slave address specification

Addresses reserved for system management bus are described below.

Slave Address	Description
0001 000	SMB host
0001 100	Response address for SMB alert
1010 001	Default address of SMB device
1001 0××	Free address

15.4.12 Arbitration

If several masters output a start condition simultaneously (when STT0 is set to 1 before STD0 is set to 1[Note]), master communication is performed while adjusting the clock until data differs. This operation is referred to as arbitration.

A master defeated in arbitration sets the arbitration defeat flag (ALD0) of SMB status register 0 (SMBS0), and sets the SCL0 and SDA0 lines to Hi-Z to release the bus.

Arbitration defeat is detected by software when ALD0 = 1 at the next interrupt request generation timing (8th or 9th clock, stop condition detection, etc.).

For the interrupt generation timing, see **15.4.7 SMB0 interrupt (INTSMB0)**.

Note STD0: SMB status register 0 (SMBS0) bit 1
STT0: SMB control register 0 (SMBC0) bit 1

Figure 15-14. Arbitration Timing Examples

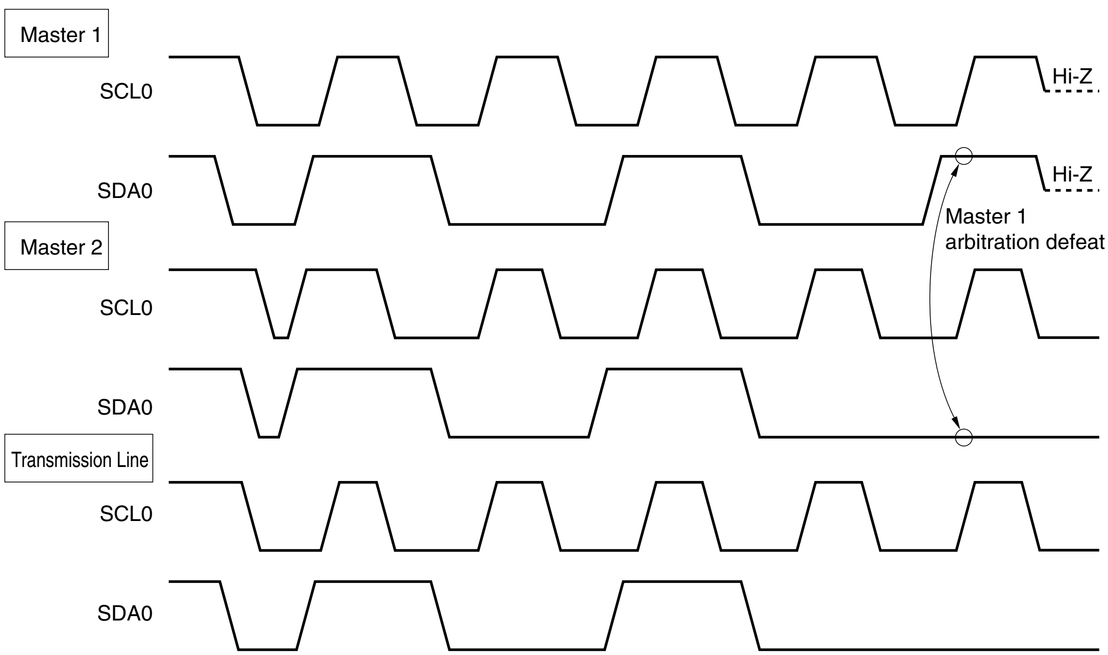


Table 15-5. Status at Arbitration and Interrupt Request Generation Timing

Status at Arbitration	Interrupt Request Generation Timing
Address transmission in progress	Falling edge of 8th or 9th clock following byte transmission[Note 1]
Read/write information following address transmission	
Extension code transmission in progress	
Read/write information following extension code transmission	
Data transmission in progress	
$\overline{\text{ACK}}$ transmission in progress following data transmission	
Data transmission in progress, restart condition detection	
Data transmission in progress, stop condition detection	During stop condition output (SPIE0 = 1)[Note 2]
Attempt to output restart condition was made, but data was low level	Falling edge of 8th or 9th clock following byte transfer[Note 1]
Attempt to output restart condition was made, but stop condition was detected	During stop condition output (SPIE0 = 1)[Note 2]
Attempt to output stop condition was made, but data was low level	Falling edge of 8th or 9th clock following byte transfer[Note 1]
Attempt to output restart condition was made, but SCL0 was low level	

Notes 1. If WTIM0 (bit 3 of SMB control register 0 (SMBC0) = 1, an interrupt request is generated at the falling edge of the 9th clock. During reception of an extension code slave address when WTIM0 = 0, an interrupt request is generated at the falling edge of the 8th clock.

2. If there is a possibility of arbitration occurring, set SPIE0 to 1 for master operation.

Remark SPIE0: SMB control register 0 (SMBC0) bit 4

15.4.13 Wakeup function

The SMB0 slave function generates an interrupt request (INTSMB0) when a local address and extension code are received. This interrupt enables release of STOP mode and HALT mode.

When the address does not match, no unnecessary interrupt request is generated, allowing greater processing efficiency.

When a start condition is detected, the wakeup standby status is entered. Because even a master (when a start condition is output) may become a slave if defeated in arbitration, the wakeup standby status is entered while address transmission is performed.

However, when a stop condition is detected, interrupt request enable/disable is determined by setting bit 4 (SPIE0) of SMB control register 0 (SMBC0) regardless of the wakeup function.

15.4.14 Communication reservation

If, during non-participation on the bus, the next master communication is desired, a start condition can be made to be sent at bus release by performing communication reservation. Non-participation on the bus includes the following two statuses.

- When unit neither master nor slave during bus arbitration
- When extension code is received and unit does not operate as slave (released bus with SMB control register 0 (SMBC0) bit 6 (LREL0) = 1, without returning $\overline{ACK}$).

When bit 1 (STT0) of SMBC0 is set during non-participation on the bus, a start condition is generated automatically after the bus is released (following detection of stop condition), and the wait status is entered.

When bus release is detected (detection of stop condition), address transmission as master is started through a SMB shift register 0 (SMB0) write operation. At this time, set SMBC0 bit 4 (SPIE0).

When STT0 is set, whether operation as a start condition or operation as communication reservation is selected depends on the bus status.

- If bus is released .... Start condition generation
- If bus is not released (standby status).... Communication reservation

The method to detect which operation is selected by STT0 is to set STT0, and reconfirm the STT0 bit after the wait time elapses.

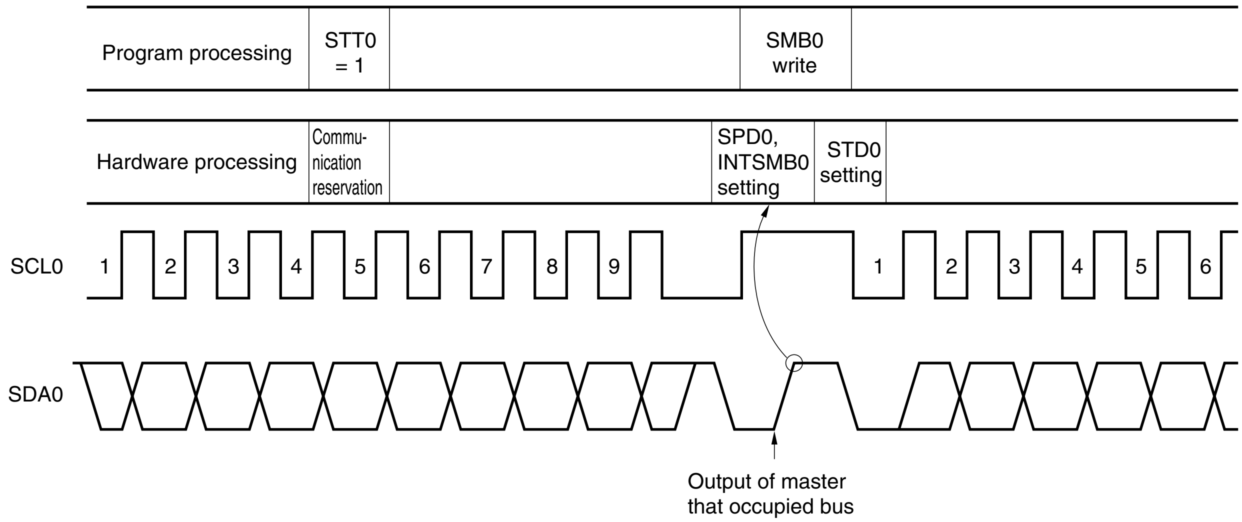
Secure the wait time by software as shown in Table 15-6. The wait time is set by bit 3 (SMC0) of SMB clock selection register 0 (SMBCL0).

Table 15-6. Wait Time

SMC0	Wait Time
0	46 clocks
1	16 clocks

The communication reservation timing is shown in Figure 15-15.

Figure 15-15. Communication Reservation Timing



SMB0: SMB shift register 0
STT0: SMB control register 0 (SMBC0) bit 1
STD0: SMB status register 0 (SMBS0) bit 1
SPD0: SMB status register 0 (SMBS0) bit 0

Communication reservations are received at the following timing. After bit 1 (STD0) of SMB status register 0 (SMBS0) becomes 1, communication reservation is done by setting bit 1 (STT0) of SMB control register 0 (SMBC0) to "1" before detection of a stop condition.

Figure 15-16. Communication Reservation Reception Timing

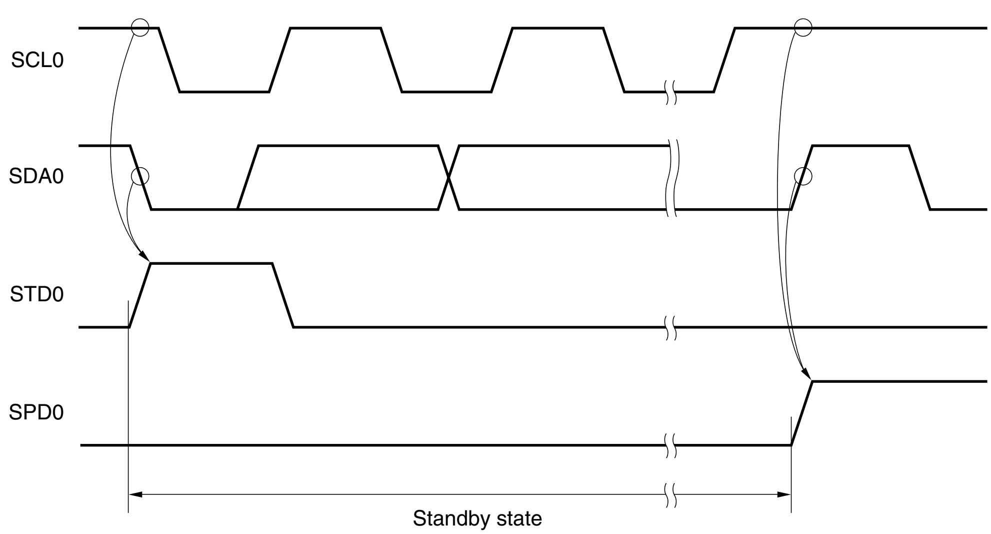
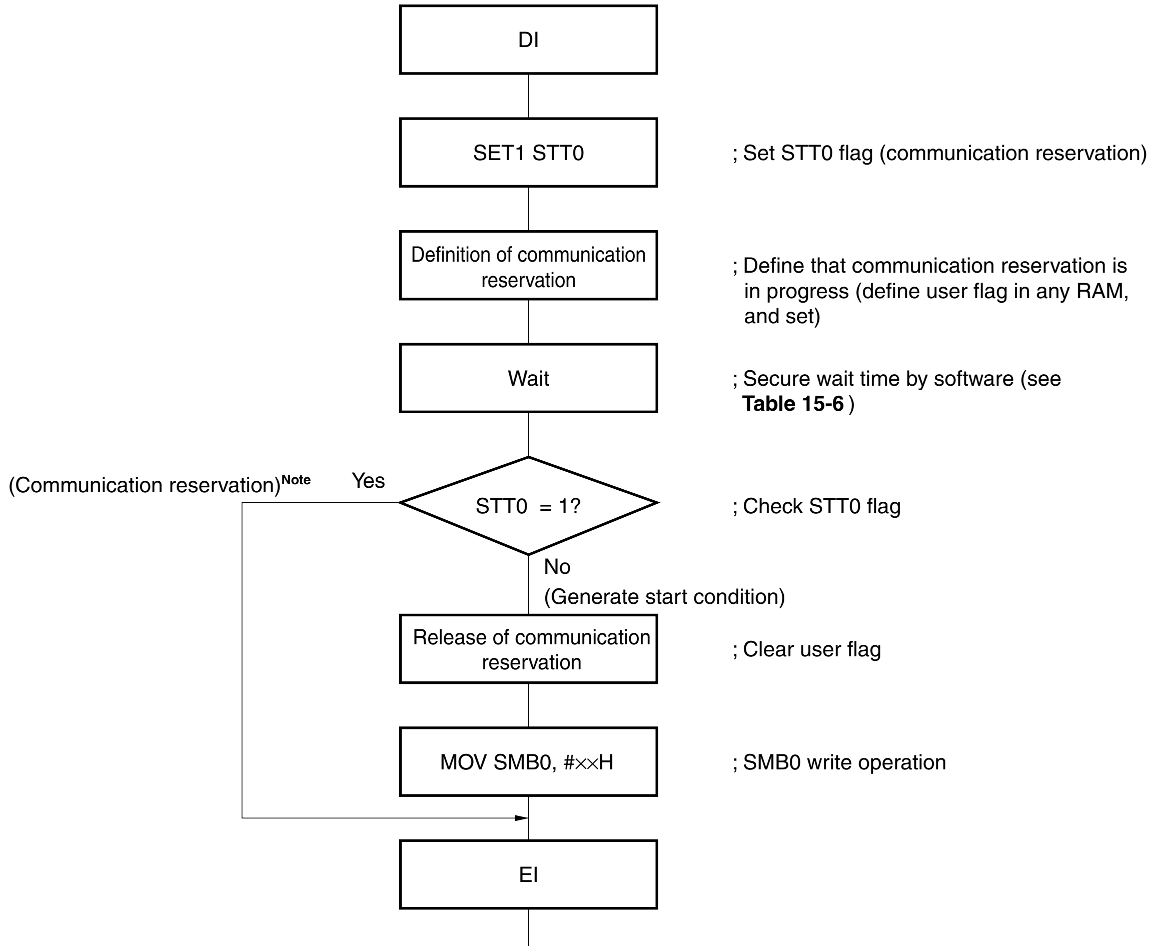


Figure 15-17 shows the communication reservation procedure.

Figure 15-17. Communication Reservation Procedure



Note During the communication reservation operation, execute writing to SMB shift register 0 (SMB0) using a stop condition interrupt.

15.4.15 Additional cautions

If, after reset, master communication is attempted from a status where no stop condition is detected (bus is not released), a stop condition must be generated and the bus released before performing master communication.

In the case of multiple masters, master communication cannot be performed while the bus is not released (stop condition not detected).

A stop condition is generated in the following sequence.

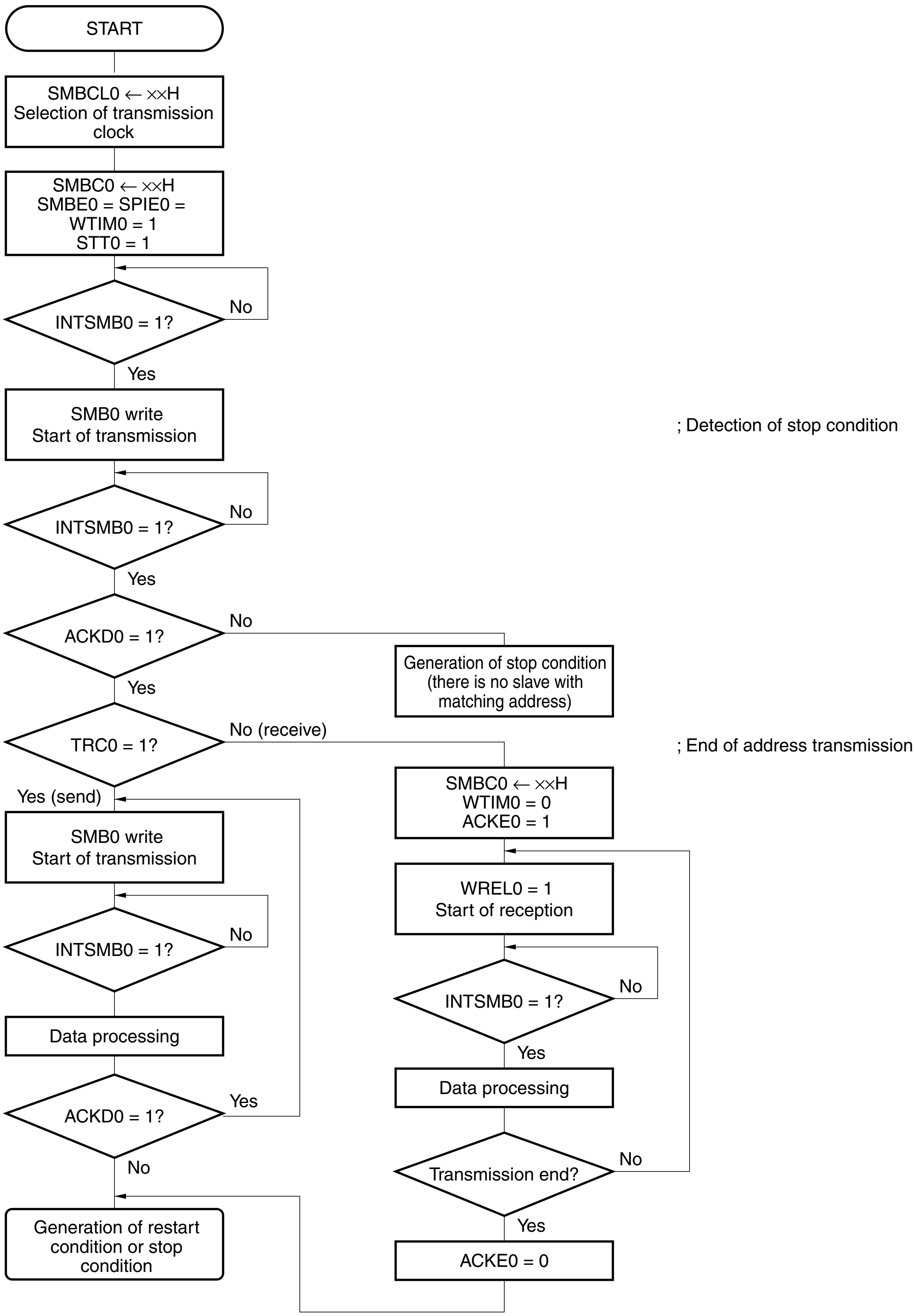
<1> Setting of SMB clock selection register 0 (SMBCL0)
<2> Setting of SMB control register 0 (SMBC0) bit 7 (SMBE0)
<3> Setting of SMBC0 bit 0 (SPT0)

15.4.16 Communication operation

(1) Master operation

The master operation sequence is illustrated below.

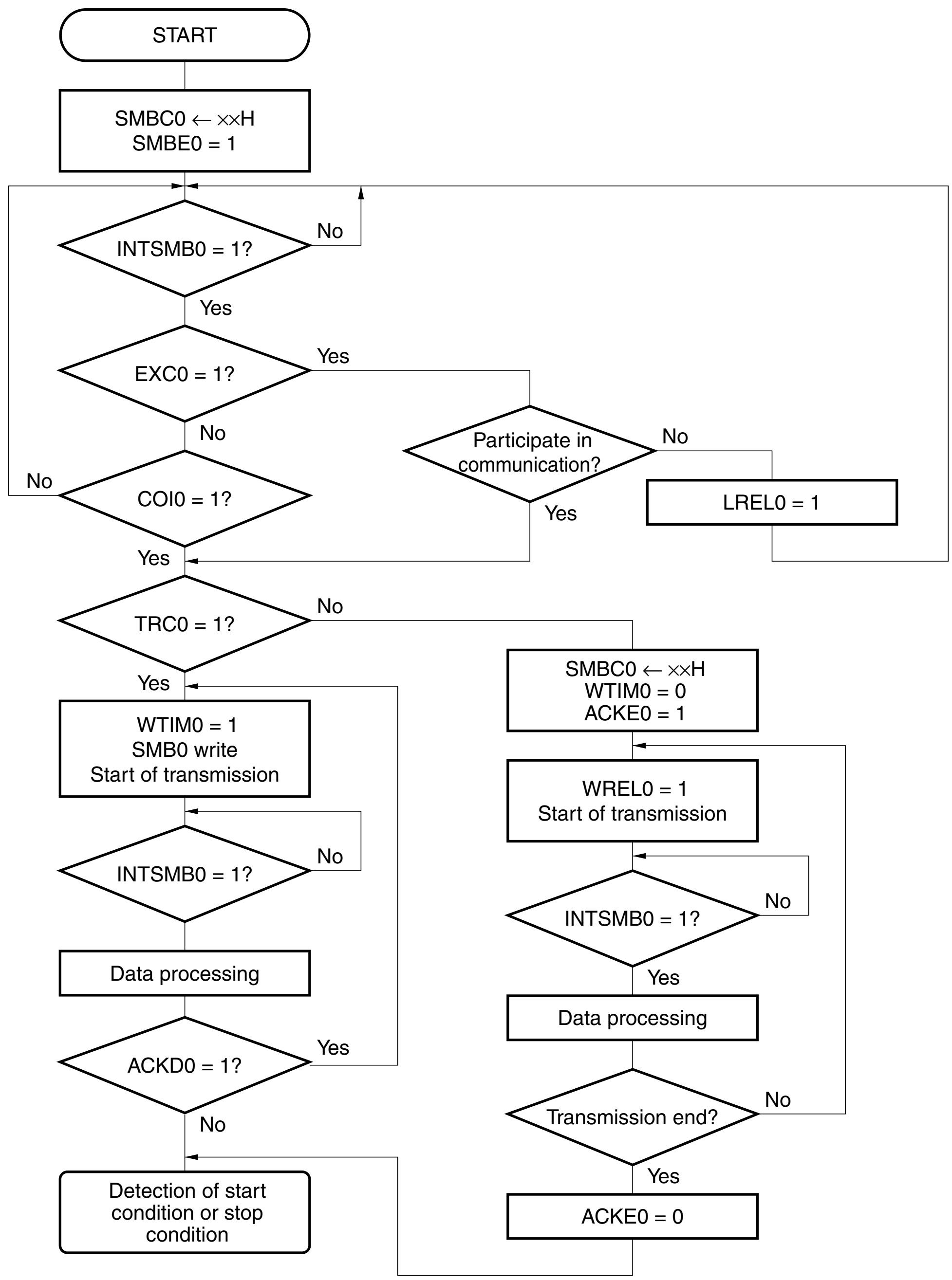
Figure 15-18. Master Operation Sequence



(2) Slave operation

The slave operation sequence is illustrated below.

Figure 15-19. Slave Operation Sequence



15.5 Timing Charts

In SMB mode, a master can select for communication a slave device from among many such devices by outputting an address to the serial bus.

After the slave address, the master sends the TRC0 bit (bit 3 of SMB status register 0 (SMBS0)) indicating the data transmission direction and starts the serial communication with the slave.

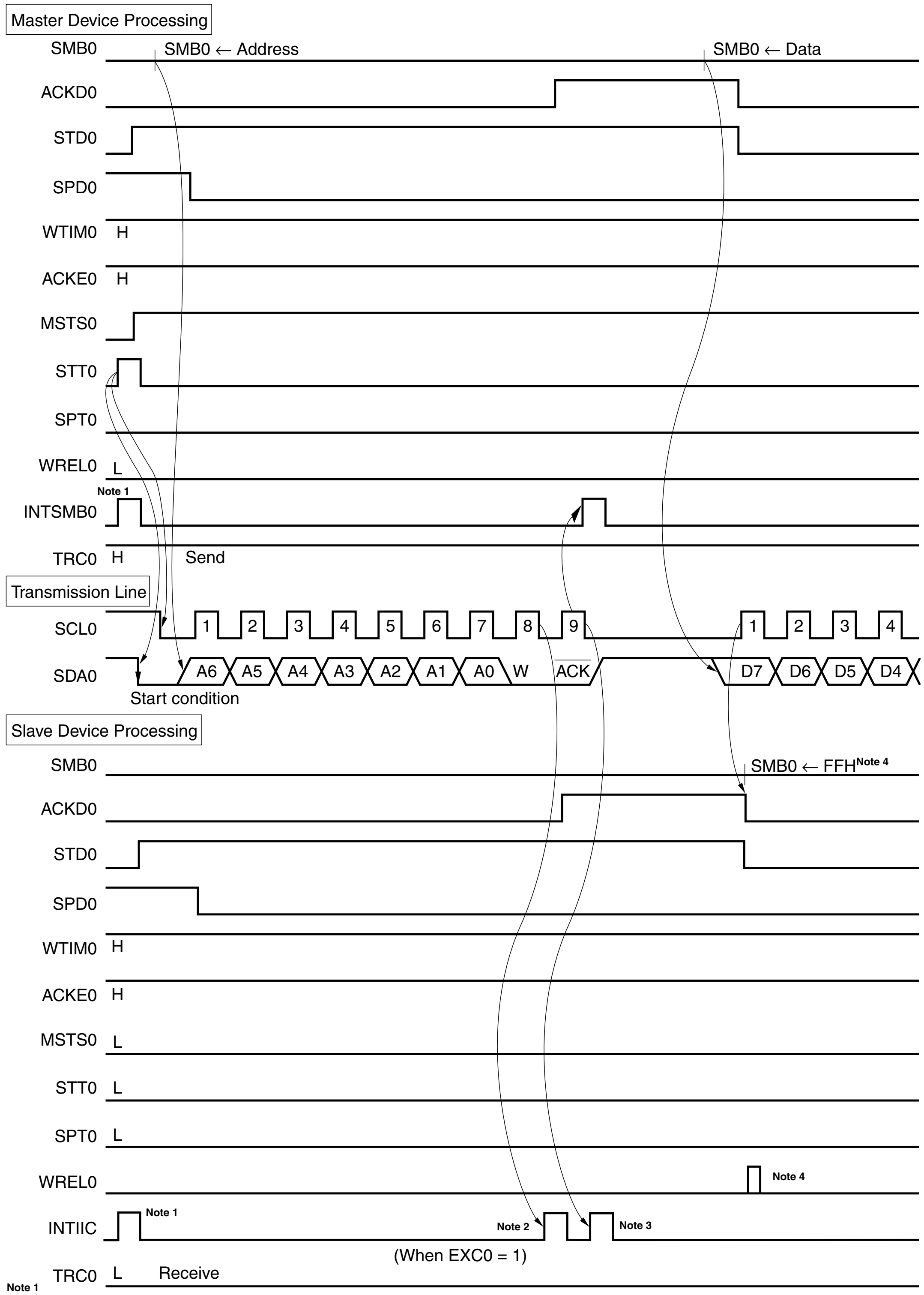
The timing charts for data transmission are shown in Figures 15-20 and 15-21.

The shift operation of SMB shift register 0 (SMB0) is performed in synchronization with the falling edge of the serial clock (SCL0), send data is transmitted to the SO0 latch and output MSB first from the SDA0 pin.

Data input to the SDA0 pin at the rising edge of SCL0 is read by SMB0.

Figure 15-20. Master → Slave Communication Example (When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)

(1) Start condition — Address



Notes 1. An interrupt signal is output only when STIE0 = 1.

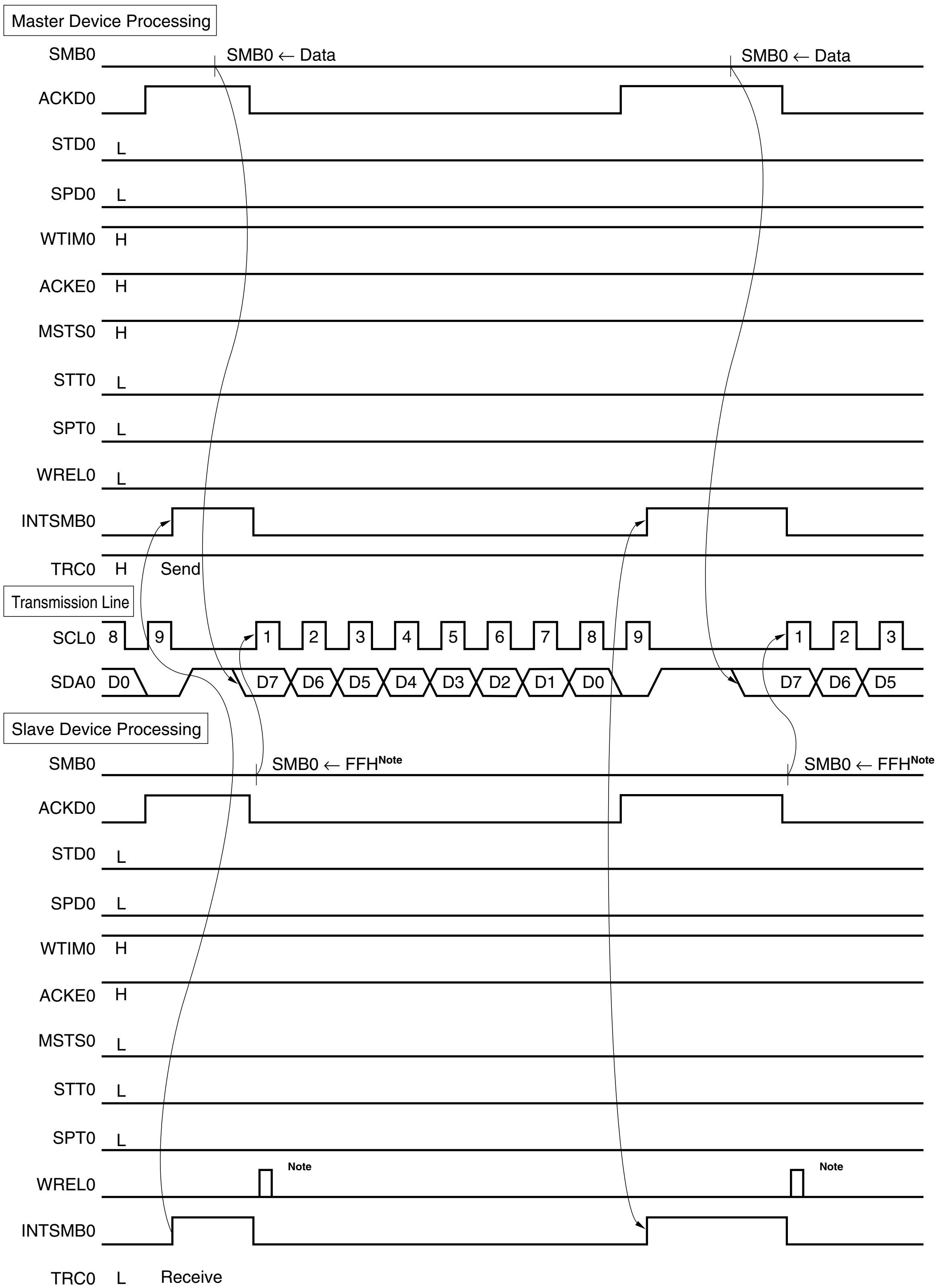
2. An interrupt signal is output only when EXC0 = 1.

3. An interrupt signal is output only when SPIE0 = 1.

4. Perform slave wait cancellation by either changing SMB0 ← FFH, or setting WREL0.

Figure 15-20. Master → Slave Communication Example (When 9-Clock Wait Is Selected for Both Master and Slave) (2/3)

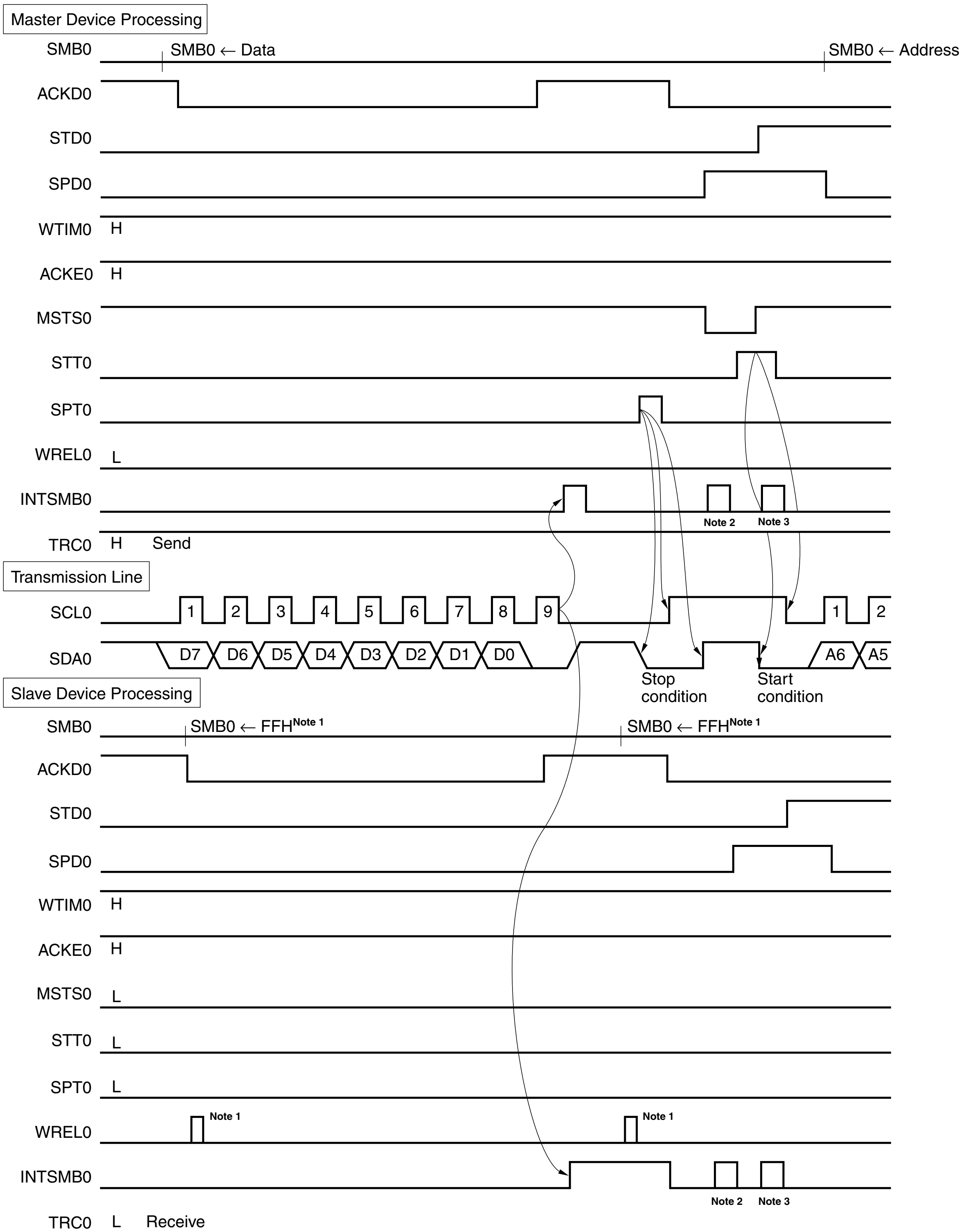
(2) Data



Note Perform slave wait cancellation by either changing SMB0 ← FFH, or setting WREL0.

Figure 15-20. Master → Slave Communication Example (When 9-Clock Wait Is Selected for Both Master and Slave) (3/3)

(3) Stop condition



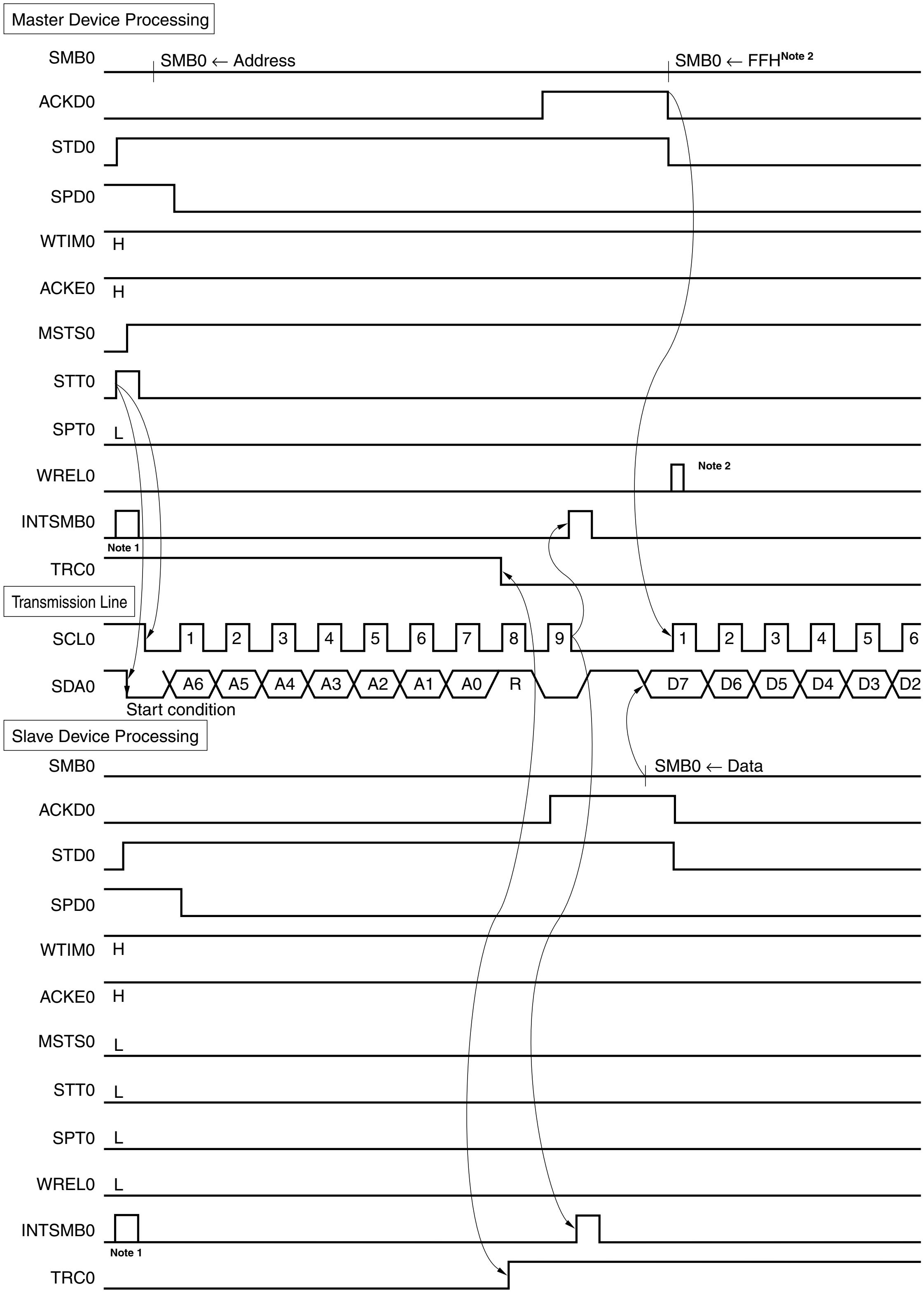
Notes 1. Perform slave wait cancellation by either changing SMB0 ← FFH, or setting WREL0.

2. An interrupt signal is output only when SPIE0 = 1.

3. An interrupt signal is output only when STIE0 = 1.

Figure 15-21. Slave → Master Communication Example (When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)

(1) Start condition — Address

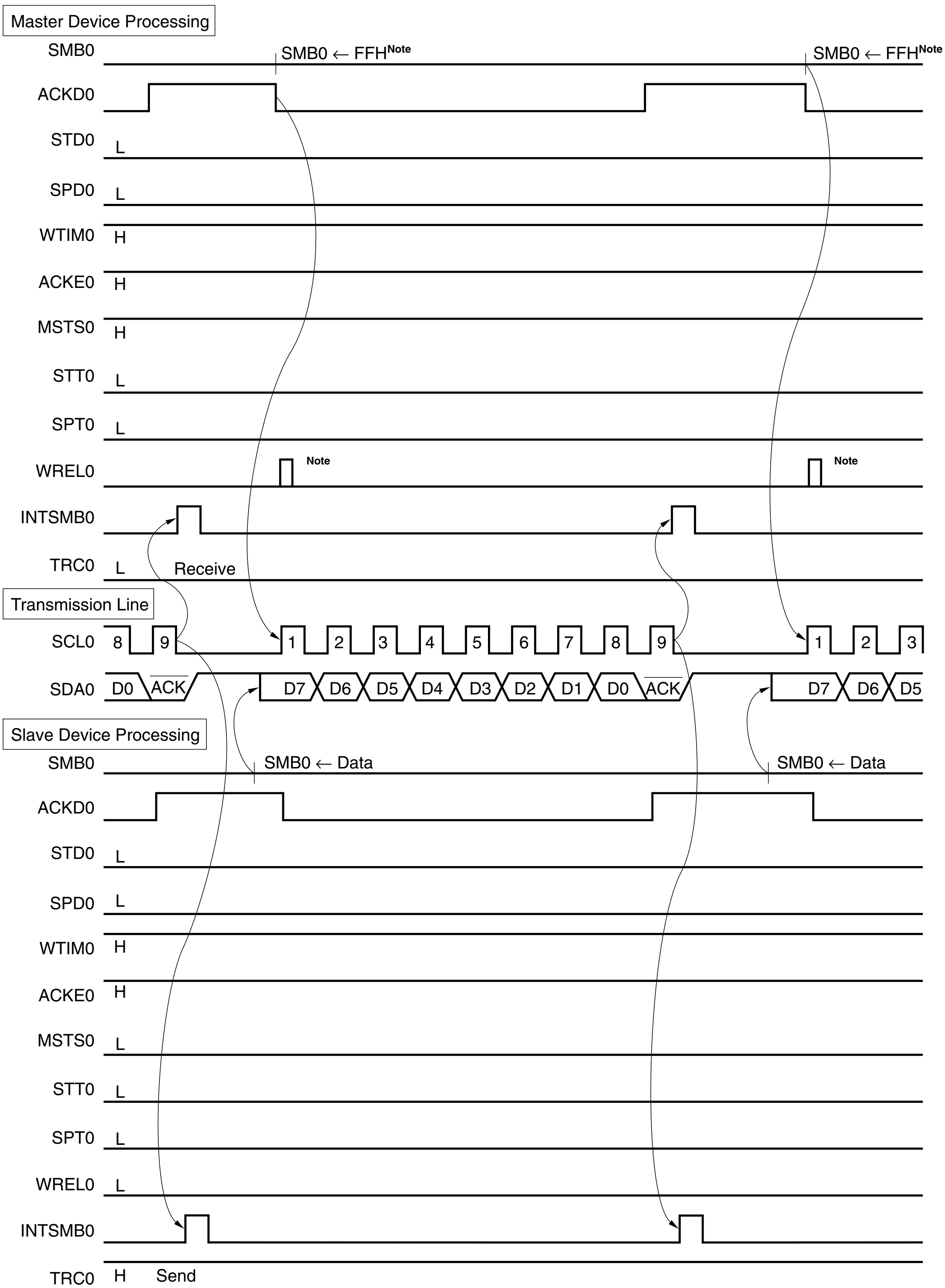


Notes 1. Only when STIE0 = 1.

2. Perform slave wait cancellation by either changing SMB0 ← FFH, or setting WREL0.

Figure 15-21. Slave → Master Communication Example (When 9-Clock Wait Is Selected for Both Master and Slave) (2/3)

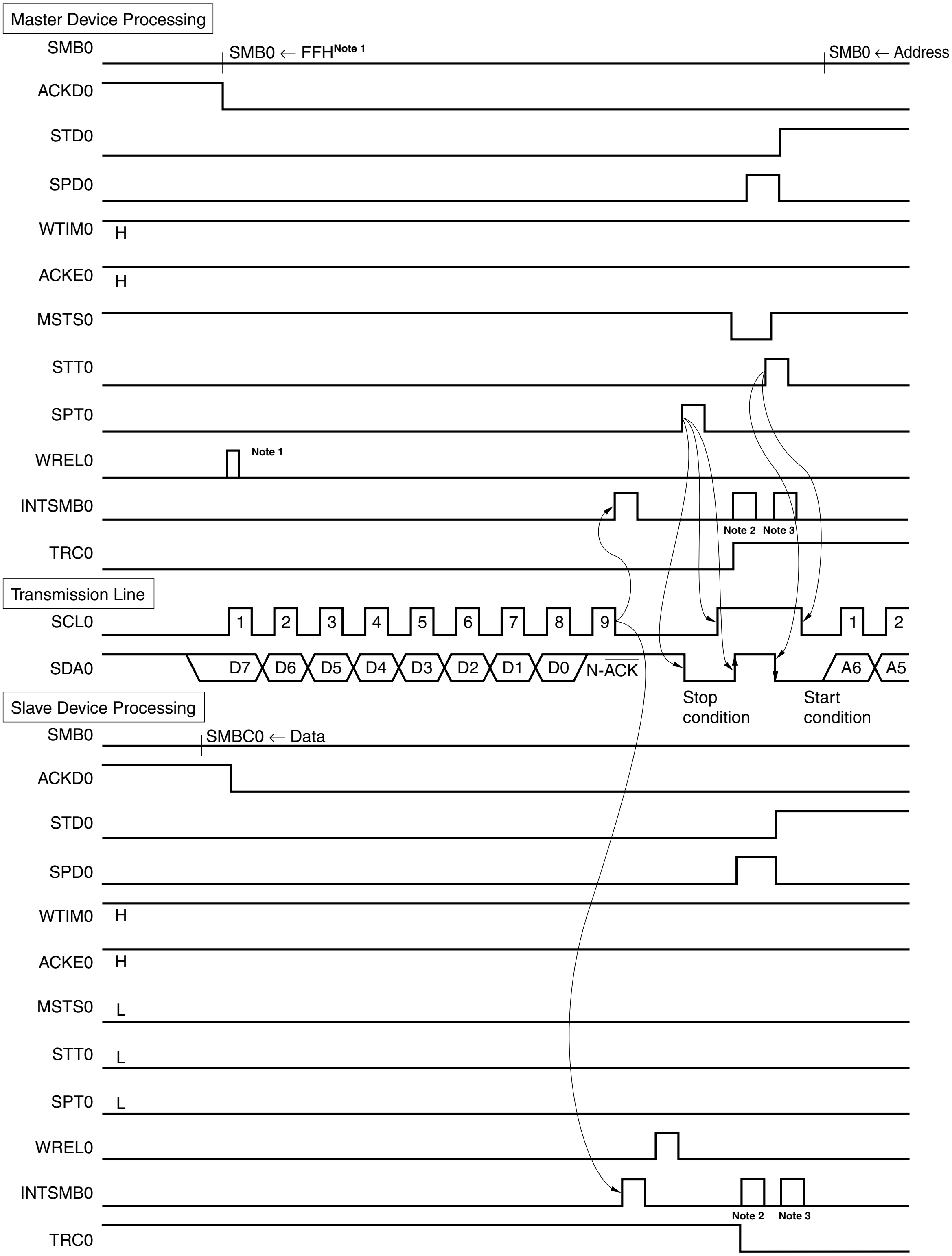
(2) Data



Note Perform slave wait cancellation by either changing SMB0 ← FFH, or setting WREL0.

Figure 15-21. Slave → Master Communication Example (When 9-Clock Wait Is Selected for Both Master and Slave) (3/3)

(3) Stop condition



Notes 1. Perform slave wait cancellation by either changing SMB0 ← FFH, or setting WREL0.

2. An interrupt signal is output only when SPIE0 = 1.

3. An interrupt signal is output only when STIE0 = 1.

CHAPTER 16 MULTIPLIER

16.1 Multiplier Function

The multiplier has the following function.

- Calculation of 8 bits × 8 bits = 16 bits

16.2 Multiplier Configuration

(1) 16-bit multiplication result storage register 0 (MUL0)

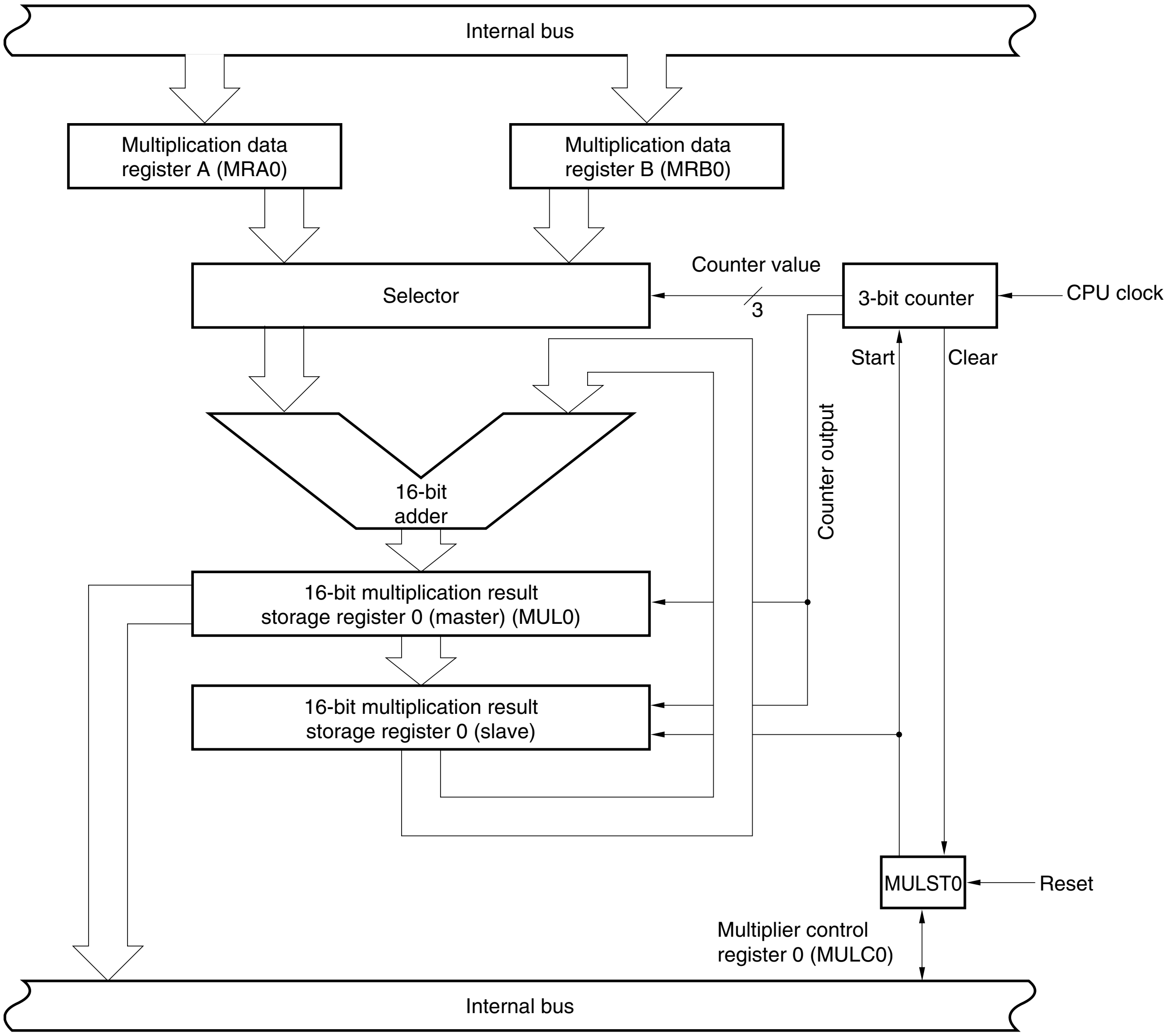
This register stores the 16-bit result of multiplication.
This register holds the result of multiplication after 16 CPU clocks have elapsed.
MUL0 is set with a 16-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input makes this register undefined.

Caution MUL0 is designed to be manipulated with a 16-bit memory manipulation instruction. It can also be manipulated with 8-bit memory manipulation instructions, however. When an 8-bit memory manipulation instruction is used to manipulate MUL0, it must be accessed using direct addressing.

(2) Multiplication data registers A and B (MRA0 and MRB0)

These are 8-bit multiplication data storage registers. The multiplier multiplies the values of MRA0 and MRB0.
MRA0 and MRB0 are set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input makes these registers undefined.
Figure 16-1 shows a block diagram of the multiplier.

Figure 16-1. Block Diagram of Multiplier



16.3 Multiplier Control Register

The multiplier is controlled by the following register.

- Multiplier control register 0 (MULC0)

MULC0 indicates the operating status of the multiplier, as well as controls the multiplier.
MULC0 is set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears this register to 00H.

Figure 16-2. Format of Multiplier Control Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
MULC0	0	0	0	0	0	0	0	MULST0	FFD2H	00H	R/W

MULST0	Multiplier operation start control bit	Operating status of multiplier
0	Stops operation after resetting counter to 0.	Operation stops
1	Enables operation	Operation in progress

Caution Bits 1 to 7 must all be set to 0.

16.4 Multiplier Operation

The multiplier of the μPD789167, 789177, 789167Y, and 789177Y Subseries can execute calculation of 8 bits $\times$ 8 bits = 16 bits.

Figure 16-3 shows the operation timing of the multiplier where MRA0 is set to AAH and MRB0 is set to D3H.

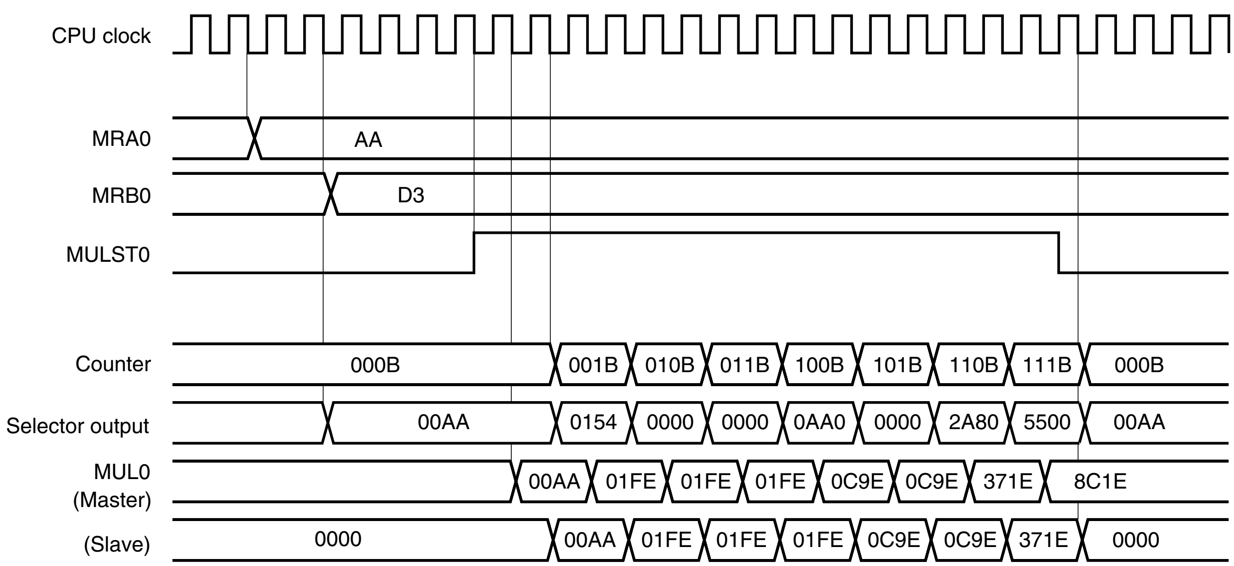
<1> Counting is started by setting MULST0.

<2> The data generated by the selector is added to the data of MUL0 at each CPU clock, and the counter value is incremented by one.

<3> If MULST0 is cleared when the counter value is 111B, the operation is stopped. At this time, MUL0 holds the data.

<4> While MULST0 is low, the counter and slave are cleared.

Figure 16-3. Multiplier Operation Timing (Example of AAH $\times$ D3H)



CHAPTER 17 INTERRUPT FUNCTIONS

17.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Non-maskable interrupt

This interrupt is acknowledged unconditionally. It does not undergo interrupt priority control and is given top priority over all other interrupt requests.

A standby release signal is generated.

The non-maskable interrupt has one interrupt source the watchdog timer.

(2) Maskable interrupt

These interrupts undergo mask control. If two or more interrupts are simultaneously generated, each interrupt has a predetermined priority as shown in Table 17-1.

A standby release signal is generated.

For the μPD789167 and 789177 Subseries, maskable interrupts have four external interrupt sources and ten internal interrupts sources. For the μPD789167Y and 789177Y Subseries, maskable interrupts have four external interrupt sources of and 12 internal interrupt sources.

17.2 Interrupt Sources and Configuration

There are a total of 15 non-maskable and maskable interrupt sources for the μPD789167 and 789177 Subseries, and a total of 17 non-maskable and maskable interrupt sources for the μPD789167Y and 789177Y Subseries (see **Table 17-1**).

Table 17-1. Interrupt Sources

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable interrupt	–	INTWDT	Watchdog timer overflow (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable interrupt	0	INTWDT	Watchdog timer overflow (when interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSR20	End of UART reception on serial interface 20	Internal	000EH	(B)
		INTCSI20	End of three-wire SIO transfer reception on serial interface 20			
	6	INTST20	End of UART transmission on serial interface 20		0010H	
	7	INTWT	Watch timer interrupt		0012H	
	8	INTWTI	Interval timer interrupt		0014H	
	9	INTTM80	Generation of match signal for 8-bit timer/event counter 80		0016H	
	10	INTTM81	Generation of match signal for 8-bit timer/event counter 81		0018H	
	11	INTTM82	Generation of match signal for 8-bit timer 82		001AH	
	12	INTTM90	Generation of match signal for 16-bit timer 90		001CH	
	13	INTSMB0[Note 3]	SMB interrupt		001EH	
	14	INTSMBOV0[Note 3]	SMB timeout interrupt		0020H	
	15	INTAD0	A/D conversion completion signal		0022H	

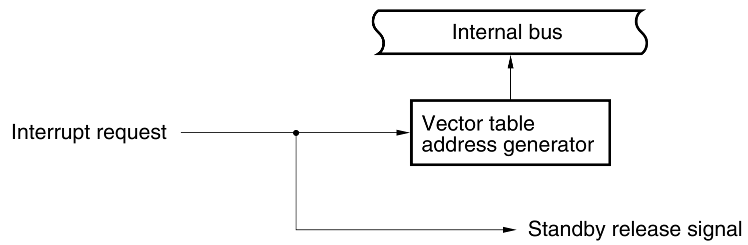
Notes 1. The priority regulates which maskable interrupt is higher when two or more maskable interrupts are generated simultaneously. Zero signifies the highest priority, and 15 is the lowest.

2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in Figure 17-1, respectively.

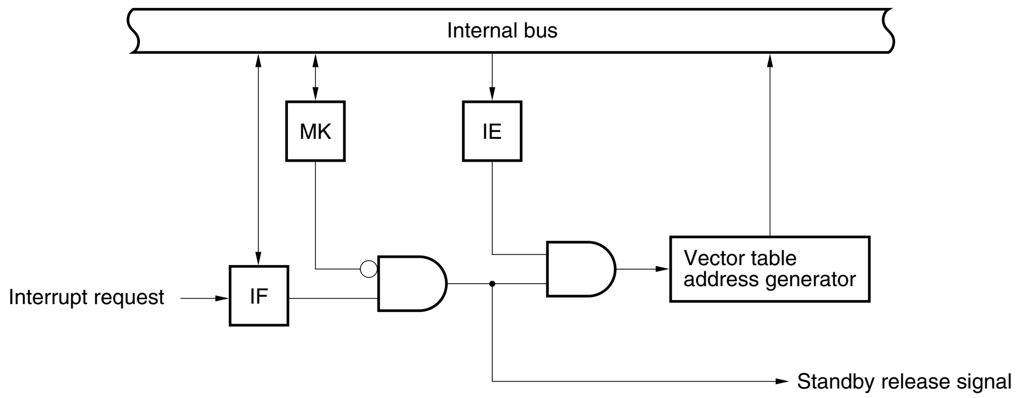
3. For the μPD789167Y and 789177Y Subseries only

Figure 17-1. Basic Configuration of Interrupt Function

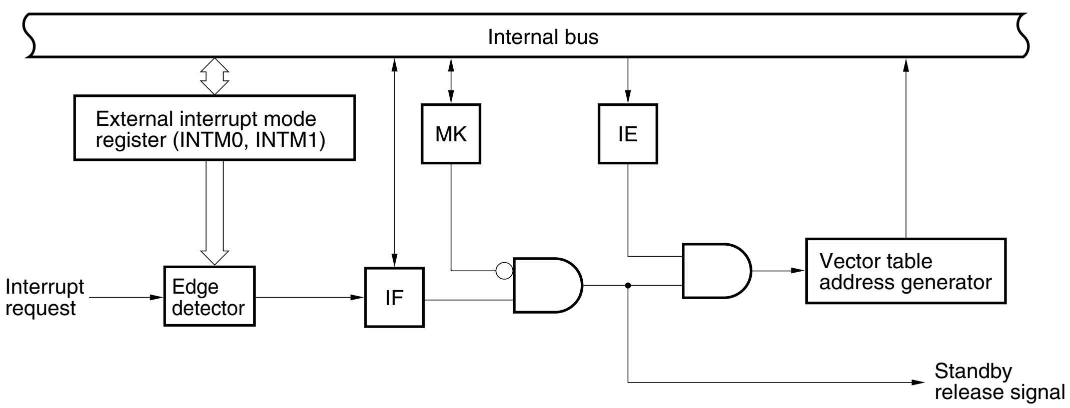
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

17.3 Interrupt Function Control Registers

The interrupt functions are controlled by the following registers.

- Interrupt request flag registers 0 and 1 (IF0 and IF1)
- Interrupt mask flag registers 0 and 1 (MK0 and MK1)
- External interrupt mode registers 0 and 1 (INTM0 and INTM1)
- Program status word (PSW)

Table 17-2 lists interrupt requests, the corresponding interrupt request flags, and interrupt mask flags.

Table 17-2. Interrupt Request Signals and Corresponding Flags

Interrupt Request Signal	Interrupt Request Flag	Interrupt Mask Flag
INTWDT	TMIF4	TMMK4
INTP0	PIF0	PMK0
INTP1	PIF1	PMK1
INTP2	PIF2	PMK2
INTP3	PIF3	PMK3
INTSR20/INTCSI20	SRIF20	SRMK20
INTST20	STIF20	STMK20
INTWT	WTIF	WTMK
INTWTI	WTIIF	WTIMK
INTTM80	TMIF80	TMMK80
INTTM81	TMIF81	TMMK81
INTTM82	TMIF82	TMMK82
INTTM90	TMIF90	TMMK90
INTSMB0[Note]	SMBIF0[Note]	SMBMK0[Note]
INTSMBOV0[Note]	SMBOVIF0[Note]	SMBOVMK0[Note]
INTAD0	ADIF0	ADMK0

Note For the μPD789167Y and 789177Y Subseries only

(1) Interrupt request flag registers (IF0 and IF1)

An interrupt request flag is set to 1 when the corresponding interrupt request is issued, or when the related instruction is executed. It is cleared to 0 when the interrupt request is acknowledged, when a $\overline{\text{RESET}}$ signal is input, or when a related instruction is executed.

IF0 and IF1 are set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears IF0 and IF1 to 00H.

Figure 17-2. Format of Interrupt Request Flag Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
IF0	WTIF	STIF20	SRIF20	PIF3	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W
	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>			
IF1	ADIF0	SMBOVIF0 Note	SMBIF0 Note	TMIF90	TMIF82	TMIF81	TMIF80	WTIIF	FFE1H	00H	R/W

××IF×	Interrupt request flag
0	No interrupt request signal has been issued.
1	An interrupt request signal has been issued; an interrupt request has been made.

Note This flag is provided for the μPD789167Y and 789177Y Subseries only. For the μPD789167 and 789177 Subseries, the flag must be set to 0.

Cautions 1. The TMIF4 flag can be read- and write-accessed only when the watchdog timer is being used as an interval timer. It must be cleared to 0 if the watchdog timer is used in watchdog timer mode 1 or 2.

2. When port 3 is being used as an output port, and its output level is changed, an interrupt request flag is set, because this port is also used as an external interrupt input. To use port 3 in output mode, therefore, the interrupt mask flag must be set to 1 in advance.

3. When an interrupt is acknowledged, the interrupt routine is entered after the interrupt request flag has been automatically cleared.

(2) Interrupt mask flag registers (MK0 and MK1)

The interrupt mask flags are used to enable and disable the corresponding maskable interrupts.

MK0 and MK1 are set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets MK0 and MK1 to FFH.

Figure 17-3. Format of Interrupt Mask Flag Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
MK0	WTMK	STMK20	SRMK20	PMK3	PMK2	PMK1	PMK0	TMMK4	FFE4H	FFH	R/W
	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>			
MK1	ADMK0	SMBOVMK0 Note	SMBMK0 Note	TMMK90	TMMK82	TMMK81	TMMK80	WTIMK	FFE5H	FFH	R/W

××MK×	Interrupt handling control
0	Enable interrupt handling.
1	Disable interrupt handling.

Note This flag is provided for the μPD789167Y and 789177Y Subseries only. For the μPD789167 and 789177 Subseries, the flag must be set to 1.

Cautions 1. When the watchdog timer is being used in watchdog timer mode 1 or 2, any attempt to read TMMK4 flag results in an undefined value being detected.

2. When port 3 is being used as an output port, and its output level is changed, an interrupt request flag is set, because this port is also used as an external interrupt input. To use port 3 in output mode, therefore, the interrupt mask flag must be set to 1 in advance.

(3) External interrupt mode register 0 (INTM0)

INTM0 is used to specify the valid edge for INTP0 to INTP2.

INTM0 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears INTM0 to 00H.

Figure 17-4. Format of External Interrupt Mode Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
INTM0	ES21	ES20	ES11	ES10	ES01	ES00	0	0	FFECH	00H	R/W

ES21	ES20	INTP2 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES11	ES10	INTP1 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES01	ES00	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Cautions 1. Bits 0 and 1 must be set to 0.

2. Before setting INTM0, set the corresponding interrupt mask flag register (××MK×) to 1 to disable interrupts.

To enable interrupts, clear the corresponding interrupt request flag (××IF×) to 0, then clear the corresponding interrupt mask flag register (××MK× to 0).

(4) External interrupt mode register 1 (INTM1)

INTM1 is used to specify the valid edge for INTP3.
INTM1 is set with an 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears INTM1 to 00H.

Figure 17-5. Format of External Interrupt Mode Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
INTM1	0	0	0	0	0	0	ES31	ES30	FFEDH	00H	R/W

ES31	ES30	INTP3 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Cautions 1. Bits 2 to 7 must be set to 0.

2. Before setting INTM1, set PMK3 to 1 to disable interrupts.
To enable interrupts, clear PIF3 to 0, then clear PMK3 to 0.

(5) Program status word (PSW)

The program status word is used to hold the instruction execution result and the current status of the interrupt requests. The IE flag, used to enable and disable maskable interrupts, is mapped to the PSW.
The PSW can be read- and write-accessed in 8-bit units, as well as using bit manipulation instructions and dedicated instructions (EI and DI). When a vector interrupt is acknowledged, the PSW is automatically saved to a stack, and the IE flag is reset to 0.
$\overline{\text{RESET}}$ input sets PSW to 02H.

Figure 17-6. Program Status Word Configuration

Symbol	7	6	5	4	3	2	1	0	After reset
PSW	IE	Z	0	AC	0	0	1	CY	02H

Z, AC, CY: Used in the execution of ordinary instructions

IE	Whether to enable/disable interrupt acknowledgment
0	Disable
1	Enable

17.4 Interrupt Processing Operation

17.4.1 Non-maskable interrupt request acknowledgment operation

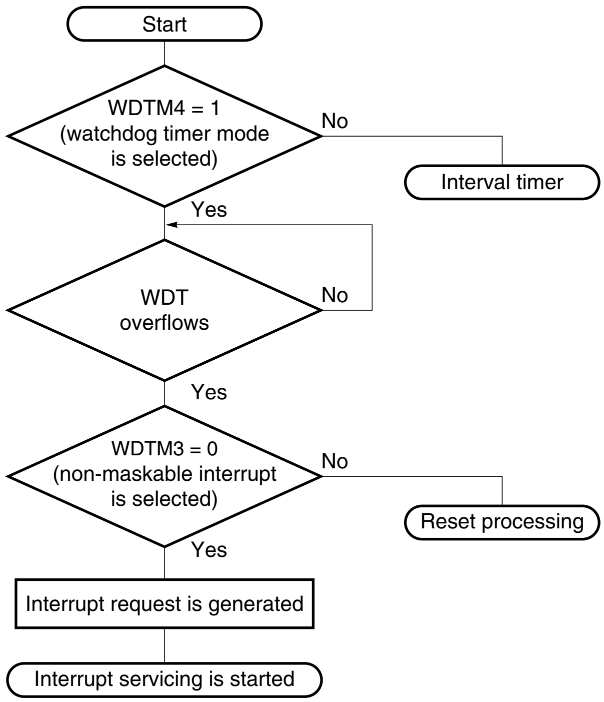
A non-maskable interrupt request is unconditionally acknowledged even when interrupts are disabled. It is not subject to interrupt priority control and takes precedence over all other interrupts.

When a non-maskable interrupt request is acknowledged, the PSW and PC are saved to the stack in that order, the IE flag is reset to 0, the contents of the vector table are loaded to the PC, and then program execution branches.

Figure 17-7 shows the flowchart from non-maskable interrupt request generation to acknowledgment. Figure 17-8 shows the timing of non-maskable interrupt request acknowledgment. Figure 17-9 shows the acknowledgment operation if multiple non-maskable interrupts are generated.

Caution During non-maskable interrupt service program execution, do not input another non-maskable interrupt request; if it is input, the service program will be interrupted and the new interrupt request will be acknowledged.

Figure 17-7. Flowchart from Non-Maskable Interrupt Request Generation to Acknowledgment



WDTM: Watchdog timer mode register

WDT: Watchdog timer

Figure 17-8. Timing of Non-Maskable Interrupt Request Acknowledgment

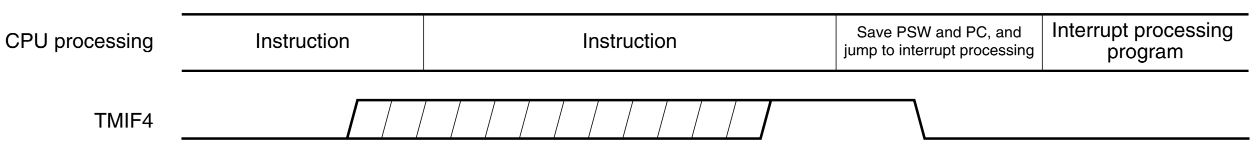
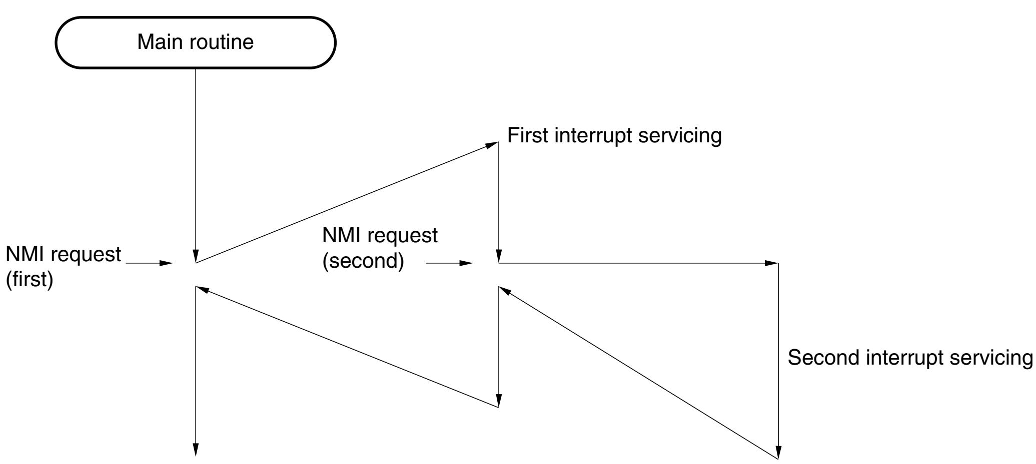


Figure 17-9. Acknowledgment Non-Maskable Interrupt Request



17.4.2 Maskable interrupt request acknowledgment operation

A maskable interrupt request can be acknowledged when the interrupt request flag is set to 1 and the corresponding interrupt mask flag is cleared to 0. A vectored interrupt request is acknowledged in the interrupt enabled status (when the IE flag is set to 1).

The time required to start the interrupt servicing after a maskable interrupt request has been generated is shown in Table 17-3.

See Figures 17-11 and 17-12 for the interrupt request acknowledging timing.

Table 17-3. Time from Generation of Maskable Interrupt Request to Processing

Minimum Time	Maximum Time[Note]
9 clocks	19 clocks

Note The wait time is maximum when an interrupt request is generated immediately before the BT and BF instruction.

Remark 1 clock: $\frac{1}{f_{CPU}}$ (f_{CPU}: CPU clock)

When two or more maskable interrupt requests are generated at the same time, they are acknowledged starting from the interrupt request assigned the highest priority.

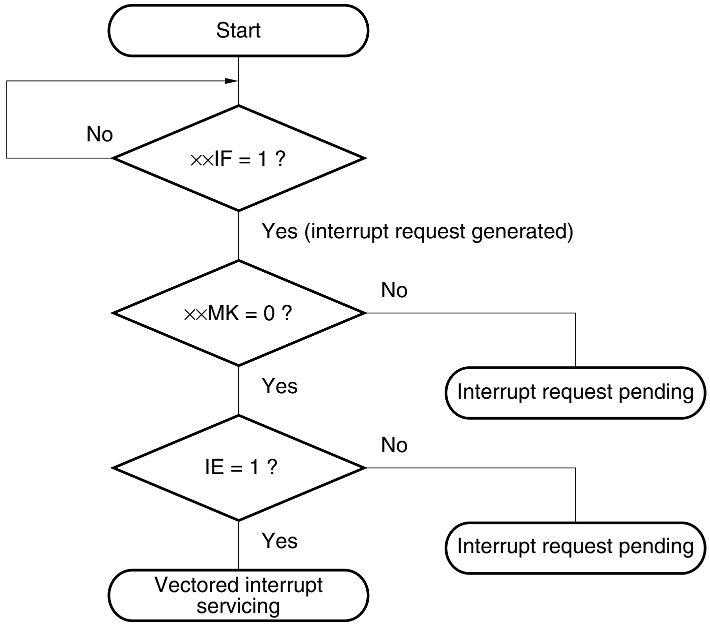
A pending interrupt is acknowledged when the status where it can be acknowledged is set.

Figure 17-10 shows the algorithm of acknowledging interrupt requests.

When a maskable interrupt request is acknowledged, the contents of the PSW and PC are saved to the stack in that order, the IE flag is reset to 0, and the data in the vector table determined for each interrupt request is loaded to the PC, and execution branches.

To return from interrupt processing, use the RETI instruction.

Figure 17-10. Interrupt Request Acknowledgment Processing Algorithm

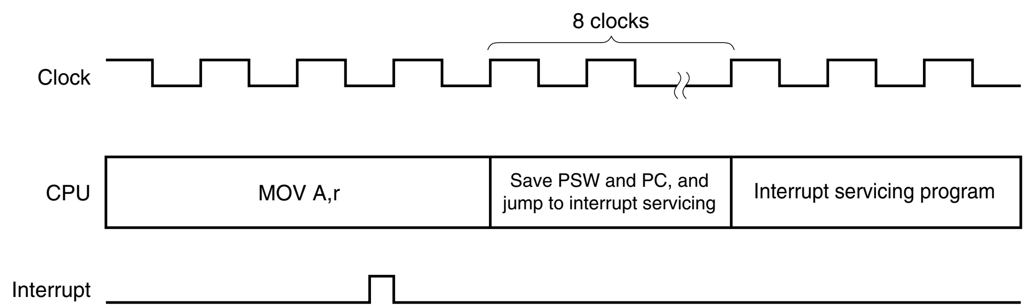


××IF: Interrupt request flag

××MK: Interrupt mask flag

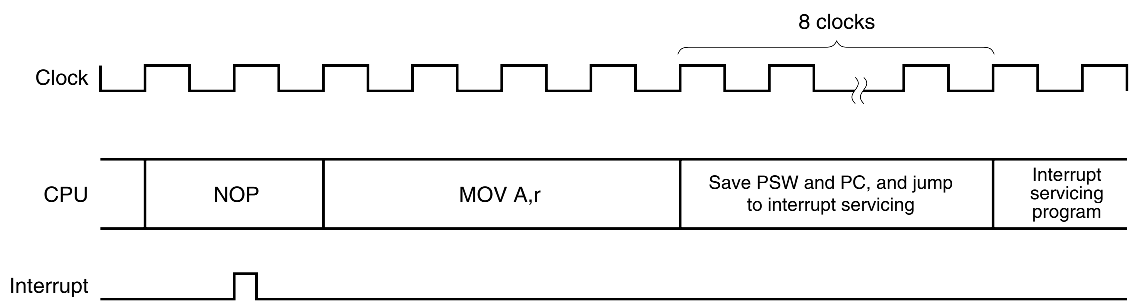
IE: Flag to control maskable interrupt request acknowledgment (1 = Enabled, 0 = Disabled)

Figure 17-11. Interrupt Request Acknowledgment Timing (Example of MOV A,r)



If an interrupt request flag (××IF) is set before instruction clock n (n = 4 to 10) under execution becomes n – 1, the interrupt is acknowledged after the instruction under execution's completed. Figure 17-11 shows an example of the interrupt request acknowledgment timing for an 8-bit data transfer instruction MOV A,r. Since this instruction is executed in 4 clocks, if an interrupt occurs within 3 clocks after the execution starts, the interrupt acknowledgment processing is performed after the MOV A,r instruction is completed.

Figure 17-12. Interrupt Request acknowledgment Timing (When Interrupt Request Flag Is Generated at Last Clock During Instruction Execution)



If an interrupt request flag (××IF) is set at the last clock of the instruction, the interrupt acknowledgment processing starts after the next instruction is executed. Figure 17-12 shows an example of the interrupt acknowledgment timing for an interrupt request flag that is set at the second clock of NOP (2-clock instruction). In this case, the MOV A,r instruction after the NOP instruction is executed, and then the interrupt acknowledgment processing is performed.

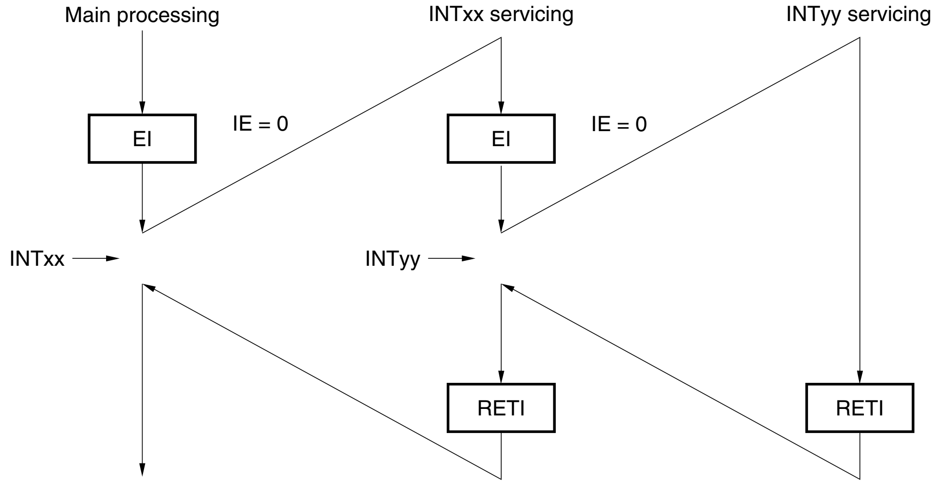
Caution Interrupt requests are reserved while interrupt request flag register 0 or 1 (IF0 or IF1) or the interrupt mask flag register 0 or 1 (MK0 or MK1) is being accessed.

17.4.3 Multiple interrupt processing

Multiple interrupt processing in which another interrupt is acknowledged while an interrupt is being serviced can be processed by priority. When two or more interrupts are generated at once, interrupt servicing is performed according to the priority assigned to each interrupt request in advance (see **Table 17-1**).

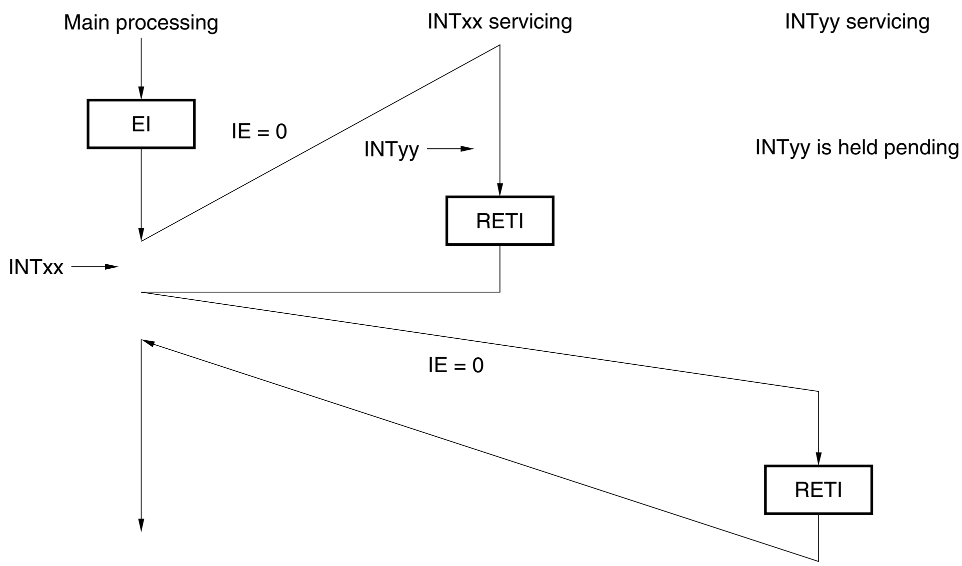
Figure 17-13. Example of Multiple Interrupts

Example 1. Multiple interrupt is acknowledged



During interrupt INTxx servicing, interrupt request INTyy is acknowledged, and multiple interrupts are generated. An EI instruction is issued before each interrupt request acknowledgment, and the interrupt request acknowledgment enabled state is set.

Example 2. Multiple interrupts are not generated because interrupts are not enabled



Because interrupts are not enabled in interrupt INTxx servicing (the EI instruction was not issued), interrupt request INTyy is not acknowledged, and multiple interrupts are not generated. The INTyy request is held pending and acknowledged after INTxx servicing is performed.

IE = 0: Interrupt request acknowledgment disabled

17.4.4 Interrupt request hold

Some instructions may hold the acknowledgment of an instruction request pending until the completion of the execution of the next instruction even if the interrupt request (maskable interrupt, non-maskable interrupt, and external interrupt) is generated during the execution. The following shows such instructions (interrupt request hold instructions).

- Manipulation instruction for interrupt request flag registers 0 and 1 (IF0 and IF1)
- Manipulation instruction for interrupt mask flag registers 0 and 1 (MK0 and MK1)

CHAPTER 18 STANDBY FUNCTION

18.1 Standby Function and Configuration

18.1.1 Standby function

The standby function is to used reduce the power consumption of the system and can be effected in the following two modes.

(1) HALT mode

This mode is set when the HALT instruction is executed. HALT mode stops the operation clock of the CPU. The system clock oscillator continues oscillating. This mode does not reduce the current consumption as much as the STOP mode, but is useful for resuming processing immediately when an interrupt request is generated, or for intermittent operations.

(2) STOP mode

This mode is set when the STOP instruction is executed. STOP mode stops the main system clock oscillator and stops the entire system. The current consumption of the CPU can be substantially reduced in this mode.

The low voltage (V_{DD} = 1.8 V min.) of the data memory can be retained. Therefore, this mode is useful for retaining the contents of the data memory at an extremely low current consumption.

STOP mode can be released by an interrupt request, so this mode can be used for intermittent operations. However, some time is required until the system clock oscillator stabilizes after STOP mode has been released. If processing must be resumed immediately by using an interrupt request, therefore, use the HALT mode.

In both modes, the previous contents of the registers, flags, and data memory before setting standby mode are all retained. In addition, the statuses of the output latches of the I/O ports and output buffers are also retained.

Caution To set STOP mode, be sure to stop the operations of the peripheral hardware, and then execute the STOP instruction.

18.1.2 Standby function control register

The wait time after STOP mode is released upon interrupt request until the oscillation stabilizes is controlled with the oscillation stabilization time selection register (OSTS).

OSTS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets OSTS to 04H. However, the oscillation stabilization time after $\overline{\text{RESET}}$ input is $2^{15}/f_X$, instead of $2^{17}/f_X$.

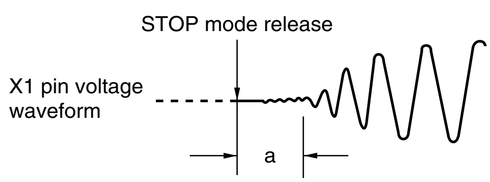
Figure 18-1. Format of Oscillation Stabilization Time Selection Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				At f_X = 10.0 MHz operation[Note]	At f_X = 5.0 MHz operation
0	0	0	$2^{12}/f_X$	409 μs	819 μs
0	1	0	$2^{15}/f_X$	3.27 ms	6.55 ms
1	0	0	$2^{17}/f_X$	13.1 ms	26.2 ms
Other than above			Setting prohibited		

Note Expanded-specification products only.

Caution The wait time after STOP mode is released does not include the time from STOP mode release to clock oscillation start (“a” in the figure below), regardless of release by $\overline{\text{RESET}}$ input or by interrupt generation.



Remark f_X: Main system clock oscillation frequency

18.2 Operation of Standby Function

18.2.1 HALT mode

(1) HALT mode

HALT mode is set by executing the HALT instruction.

The operation status in HALT mode is shown in the following table.

Table 18-1. Operation Statuses in HALT Mode

Item	HALT Mode Operation Status While Main System Clock Is Operating		HALT Mode Operation Status While Subsystem Clock Is Operating	
	While Subsystem Clock Is Operating	While Subsystem Clock Is Not Operating	While Main System Clock Is Operating	While Main System Clock Is Not Operating
Main system clock generator	Main system clock oscillation enabled			Does not operate
CPU	Operation disabled			
Port (output latch)	Remains in the state existing before the selection of HALT mode			
16-bit timer (TM90)	Operation enabled	Operation enabled[Note 1]	Operation enabled	Operation enabled[Note 2]
8-bit timer/event counter (TM80)	Operation enabled			Operation enabled[Note 3]
8-bit timer/event counter (TM81)	Operation enabled			Operation enabled[Note 4]
8-bit timer (TM82)	Operation enabled	Operation enabled[Note 1]	Operation enabled	Operation enabled[Note 5]
Watch timer	Operation enabled	Operation enabled[Note 1]	Operation enabled	Operation enabled[Note 5]
Watchdog timer	Operation enabled		Operation disabled	
Serial interface 20	Operation enabled			Operation enabled[Note 6]
SMB0	Operation enabled			Operation enabled[Note 7]
A/D converter	Operation disabled			
Multiplier	Operation disabled			
External interrupt	Operation enabled[Note 8]			

Notes 1. Operation is enabled when the main system clock is selected.

2. Operation is enabled when the subsystem clock is selected and when buzzer output is enabled (for details, see **8.5 Notes on 16-Bit Timer 90**).

3. Operation is enabled only when TI80 is selected as the count clock.

4. Operation is enabled only when TI81 is selected as the count clock.

5. Operation is enabled when the subsystem clock is selected.

6. Operation is enabled in both 3-wire serial I/O and UART modes while an external clock is being used.

7. An interrupt can be generated when addresses match during the slave operation.

8. Maskable interrupt that is not masked

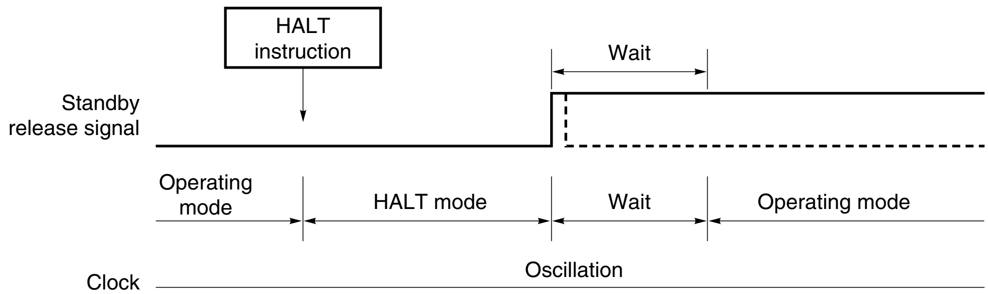
(2) Releasing HALT mode

HALT mode can be released by the following three sources.

(a) Releasing by unmasked interrupt request

HALT mode is released by an unmasked interrupt request. In this case, if the interrupt request is enabled to be acknowledged, vectored interrupt servicing is performed. If interrupts are disabled, the instruction at the next address is executed.

Figure 18-2. Releasing HALT Mode by Interrupt



Remarks 1. The broken lines indicate the case where the interrupt request that has released standby mode is acknowledged.

2. The wait time is as follows:

- When vectored interrupt servicing is performed: 9 to 10 clocks
- When vectored interrupt servicing is not performed: 1 to 2 clocks

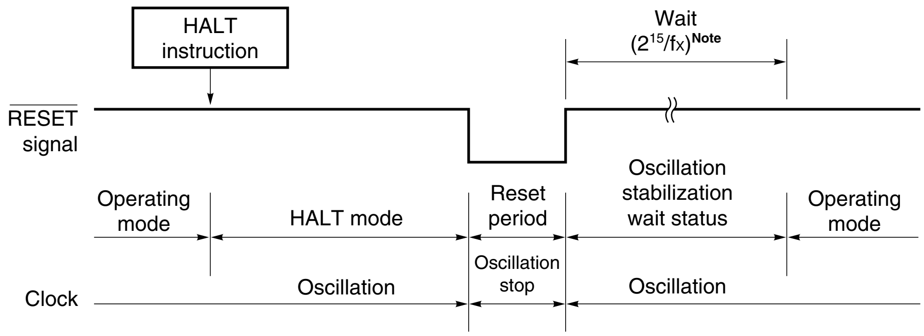
(b) Releasing by non-maskable interrupt request

HALT mode is released regardless of whether interrupts are enabled or disabled, and vectored interrupt servicing is performed.

(c) Releasing by $\overline{\text{RESET}}$ input

When HALT mode is released by the $\overline{\text{RESET}}$ signal, execution branches to the reset vector address in the same manner as the ordinary reset operation, and program execution is started.

Figure 18-3. Releasing HALT Mode by $\overline{\text{RESET}}$ Input



Note 3.27 ms (at fx = 10.0 MHz operation), 6.55 ms (at fx = 5.0 MHz operation)

Table 18-2. Operation after Release of HALT Mode

Releasing Source	MK××	IE	Operation
Maskable interrupt request	0	0	Executes next address instruction
	0	1	Executes interrupt servicing
	1	×	Retains HALT mode
Non-maskable interrupt request	–	×	Executes interrupt servicing
$\overline{\text{RESET}}$ input	–	–	Reset processing

×: Don't care

18.2.2 STOP mode

(1) Setting and operation status of STOP mode

STOP mode is set by executing the STOP instruction.

Caution Because standby mode can be released by an interrupt request signal, standby mode is released as soon as it is set if there is an interrupt source whose interrupt request flag is set and interrupt mask flag is reset. When STOP mode is set, therefore, HALT mode is set immediately after the STOP instruction has been executed, the wait time set by the oscillation stabilization time selection register (OSTS) elapses, and then operation mode is set.

The operation status in STOP mode is shown in the following table.

Table 18-3. Operation Statuses in STOP Mode

Item	STOP Mode Operation Status While Main System Clock Is Operating	
	While Subsystem Clock Is Operating	While Subsystem Clock Is Not Operating
Main system clock generator	Main system clock oscillation stopped	
CPU	Operation disabled	
Port (output latch)	Remains in the state existing before the selection of STOP mode	
16-bit timer (TM90)	Operation enabled[Note 1]	Operation disabled
8-bit timer/event counter (TM80)	Operation enabled[Note 2]	
8-bit timer/event counter (TM81)	Operation enabled[Note 3]	
8-bit timer (TM82)	Operation enabled[Note 4]	Operation disabled
Watch timer	Operation enabled[Note 4]	Operation disabled
Watchdog timer	Operation disabled	
Serial interface 20	Operation enabled[Note 5]	
SMB0	Operation enabled[Note 6]	
A/D converter	Operation disabled	
Multiplier	Operation disabled	
External interrupt	Operation enabled[Note 7]	

Notes 1. Operation is enabled when the subsystem clock is selected and when buzzer output is enabled.

2. Operation is enabled only when TI80 is selected as the count clock.

3. Operation is enabled only when TI81 is selected as the count clock.

4. Operation is enabled when the subsystem clock is selected.

5. Operation is enabled in both 3-wire serial I/O and UART modes while an external clock is being used.

6. An interrupt can be generated when addresses match during the slave operation.

7. Maskable interrupt that is not masked

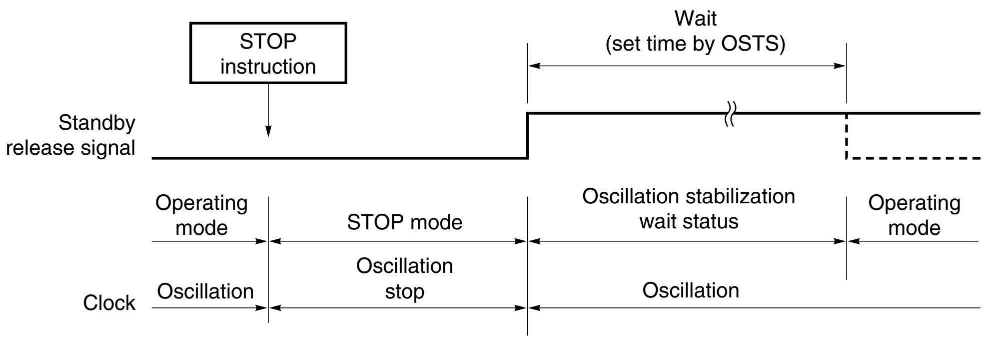
(2) Releasing STOP mode

STOP mode can be released by the following two sources.

(a) Releasing by unmasked interrupt request

STOP mode can be released by an unmasked interrupt request. In this case, if the interrupt is enabled to be acknowledged, vectored interrupt servicing is performed, after the oscillation stabilization time has elapsed. If the interrupt acknowledgment is disabled, the instruction at the next address is executed.

Figure 18-4. Releasing STOP Mode by Interrupt

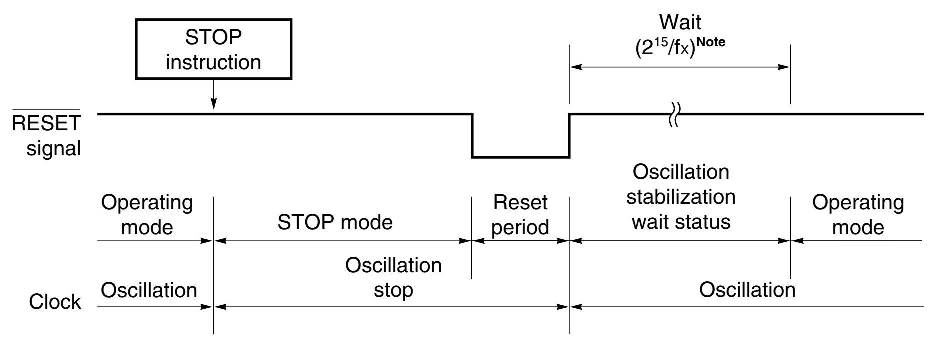


Remark The broken lines indicate the case where the interrupt request that has released standby mode is acknowledged.

(b) Releasing by $\overline{\text{RESET}}$ input

When STOP mode is released by the $\overline{\text{RESET}}$ signal, the reset operation is performed after the oscillation stabilization time has elapsed.

Figure 18-5. Releasing STOP Mode by $\overline{\text{RESET}}$ Input



Note 3.27 ms (at fx = 10.0 MHz operation), 6.55 ms (at fx = 5.0 MHz operation)

Table 18-4. Operation After Release of STOP Mode

Releasing Source	MK××	IE	Operation
Maskable interrupt request	0	0	Executes next address instruction
	0	1	Executes interrupt servicing
	1	×	Retains STOP mode
$\overline{\text{RESET}}$ input	–	–	Reset processing

×: Don't care

CHAPTER 19 RESET FUNCTION

The following two operations are available to generate reset signals.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by program loop time detected by watchdog timer

External and internal reset have no functional differences. In both cases, program execution starts at the address at 0000H and 0001H by reset signal input.

When a low level is input to the $\overline{\text{RESET}}$ pin or the watchdog timer overflows, a reset is applied and each hardware is set to the status shown in Table 19-1. Each pin is high impedance during reset input or during oscillation stabilization time just after reset release.

When a high level is input to the $\overline{\text{RESET}}$ pin, the reset is released and program execution is started after the oscillation stabilization time has elapsed. The reset applied by the watchdog timer overflow is automatically released after reset, and program execution is started after the oscillation stabilization time has elapsed (see **Figures 19-2** through **19-4**).

Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.
2. When STOP mode is released by reset, the STOP mode contents are held during reset input. However, the port pins become high impedance.

Figure 19-1. Block Diagram of Reset Function

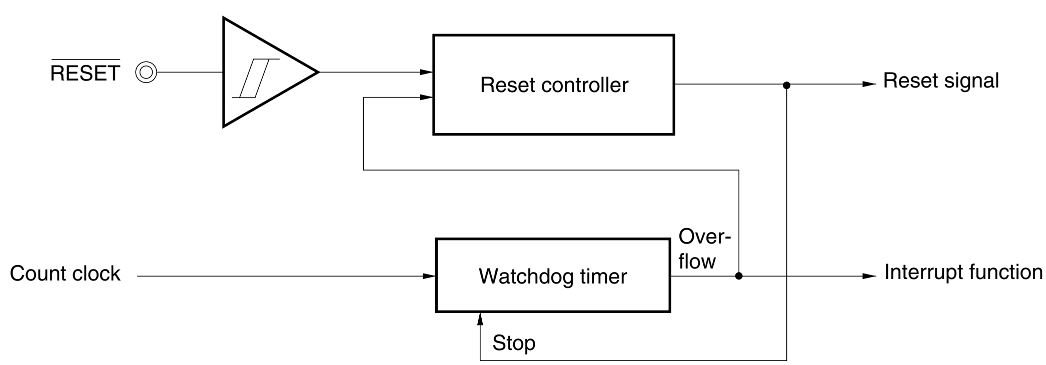


Figure 19-2. Reset Timing by $\overline{\text{RESET}}$ Input

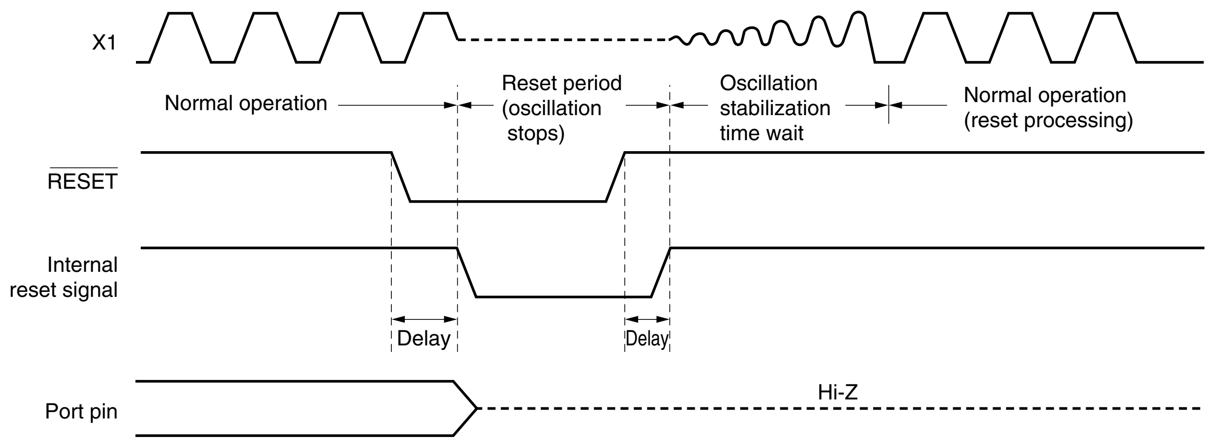


Figure 19-3. Reset Timing by Overflow in Watchdog Timer

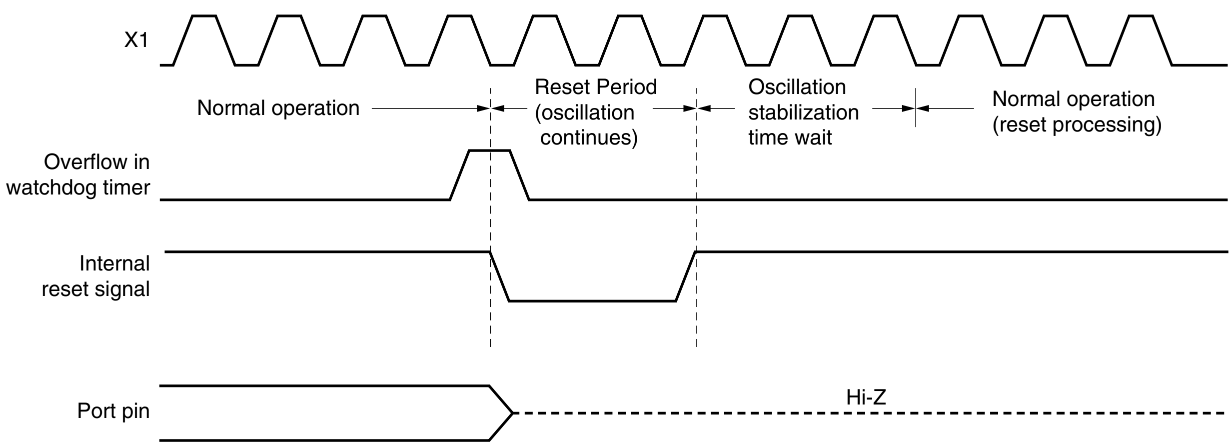


Figure 19-4. Reset Timing by $\overline{\text{RESET}}$ Input in STOP Mode

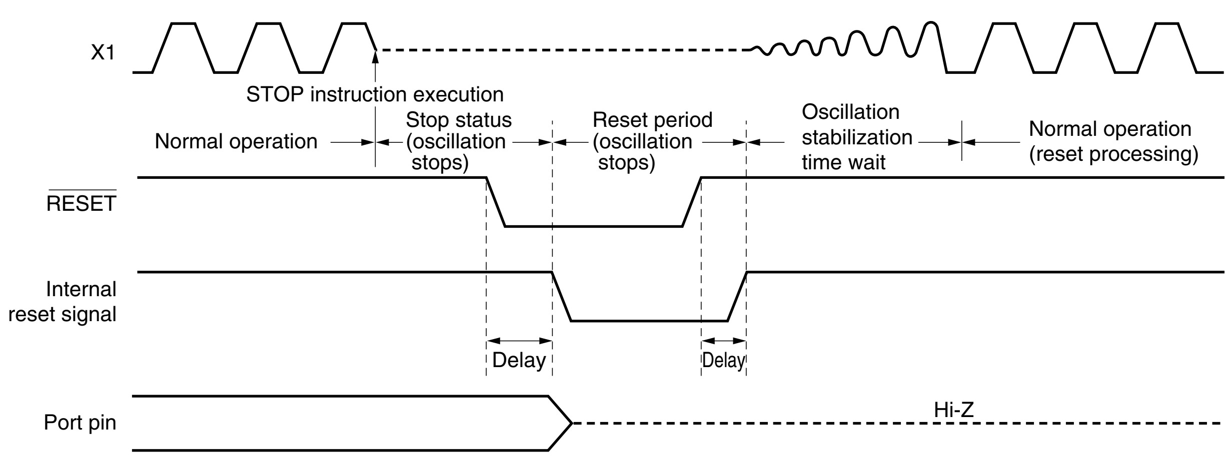


Table 19-1. State of Hardware After Reset (1/2)

Hardware		State After Reset
Program counter (PC)[Note 1]		Loaded with the contents of the reset vector table (0000H, 0001H)
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined[Note 2]
	General-purpose register	Undefined[Note 2]
Ports (P0 to P3, P5, P6) (output latch)		00H
Port mode registers (PM0 to PM3, PM5)		FFH
Pull-up resistor option registers (PU0, PUB2, PUB3)		00H
Processor clock control register (PCC)		02H
Suboscillation mode register (SCKM)		00H
Subclock control register (CSS)		00H
Oscillation stabilization time selection register (OSTS)		04H
16-bit timer 90	Timer counter (TM90)	0000H
	Compare register (CR90)	FFFFH
	Capture register (TCP90)	Undefined
	Mode control register (TMC90)	00H
	Buzzer output control register (BZC90)	00H
8-bit timer/event counters 80 to 82	Timer counters (TM80 to TM82)	00H
	Compare registers (CR80 to CR82)	Undefined
	Mode control registers (TMC80 to TMC82)	00H
Watch timer	Mode control register (WTM)	00H
Watchdog timer	Timer clock selection register (TCL2)	00H
	Mode register (WDTM)	00H
A/D converter	Mode register (ADM0)	00H
	A/D input selection register (ADS0)	00H
	A/D conversion result register (ADCR0)	Undefined
Serial interface 20	Mode register (CSIM20)	00H
	Asynchronous serial interface mode register (ASIM20)	00H
	Asynchronous serial interface status register (ASIS20)	00H
	Baud rate generator control register (BRGC20)	00H
	Transmission shift register (TXS20)	FFH
	Reception buffer register (RXB20)	Undefined

Notes 1. While a reset signal is being input, and during the oscillation stabilization period, the contents of the PC will be undefined, while the remainder of the hardware will be the same as after the reset.

2. In standby mode, the RAM enters the hold state after a reset.

Table 19-1. State of Hardware After Reset (2/2)

Hardware		State After Reset
SMB0	Control register (SMBC0)	00H
	Status register (SMBS0)	00H
	Clock selection register (SMBCL0)	00H
	Slave address register (SMBSVA0)	00H
	Mode register (SMBM0)	20H
	Input level setting register (SMBVI0)	00H
	Shift register (SMB0)	00H
Multiplier	16-bit multiplication result storage register (MUL0)	Undefined
	Multiplication data registers (MRA0, MRB0)	Undefined
	Multiplier control register (MULC0)	00H
Interrupts	Request flag registers (IF0, IF1)	00H
	Mask flag registers (MK0, MK1)	FFH
	External interrupt mode registers (INTM0, INTM1)	00H

CHAPTER 20 FLASH MEMORY VERSION

The μPD78F9177, μPD78F9177A, μPD78F9177A(A), and μPD78F9177A(A1) are flash memory versions of the μPD789177 Subseries.

The μPD78F9177Y, μPD78F9177AY, and μPD78F9177AY(A) are flash memory versions of the μPD789177Y Subseries.

The μPD78F9177, μPD78F9177A, μPD78F9177A(A), and μPD78F9177A(A1) replace the internal ROM of the μPD789167 and 789177 Subseries with flash memory, while the μPD78F9177Y, μPD78F9177AY, and μPD78F9177AY(A) replace the internal ROM of the μPD789167Y and 789177Y Subseries with flash memory. The differences between the flash memory and mask ROM versions are shown in Table 20-1.

Table 20-1. Differences Between Flash Memory and Mask ROM Versions

Item		Flash Memory		Mask ROM			
		μPD78F9177A μPD78F9177AY μPD78F9177A(A) μPD78F9177AY(A) μPD78F9177AY(A1)	μPD78F9177 μPD78F9177Y	μPD789166 μPD789166Y μPD789166(A) μPD789166Y(A) μPD789166(A1) μPD789166(A2)	μPD789167 μPD789167Y μPD789167(A) μPD789167Y(A) μPD789167(A1) μPD789167(A2)	μPD789176 μPD789176Y μPD789176(A) μPD789176Y(A) μPD789176(A1) μPD789176(A2)	μPD789177 μPD789177Y μPD789177(A) μPD789177Y(A) μPD789177(A1) μPD789177(A2)
Internal memory	ROM structure	Flash Memory		Mask ROM			
	ROM capacity	24 KB		16 KB	24 KB	16 KB	24 KB
	High-speed RAM	512 bytes					
Minimum instruction execution time		0.2 μs (at 10 MHz operation)	0.4 μs (at 5 MHz operation)	Expanded-specification products: 0.2 μs (at 10 MHz operation) (A1) products, (A2) products, and conventional products: 0.4 μs (at 5 MHz operation)			
A/D converter resolution		10 bits		8 bits		10 bits	
Specification of on-chip pull-up resistors for P50 to P53 by mask option		Disabled		Enabled			
V_{PP} pin		Provided		Not provided			
Electrical specifications		Refer to the ELECTRICAL SPECIFICATIONS chapters.					

Cautions 1. There are differences in the amount of noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering sample, ES) of the mask ROM version.

2. When using A/D conversion result register 0 (ADCR0) with an 8-bit A/D converter (μPD789167 and 789167Y Subseries), manipulate with an 8-bit memory manipulation instruction; when using it with a 10-bit A/D converter (μPD789177 and 789177Y Subseries), use a 16-bit memory manipulation instruction.

When the flash memory version of the μPD789167 or 789167Y Subseries, is used, however, ADCR0 can be manipulated with an 8-bit memory manipulation instruction. In this case, use an object file assembled with the μPD789167 or 789167Y Subseries.

20.1 Flash Memory Characteristics

Flash memory programming is performed by connecting a dedicated flash programmer (Flashpro III (part no. FL-PR3, PG-FP3) or Flashpro IV (part no. FL-PR4, PG-FP4)) to the target system with the μPD78F9177, μPD78F9177Y, μPD78F9177A, and μPD78F9177AY mounted on the target system (on-board). A flash memory program adapter (FA adapter), which is a target board used exclusively for programming, is also provided.

Remark FL-PR3, FL-PR4, and the program adapter are the products made by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

Programming using flash memory has the following advantages.

- Software can be modified after the microcontroller is solder-mounted on the target system.
- Distinguishing software facilities low-quantity, varied model production
- Easy data adjustment when starting mass production

20.1.1 Programming environment

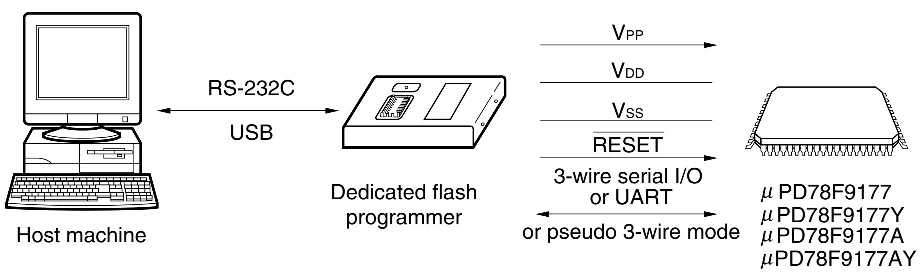
The following shows the environment required for μPD78F9177, μPD78F9177Y, μPD78F9177A, and μPD78F9177AY flash memory programming.

When Flashpro III or Flashpro IV is used as a dedicated flash programmer, a host machine is required to control the dedicated flash programmer. Communication between the host machine and flash programmer is performed via RS-232C/USB (Rev. 1.1).

For details, refer to the manual for Flashpro III or Flashpro IV.

Remark USB is supported by Flashpro IV only.

Figure 20-1. Environment for Writing Program to Flash Memory



20.1.2 Communication mode

Use the communication mode shown in Table 20-2 to perform communication between the dedicated flash programmer and μPD78F9177, μPD78F9177Y, μPD78F9177A, and μPD78F9177AY.

Table 20-2. Communication Mode List

Communication Mode	TYPE Setting[Note 1]					Pins Used	Number of V_{PP} Pulses
	COMM PORT	SIO Clock	CPU Clock[Notes 2, 3]		Multiple Rate		
			In Flashpro	On Target Board			
3-wire serial I/O (SIO3)	SIO ch-0 (3-wired, sync.)	100 Hz to 1.25 MHz[Note 3]	1, 2, 4, 5, 6, 8, 10 MHz[Note 4]	1 to 10 MHz	1.0	SI20/RxD20/P22 SO20/TxD20/P21 $\overline{SCK20}$/ASCK20/P20	0
	SIO ch-1 (3-wired, sync.)[Note 8]					P02 P01 P00	1[Note 8]
SMB[Note 5]	I2C ch-0	10 to 100 kHz	1, 2, 4, 5, 6, 8, 10 MHz[Note 4]	1 to 10 MHz	1.0	SCL0/P23 SDA0/P24	4
UART	UART ch-0 (Async.)	4,800 to 76,800 bps[Notes 3, 6]	5, 10 MHz[Note 7]	4.91, 5, 10 MHz	1.0	RxD20/SI20/P22 TxD20/SO20/P21	8
Pseudo 3-wire[Note 9]	Port A (Pseudo 3-wire)	100 Hz to 1 kHz	1, 2, 4, 5 MHz	1 to 5 MHz	1.0	P02 P01 P00	12[Note 9]

Notes
1. Selection items for TYPE settings on the dedicated flash programmer (Flashpro III or Flashpro IV).
2. Setting a frequency 5 MHz or higher for the μPD78F9177 and μPD78F9177Y is prohibited.
3. The possible setting range differs depending on the voltage. For details, refer to chapters related to the ELECTRICAL SPECIFICATIONS chapters.
4. Only 2, 4, 8 MHz in Flashpro III.
5. For the μPD78F9177Y and μPD78F9177AY only. Set SLAVE ADDRESS to 10H.
6. Because signal wave slew also affects UART communication, in addition to the baud rate error, thoroughly evaluate the slew and baud rate error.
7. Available only in Flashpro IV. When using Flashpro III, be sure to select the clock of the resonator on the board. UART cannot be used with the clock supplied by Flashpro III.
8. In the μPD78F9177A and μPD78F9177AY only.
9. In the μPD78F9177 and μPD78F9177Y only. Serial transfer is performed by controlling the ports by software.

Figure 20-2. Communication Mode Selection Format

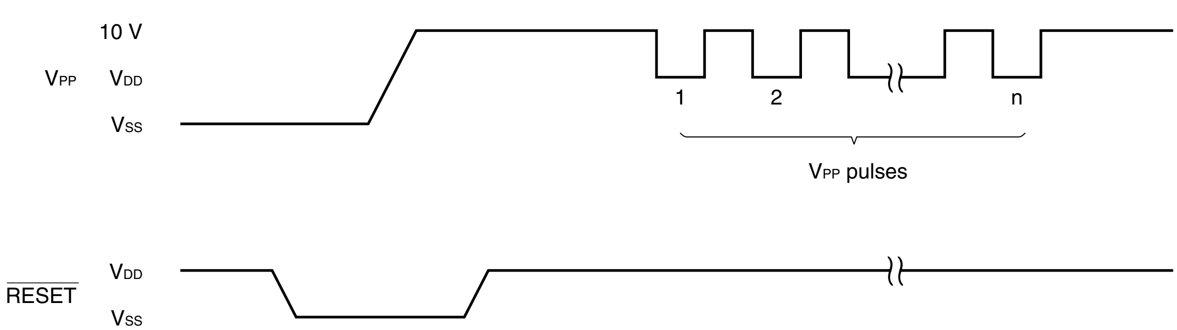
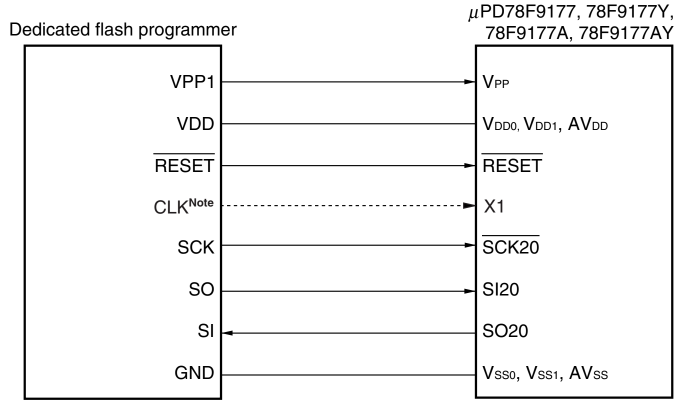
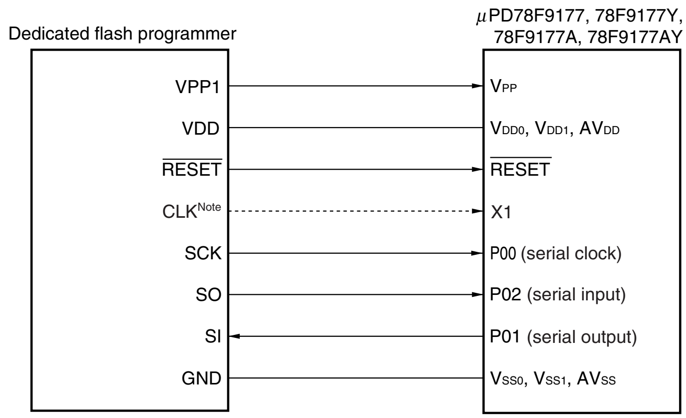


Figure 20-3. Example of Connection with Dedicated Flash Programmer (1/2)

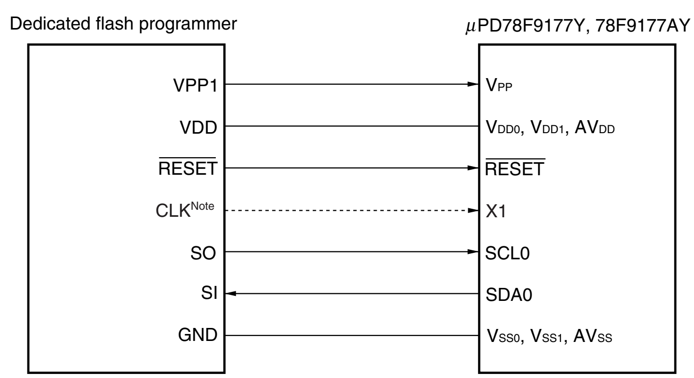
(a) 3-wire serial I/O (SIO-ch0)



(b) 3-wire serial I/O (SIO-ch1) or pseudo 3-wire mode



(c) SMB

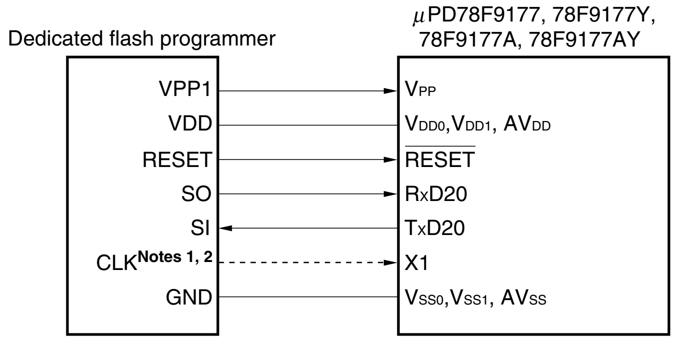


Note Connect this pin when the system clock is supplied from the dedicated flash programmer. If a resonator is already connected to the X1 pin, the CLK pin does not need to be connected.

Caution The V_{DD} pin, if already connected to the power supply, must be connected to the VDD pin of the dedicated flash programmer. Before using the power supply connected to the V_{DD} pin, supply voltage before starting programming.

Figure 20-3. Example of Connection with Dedicated Flash Programmer (2/2)

(d) UART



Notes 1. Connect this pin when the system clock is supplied from the dedicated flash programmer. If a resonator is already connected to the X1 pin, the CLK pin does not need to be connected.

2. When using UART with Flashpro III, the clock of the resonator connected to the X1 pin must be used, so connection to the CLK pin is not necessary.

Caution The V_{DD} pin, if already connected to the power supply, must be connected to the VDD pin of the dedicated flash programmer. Before using the power supply connected to the V_{DD} pin, supply voltage before starting programming.

If Flashpro III or Flashpro IV is used as a dedicated flash programmer, the following signals are generated for the μPD78F9177, μPD78F9177Y, μPD78F9177A, and μPD78F9177AY. For details, refer to the manual of Flashpro III or Flashpro IV.

Table 20-3. Pin Connection List

Signal Name	I/O	Pin Function	Pin Name	3-Wire Serial I/O (SIO-ch0)	3-Wire Serial I/O (SIO-ch1)Note 1	SMBNote 2	UART	Pseudo 3-WireNote 3
VPP1	Output	Write voltage	V_{PP}	◎	◎	◎	◎	◎
VPP2	–	–	–	×	×	×	×	×
VDD	I/O	V_{DD} voltage generation/ voltage monitoring	V_{DD0}/V_{DD1}/AV_{DD}	◎ Note 4	◎ Note 4	◎ Note 4	◎ Note 4	◎ Note 4
GND	–	Ground	V_{SS0}/V_{SS1}/AV_{SS}	◎	◎	◎	◎	◎
CLK	Output	Clock output	X1	○	○	○	○	○
RESET	Output	Reset signal	$\overline{\text{RESET}}$	◎	◎	◎	◎	◎
SI	Input	Receive signal	SO20/P01/ SDA0/TxD20	◎	◎	◎	◎	◎
SO	Output	Transmit signal	SI20/P02/SCL0 /RxD20	◎	◎	◎	◎	◎
SCK	Output	Transfer clock	$\overline{\text{SCK20}}$/P00	◎	◎	×	×	◎
HS	Input	Handshake signal	–	×	×	×	×	×

Notes 1. In the μPD78F9177A and μPD78F9177AY only

2. In the μPD78F9177Y and μPD78F9177AY only

3. In the μPD78F9177 and μPD78F9177Y only

4. V_{DD} voltage must be supplied before programming is started.

Remark ◎: Pin must be connected.

○: If the signal is supplied on the target board, pin does not need to be connected.

×: Pin does not need to be connected.

20.1.3 On-board pin processing

When performing programming on the target system, provide a connector on the target system to connect the dedicated flash programmer.

An on-board function that allows switching between normal operation mode and flash memory programming mode may be required in some cases.

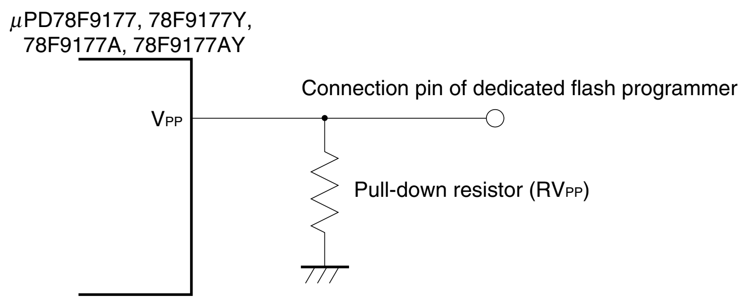
<V_{PP} pin>

In normal operation mode, input 0 V to the V_{PP} pin. In flash memory programming mode, a write voltage of 10.0 V (TYP.) is supplied to the VPP pin, so perform one of the following (1) or (2).

(1) Connect a pull-down resistor (RV_{PP} = 10 kΩ) to the V_{PP} pin.
(2) Use the jumper on the board to switch the V_{PP} pin input to either the writer or directly to GND.

A V_{PP} pin connection example is shown below.

Figure 20-4. V_{PP} Pin Connection Example



<Serial interface pin>

The following shows the pins used by the serial interface.

Serial Interface		Pins Used
3-wire serial I/O	SIO-ch0	SI20, SO20, $\overline{SCK20}$
	SIO-ch1[Note 1]	P00, P01, P02
SMB[Note 2]		SCL0, SDA0
UART		RxD20, TxD20
Pseudo 3-wire[Note 3]		P00, P01, P02

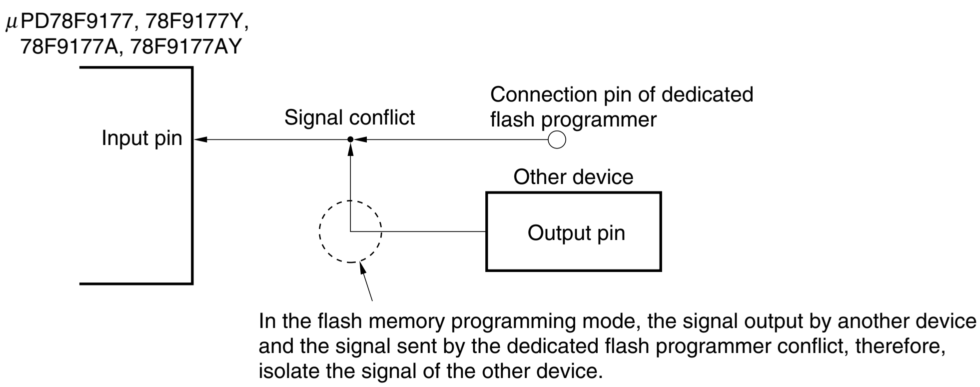
Notes 1. In the μPD78F9177A and μPD78F9177AY only
2. In the μPD78F9177Y and μPD78F9177AY only
3. In the μPD78F9177 and μPD78F9177Y only

When connecting the dedicated flash programmer to a serial interface pin that is connected to another device on-board, signal conflict or abnormal operation of the other device may occur. Care must therefore be taken with such connections.

(1) Signal conflict

If the dedicated flash programmer (output) is connected to a serial interface pin (input) that is connected to another device (output), a signal conflict occurs. To prevent this, isolate the connection with the other device or set the other device to the output high impedance status.

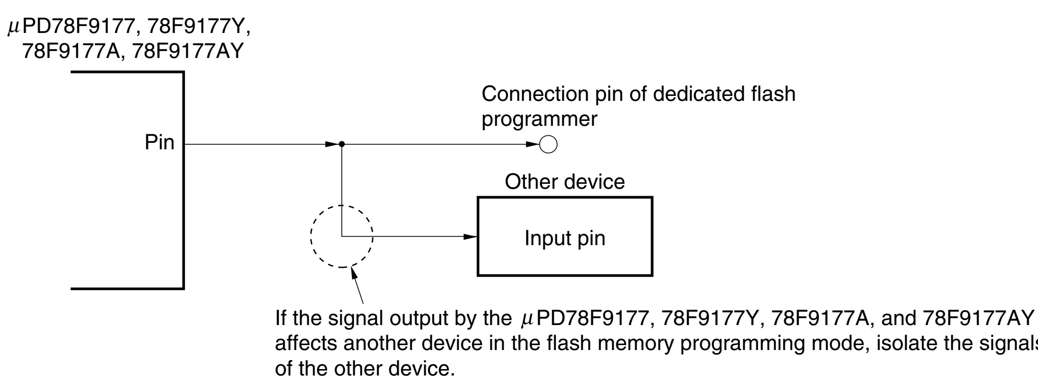
Figure 20-5. Signal Conflict (Input Pin of Serial Interface)

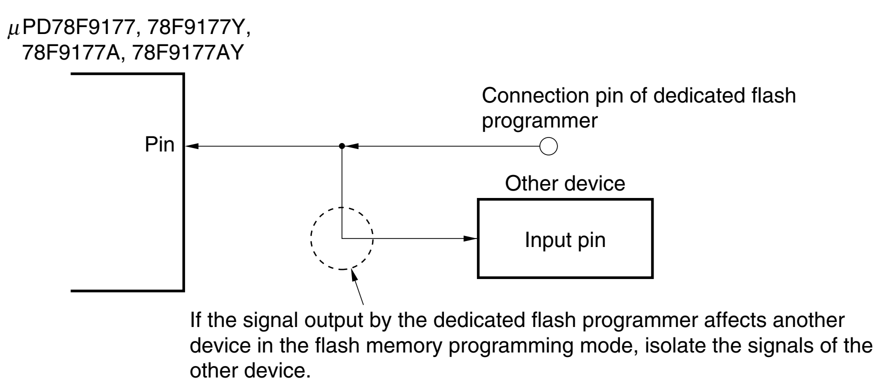


(2) Abnormal operation of other device

If the dedicated flash programmer (output or input) is connected to a serial interface pin (input or output) that is connected to another device (input), a signal is output to the device, and this may cause an abnormal operation. To prevent this abnormal operation, isolate the connection with the other device or set so that the input signals to the other device are ignored.

Figure 20-6. Abnormal Operation of Other Device



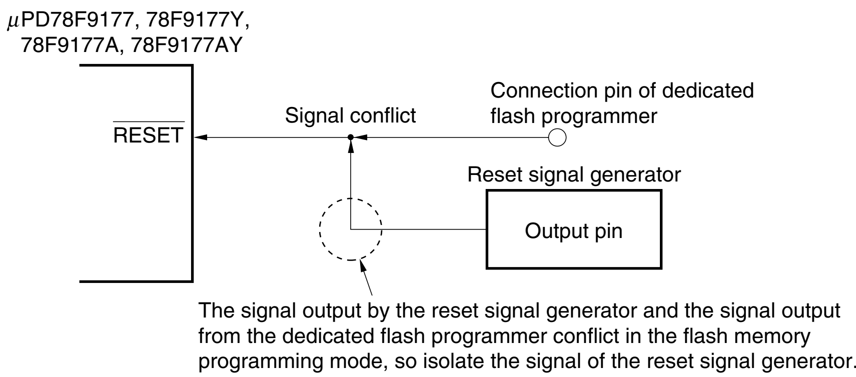


<RESET pin>

If the reset signal of the dedicated flash programmer is connected to the RESET pin connected to the reset signal generator on-board, a signal conflict occurs. To prevent this, isolate the connection with the reset signal generator.

If the reset signal is input from the user system in the flash memory programming mode, a normal programming operation cannot be performed. Therefore, do not input reset signals from other than the dedicated flash programmer.

Figure 20-7. Signal Conflict (RESET Pin)



<Port pins>

When the μPD78F9177, μPD78F9177Y, μPD78F9177A, and μPD78F9177AY enter the flash memory programming mode, all the pins other than those that communicate in flash memory programmer are in the same status as immediately after reset.

If the external device does not recognize initial statuses such as the output high impedance status, therefore, connect the external device to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor.

<Oscillator>

When using the on-board clock, connect X1, X2, XT1, and XT2 as required in the normal operation mode.

When using the clock output of the flash programmer, connect it directly to X1, disconnecting the main oscillator on-board, and leave the X2 pin open. The subclock conforms to the method in the normal operation mode.

<Power supply>

To use the power output from the flash programmer, connect the V_{DD0} and V_{DD1} pins to VDD of the flash programmer, and the V_{SS0} and V_{SS1} pins to GND of the flash programmer.

To use the on-board power supply, make connections that accord with the normal operation mode. However, because the voltage is monitored by the flash programmer, be sure to connect VDD of the flash programmer.

Supply the same power as in the normal operation mode to the other power supply pins (AV_{DD}, AV_{REF}, and AV_{SS}).

20.1.4 Connection of adapter for flash writing

The following figures show the examples of recommended connection when the adapter for flash writing is used.

Figure 20-8. Wiring Example for Flash Writing Adapter in 3-Wire Serial I/O Mode (SIO-ch0) (1/2)

(a) 44-pin plastic LQFP (10 × 10)

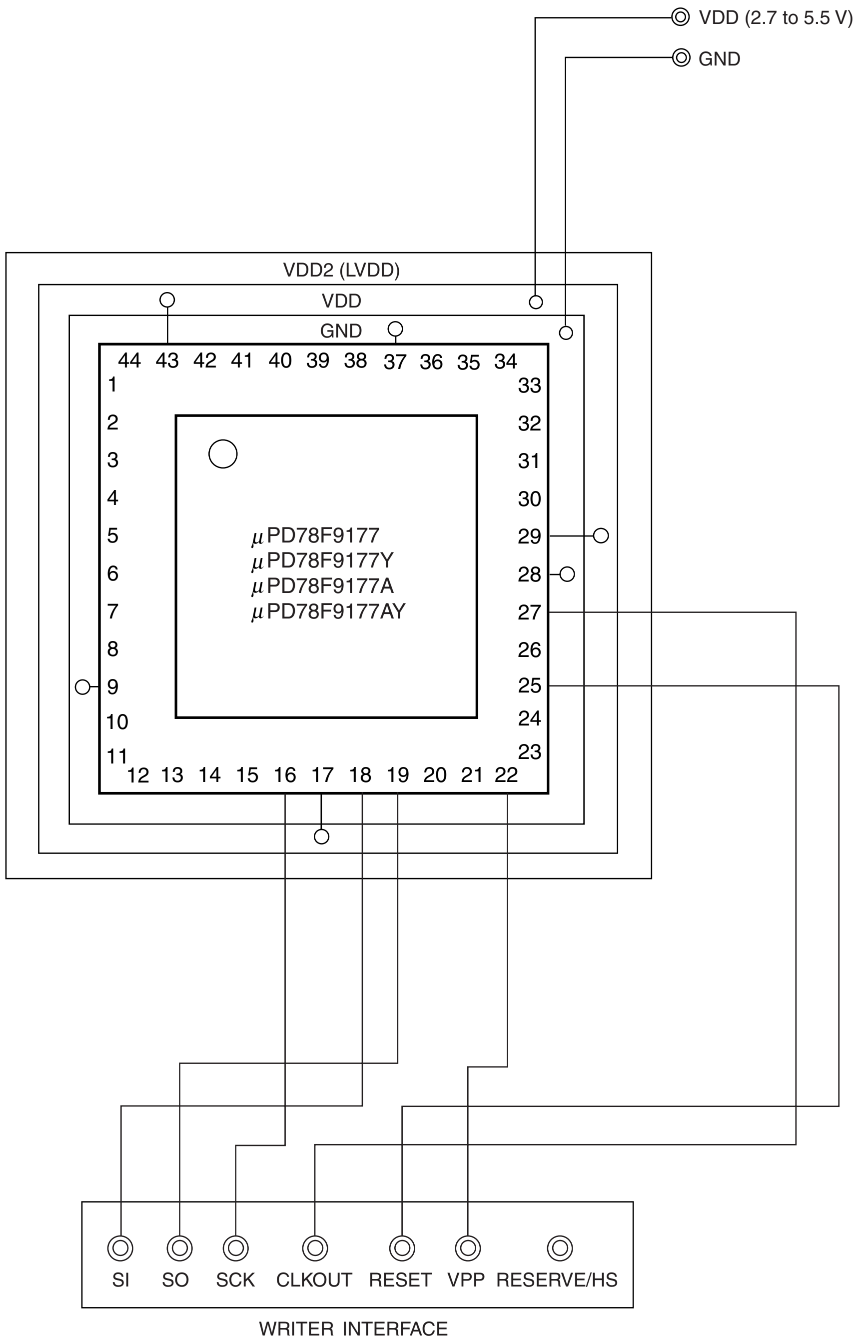


Figure 20-8. Wiring Example for Flash Writing Adapter in 3-Wire Serial I/O Mode (SIO-ch0) (2/2)

(b) 48-pin plastic TQFP (fine pitch) (7 × 7)

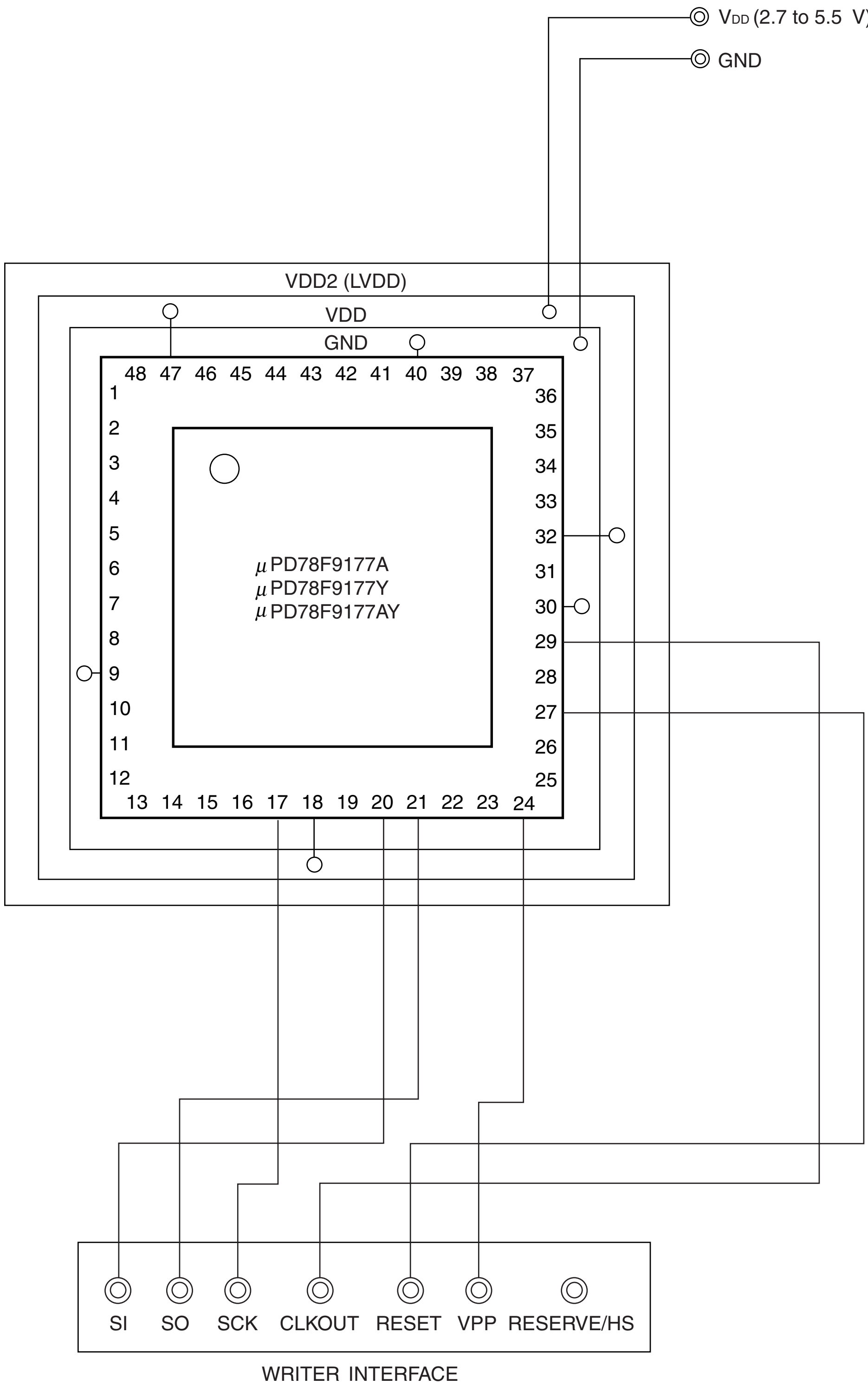


Figure 20-9. Wiring Example for Flash Writing Adapter in 3-Wire Serial I/O Mode (SIO-ch1) or Pseudo 3-Wire Mode (1/2)

(a) 44-pin plastic LQFP (10 × 10)

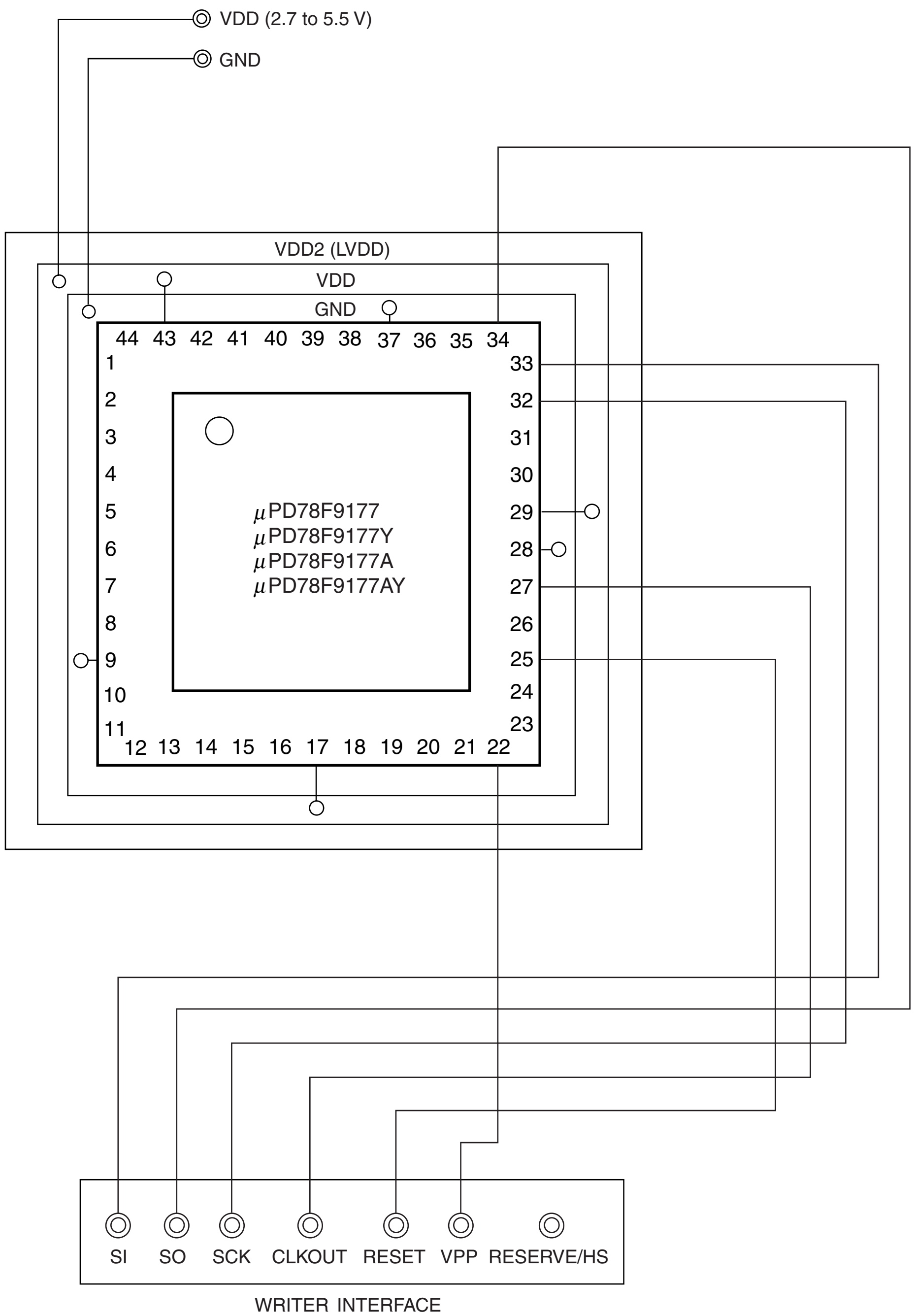


Figure 20-9. Wiring Example for Flash Writing Adapter in 3-Wire Serial I/O Mode (SIO-ch1) or Pseudo 3-Wire Mode (2/2)

(b) 48-pin plastic TQFP (fine pitch) (7 × 7)

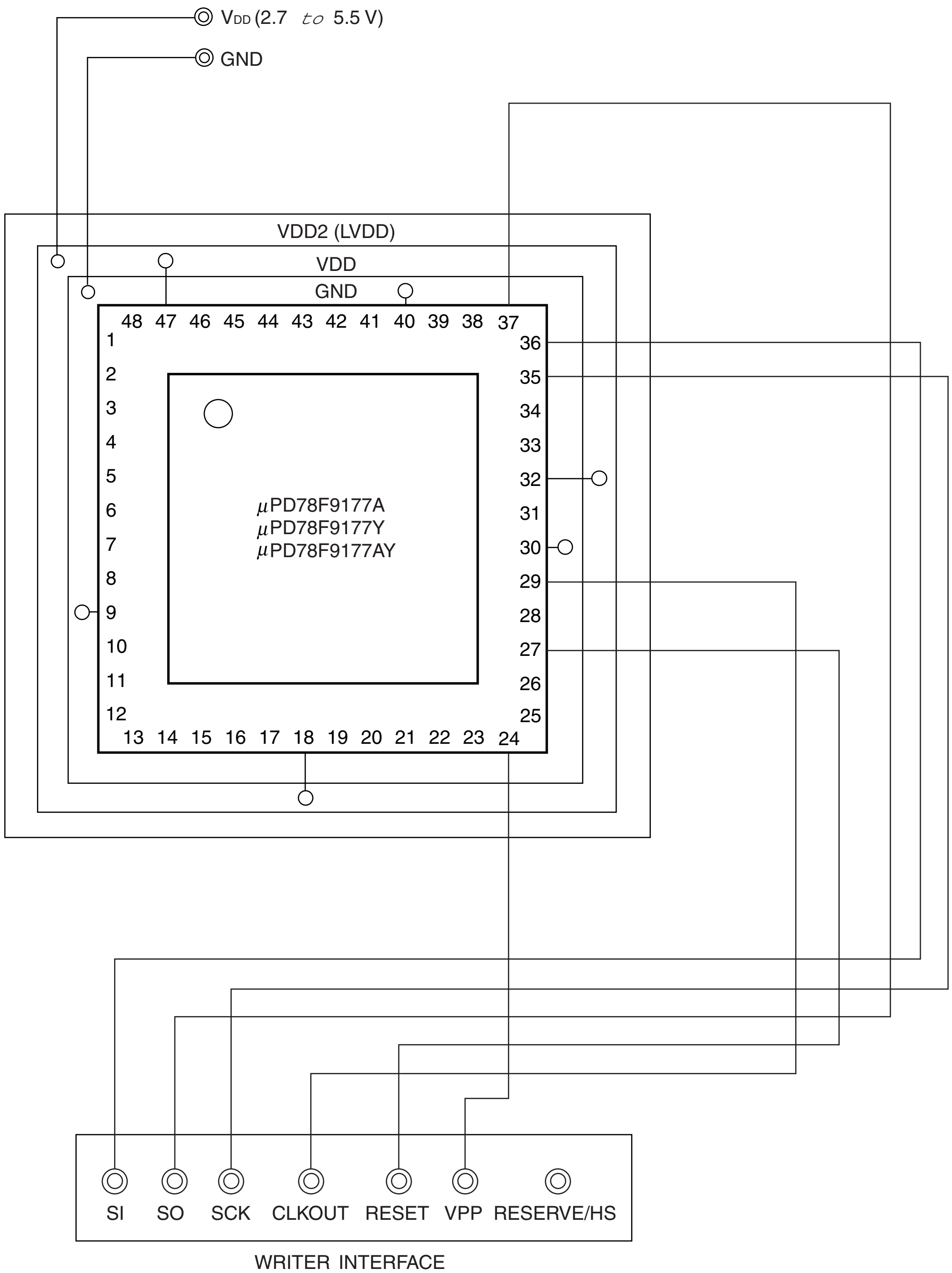


Figure 20-10. Wiring Example for Flash Writing Adapter in SMB Mode (1/2)

(a) 44-pin plastic LQFP (10 × 10)

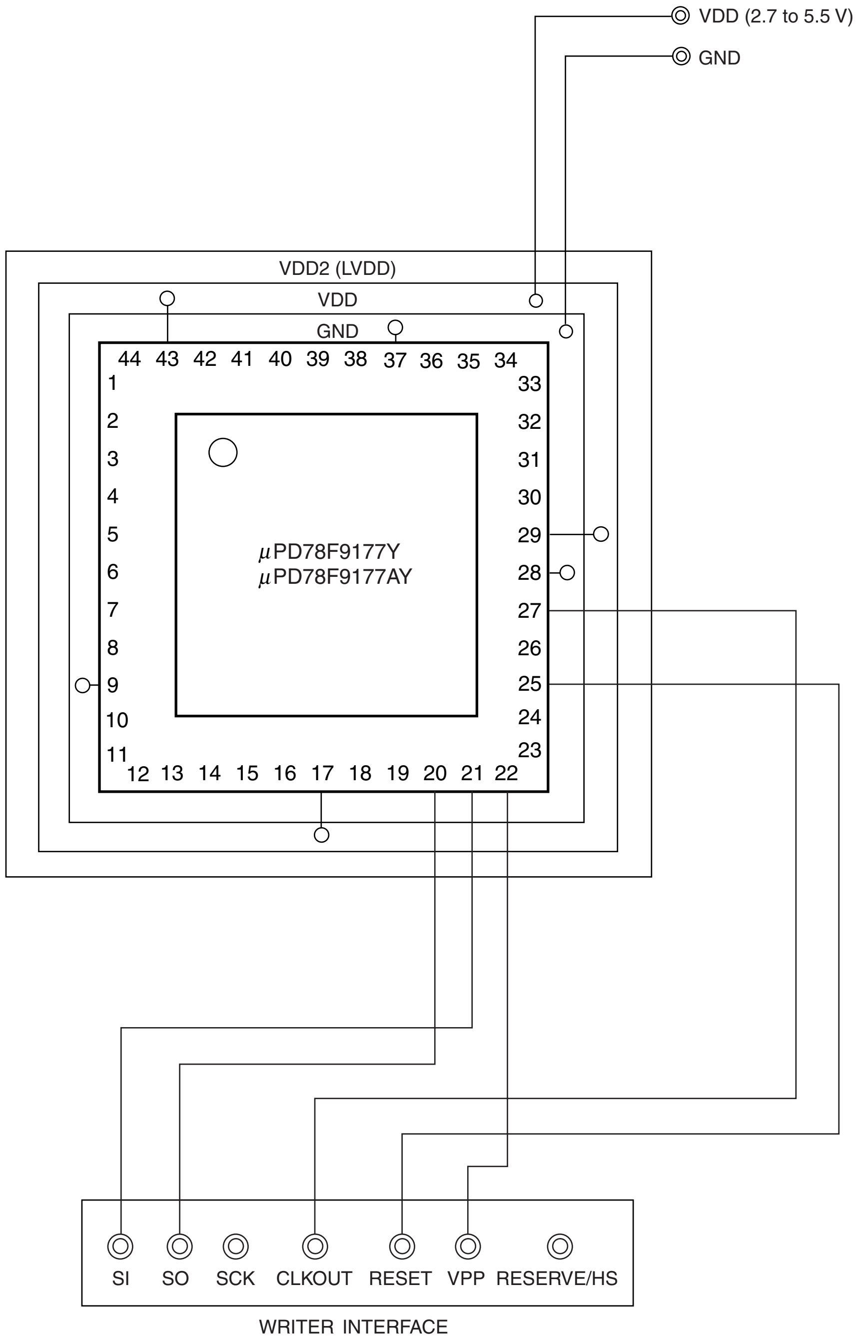


Figure 20-10. Wiring Example for Flash Writing Adapter in SMB Mode (2/2)

(b) 48-pin plastic TQFP (fine pitch) (7 × 7)

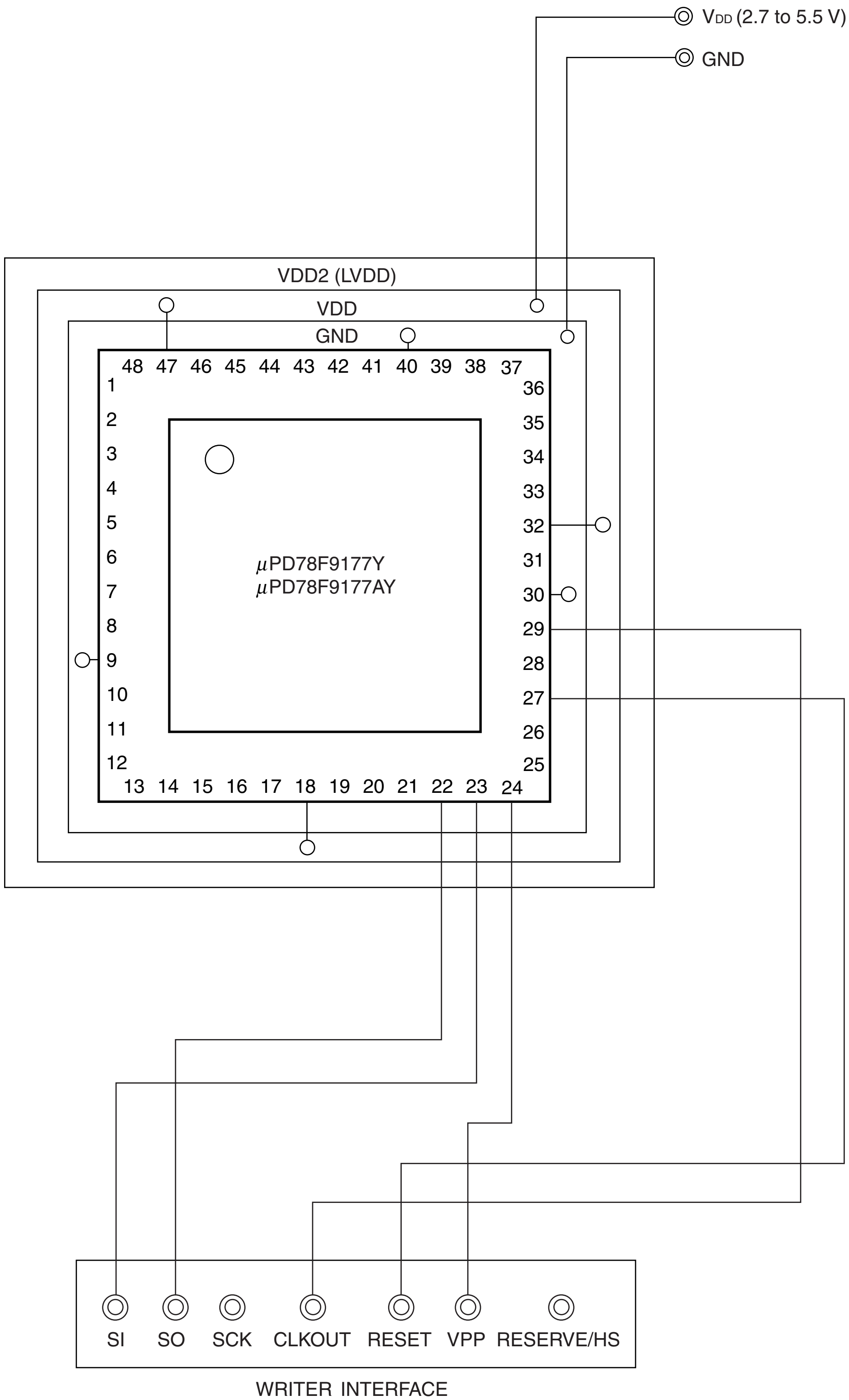


Figure 20-11. Wiring Example for Flash Writing Adapter in UART Mode (1/2)

(a) 44-pin plastic LQFP (10 × 10)

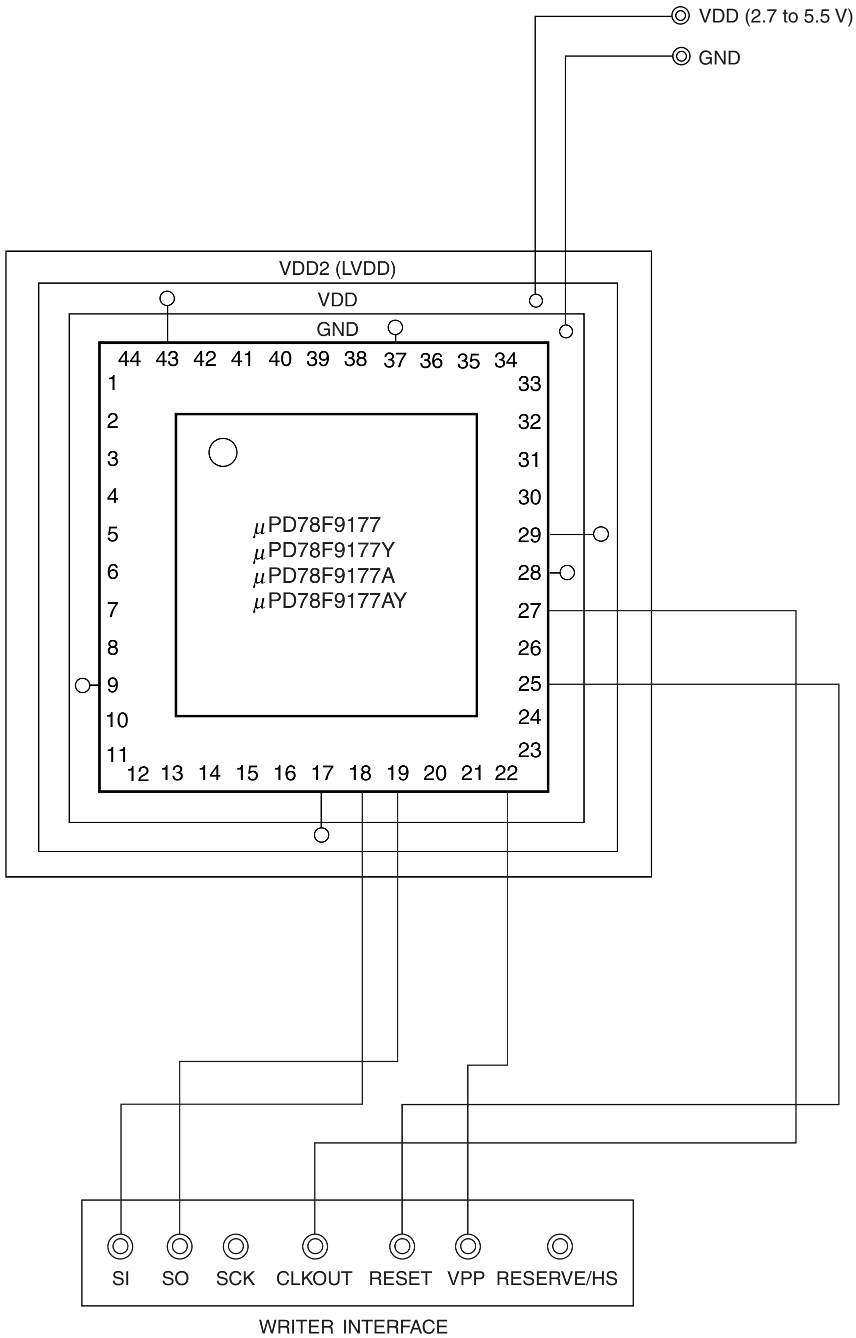
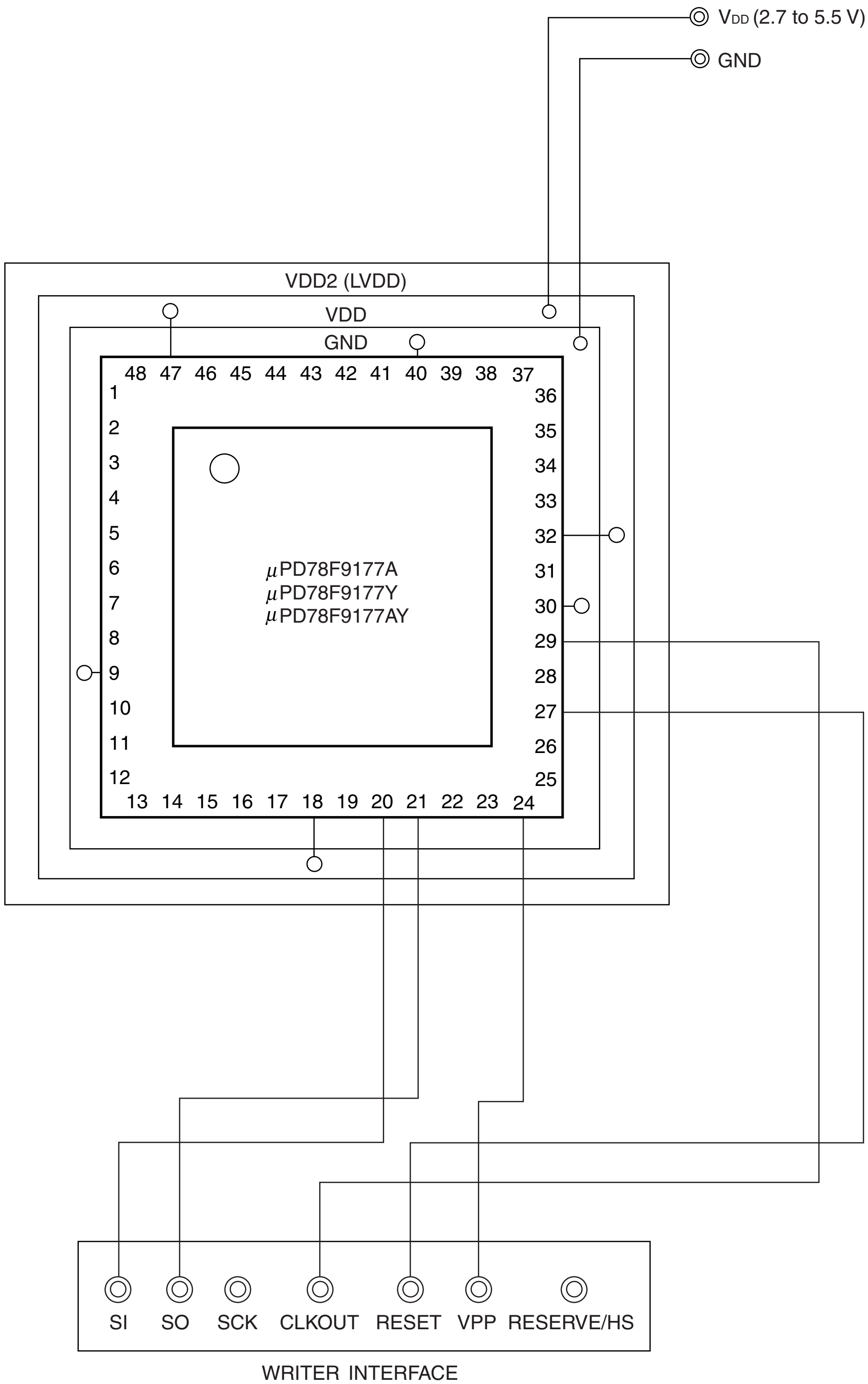


Figure 20-11. Wiring Example for Flash Writing Adapter in UART Mode (2/2)

(b) 48-pin plastic TQFP (fine pitch) (7 × 7)



CHAPTER 21 MASK OPTION

Table 21-1. Selection of Mask Option for Pins

Pin	Mask Option
P50 to P53	Whether a pull-up resistor is to be incorporated can be specified in 1-bit units.

For P50 to P53 (port 5), whether a pull-up resistor is to be incorporated can be specified by a mask option. The mask option is specified in 1-bit units.

Caution The flash memory versions do not provide a mask option pull-up resistor incorporation function.

CHAPTER 22 INSTRUCTION SET

This chapter lists the instruction set of the μPD789167, 789177, 789167Y, and 789177Y Subseries. For details of the operation and machine language (instruction code) of each instruction, refer to **78K/0S Series Instruction User's Manual (U11047E)**.

22.1 Operation

22.1.1 Operand identifiers and description methods

Operands are described in "Operand" column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Uppercase letters the and symbols, #, !, $, and [ ] are keywords and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, $ and [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 22-1. Operand Identifiers and Description Methods

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special-function register symbol
saddr saddrp	FE20H to FF1FH Immediate data or labels FE20H to FF1FH Immediate data or labels (even addresses only)
addr16 addr5	0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions) 0040H to 007FH Immediate data or labels (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

Remark See **Table 5-3 Special-Function Registers** for symbols of special-function registers.

22.1.2 Description of "Operation" column

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
( ):	Memory contents indicated by address or register contents in parenthesis
$\times_H$, $\times_L$:	Higher 8 bits and lower 8 bits of 16-bit register
$\wedge$:	Logical product (AND)
$\vee$:	Logical sum (OR)
$\forall$:	Exclusive logical sum (exclusive OR)
—:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

22.1.3 Description of "Flag" column

(Blank):	Unchanged
0:	Cleared to 0
1:	Set to 1
$\times$:	Set/cleared according to the result
R:	Previously saved value is stored

22.2 Operation List

Mnemonic	Operands	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ sfr			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			

Notes 1. Except r = A.

2. Except r = A, X.

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operands	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note	1	4	AX ← rp			
	rp, AX Note	1	4	rp ← AX			
XCHW	AX, rp Note	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×

Note Only when rp = BC, DE, or HL.

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operands	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊽ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊽ byte	×		
	A, r	2	4	A ← A ⊽ r	×		
	A, saddr	2	4	A ← A ⊽ (saddr)	×		
	A, !addr16	3	8	A ← A ⊽ (addr16)	×		
	A, [HL]	1	6	A ← A ⊽ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊽ (HL + byte)	×		

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operands	Bytes	Clocks	Operation	Flag Z	Flag AC	Flag CY
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW.bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operands	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
CALL	!addr16	3	6	(SP – 1) ← $(PC + 3)_H$, (SP – 2) ← $(PC + 3)_L$, PC ← addr16, SP ← SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← $(PC + 1)_H$, (SP – 2) ← $(PC + 1)_L$, PC_H ← (00000000, addr5 + 1), PC_L ← (00000000, addr5), SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP – 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC_H ← A, PC_L ← X			
BC	$saddr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1			
BNC	$saddr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0			
BZ	$saddr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1			
BNZ	$saddr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0			
BT	saddr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr.bit) = 1			
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr.bit = 1			
	A.bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A.bit = 1			
	PSW.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW.bit = 1			
BF	saddr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr.bit) = 0			
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr.bit = 0			
	A.bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A.bit = 0			
	PSW.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW.bit = 0			
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0			
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0			
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0			
NOP		1	2	No Operation			
EI		3	6	IE ← 1 (Enable Interrupt)			
DI		3	6	IE ← 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

22.3 Instructions Listed by Addressing Type

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, INC, DEC, ROR, ROL, RORC, ROLC, PUSH, POP, DBNZ

1st Operand \ 2nd Operand	#byte	A	r	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV[Note] XCH[Note] ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											
[HL + byte]		MOV											

Note Except r = A.

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand / 1st Operand	#word	AX	rp[Note]	saddrp	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	
rp	MOVW	MOVW[Note]				INCW DECW PUSH POP
saddrp		MOVW				
sp		MOVW				

Note Only when rp = BC, DE, or HL.

(3) Bit manipulation instructions

SET1, CLR1, NOT1, BT, BF

2nd Operand / 1st Operand	$addr16	None
A.bit	BT BF	SET1 CLR1
sfr.bit	BT BF	SET1 CLR1
saddr.bit	BT BF	SET1 CLR1
PSW.bit	BT BF	SET1 CLR1
[HL].bit		SET1 CLR1
CY		SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLT, BR, BC, BNC, BZ, BNZ, DBNZ

2nd Operand / 1st Operand	AX	!addr16	[addr5]	$addr16
Basic instructions	BR	CALL BR	CALLT	BR BC BNC BZ BNZ
Compound instructions				DBNZ

(5) Other instructions

RET, RETI, NOP, EI, DI, HALT, STOP

CHAPTER 23 ELECTRICAL SPECIFICATIONS (μPD78916x, 17x, 16xY, 17xY, 16x(A), 17x(A), 16xY(A), 17xY(A))

Remark The values listed in this chapter are for expanded-specification products.

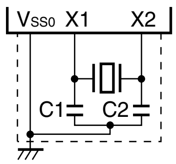
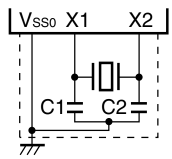
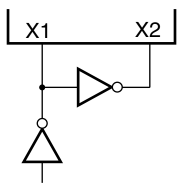
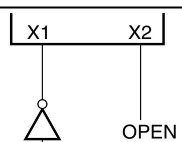
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}	$AV_{DD} - 0.3\ V \leq V_{DD} \leq AV_{DD} + 0.3\ V$		–0.3 to +6.5	V
	AV_{DD}	$AV_{REF} \leq AV_{DD} + 0.3\ V$			V
	AV_{REF}	$AV_{REF} \leq V_{DD} + 0.3\ V$			V
Input voltage	V_{I1}	Pins other than P50 to P53, P23, P24		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P23, P24		–0.3 to +5.5	V
	V_{I3}	P50 to P53	N-ch open drain	–0.3 to +13	V
			On-chip pull-up resistor	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78916x, 78917x, 78916xY, 78917xY	–10	mA
		Total for all pins		–30	mA
		Per pin	μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A)	–7	mA
		Total for all pins		–22	mA
Output current, low	I_{OL}	Per pin	μPD78916x, 78917x, 78916xY, 78917xY	30	mA
		Total for all pins		160	mA
		Per pin	μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A)	10	mA
		Total for all pins		120	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
			V_{DD} = 1.8 to 5.5 V			30	ms
External clock		X1 input frequency (f_X)[Note 1]	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.5 to 5.5 V	45		500	ns
			V_{DD} = 3.0 to 5.5 V	75		500	ns
			V_{DD} = 1.8 to 5.5 V	85		500	ns
		X1 input frequency (f_X)[Note 1]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Recommended Oscillator Constant (μPD78916x, 17x, 16xY, and 17xY)

Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remarks
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd. (Standard type)	CSBLA1M00J58-B0	1.000	150	150	2.2	5.5	Without on-chip capacitor
	CSBFB1M00J58-R1						
	CSTCC2M00G56-R0	2.000	–	–	1.8	5.5	With on-chip capacitor
	CSTLS2M00G56-B0						
	CSTCR4M00G53-R0	4.000					
	CSTLS4M00G53-B0						
	CSTCR4M19G53-R0	4.195					
	CSTLS4M19G53-B0						
	CSTCR4M91G53-R0	4.915					
	CSTLS4M91G53-B0						
	CSTCR5M00G53-R0	5.000					
	CSTLS5M00G53-B0						
	CSTCR6M00G53-R0	6.000					
	CSTLS6M00G53-B0						
	CSTCE8M00G52-R0	8.000					
	CSTLS8M00G53-B0						
	CSTCE8M38G52-R0	8.388					
	CSTLS8M38G53-B0						
	CSTCE10M0G52-R0	10.000					
	CSTLS10M0G53-B0				1.9	5.5	
Murata Mfg. Co., Ltd. (Low-voltage drive type)	CSTLS10M0G53093-B0	10.000	–	–	1.8	5.5	With on-chip capacitor

Caution The oscillator constant is a reference value based on evaluation in specific environments by the resonator manufacturer. If the oscillator characteristics need to be optimized in the actual application, request the resonator manufacturer for evaluation on the implementation circuit. Note that the oscillation voltage and oscillation frequency merely indicate the characteristics of the oscillator. Use the internal operation conditions of the μPD78916x, 17x, 16xY, and 17xY within the specifications of the DC and AC characteristics.

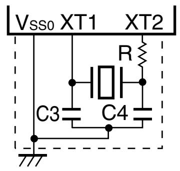
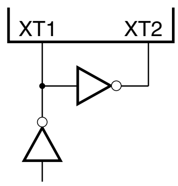
Recommended Oscillator Constant (μPD78916x(A), 17x(A), 16xY(A), and 17xY(A))

Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remarks
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSTCC2M00G56A-R0	2.000	–	–	1.8	5.5	On-chip capacitor
	CSTCR4M00G53A-R0	4.000					
	CSTCR4M19G53A-R0	4.195					
	CSTCR4M91G53A-R0	4.915					
	CSTCR5M00G53A-R0	5.000					
	CSTCR6M00G53A-R0	6.000					
	CSTCE8M00G52A-R0	8.000					
	CSTCE8M38G52A-R0	8.388					
	CSTCE10M0G52A-R0	10.000					

Caution **The oscillator constant is a reference value based on evaluation in specific environments by the resonator manufacturer. If the oscillator characteristics need to be optimized in the actual application, request the resonator manufacturer for evaluation on the implementation circuit. Note that the oscillation voltage and oscillation frequency merely indicate the characteristics of the oscillator. Use the internal operation conditions of the μPD78916x(A), 17x(A), 16xY(A), and 17xY(A) within the specifications of the DC and AC characteristics.**

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
			V_{DD} = 1.8 to 5.5 V			10	s
External clock		XT1 input frequency (f_{XT})Note 1		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78916x, 78917x, 78916xY, 78917xY			–1	mA
		Total for all pins				–15	mA
		Per pin	μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A)			–1	mA
		Total for all pins				–11	mA
Output current, low	I_{OL}	Per pin	μPD78916x, 78917x, 78916xY, 78917xY			10	mA
		Total for all pins				80	mA
		Per pin	μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A)			3	mA
		Total for all pins				60	mA
Input voltage, high	V_{IH1}	P00 to P05, P10, P11, P60 to P67	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53, N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		12	V
		P50 to P53, On-chip pull-up resistor	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{RESET}$, P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P05, P10, P11, P60 to P67	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL3}	$\overline{RESET}$, P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
			V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH}	Pins other than P23, P24, P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78916x, 78917x, 78916xY, 78917xY)			1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A))			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78916x, 78917x, 78916xY, 78917xY)			1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A))			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA			0.4	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input current leakage, high	I_{LIH1}	$V_I = V_{DD}$	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 12 V Note 1	P50 to P53 (N-ch open drain)			20	μA
Input current leakage, low	I_{LIL1}	V_I = 0 V	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–3 Note 2	μA
Output current leakage, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output current leakage, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistor	R_1	V_I = 0 V, for pins other than P23, P24, and P50 to P53		50	100	200	kΩ
Mask option pull-up resistor	R_2	V_I = 0 V, P50 to P53		15	30	60	kΩ

Notes 1. When pull-up resistors are not connected to P50 to P53 (specified by the mask option).

2. A low-level input leakage current of –60 μA (MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 when on-chip pull-up resistors are not connected to P50 to P53 (specified by the mask option) and P50 to P53 are set to input mode. At times other than this, a –3 μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1}[Note 1]	10.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10%[Note 4]		3.2	8.0	mA
		6.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10%[Note 4]		2.0	4.7	mA
		5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10%[Note 4]		1.8	4.0	mA
			V_{DD} = 3.0 V ± 10%[Note 5]		0.6	1.2	mA
			V_{DD} = 2.0 V ± 10%[Note 5]		0.35	0.7	mA
	I_{DD2}[Note 1]	10.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10%[Note 4]		1.5	3.0	mA
		6.0 MHz Crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10%[Note 4]		0.9	1.8	mA
		5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10%[Note 4]		0.75	1.5	mA
			V_{DD} = 3.0 V ± 10%[Note 5]		0.4	0.8	mA
			V_{DD} = 2.0 V ± 10%[Note 5]		0.25	0.5	mA
	I_{DD3}[Note 1]	32.768 kHz crystal oscillation operating mode[Note 3] (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ± 10%		25	90	μA
			V_{DD} = 3.0 V ± 10%		7.0	50	μA
			V_{DD} = 2.0 V ± 10%		3.5	30	μA
	I_{DD4}[Note 1]	32.768 kHz crystal oscillation HALT mode[Note 3] (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ± 10%		16	75	μA
			V_{DD} = 3.0 V ± 10%		4.5	35	μA
			V_{DD} = 2.0 V ± 10%		2.3	18	μA
	I_{DD5}[Note 1]	32.768 kHz crystal stop STOP mode	V_{DD} = 5.0 V ± 10%		0.1	10	μA
			V_{DD} = 3.0 V ± 10%		0.05	5.0	μA
			V_{DD} = 2.0 V ± 10%		0.05	3.0	μA
	I_{DD6}[Note 2]	10.0 MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V ± 10%[Note 4]		4.0	10.0	mA
		6.0 MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V ± 10%[Note 4]		2.8	6.7	mA
		5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10%[Note 4]		2.6	6.0	mA
			V_{DD} = 3.0 V ± 10%[Note 5]		1.4	3.2	mA
			V_{DD} = 2.0 V ± 10%[Note 5]		1.15	2.7	mA

Notes 1. The AV_{REF}ON (ADCS0 (bit 7 of ADM0; A/D converter mode register 0) = 1), AV_{DD}, and the port current (including the current flowing through the internal pull-up resistors) are not included.

2. The AV_{REF}ON (ADCS0 =1) and port current (including the current flowing through the internal pull-up resistors) are not included. Refer to the A/D converter characteristics for the current flowing through AV_{REF}.

3. When the main system clock is stopped.

4. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H.)

5. During low-speed mode operation (when PCC is set to 02H)

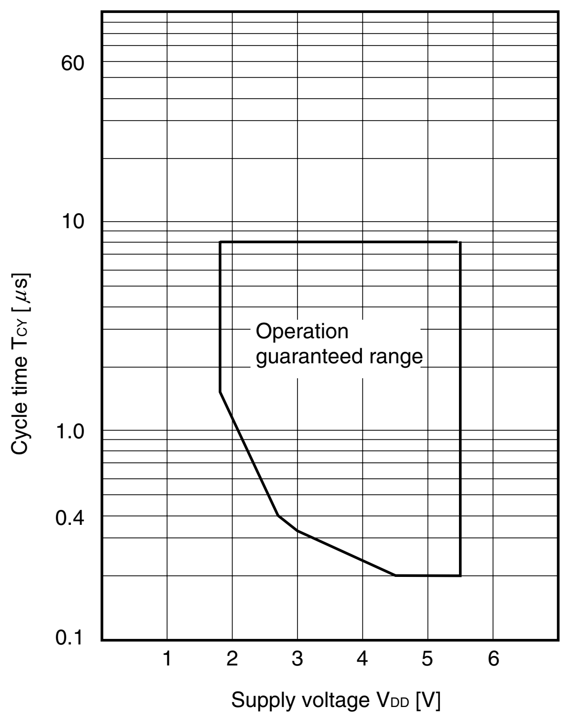
Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operation based on the main system clock	V_{DD} = 4.5 to 5.5 V	0.2		8	μs
			V_{DD} = 3.0 to 5.5 V	0.33		8	μs
			V_{DD} = 2.7 to 5.5 V	0.4		8	μs
			V_{DD} = 1.8 to 5.5 V	1.6		8	μs
		Operation based on the subsystem clock		114	122	125	μs
TI80 and TI81 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
		V_{DD} = 1.8 to 5.5 V		0		275	kHz
TI80 and TI81 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
		V_{DD} = 1.8 to 5.5 V		1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3		10			μs
$\overline{RESET}$ input low-level width	t_{RSL}			10			μs
CPT90 input high-/low-level width	t_{CPH}, t_{CPL}			10			μs

T_{CY} vs. V_{DD} (main system clock)



(2) Serial interface SIO20 (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2 – 50			ns
		V_{DD} = 1.8 to 5.5 V		t_{KCY1}/2 – 150			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode ($\overline{SCK20}$...External clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		900			ns
		V_{DD} = 1.8 to 5.5 V		3500			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$ ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (when using $\overline{SS20}$, to $\overline{SS20}$ ↓)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (when using $\overline{SS20}$, from $\overline{SS20}$ ↑)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
		V_{DD} = 1.8 to 5.5 V	3500			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise time, fall time	t_R, t_F				1	μs

(3) Serial interface SMB0 (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (μPD78916xY, 78917xY, 78916xY(A), 78917xY(A) only)

(a) DC characteristics

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	SCL0, SDA0 (at hysteresis)		$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	SCL0, SDA0 (at hysteresis)		0		$0.2V_{DD}$	V
Output voltage, low	V_{OL}	SCL0, SDA0	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
Input current leakage, high	I_{LIH}	SCL0, SDA0	$V_I = V_{DD}$			3	μA
Input current leakage, low	I_{LIL}	SCL0, SDA0	V_I = 0 V			–3	μA

(b) DC characteristics (when using comparator)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input range	V_{SDA}, V_{SCL}	V_{DD} = 1.8 to 5.5 V	0		5.5	V
Transfer level	V_{ISDA}, V_{ISCL}	$4.5 \leq V_{DD} \leq 5.5$ V	$0.72V_{ISMB}$	V_{ISMB}	$1.28V_{ISMB}$	V
		$3.3 \leq V_{DD} < 4.5$ V	$0.78V_{ISMB}$	V_{ISMB}	$1.22V_{ISMB}$	V
		$2.7 \leq V_{DD} < 3.3$ V	$0.75V_{ISMB}$	V_{ISMB}	$1.25V_{ISMB}$	V
		$1.8 \leq V_{DD} < 2.7$ V	$0.90V_{ISMB}$	V_{ISMB}	$1.45V_{ISMB}$	V
Input level threshold value Note	V_{ISMB}	LVL01, LVL00 = 0, 1		$0.25 \times V_{DD}$		V
		LVL01, LVL00 = 1, 0		$0.375 \times V_{DD}$		V
		LVL01, LVL00 = 1, 1		$0.5 \times V_{DD}$		V

Note V_{ISMB} is an input level threshold value selected by bits LVL00 and LVL01 (bits 0 and 1 of SMB input level setting register 0 (SMBVI0)).

According to the SMB standard (V1.1), the maximum value of low-level input voltage is 0.8 V, and the minimum value of high-level input voltage, 2.1 V. To satisfy these conditions, set LVL01 and LVL00 as follows.

- When V_{DD} = 1.8 to 3.3 V: LVL01, LVL00 = 1, 1 ($0.5 \times V_{DD}$)
- When V_{DD} = 3.3 to 4.5 V: LVL01, LVL00 = 1, 0 ($0.375 \times V_{DD}$)
- When V_{DD} = 4.5 to 5.5 V: LVL01, LVL00 = 0, 1 ($0.25 \times V_{DD}$)

"LVL01, LVL00 = 0, 0" is not possible since this setting does not satisfy the SMB standard (V1.1).

(c) AC characteristics

Parameter		Symbol	SMB Mode		Standard Mode I^2C Bus		High-Speed Mode I^2C Bus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	10	100	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	–	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	–	4.0	–	0.6	–	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	–	4.7	–	0.6	–	μs
Stop condition setup time		$t_{SU:STO}$	4.0	–	4.0	–	0.6	–	μs
Data hold time	When using CBUS-compatible master	$t_{HD:DAT}$	–	–	5	–	–	–	μs
	When using SMB/IIC bus		300	–	0[Note 2]	–	0[Note 2]	900[Note 3]	ns
Data setup time		$t_{SU:DAT}$	250	–	250	–	100[Note 4]	–	ns
SCL0 clock low-level width		t_{LOW}	4.7	–	4.7	–	1.3	–	μs
SCL0 clock high-level width		t_{HIGH}	4.0	50	4.0	–	0.6	–	μs
SCL0 and SDA0 signal fall time		t_F	–	300	–	300	–	300	ns
SCL0 and SDA0 signal rise time		t_R	–	1000	–	1000	–	300	ns
Spike pulse width controlled by input filter		t_{SP}	–	–	–	–	0	50	ns
Timeout		$t_{TIMEOUT}$	25	35	–	–	–	–	ms
Total extended time of SCL0 clock low-level period (slave)		$t_{LOW:SEXT}$	–	25	–	–	–	–	ms
Total extended time of cumulative clock low-level period (master)		$t_{LOW:MEXT}$	–	10	–	–	–	–	ms
Capacitive load per each bus line		Cb	–	–	–	400	–	400	pF

Notes 1. In the start condition, the first clock pulse is generated after this hold time.

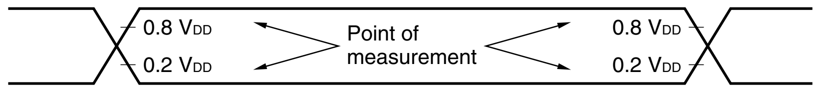
2. To fill in the undefined area of the SCL0 falling edge, it is necessary for the device to internally provide at least 300 ns of hold time for the SDA0 signal (which is $V_{IHmin.}$ of the SCL0 signal).

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

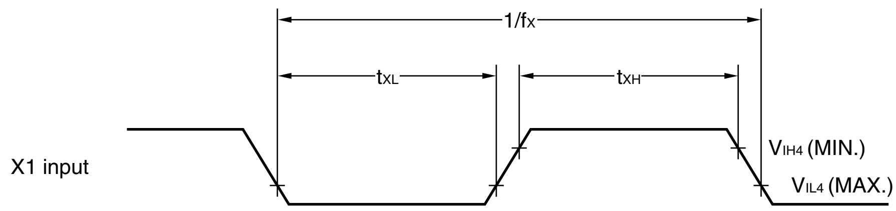
4. The high-speed mode I^2C bus is available in the SMB mode and the standard mode I^2C bus system. At this time, the conditions described below must be satisfied.

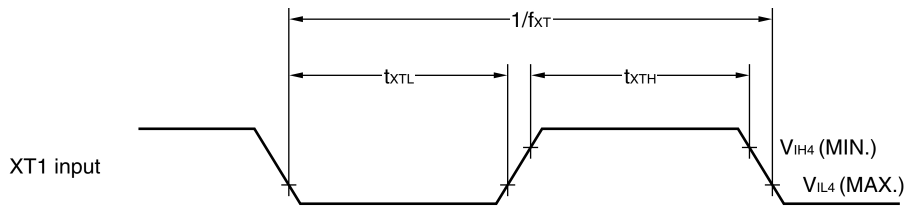
- If the device extends the SCL0 signal low state hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time
  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.}$+ $t_{SU:DAT}$ = 1000 + 250 = 1250 ns by the SMB mode or the standard mode I^2C bus specification).

AC Timing Measurement Points (Excluding X1 and XT1 Inputs)

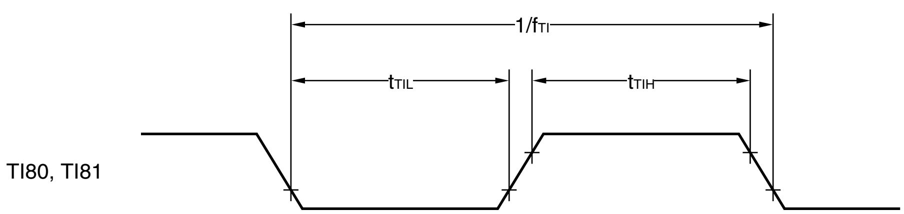


Clock Timing

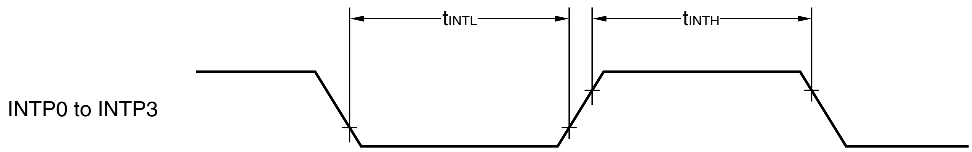




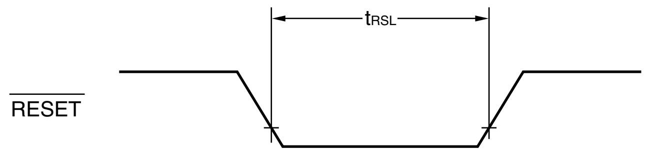
TI Timing



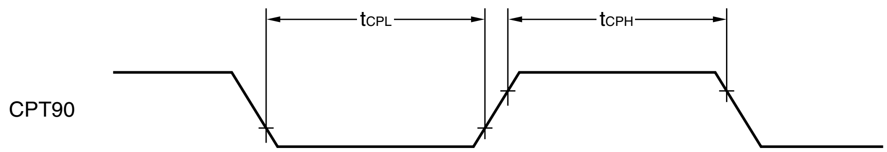
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing

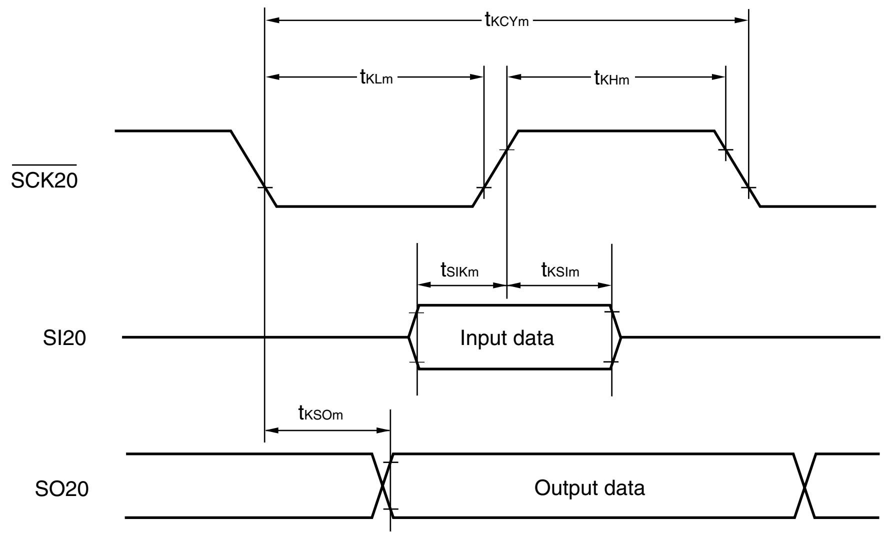


CPT90 Input Timing



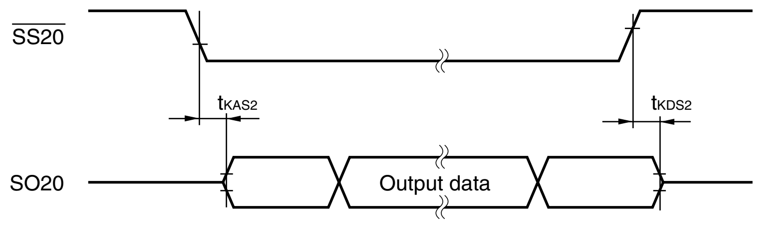
Serial Transfer Timing

3-wire serial I/O mode:

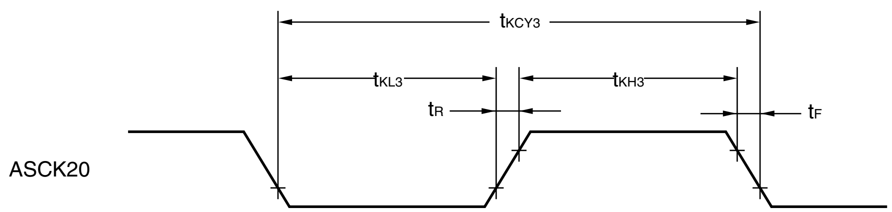


Remark m = 1, 2

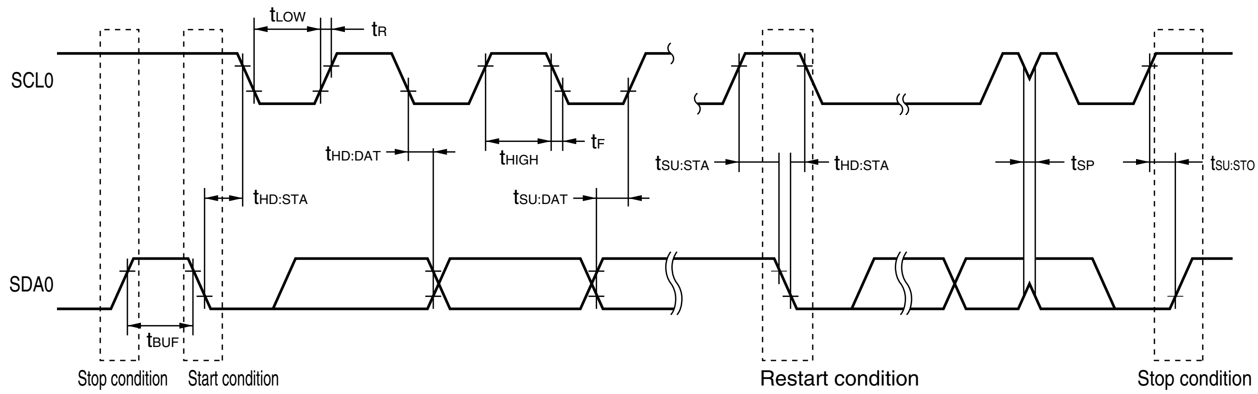
3-wire serial I/O mode (when using SS20):



UART mode (external clock input):



SMB mode:



8-Bit A/D Converter Characteristics (μPD78916x, 78916xY, 78916x(A), 78916xY(A))

(T_A = –40 to +85°C, 1.8 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]		2.7 ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
		1.8 ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	12		100	μs
		2.7 ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		1.8 ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	28		100	μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.2%FSR).

Remark FSR: Full scale range

10-Bit A/D Converter Characteristics (μPD78917x, 78917xY, 78917x(A), 78917xY(A))

(T_A = –40 to +85°C, 1.8 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	12		100	μs
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	28		100	μs
Zero-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Full-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Integral linearity error[Note]	INL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±4.5	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±8.5	LSB
Differential linearity error[Note]	DNL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full scale range

Data Memory STOP Mode Low Power Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

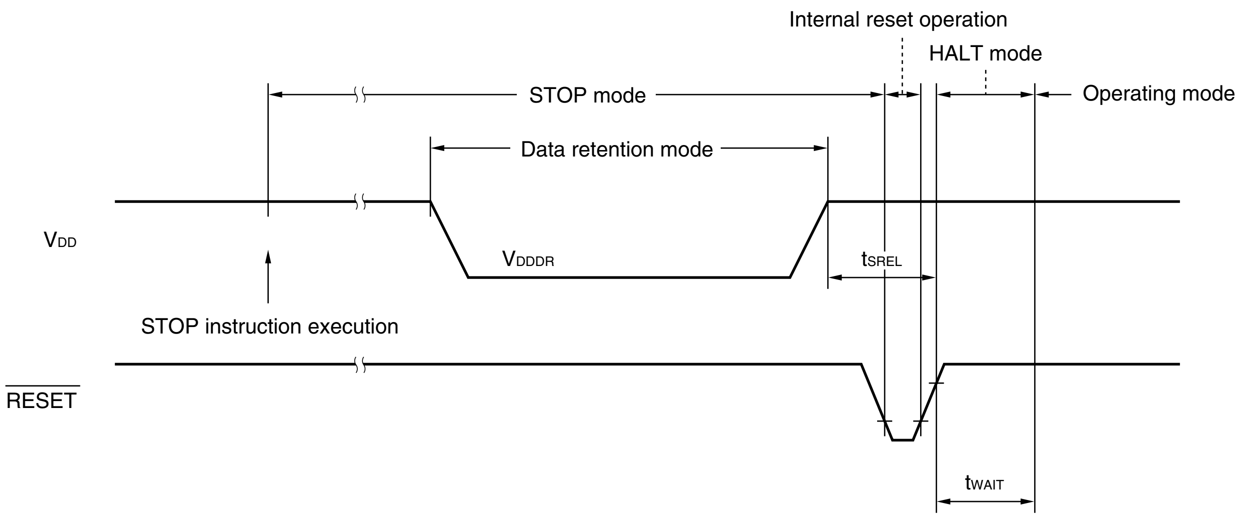
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time Note 1	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.

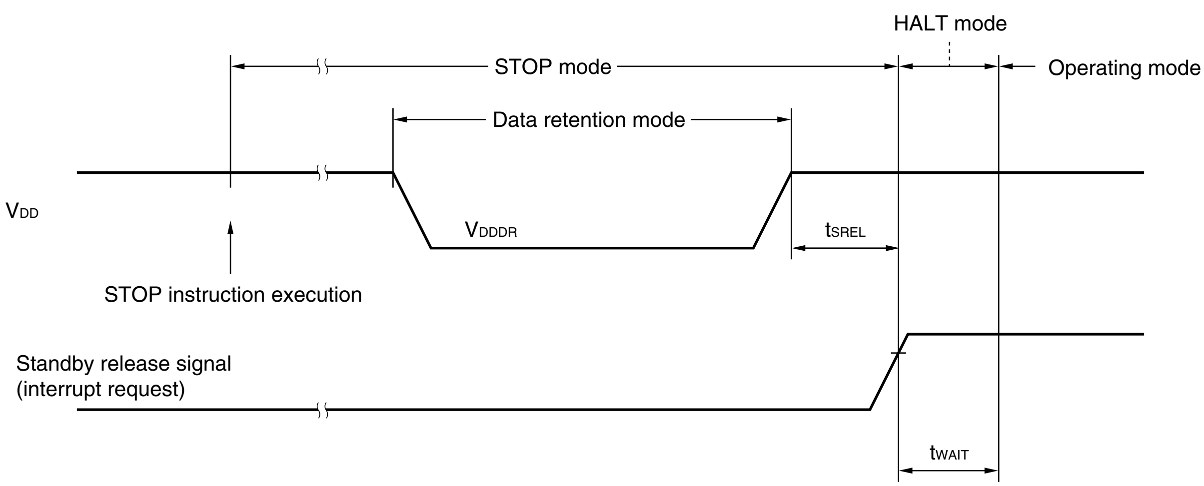
2. By using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS), $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected.

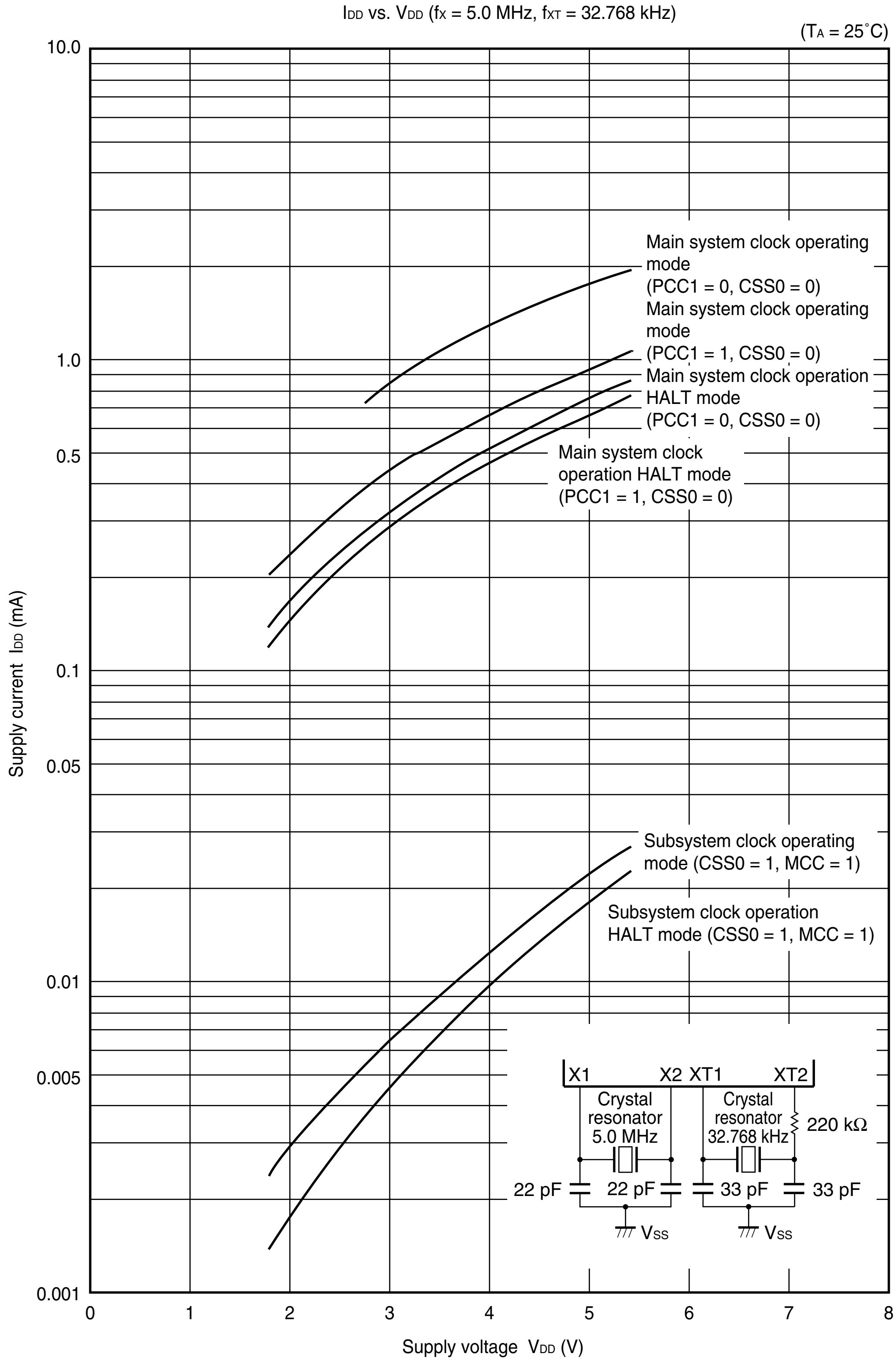
Remark fx: Main system clock oscillation frequency

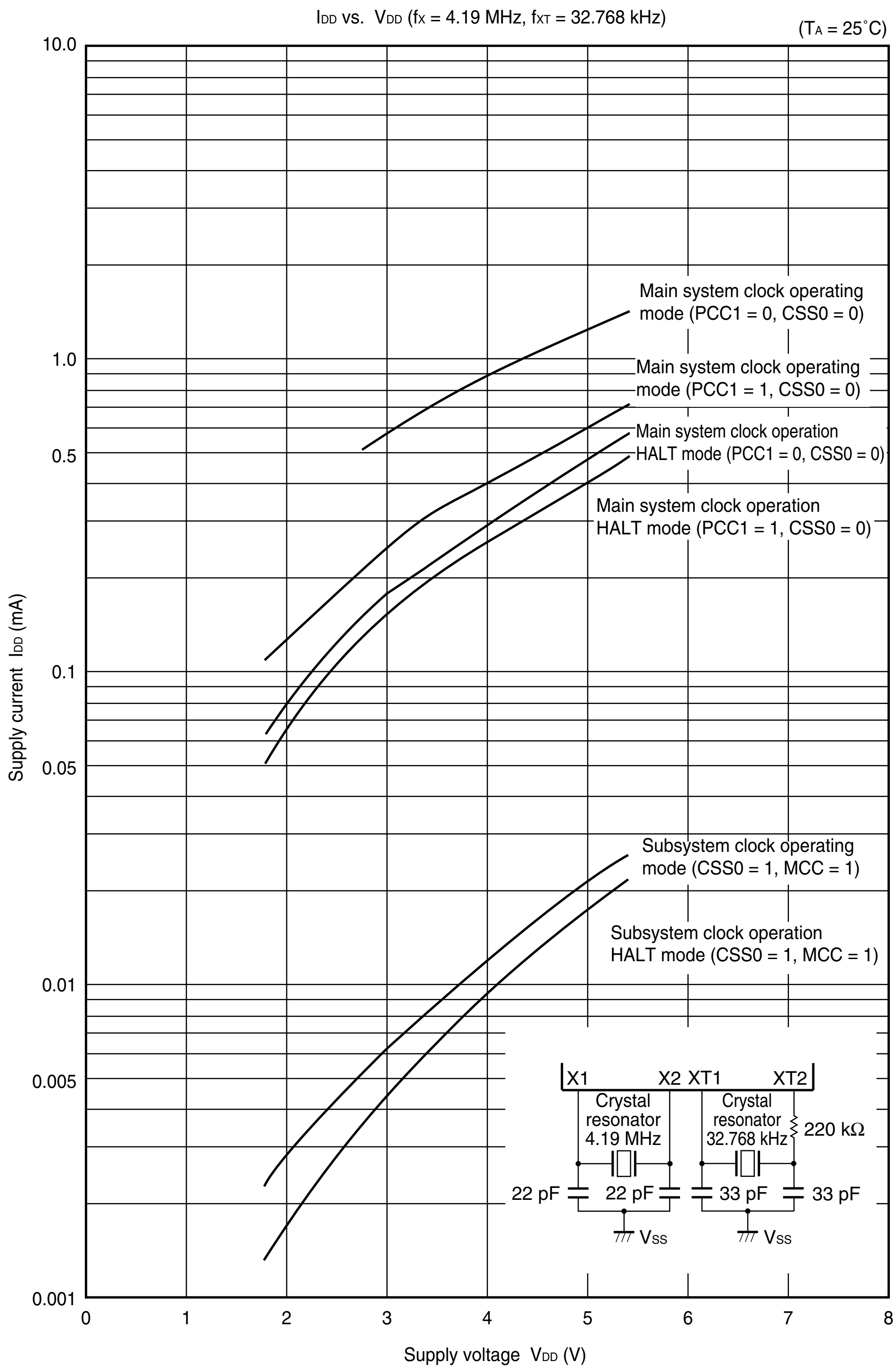
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

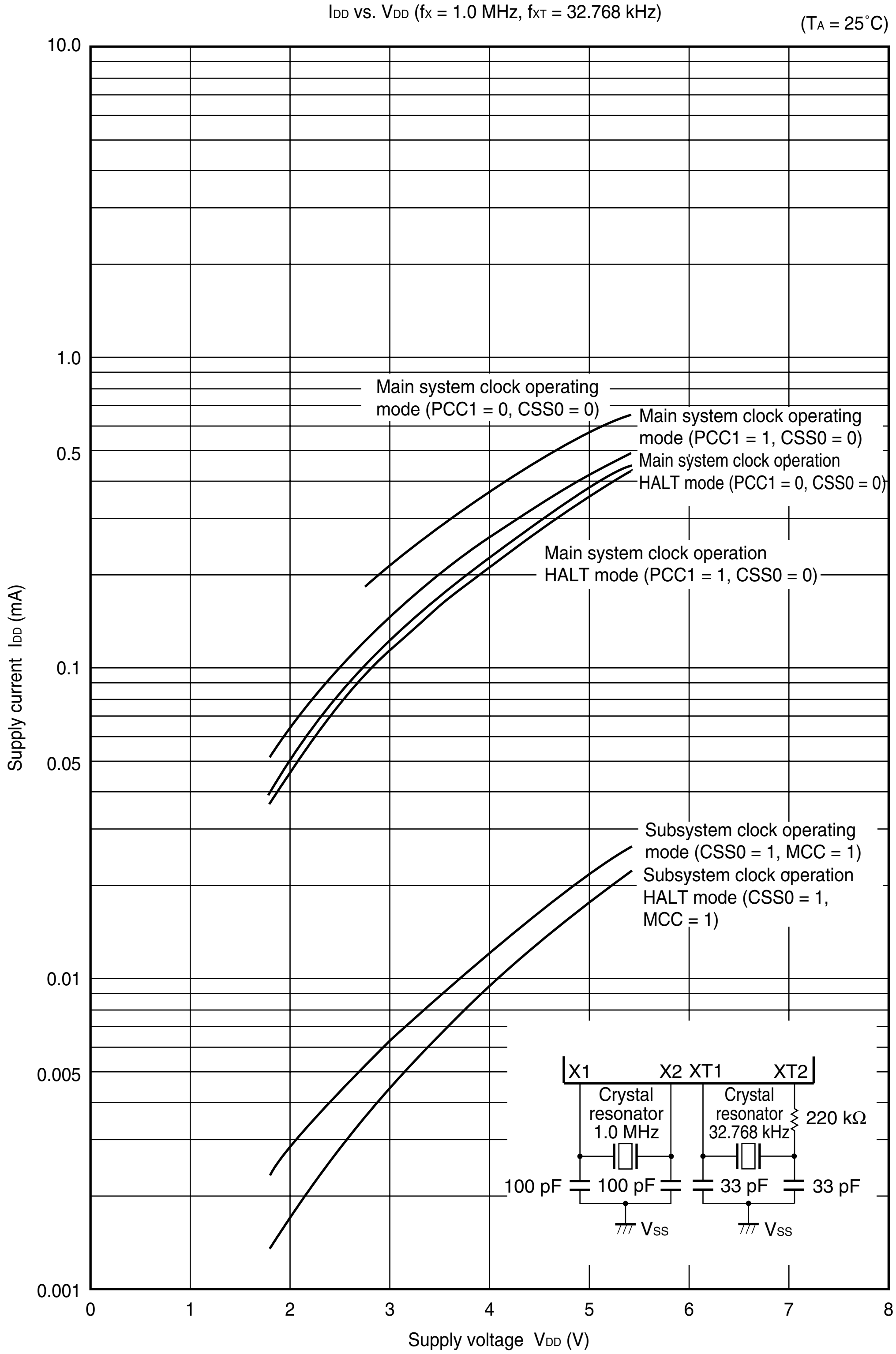


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)




IDD vs. VDD (fX = 5.0 MHz, fXT = 32.768 kHz)
(TA = 25˚C)
Supply current IDD (mA)
10.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
8
Supply voltage VDD (V)
Main system clock operating mode (PCC1 = 0, CSS0 = 0)
Main system clock operating mode (PCC1 = 1, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 0, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 1, CSS0 = 0)
Subsystem clock operating mode (CSS0 = 1, MCC = 1)
Subsystem clock operation HALT mode (CSS0 = 1, MCC = 1)
X1
X2
XT1
XT2
Crystal resonator 5.0 MHz
Crystal resonator 32.768 kHz
220 kΩ
22 pF
22 pF
33 pF
33 pF
VSS
VSS


IDD vs. VDD (fX = 4.19 MHz, fXT = 32.768 kHz)
(TA = 25°C)
10.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
8
Supply current IDD (mA)
Supply voltage VDD (V)
Main system clock operating mode (PCC1 = 0, CSS0 = 0)
Main system clock operating mode (PCC1 = 1, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 0, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 1, CSS0 = 0)
Subsystem clock operating mode (CSS0 = 1, MCC = 1)
Subsystem clock operation HALT mode (CSS0 = 1, MCC = 1)
X1
X2
XT1
XT2
Crystal resonator 4.19 MHz
Crystal resonator 32.768 kHz
220 kΩ
22 pF
22 pF
33 pF
33 pF
VSS
VSS


IDD vs. VDD (fX = 1.0 MHz, fXT = 32.768 kHz)
(TA = 25°C)
10.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
8
Supply current IDD (mA)
Supply voltage VDD (V)
Main system clock operating mode (PCC1 = 0, CSS0 = 0)
Main system clock operating mode (PCC1 = 1, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 0, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 1, CSS0 = 0)
Subsystem clock operating mode (CSS0 = 1, MCC = 1)
Subsystem clock operation HALT mode (CSS0 = 1, MCC = 1)
X1
X2 XT1
XT2
Crystal resonator 1.0 MHz
Crystal resonator 32.768 kHz
220 kΩ
100 pF
100 pF
33 pF
33 pF
VSS
VSS

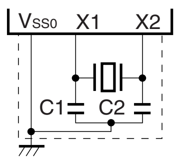
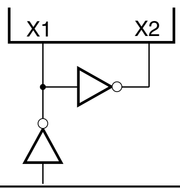
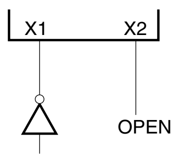
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}	AV_{DD} – 0.3 V ≤ V_{DD} ≤ AV_{DD} + 0.3 V		–0.3 to +6.5	V
	AV_{DD}	AV_{REF} ≤ AV_{DD} + 0.3 V			V
	AV_{REF}	AV_{REF} ≤ V_{DD} + 0.3 V			V
Input voltage	V_{I1}	Pins other than P50 to P53, P23, P24		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P23, P24		–0.3 to +5.5	V
	V_{I3}	P50 to P53	N-ch open drain	–0.3 to +13	V
			On-chip pull-up resistor	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78916x(A1), 78917x(A1)	–4	mA
		Total for all pins		–14	mA
		Per pin	μPD78916x(A2), 78917x(A2)	–2	mA
		Total for all pins		–6	mA
Output current, low	I_{OL}	Per pin	μPD78916x(A1), 78917x(A1)	5	mA
		Total for all pins		80	mA
		Per pin	μPD78916x(A2), 78917x(A2)	2	mA
		Total for all pins		40	mA
Operating ambient temperature	T_A	μPD78916x(A1), 78917x(A1)		–40 to +110	°C
		μPD78916x(A2), 78917x(A2)		–40 to +125	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics
(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

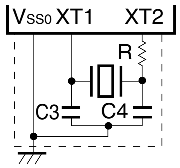
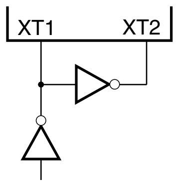
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

3. For ceramic resonator, use the part number for which the resonator manufacturer guarantees operation under the following conditions.
μPD78916x(A1), 78917x(A1): T_A = 110°C
μPD78916x(A2), 78917x(A2): T_A = 125°C

Remark For the resonator selection and oscillator constant, users are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics
(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2			1.2	2	s
External clock		XT1 input frequency (f_{XT})Note 1		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, users are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2))) (1/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78916x(A1), 78917x(A1)			–1	mA
		Total for all pins				–7	mA
		Per pin	μPD78916x(A2), 78917x(A2)			–1	mA
		Total for all pins				–3	mA
Output current, low	I_{OL}	Per pin	μPD78916x(A1), 78917x(A1)			1.6	mA
		Total for all pins				40	mA
		Per pin	μPD78916x(A2), 78917x(A2)			1.6	mA
		Total for all pins				20	mA
Input voltage, high	V_{IH1}	P00 to P05, P10, P11, P60 to P67		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	P50 to P53	N-ch open drain	$0.7V_{DD}$		10	V
			On-chip pull-up resistor	$0.7V_{DD}$		V_{DD}	V
	V_{IH3}	$\overline{RESET}$, P20 to P26, P30 to P33		$0.8V_{DD}$		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P05, P10, P11, P60 to P67		0		$0.3V_{DD}$	V
	V_{IL2}	P50 to P53		0		$0.3V_{DD}$	V
	V_{IL3}	$\overline{RESET}$, P20 to P26, P30 to P33		0		$0.2V_{DD}$	V
	V_{IL4}	X1, X2, XT1, XT2		0		0.1	V
Output voltage, high	V_{OH}	Pins other than P23, P24, P50 to P53	I_{OH} = –1 mA	V_{DD} – 2.0			V
			I_{OH} = –100 μA	V_{DD} – 1.0			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	I_{OL} = 1.6 mA			2.0	V
			I_{OL} = 400 μA			1.0	V
	V_{OL2}	P50 to P53	I_{OL} = 1.6 mA			1.0	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2))) (2/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_I = V_{DD}$	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			10	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 10 V[Note1]	P50 to P53 (N-ch open drain)			80	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			–10	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–10[Note 2]	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–10	μA
Software pull-up resistor	R_1	V_I = 0 V, for pins other than P23, P24, and P50 to P53		50	100	300	kΩ
Mask option pull-up resistor	R_2	V_I = 0 V, P50 to P53	μPD78916x(A1), 78917x(A1)	15	30	100	kΩ
			μPD78916x(A2), 78917x(A2)	10	30	100	kΩ

Notes 1. When pull-up resistors are not connected to P50 to P53 (specified by mask option).

2. A low-level input leakage current of –60 μA (MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 when on-chip pull-up resistors are not connected to P50 to P53 (specified by mask option) and P50 to P53 are set to input mode. At times other than this, a –10 μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2))) (3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1} Note 1	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		2.0	8.0	mA
	I_{DD2} Note 1	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		1.0	5.0	mA
	I_{DD3} Note 1	32.768 kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ±10%		30	1200	μA
	I_{DD4} Note 1	32.768 kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ±10%		25	1100	μA
	I_{DD5} Note 1	32.768 kHz crystal stop STOP mode	V_{DD} = 5.0 V ± 10%		0.1	1000	μA
	I_{DD6} Note 2	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		3.0	10.0	mA

Notes 1. The AV_{REF}ON (ADCS0 (bit 7 of ADM0; A/D converter mode register 0) = 1), AV_{DD}, and port current (including the current flowing through the internal pull-up resistors) is not included.

2. The AV_{REF}ON (ADCS0 =1) and port current (including the current flowing through the internal pull-up resistors) is not included. Refer to the A/D converter characteristics for the current flowing through AV_{REF}.

3. When the main system clock is stopped.

4. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H.)

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

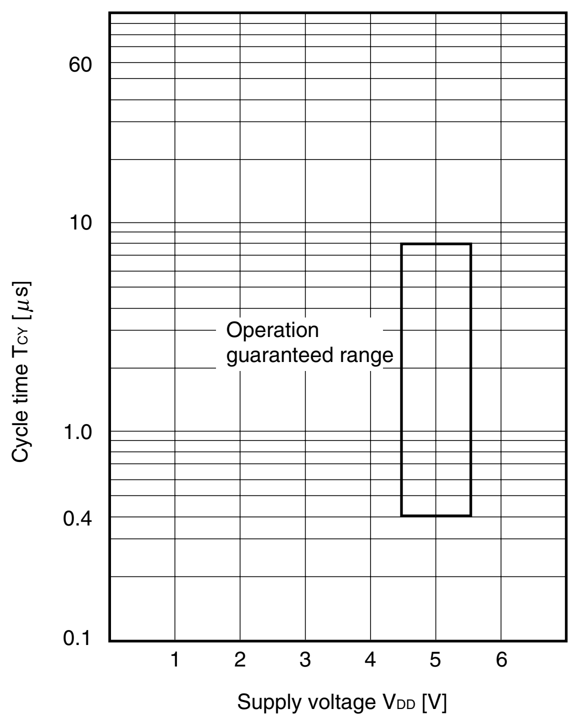
AC Characteristics

(1) Basic operation

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operation based on the main system clock	0.4		8	μs
		Operation based on the subsystem clock	114	122	125	μs
TI80 and TI81 input frequency	f_{TI}		0		4	MHz
TI80 and TI81 input high-/low-level width	t_{TIH}, t_{TIL}		0.1			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3	10			μs
$\overline{RESET}$ input low-level width	t_{RSL}		10			μs
CPT90 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs. V_{DD} (main system clock)



(2) Serial interface 20

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

(a) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 – 50			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK1}		150			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI1}		400			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	0		250	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode ($\overline{SCK20}$...External clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}		900			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK2}		100			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI2}		400			ns
SO20 output delay time from $\overline{SCK20}$ ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns
SO20 setup time (when using $\overline{SS20}$, to $\overline{SS20}$ ↓)	t_{KAS2}				120	ns
SO20 disable time (when using $\overline{SS20}$, from $\overline{SS20}$ ↑)	t_{KDS2}				240	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

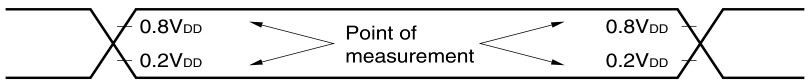
(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					78125	bps

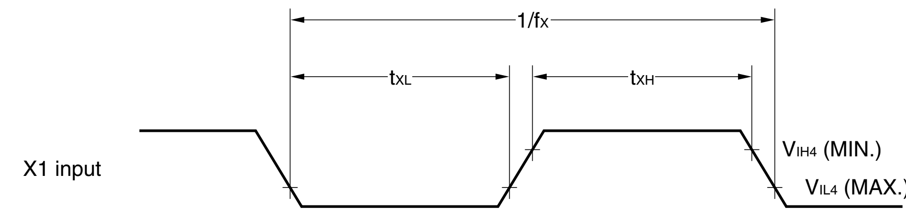
(d) UART mode (external clock input)

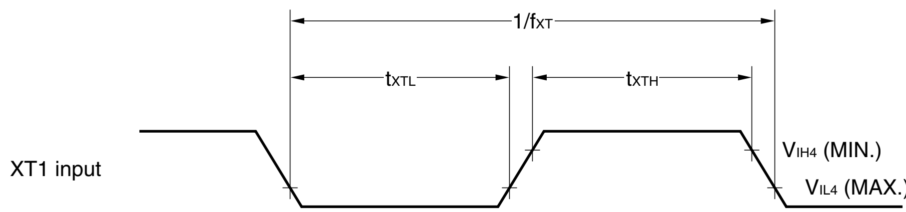
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}		900			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}		400			ns
Transfer rate					39063	bps
ASCK20 rise time, fall time	t_R, t_F				1	μs

AC Timing Measurement Points (Excluding X1 and XT1 Inputs)

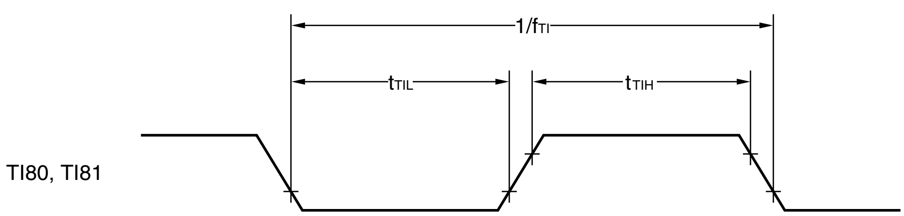


Clock Timing

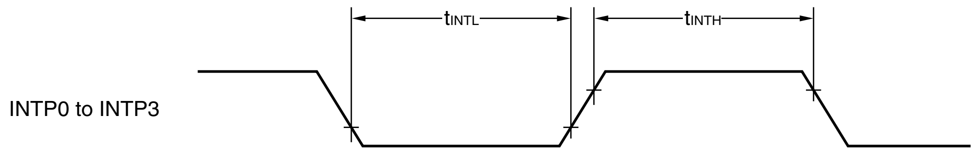




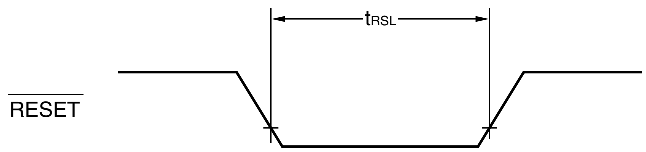
TI Timing



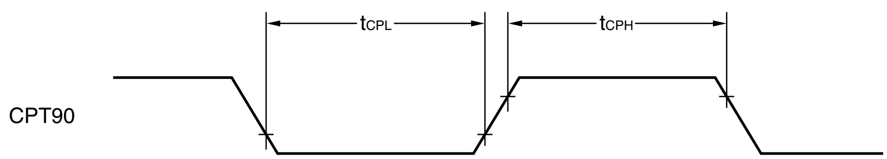
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing

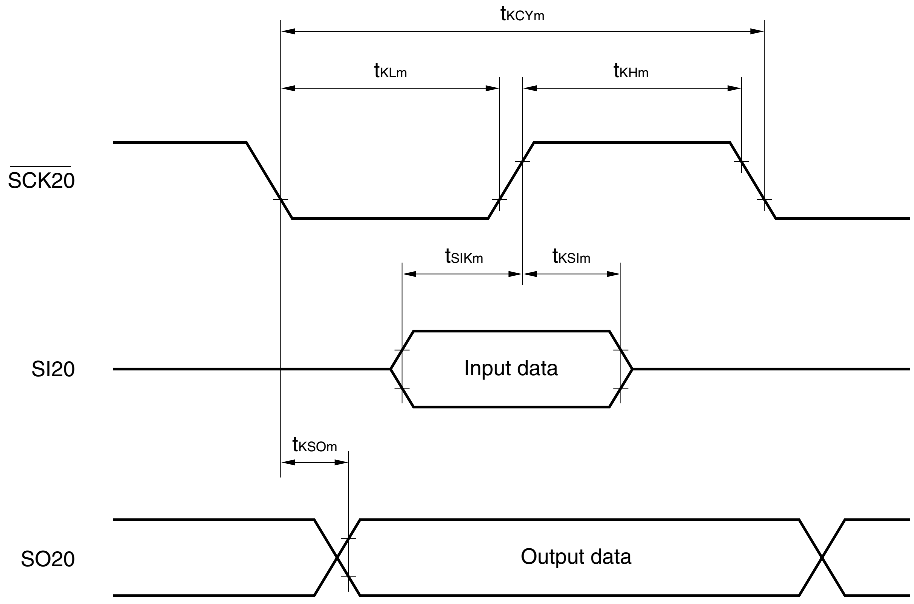


CPT90 Input Timing



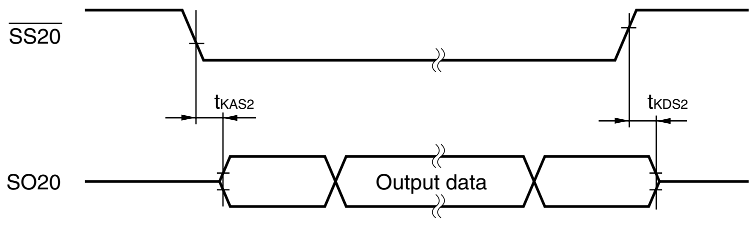
Serial Transfer Timing

3-wire serial I/O mode:

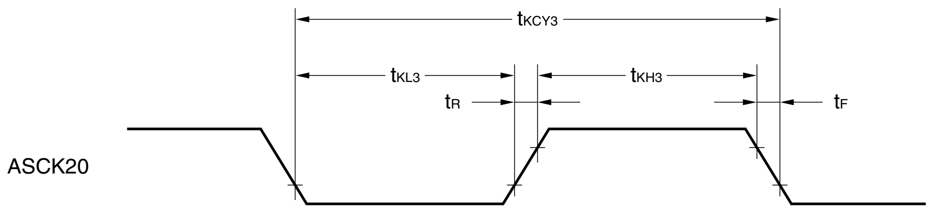


Remark m = 1, 2

3-wire serial I/O mode (when using $\overline{SS20}$):



UART mode (external clock input):



8-Bit A/D Converter Characteristics (μPD78916x(A1), 78916x(A2))
(T_A = –40 to +110°C (μPD78916x(A1)), –40 to +125°C (μPD78916x(A2))
4.5 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]				±0.4	±1.0	%FSR
Conversion time	t_{CONV}		14		28	μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.2%FSR).

Remark FSR: Full scale range

10-Bit A/D Converter Characteristics (μPD78917x(A1), 78917x(A2))
(T_A = –40 to +110°C (μPD78917x(A1)), –40 to +125°C (μPD78917x(A2))
4.5 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]				±0.2	±0.6	%FSR
Conversion time	t_{CONV}		14		28	μs
Zero-scale error[Note]					±0.6	%FSR
Full-scale error[Note]					±0.6	%FSR
Integral linearity error[Note]	INL				±4.5	LSB
Differential linearity error[Note]	DNL				±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full scale range

Data Memory STOP Mode Low Power Supply Voltage Data Retention Characteristics
(T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

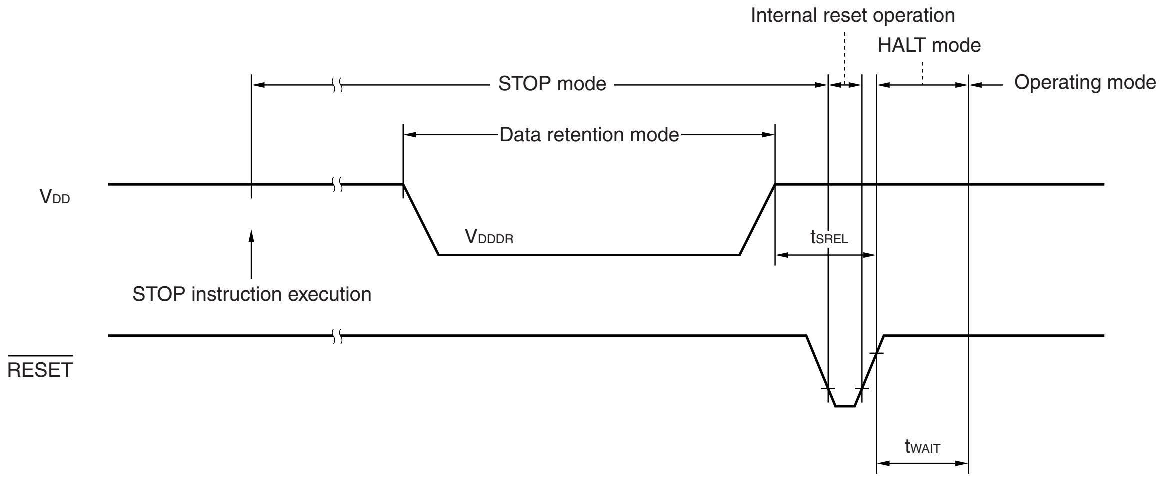
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		4.5		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.

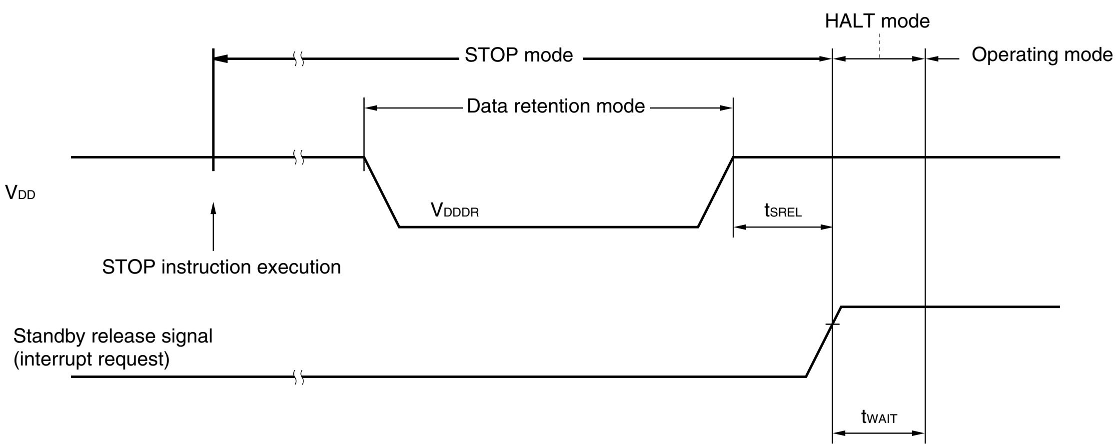
2. $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected by using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

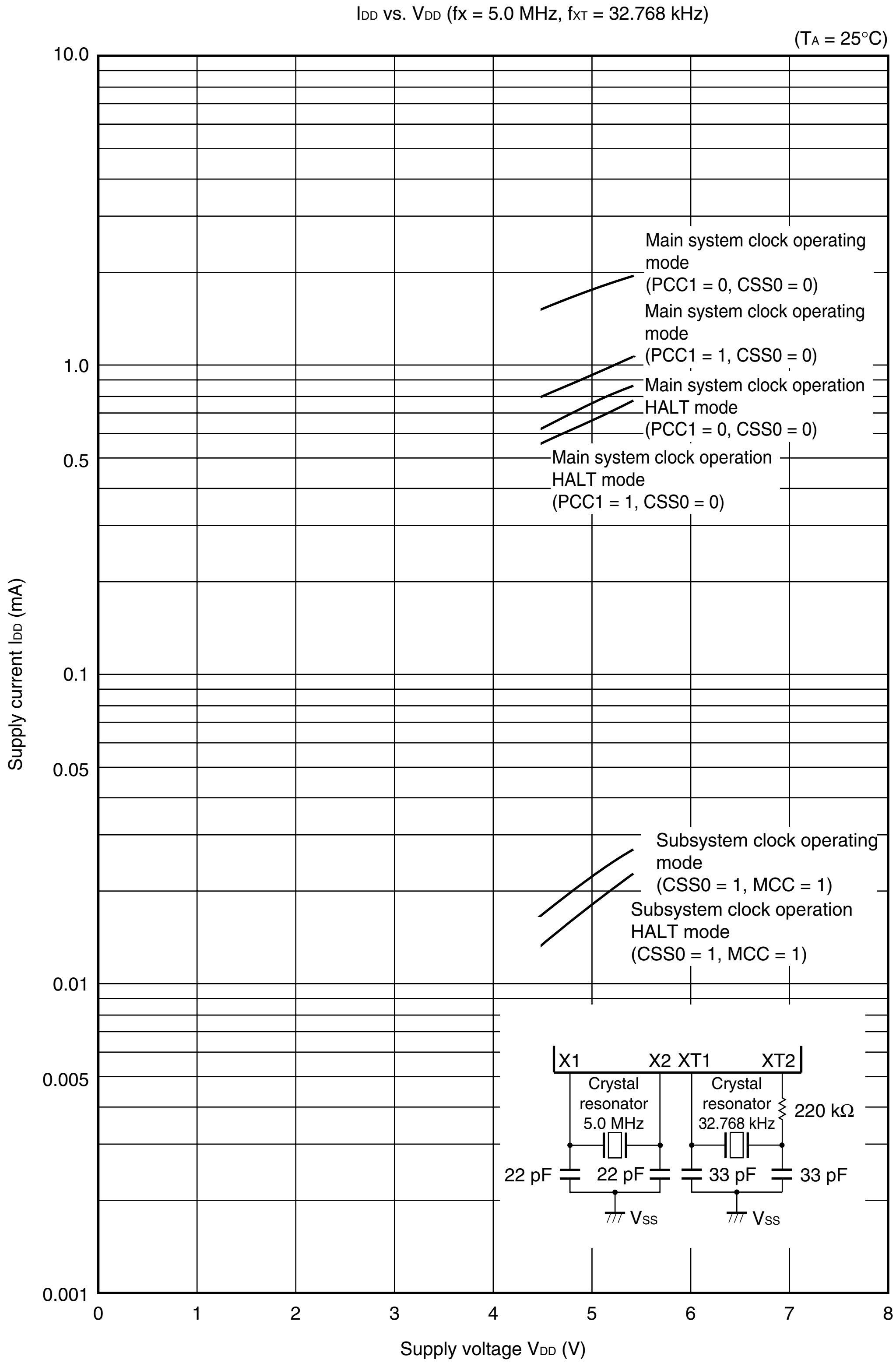
Remark f_X: Main system clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

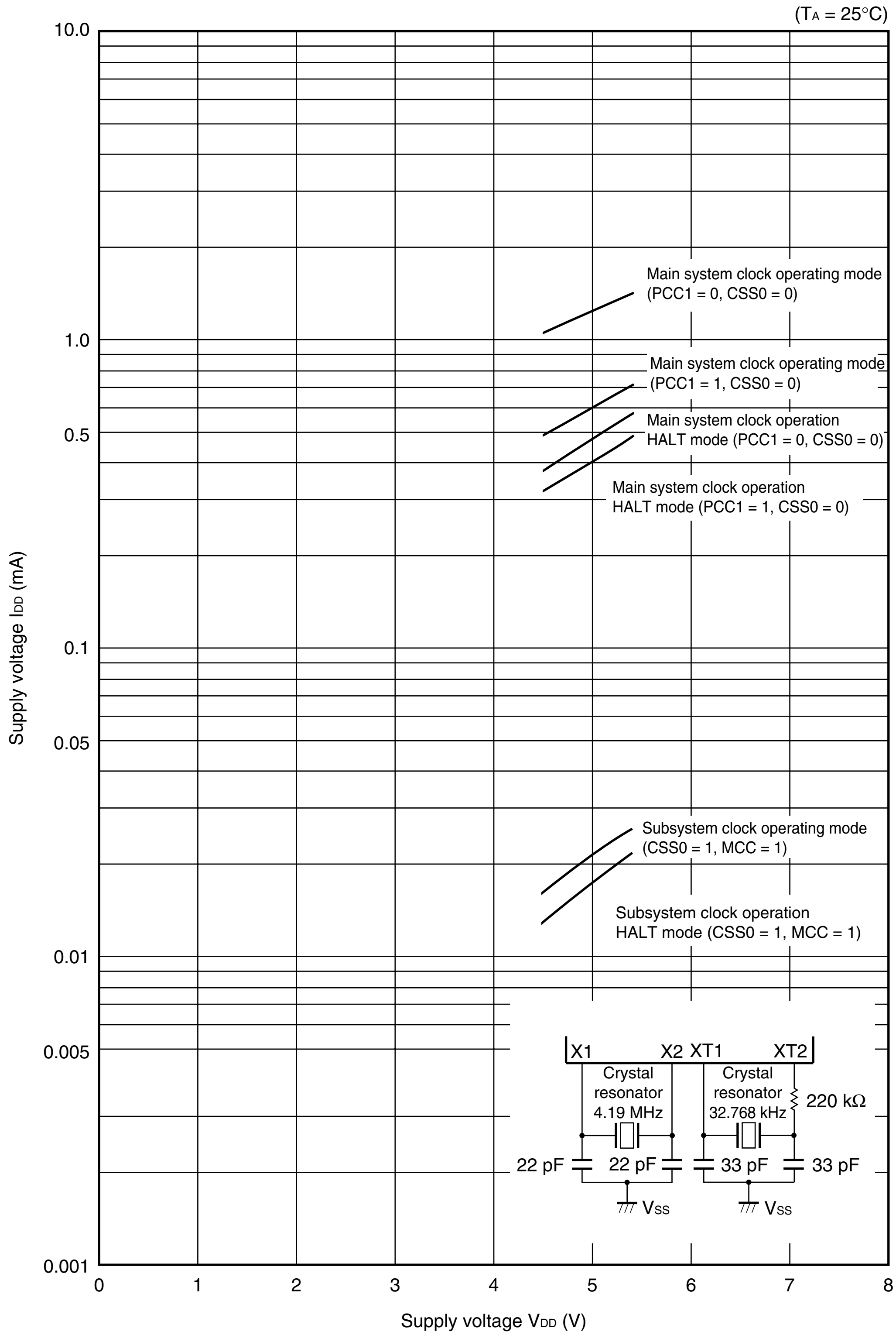


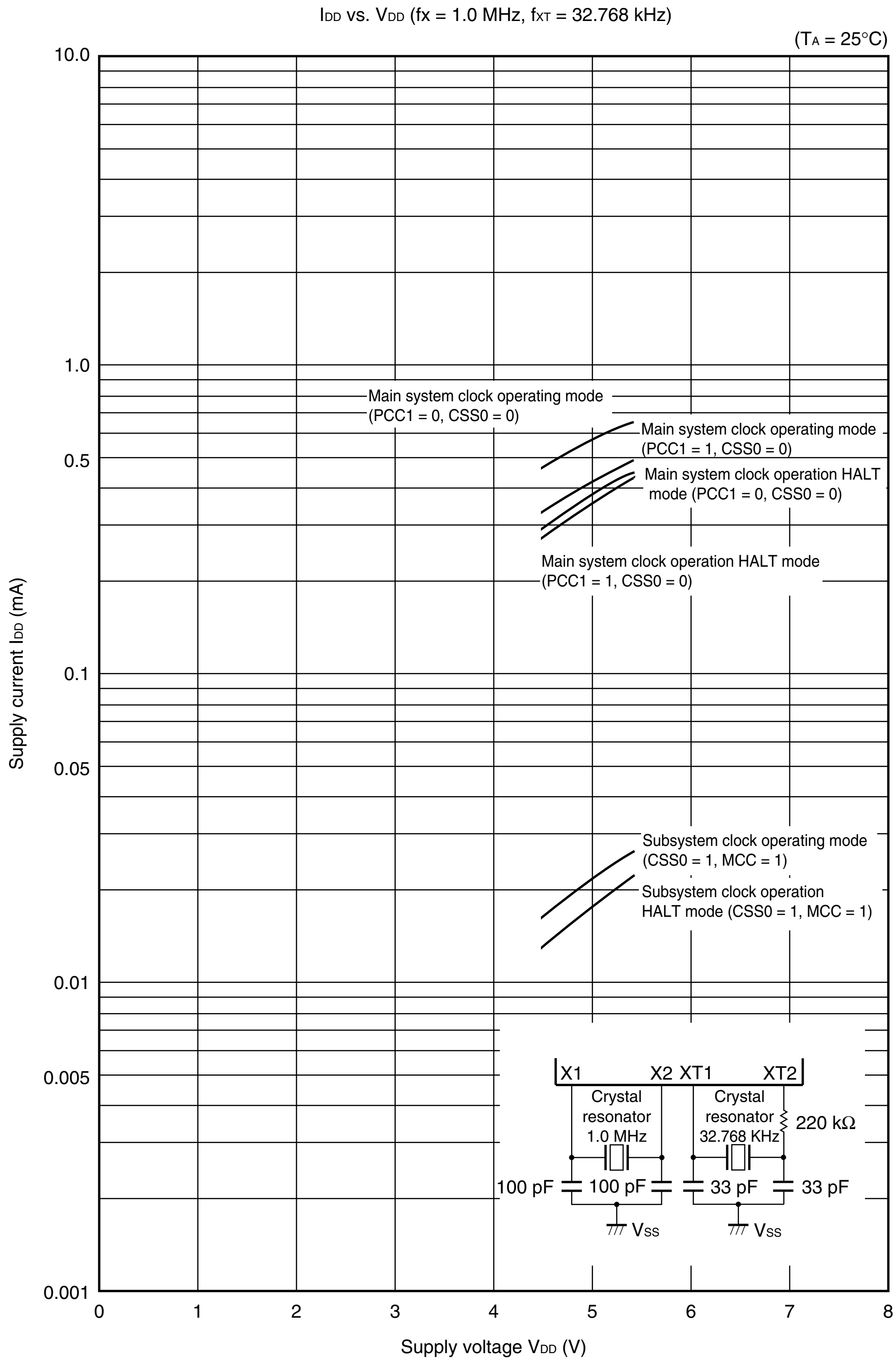
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)




IDD vs. VDD (fx = 5.0 MHz, fXT = 32.768 kHz)
(TA = 25°C)
10.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
8
Supply current IDD (mA)
Supply voltage VDD (V)
Main system clock operating mode (PCC1 = 0, CSS0 = 0)
Main system clock operating mode (PCC1 = 1, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 0, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 1, CSS0 = 0)
Subsystem clock operating mode (CSS0 = 1, MCC = 1)
Subsystem clock operation HALT mode (CSS0 = 1, MCC = 1)
X1
X2 XT1
XT2
Crystal resonator 5.0 MHz
Crystal resonator 32.768 kHz
220 kΩ
22 pF
22 pF
33 pF
33 pF
VSS
VSS

I_{DD} vs. V_{DD} (f_X = 4.19 MHz, f_{XT} = 32.768 kHz)



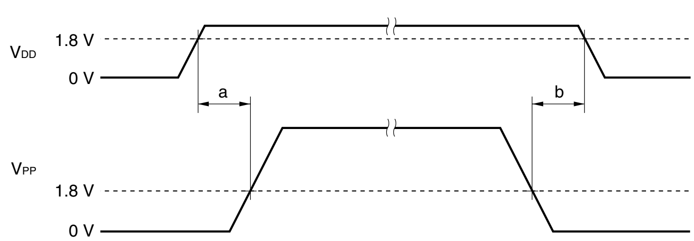

IDD vs. VDD (fx = 1.0 MHz, fXT = 32.768 kHz)
(TA = 25°C)
10.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
8
Supply current IDD (mA)
Supply voltage VDD (V)
Main system clock operating mode (PCC1 = 0, CSS0 = 0)
Main system clock operating mode (PCC1 = 1, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 0, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 1, CSS0 = 0)
Subsystem clock operating mode (CSS0 = 1, MCC = 1)
Subsystem clock operation HALT mode (CSS0 = 1, MCC = 1)
X1
X2 XT1
XT2
Crystal resonator 1.0 MHz
Crystal resonator 32.768 KHz
220 kΩ
100 pF
100 pF
33 pF
33 pF
VSS
VSS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}	AV_{DD} – 0.3 V ≤ V_{DD} ≤ AV_{DD} + 0.3 V		–0.3 to +6.5	V
	AV_{DD}	AV_{REF} ≤ AV_{DD} + 0.3 V			V
	AV_{REF}	AV_{REF} ≤ V_{DD} + 0.3 V			V
	V_{PP}	**Note**		–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P50 to P53, P23, P24		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P23, P24		–0.3 to +5.5	V
	V_{I3}	P50 to P53		–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	µPD78F9177A, µPD78F9177AY	–10	mA
		Total for all pins		–30	mA
		Per pin	µPD78F9177A(A), µPD78F9177AY(A)	–7	mA
		Total for all pins		–22	mA
Output current, low	I_{OL}	Per pin	µPD78F9177A, µPD78F9177AY	30	mA
		Total for all pins		160	mA
		Per pin	µPD78F9177A(A), µPD78F9177AY(A)	10	mA
		Total for all pins		120	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		During flash memory programming		+10 to +40	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

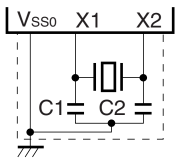
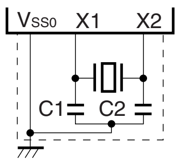
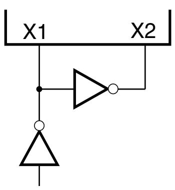
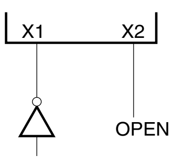
- **When supply voltage rises**
  V_{PP} must exceed V_{DD} 10 µs or more after V_{DD} has reached the lower-limit value (1.8 V) of the operating voltage range (see **a** in the figure below).
- **When supply voltage drops**
  V_{DD} must be lowered 10 µs or more after V_{PP} falls below the lower-limit value (1.8 V) of the operating voltage range of V_{DD} (see **b** in the figure below).



Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
			V_{DD} = 1.8 to 5.5 V			30	ms
External clock		X1 input frequency (f_X) Note 1	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.5 to 5.5 V	45		500	ns
			V_{DD} = 3.0 to 5.5 V	75		500	ns
			V_{DD} = 1.8 to 5.5 V	85		500	ns
		X1 input frequency (f_X) Note 1	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Recommended Oscillator Constant (μPD78F9177A and 78F9177AY)

Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remarks
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd. (Standard type)	CSBLA1M00J58-B0	1.000	150	150	2.4	5.5	Without on-chip capacitor
	CSBFB1M00J58-R1						
	CSTCC2M00G56-R0	2.000	–	–	1.8	5.5	With on-chip capacitor
	CSTLS2M00G56-B0						
	CSTCR4M00G53-R0	4.000					
	CSTLS4M00G53-B0				1.9	5.5	
	CSTCR4M19G53-R0	4.195			1.8	5.5	
	CSTLS4M19G53-B0				1.9	5.5	
	CSTCR4M91G53-R0	4.915					
	CSTLS4M91G53-B0				2.1	5.5	
	CSTCR5M00G53-R0	5.000			1.9	5.5	
	CSTLS5M00G53-B0				2.1	5.5	
	CSTCR6M00G53-R0	6.000			1.9	5.5	
	CSTLS6M00G53-B0				2.1	5.5	
	CSTCE8M00G52-R0	8.000			1.8	5.5	
	CSTLS8M00G53-B0				2.0	5.5	
	CSTCE8M38G52-R0	8.388			1.8	5.5	
	CSTLS8M38G53-B0				2.0	5.5	
	CSTCE10M0G52-R0	10.000					
	CSTLS10M0G53-B0				2.2	5.5	
Murata Mfg. Co., Ltd. (Low-voltage drive type)	CSTLS4M00G53093-B0	4.000	–	–	1.8	5.5	With on-chip capacitor
	CSTLS4M19G53093-B0	4.195					
	CSTCR4M91G53093-R0	4.915					
	CSTLS4M91G53U-B0						
	CSTCR5M00G53093-R0	5.000					
	CSTLS5M00G53U-B0						
	CSTCR6M00G53093-R0	6.000					
	CSTLS6M00G53U-B0						
	CSTLS8M00G53U-B0	8.000					
	CSTLS8M38G53U-B0	8.388					
	CSTLS10M0G53U-B0	10.000					

Caution The oscillator constant is a reference value based on evaluation in specific environments by the resonator manufacturer. If the oscillator characteristics need to be optimized in the actual application, request the resonator manufacturer for evaluation on the implementation circuit. Note that the oscillation voltage and oscillation frequency merely indicate the characteristics of the oscillator. Use the internal operation conditions of the μPD78F9177A and 78F9177AY within the specifications of the DC and AC characteristics.

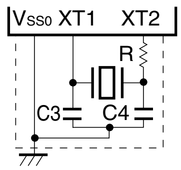
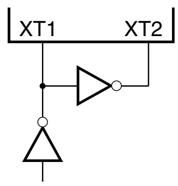
Recommended Oscillator Constant (μPD78F9177A(A) and 78F9177AY(A))

Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remarks
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd. (Standard type)	CSTCC2M00G56A-R0	2.000	–	–	1.8	5.5	With on-chip capacitor
	CSTCR4M00G53A-R0	4.000					
	CSTCR4M19G53A-R0	4.195					
	CSTCR4M91G53A-R0	4.915			1.9	5.5	
	CSTCR5M00G53A-R0	5.000					
	CSTCR6M00G53A-R0	6.000					
	CSTCE8M00G52A-R0	8.000			1.8	5.5	
	CSTCE8M38G52A-R0	8.388					
	CSTCE10M0G52A-R0	10.000			2.0	5.5	
Murata Mfg. Co., Ltd. (Low-voltage drive type)	CSTCR4M91G53A093-R0	4.915	–	–	1.8	5.5	With on-chip capacitor
	CSTCR5M00G53A093-R0	5.000					
	CSTCR6M00G53A093-R0	6.000					

Caution The oscillator constant is a reference value based on evaluation in specific environments by the resonator manufacturer. If the oscillator characteristics need to be optimized in the actual application, request the resonator manufacturer for evaluation on the implementation circuit. Note that the oscillation voltage and oscillation frequency merely indicate the characteristics of the oscillator. Use the internal operation conditions of the μPD78F9177A(A) and 78F9177AY(A) within the specifications of the DC and AC characteristics.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})^Note 1^		32	32.768	35	kHz
		Oscillation stabilization time^Note 2^	V_{DD} = 4.5 to 5.5 V		1.2	2	s
			V_{DD} = 1.8 to 5.5 V			10	s
External clock		XT1 input frequency (f_{XT})^Note 1^		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation stabilization wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78F9177A, μPD78F9177AY			–1	mA
		Total for all pins				–15	mA
		Per pin	μPD78F9177A(A), μPD78F9177AY(A)			–1	mA
		Total for all pins				–11	mA
Output current, low	I_{OL}	Per pin	μPD78F9177A, μPD78F9177AY			10	mA
		Total for all pins				80	mA
		Per pin	μPD78F9177A(A), μPD78F9177AY(A)			3	mA
		Total for all pins				60	mA
Input voltage, high	V_{IH1}	P00 to P05, P10, P11,P60 to P67	V_{DD} = 2.7 to 5.5 V	$0.7V_{DD}$		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	$0.9V_{DD}$		V_{DD}	V
	V_{IH2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	$0.7V_{DD}$		12	V
			V_{DD} = 1.8 to 5.5 V	$0.9V_{DD}$		12	V
	V_{IH3}	$\overline{RESET}$, P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	$0.8V_{DD}$		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	$0.9V_{DD}$		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P05, P10, P11, P60 to P67	V_{DD} = 2.7 to 5.5 V	0		$0.3V_{DD}$	V
			V_{DD} = 1.8 to 5.5 V	0		$0.1V_{DD}$	V
	V_{IL2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0		$0.3V_{DD}$	V
			V_{DD} = 1.8 to 5.5 V	0		$0.1V_{DD}$	V
	V_{IL3}	$\overline{RESET}$,P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0		$0.2V_{DD}$	V
			V_{DD} = 1.8 to 5.5 V	0		$0.1V_{DD}$	V
	V_{IL4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
			V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH}	Pins other than P23, P24, P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78F9177A, μPD78F9177AY) V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78F9177(A), μPD78F9177AY(A))			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78F9177A, μPD78F9177AY) V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78F9177(A), μPD78F9177AY(A))			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
Input leakage current, high	I_{LIH1}	$V_I = V_{DD}$	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–3 Note	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistor	R_1	V_I = 0 V, for pins other than P23, P24, and P50 to P53		50	100	200	kΩ

Note A low-level input leakage current of –60 μA (MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 and P50 to P53 are set to input mode. At times other than this, –3 μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1} Note 1	10.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10% Note 4		10.0	20.0	mA
		6.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10% Note 4		6.0	12.0	mA
		5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10% Note 4		5.0	10.0	mA
			V_{DD} = 3.0 V ± 10% Note 5		1.2	2.5	mA
			V_{DD} = 2.0 V ± 10% Note 5		1.0	2.0	mA
	I_{DD2} Note 1	10.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10% Note 4		1.2	6.0	mA
		6.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10% Note 4		0.9	2.8	mA
		5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10% Note 4		0.8	2.5	mA
			V_{DD} = 3.0 V ± 10% Note 5		0.4	2.0	mA
			V_{DD} = 2.0 V ± 10% Note 5		0.25	1.5	mA
	I_{DD3} Note 1	32.768 kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ± 10%		100	320	μA
			V_{DD} = 3.0 V ± 10%		80	240	μA
			V_{DD} = 2.0 V ± 10%		65	210	μA
	I_{DD4} Note 1	32.768 kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ± 10%		18	120	μA
			V_{DD} = 3.0 V ± 10%		5.0	50	μA
			V_{DD} = 2.0 V ± 10%		2.5	30	μA
	I_{DD5} Note 1	32.768 kHz crystal stop STOP mode	V_{DD} = 5.0 V ± 10%		0.1	30	μA
			V_{DD} = 3.0 V ± 10%		0.05	10	μA
			V_{DD} = 2.0 V ± 10%		0.05	10	μA
	I_{DD6} Note 2	10.0 MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V ± 10% Note 4		10.8	22.0	mA
		6.0 MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V ± 10% Note 4		6.8	14.0	mA
		5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10% Note 4		5.8	12.0	mA
			V_{DD} = 3.0 V ± 10% Note 5		2.0	4.5	mA
			V_{DD} = 2.0 V ± 10% Note 5		1.8	4.0	mA

Notes 1. The $AV_{REF}ON$ (ADCS0 (bit 7 of ADM0; A/D converter mode register 0) = 1), AV_{DD}, and the port current (including the current flowing through the internal pull-up resistors) are not included.

2. The $AV_{REF}ON$ (ADCS0 =1) and port current (including the current flowing through the internal pull-up resistors) are not included. Refer to the A/D converter characteristics for the current flowing through AV_{REF}.

3. When the main system clock is stopped.

4. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H.)

5. During low-speed mode operation (when PCC is set to 02H)

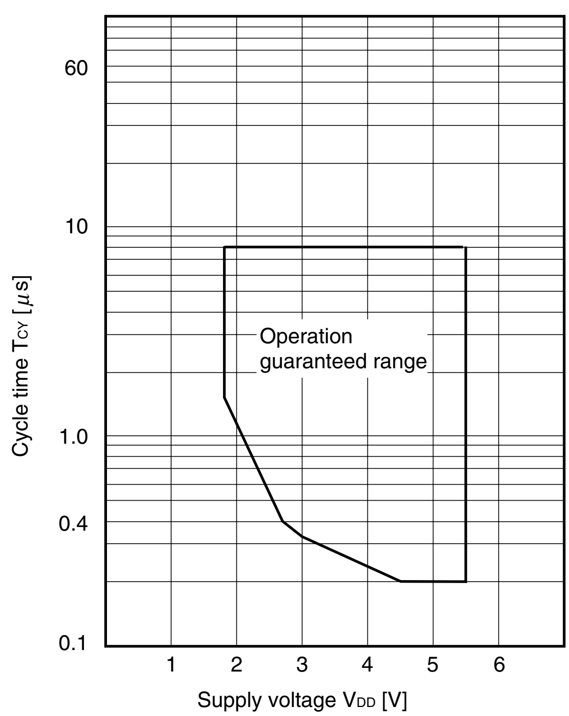
Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operation based on the main system clock	V_{DD} = 4.5 to 5.5 V	0.2		8	μs
			V_{DD} = 3.0 to 5.5 V	0.333		8	μs
			V_{DD} = 2.7 to 5.5 V	0.4		8	μs
			V_{DD} = 1.8 to 5.5 V	1.6		8	μs
		Operation based on the subsystem clock		114	122	125	μs
TI80 and TI81 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
		V_{DD} = 1.8 to 5.5 V		0		275	kHz
TI80 and TI81 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
		V_{DD} = 1.8 to 5.5 V		1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3		10			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}			10			μs
CPT90 input high-/low-level width	t_{CPH}, t_{CPL}			10			μs

T_{CY} vs. V_{DD} (main system clock)



(2) Serial interface SIO20 (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2 – 50			ns
		V_{DD} = 1.8 to 5.5 V		t_{KCY1}/2 – 150			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode ($\overline{SCK20}$...External clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		900			ns
		V_{DD} = 1.8 to 5.5 V		3500			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$ ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (when using $\overline{SS20}$, to $\overline{SS20}$ ↓)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (when using $\overline{SS20}$, from $\overline{SS20}$ ↑)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
		V_{DD} = 1.8 to 5.5 V	3500			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise time, fall time	t_R, t_F				1	μs

(3) Serial interface SMB0 (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (μPD78F9177AY, 78F9177AY(A) only)

(a) DC characteristics

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	SCL0, SDA0 (at hysteresis)		$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	SCL0, SDA0 (at hysteresis)		0		$0.2V_{DD}$	V
Output voltage, low	V_{OL}	SCL0, SDA0	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH}	SCL0, SDA0	$V_I = V_{DD}$			3	μA
Input leakage current, low	I_{LIL}	SCL0, SDA0	V_I = 0 V			–3	μA

(b) DC characteristics (when using comparator)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input range	V_{SDA}, V_{SCL}	V_{DD} = 1.8 to 5.5 V	0		5.5	V
Transfer level	V_{ISDA}, V_{ISCL}	$4.5 \le V_{DD} \le 5.5$ V	$0.72V_{ISMB}$	V_{ISMB}	$1.28V_{ISMB}$	V
		$3.3 \le V_{DD} < 4.5$ V	$0.78V_{ISMB}$	V_{ISMB}	$1.22V_{ISMB}$	V
		$2.7 \le V_{DD} < 3.3$ V	$0.75V_{ISMB}$	V_{ISMB}	$1.25V_{ISMB}$	V
		$1.8 \le V_{DD} < 2.7$ V	$0.90V_{ISMB}$	V_{ISMB}	$1.45V_{ISMB}$	V
Input level threshold value^{Note}	V_{ISMB}	LVL01, LVL00 = 0, 1		$0.25 \times V_{DD}$		V
		LVL01, LVL00 = 1, 0		$0.375 \times V_{DD}$		V
		LVL01, LVL00 = 1, 1		$0.5 \times V_{DD}$		V

Note V_{ISMB} is an input level threshold value selected by bits LVL00 and LVL01 (bits 0 and 1 of SMB input level setting register 0 (SMBVI0)).

According to the SMB standard (V1.1), the maximum value of low-level input voltage is 0.8 V, and the minimum value of high-level input voltage, 2.1 V. To satisfy these conditions, set LVL01 and LVL00 as follows;

- When V_{DD} = 1.8 to 3.3 V: LVL01, LVL00 = 1, 1 ($0.5 \times V_{DD}$)
- When V_{DD} = 3.3 to 4.5 V: LVL01, LVL00 = 1, 0 ($0.375 \times V_{DD}$)
- When V_{DD} = 4.5 to 5.5 V: LVL01, LVL00 = 0, 1 ($0.25 \times V_{DD}$)

"LVL01, LVL00 = 0, 0" is not available since this setting does not satisfy the SMB standard (V1.1).

(c) AC characteristics

Parameter		Symbol	SMB Mode		Standard Mode I²C Bus		High-speed Mode I²C Bus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	10	100	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	–	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	–	4.0	–	0.6	–	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	–	4.7	–	0.6	–	μs
Stop condition setup time		$t_{SU:STO}$	4.0	–	4.0	–	0.6	–	μs
Data hold time	When using CBUS-compatible master	$t_{HD:DAT}$	–	–	5	–	–	–	μs
	When using SMB/IIC bus		300	–	0[Note 2]	–	0[Note 2]	900[Note 3]	ns
Data setup time		$t_{SU:DAT}$	250	–	250	–	100[Note 4]	–	ns
SCL0 clock low-level width		t_{LOW}	4.7	–	4.7	–	1.3	–	μs
SCL0 clock high-level width		t_{HIGH}	4.0	50	4.0	–	0.6	–	μs
SCL0 and SDA0 signal fall time		t_F	–	300	–	300	–	300	ns
SCL0 and SDA0 signal rise time		t_R	–	1000	–	1000	–	300	ns
Spike pulse width controlled by input filter		t_{SP}	–	–	–	–	0	50	ns
Timeout		$t_{TIMEOUT}$	25	35	–	–	–	–	ms
Total extended time of SCL0 clock low-level period (slave)		$t_{LOW:SEXT}$	–	25	–	–	–	–	ms
Total extended time of cumulative clock low-level period (master)		$t_{LOW:MEXT}$	–	10	–	–	–	–	ms
Capacitive load per each bus line		Cb	–	–	–	400	–	400	pF

Notes 1. In the start condition, the first clock pulse is generated after this hold time.

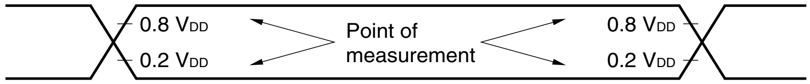
2. To fill in the undefined area of the SCL0 falling edge, it is necessary for the device to internally provide at least 300 ns of hold time for the SDA0 signal (which is $V_{IHmin.}$ of the SCL0 signal).

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

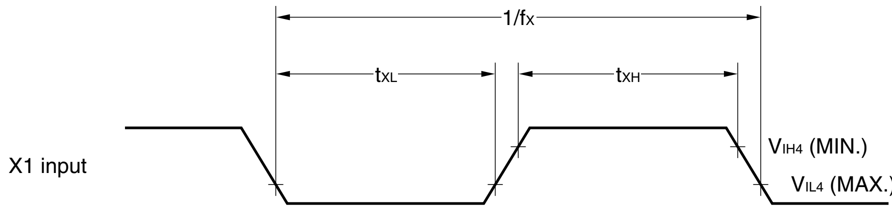
4. The high-speed mode I²C bus is available in the SMB mode and the standard mode I²C bus system. At this time, the conditions described below must be satisfied.

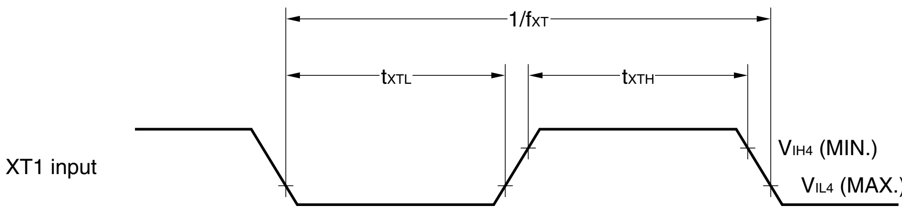
- If the device extends the SCL0 signal low state hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time
  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.}$+ $t_{SU:DAT}$ = 1000 + 250 = 1250 ns by the SMB mode or the standard mode I²C bus specification).

AC Timing Measurement Points (Excluding X1 and XT1 Inputs)

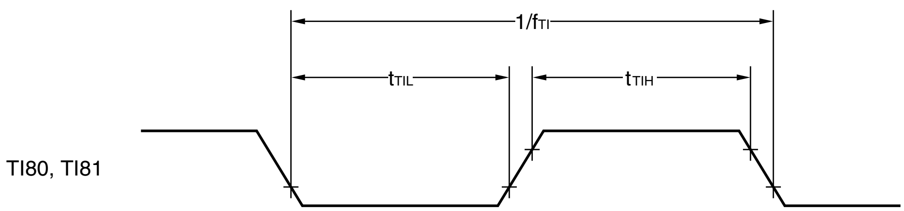


Clock Timing

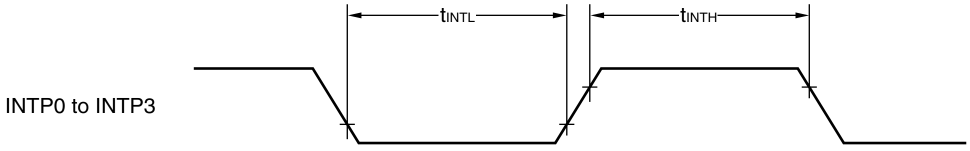




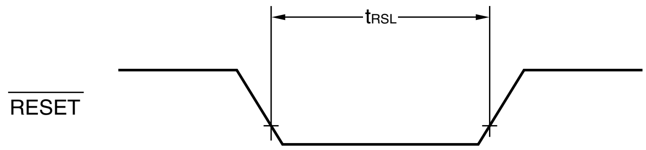
TI Timing



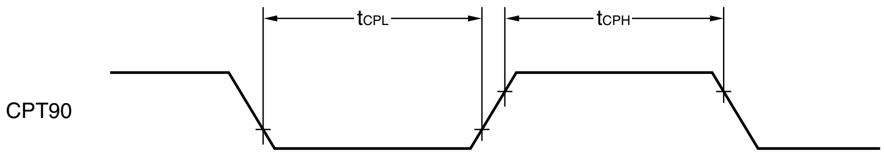
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing

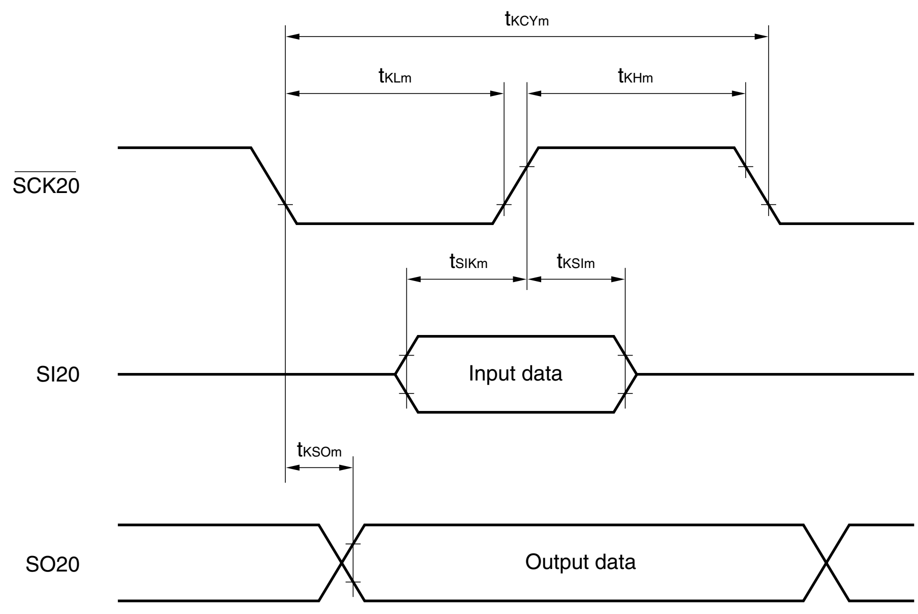


CPT90 Input Timing



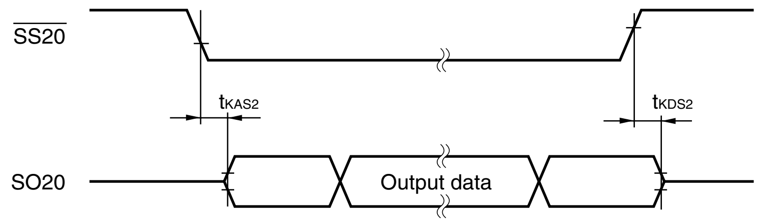
Serial Transfer Timing

3-wire serial I/O mode:

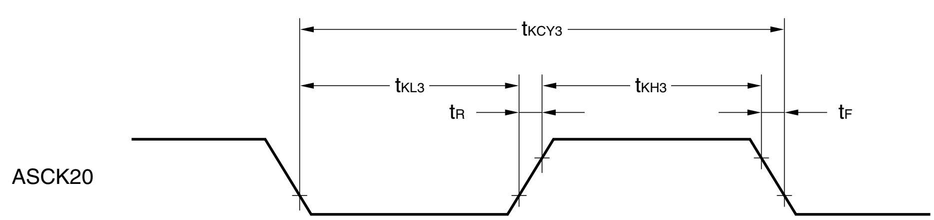


Remark m = 1, 2

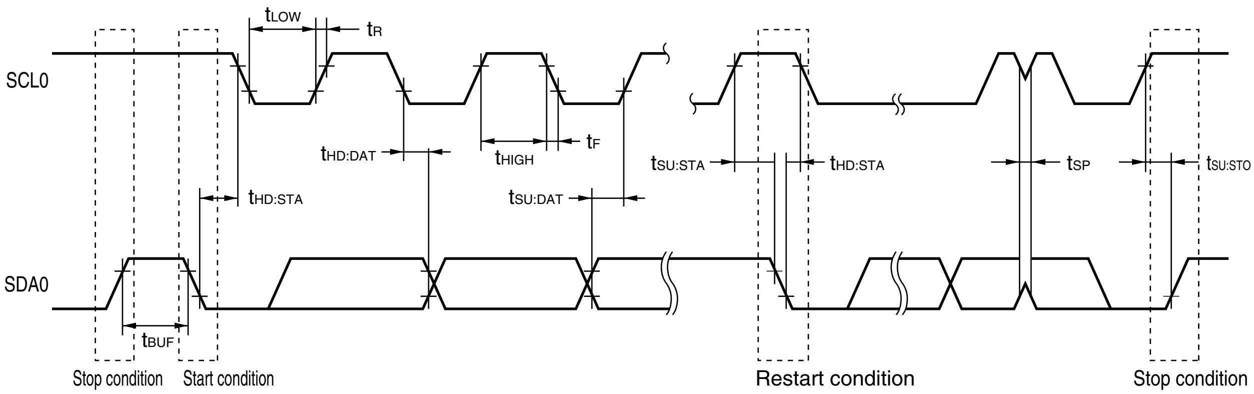
3-wire serial I/O mode (when using $\overline{SS20}$):



UART mode (external clock input):



SMB mode:


tLOW
tR
SCL0
tHD:DAT
tHIGH
tF
tSU:STA
tHD:STA
tSP
tSU:STO
tHD:STA
tSU:DAT
SDA0
tBUF
Stop condition
Start condition
Restart condition
Stop condition

10-Bit A/D Converter Characteristics (T_A = –40 to +85°C, 1.8 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	12		100	μs
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	28		100	μs
Zero-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Full-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Integral linearity error[Note]	INL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±4.5	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±8.5	LSB
Differential linearity error[Note]	DNL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full scale range

Flash Memory Write/Erase Characteristics (T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin)Note 1	I_{DDW}	When V_{PP} supply voltage = V_{PP1} (5.0 MHz operation)			23	mA
Write current (V_{PP} pin)	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			20	mA
Erase current (V_{DD} pin)Note 1	I_{DDE}	When V_{PP} supply voltage = V_{PP1} (5.0 MHz operation)			23	mA
Erase current (V_{PP} pin)	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			100	mA
Unit erase timeNote 2	t_{er}		0.2	0.2	0.2	s
Total erase time	t_{era}				20	s
Write countNote 3		Erase/write is regarded as 1 cycle	20	20	20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

Notes 1. The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) and AV_{DD} current are not included.

2. The prewrite time before erasure and the erase verify time (writeback time) is not included.

3. When a product is first written after shipment, “erase → write” is taken as one rewrite.

Data Memory STOP Mode Low Power Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

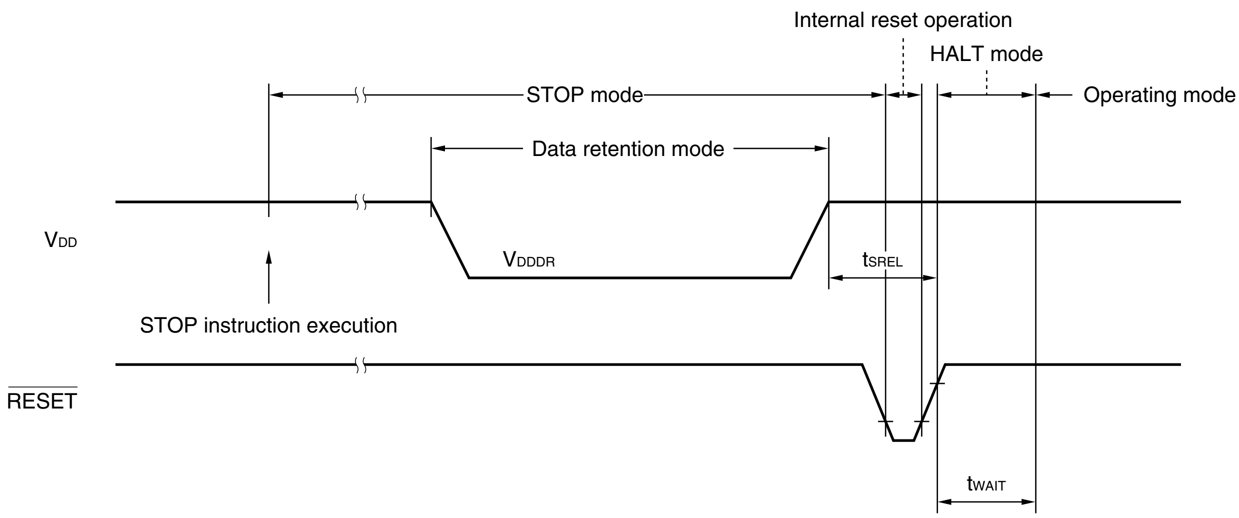
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait timeNote 1	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.

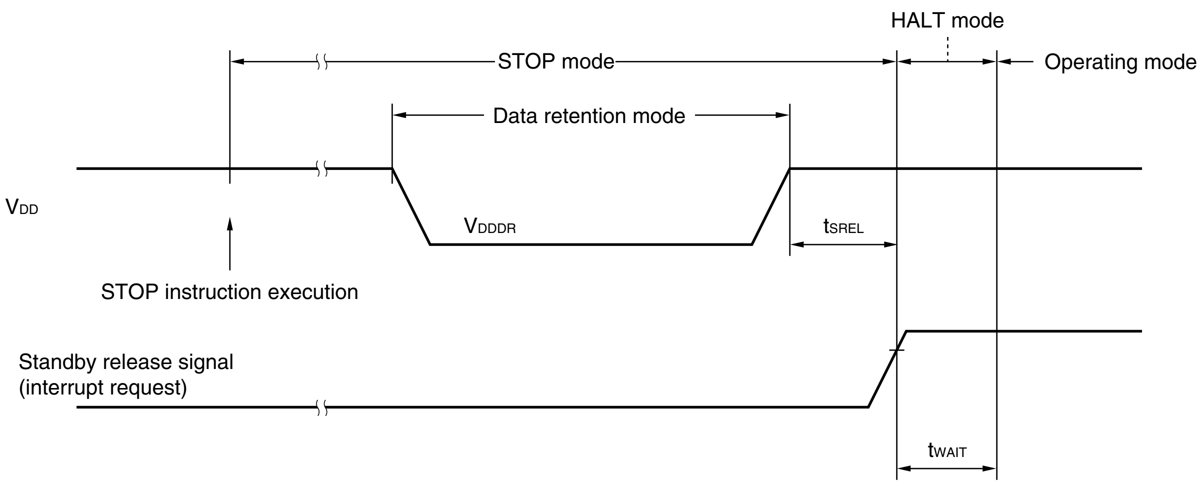
2. By using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS), $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected.

Remark f_X: Main system clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

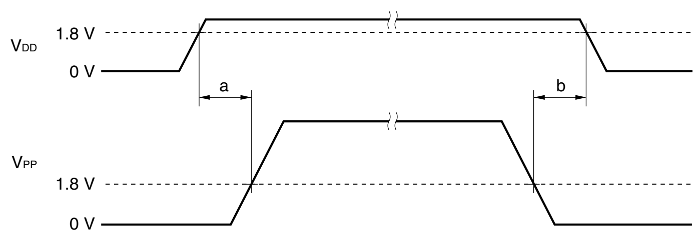


Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	AV_{DD} – 0.3 V ≤ V_{DD} ≤ AV_{DD} + 0.3 V	–0.3 to +6.5	V
	AV_{DD}	AV_{REF} ≤ AV_{DD} + 0.3 V		V
	AV_{REF}	AV_{REF} ≤ V_{DD} + 0.3 V		V
	V_{PP}	**Note**	–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P50 to P53, P23, P24	–0.3 to V_{DD} + 0.3	V
	V_{I2}	P23, P24	–0.3 to +5.5	V
	V_{I3}	P50 to P53	–0.3 to +13	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	–10	mA
		Total for all pins	–30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total for all pins	160	mA
Operating ambient temperature	T_A	In normal operation mode	–40 to +85	°C
		During flash memory programming	+10 to +40	°C
Storage temperature	T_{stg}		–40 to +125	°C

Note Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

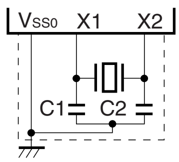
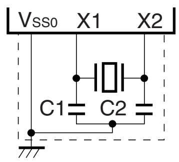
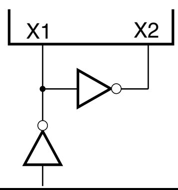
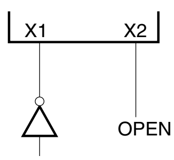
- **When supply voltage rises**
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (1.8 V) of the operating voltage range (see **a** in the figure below).
- **When supply voltage drops**
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (1.8 V) of the operating voltage range of V_{DD} (see **b** in the figure below).



Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
			V_{DD} = 1.8 to 5.5 V			30	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)[Note 1]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

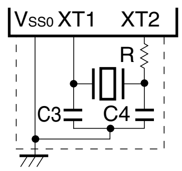
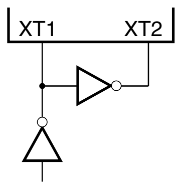
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
			V_{DD} = 1.8 to 5.5 V			10	s
External clock		XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation stabilization wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–15	mA
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V_{IH1}	P00 to P05, P10, P11,P60 to P67	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
			V_{DD} = 1.8 to 5.5 V, T_A = 25 to +85°C	0.9V_{DD}		12	V
	V_{IH3}	$\overline{RESET}$, P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P05, P10, P11, P60 to P67	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL3}	$\overline{RESET}$,P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
			V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH}	Pins other than P23, P24, P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–3 Note	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistor	R_1	V_I = 0 V, for pins other than P23, P24, and P50 to P53		50	100	200	kΩ

Note A low-level input leakage current of –60 μA (MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 and P50 to P53 are set to input mode. At times other than this, a –3 μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1} Note 1	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10% Note 4		5.0	15.0	mA
			V_{DD} = 3.0 V ± 10% Note 5		2.0	5.0	mA
			V_{DD} = 2.0 V ± 10% Note 5		1.5	3.0	mA
	I_{DD2} Note 1	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10% Note 4		2.0	6.0	mA
			V_{DD} = 3.0 V ± 10% Note 5		1.0	2.5	mA
			V_{DD} = 2.0 V ± 10% Note 5		0.75	1.5	mA
	I_{DD3} Note 1	32.768 kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ± 10%		250	750	μA
			V_{DD} = 3.0 V ± 10%		200	600	μA
			V_{DD} = 2.0 V ± 10%		150	450	μA
	I_{DD4} Note 1	32.768 kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ± 10%		50	150	μA
			V_{DD} = 3.0 V ± 10%		30	90	μA
			V_{DD} = 2.0 V ± 10%		20	60	μA
	I_{DD5} Note 1	32.768 kHz crystal stop STOP mode	V_{DD} = 5.0 V ± 10%		0.1	30	μA
			V_{DD} = 3.0 V ± 10%		0.05	10	μA
			V_{DD} = 2.0 V ± 10%		0.05	10	μA
	I_{DD6} Note 2	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10% Note 4		6.0	17.0	mA
			V_{DD} = 3.0 V ± 10% Note 5		3.0	7.0	mA
			V_{DD} = 2.0 V ± 10% Note 5		2.5	5.0	mA

Notes 1. The AV_{REF}ON (ADCS0 (bit 7 of ADM0; A/D converter mode register 0) = 1), AV_{DD}, and the port current (including the current flowing through the internal pull-up resistors) are not included.

2. The AV_{REF}ON (ADCS0 =1) and port current (including the current flowing through the internal pull-up resistors) are not included. Refer to the A/D converter characteristics for the current flowing through AV_{REF}.

3. When the main system clock is stopped.

4. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H.)

5. During low-speed mode operation (when PCC is set to 02H)

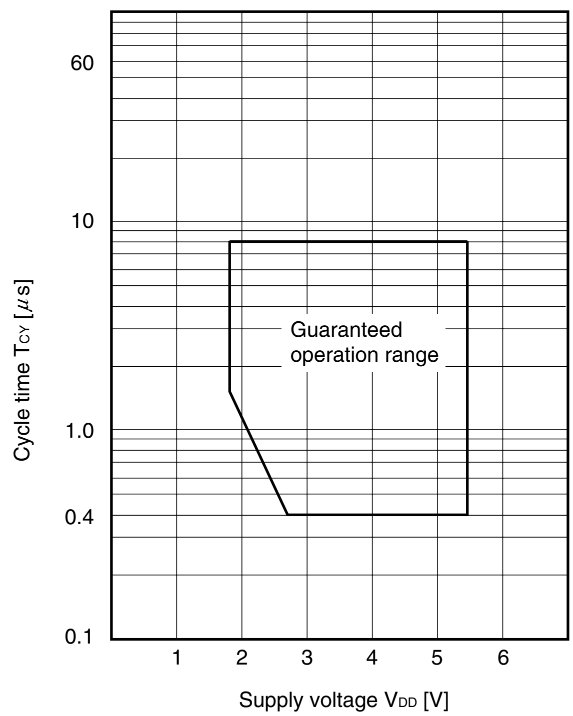
Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operation based on the main system clock	V_{DD} = 2.7 to 5.5 V	0.4		8	μs
			V_{DD} = 1.8 to 5.5 V	1.6		8	μs
		Operation based on the subsystem clock		114	122	125	μs
TI80 and TI81 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
		V_{DD} = 1.8 to 5.5 V		0		275	kHz
TI80 and TI81 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
		V_{DD} = 1.8 to 5.5 V		1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3		10			μs
$\overline{RESET}$ input low-level width	t_{RSL}			10			μs
CPT90 input high-/low-level width	t_{CPH}, t_{CPL}			10			μs

T_{CY} vs. V_{DD} (main system clock)



(2) Serial interface SIO20 (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode (SCK20...Internal clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCK20 cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
SCK20 high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 - 50$			ns
		V_{DD} = 1.8 to 5.5 V		$t_{KCY1}/2 - 150$			ns
SI20 setup time (to SCK20 ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from SCK20 ↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from SCK20↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode (SCK20...External clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCK20 cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		900			ns
		V_{DD} = 1.8 to 5.5 V		3500			ns
SCK20 high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to SCK20 ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from SCK20 ↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from SCK20 ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (when using SS20, to SS20 ↓)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (when using SS20, from SS20 ↑)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
		V_{DD} = 1.8 to 5.5 V	3500			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise time, fall time	t_R, t_F				1	μs

(3) Serial interface SMB0 (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (μPD78F9177Y only)

(a) DC characteristics

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	SCL0, SDA0 (at hysteresis)		$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	SCL0, SDA0 (at hysteresis)		0		$0.2V_{DD}$	V
Output voltage, low	V_{OL}	SCL0, SDA0	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH}	SCL0, SDA0	$V_I = V_{DD}$			3	μA
Input leakage current, low	I_{LIL}	SCL0, SDA0	V_I = 0 V			–3	μA

(b) DC characteristics (when using comparator)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input range	V_{SDA}, V_{SCL}	V_{DD} = 1.8 to 5.5 V	0		5.5	V
Transfer level	V_{ISDA}, V_{ISCL}	$4.5 \le V_{DD} \le 5.5$ V	$0.72V_{ISMB}$	V_{ISMB}	$1.28V_{ISMB}$	V
		$3.3 \le V_{DD} < 4.5$ V	$0.78V_{ISMB}$	V_{ISMB}	$1.22V_{ISMB}$	V
		$2.7 \le V_{DD} < 3.3$ V	$0.75V_{ISMB}$	V_{ISMB}	$1.25V_{ISMB}$	V
		$1.8 \le V_{DD} < 2.7$ V	$0.90V_{ISMB}$	V_{ISMB}	$1.45V_{ISMB}$	V
Input level threshold value[Note]	V_{ISMB}	LVL01, LVL00 = 0, 1		$0.25 \times V_{DD}$		V
		LVL01, LVL00 = 1, 0		$0.375 \times V_{DD}$		V
		LVL01, LVL00 = 1, 1		$0.5 \times V_{DD}$		V

Note V_{ISMB} is an input level threshold value selected by bits LVL00 and LVL01 (bits 0 and 1 of SMB input level setting register 0 (SMBVI0)).

According to the SMB standard (V1.1), the maximum value of low-level input voltage is 0.8 V, and the minimum value of high-level input voltage, 2.1 V. To satisfy these conditions, set LVL01 and LVL00 as follows;

- When V_{DD} = 1.8 to 3.3 V: LVL01, LVL00 = 1, 1 ($0.5 \times V_{DD}$)
- When V_{DD} = 3.3 to 4.5 V: LVL01, LVL00 = 1, 0 ($0.375 \times V_{DD}$)
- When V_{DD} = 4.5 to 5.5 V: LVL01, LVL00 = 0, 1 ($0.25 \times V_{DD}$)

“LVL01, LVL00 = 0, 0” is not available since this setting does not satisfy the SMB standard (V1.1).

(c) AC characteristics

Parameter		Symbol	SMB Mode		Standard Mode I^2C Bus		High-speed Mode I^2C Bus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	10	100	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	–	4.7	–	1.3	–	μs
Hold time Note 1		$t_{HD:STA}$	4.0	–	4.0	–	0.6	–	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	–	4.7	–	0.6	–	μs
Stop condition setup time		$t_{SU:STO}$	4.0	–	4.0	–	0.6	–	μs
Data hold time	When using CBUS-compatible master	$t_{HD:DAT}$	–	–	5	–	–	–	μs
	When using SMB/IIC bus		300	–	0 Note 2	–	0 Note 2	900 Note 3	ns
Data setup time		$t_{SU:DAT}$	250	–	250	–	100 Note 4	–	ns
SCL0 clock low-level width		t_{LOW}	4.7	–	4.7	–	1.3	–	μs
SCL0 clock high-level width		t_{HIGH}	4.0	50	4.0	–	0.6	–	μs
SCL0 and SDA0 signal fall time		t_F	–	300	–	300	–	300	ns
SCL0 and SDA0 signal rise time		t_R	–	1000	–	1000	–	300	ns
Spike pulse width controlled by input filter		t_{SP}	–	–	–	–	0	50	ns
Timeout		$t_{TIMEOUT}$	25	35	–	–	–	–	ms
Total extended time of SCL0 clock low-level period (slave)		$t_{LOW:SEXT}$	–	25	–	–	–	–	ms
Total extended time of cumulative clock low-level period (master)		$t_{LOW:MEXT}$	–	10	–	–	–	–	ms
Capacitive load per each bus line		Cb	–	–	–	400	–	400	pF

Notes 1. In the start condition, the first clock pulse is generated after this hold time.

2. To fill in the undefined area of the SCL0 falling edge, it is necessary for the device to internally provide at least 300 ns of hold time for the SDA0 signal (which is $V_{IHmin.}$ of the SCL0 signal).

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

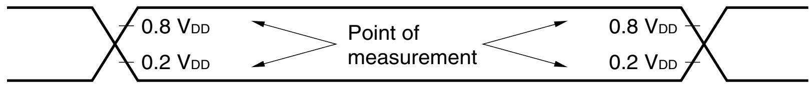
4. The high-speed mode I^2C bus is available in the SMB mode and the standard mode I^2C bus system. At this time, the conditions described below must be satisfied.

- If the device extends the SCL0 signal low state hold time

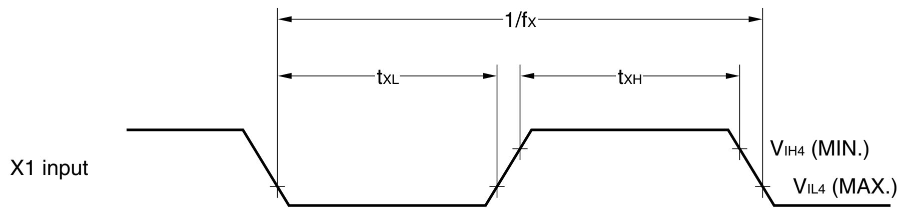
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time

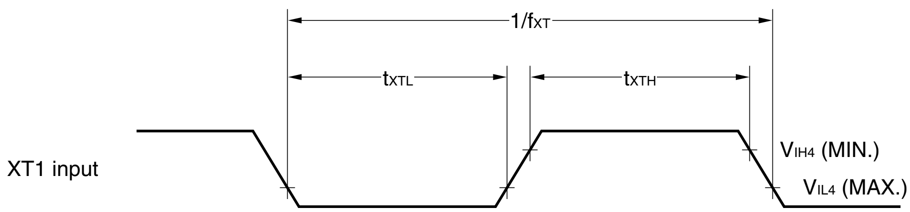
  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns by the SMB mode or the standard mode I^2C bus specification).

AC Timing Measurement Points (Excluding X1 and XT1 Inputs)

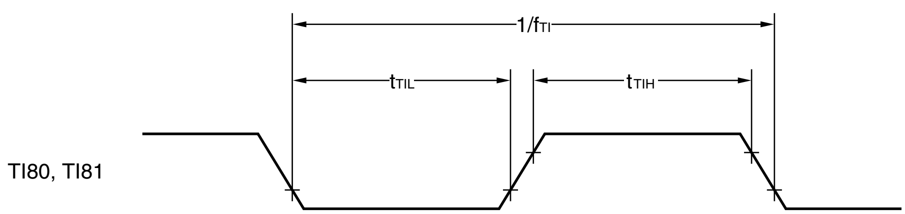


Clock Timing

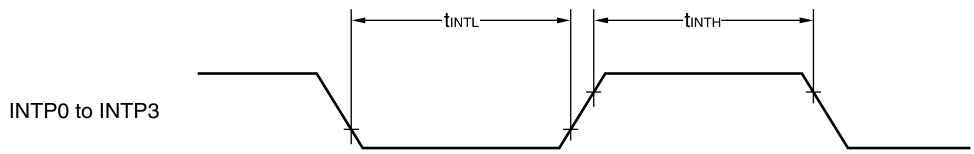




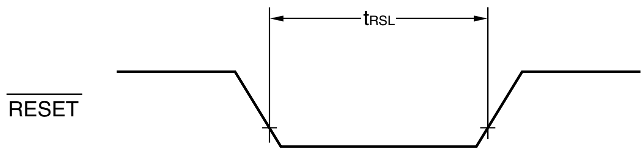
TI Timing



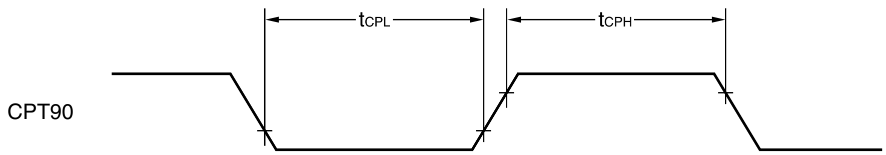
Interrupt Input Timing



RESET Input Timing

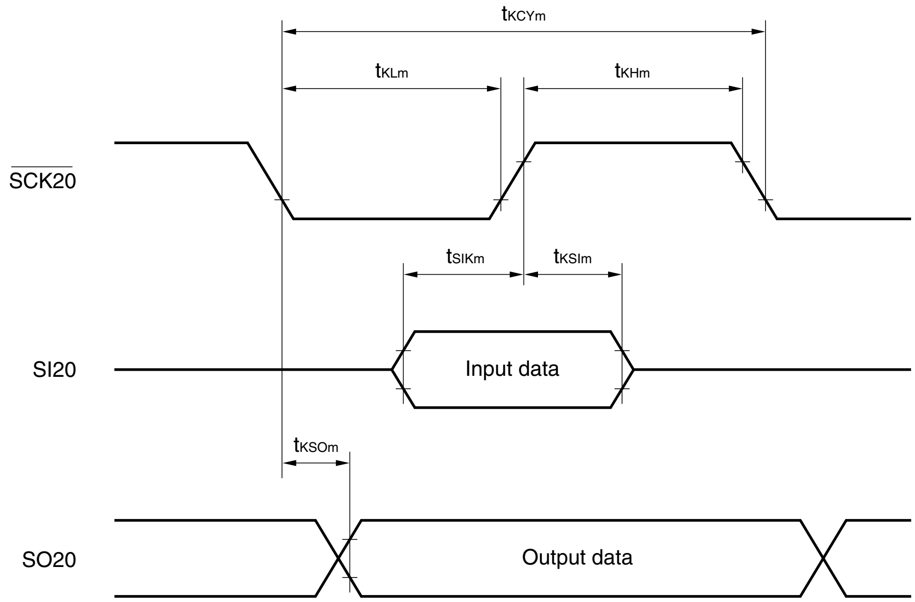


CPT90 Input Timing



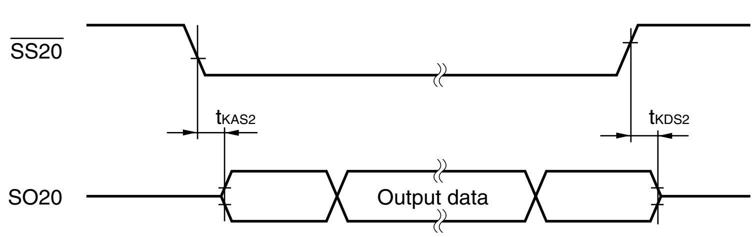
Serial Transfer Timing

3-wire serial I/O mode:

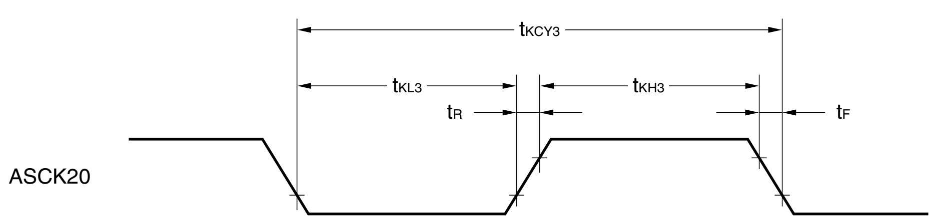


Remark m = 1, 2

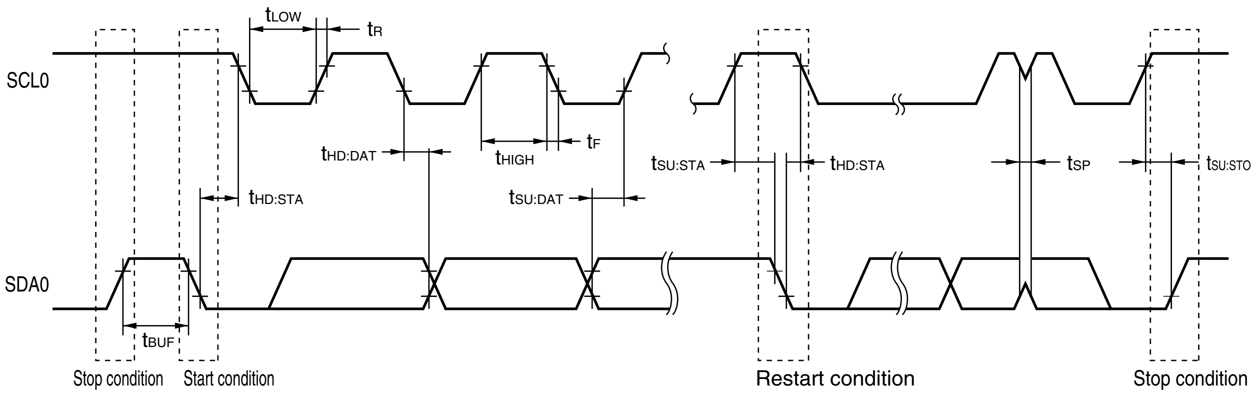
3-wire serial I/O mode (when using SS20):



UART mode (external clock input):



SMB mode:


tLOW
tR
SCL0
tHD:DAT
tHIGH
tF
tSU:STA
tHD:STA
tSP
tSU:STO
tHD:STA
tSU:DAT
SDA0
tBUF
Stop condition
Start condition
Restart condition
Stop condition

10-Bit A/D Converter Characteristics (T_A = –40 to +85°C, 1.8 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error Note		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	28		100	μs
Zero-scale error Note		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Full-scale error Note		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Integral linearity error Note	INL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±4.5	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±8.5	LSB
Differential linearity error Note	DNL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full scale range

Flash Memory Write/Erase Characteristics (T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin)Note 1	I_{DDW}	When V_{PP} supply voltage = V_{PP1} (5.0 MHz operation)			18	mA
Write current (V_{PP} pin)	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			7.5	mA
Erase current (V_{DD} pin)Note 1	I_{DDE}	When V_{PP} supply voltage = V_{PP1} (5.0 MHz operation)			18	mA
Erase current (V_{PP} pin)	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			100	mA
Unit erase timeNote 2	t_{er}		0.5	1	1	s
Total erase time	t_{era}				20	s
Write countNote 3		Erase/write is regarded as 1 cycle	20	20	20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

Notes 1. The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) and AV_{DD} current are not included.

2. The prewrite time before erasure and the erase verify time (writeback time) is not included.

3. When a product is first written after shipment, “erase → write” is taken as one rewrite.

Data Memory STOP Mode Low Power Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

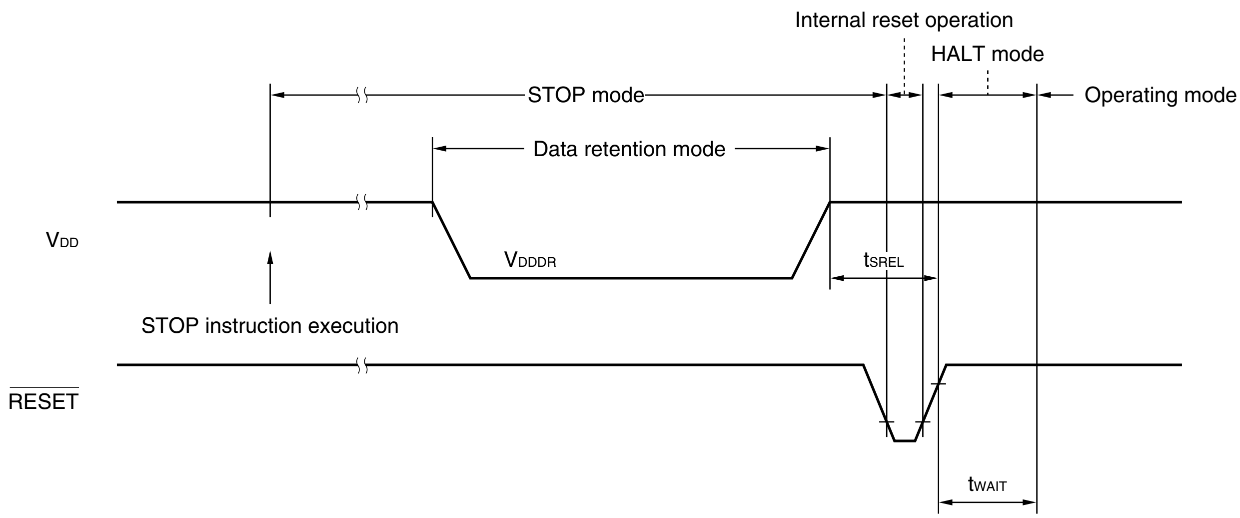
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait timeNote 1	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.

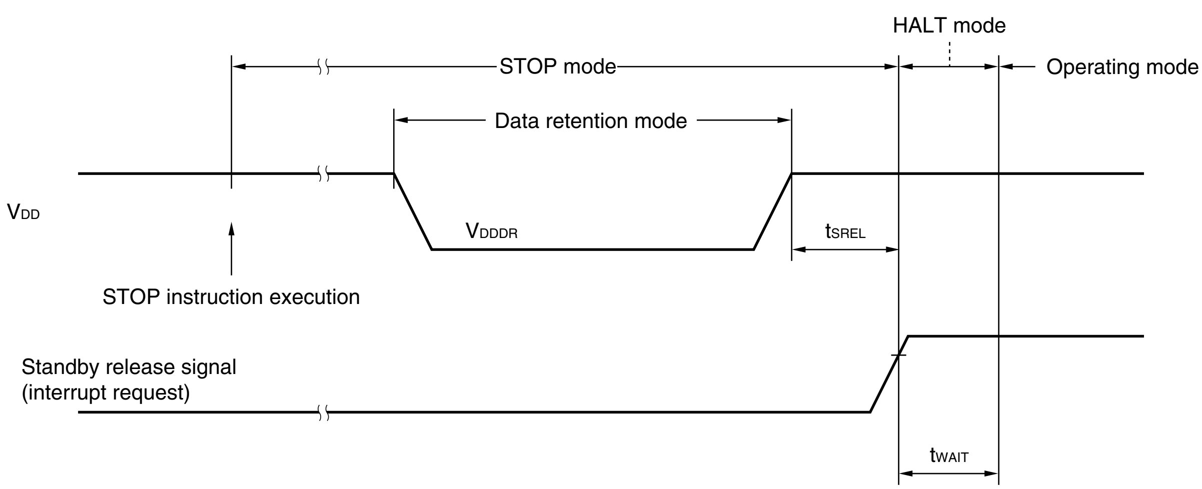
2. By using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS), $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected.

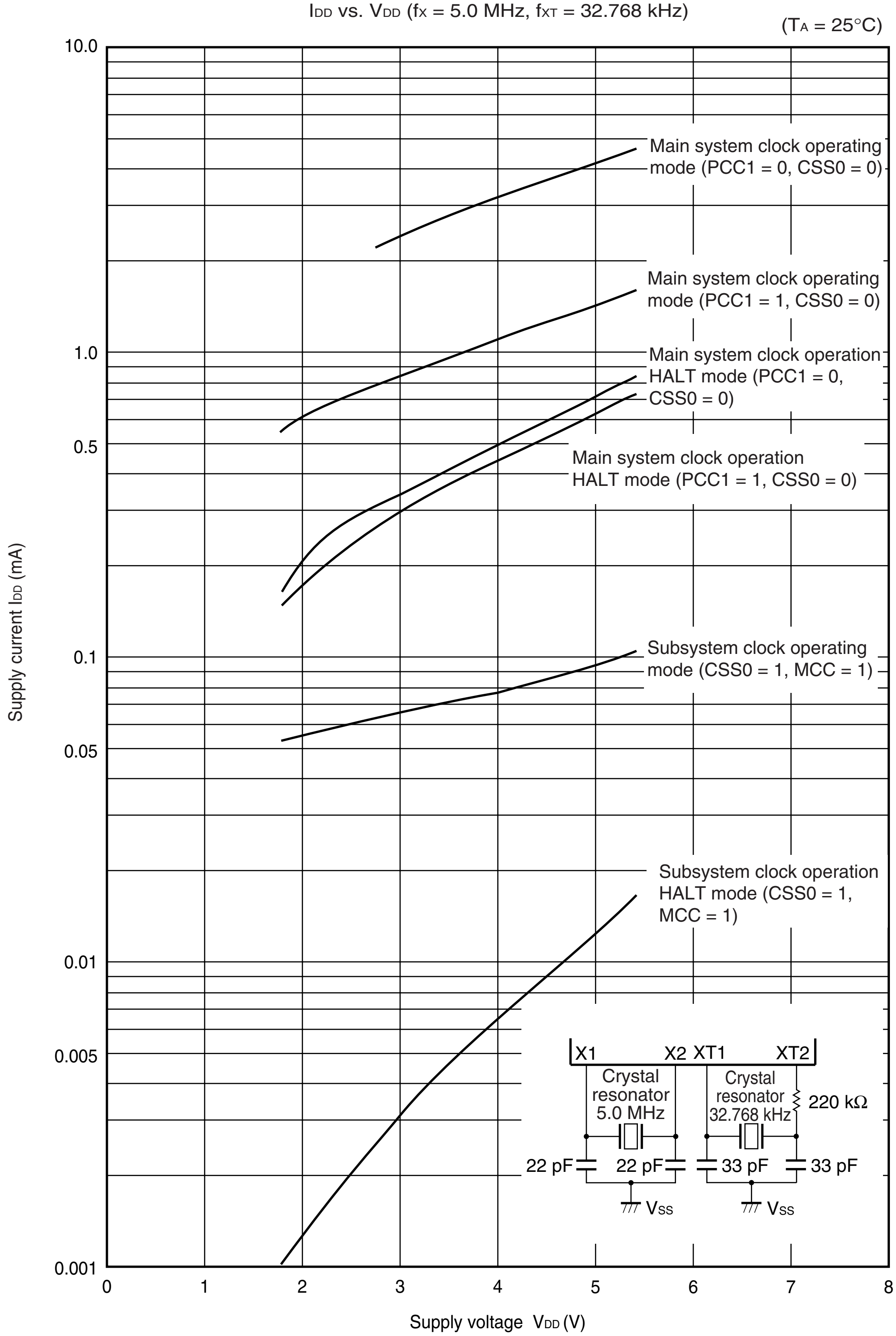
Remark f_X: Main system clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



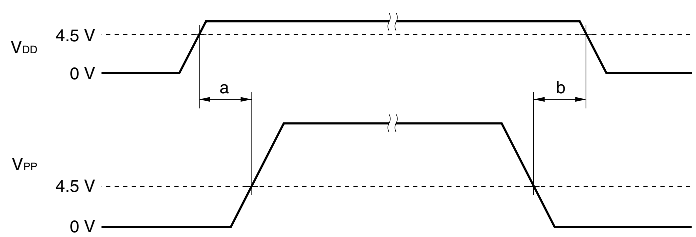

IDD vs. VDD (fX = 5.0 MHz, fXT = 32.768 kHz)
(TA = 25°C)
Main system clock operating mode (PCC1 = 0, CSS0 = 0)
Main system clock operating mode (PCC1 = 1, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 0, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 1, CSS0 = 0)
Subsystem clock operating mode (CSS0 = 1, MCC = 1)
Subsystem clock operation HALT mode (CSS0 = 1, MCC = 1)
X1
X2
XT1
XT2
Crystal resonator 5.0 MHz
Crystal resonator 32.768 kHz
220 kΩ
22 pF
22 pF
33 pF
33 pF
VSS
VSS
Supply current IDD (mA)
10.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
8
Supply voltage VDD (V)

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	AV_{DD} – 0.3 V ≤ V_{DD} ≤ AV_{DD} + 0.3 V	–0.3 to +6.5	V
	AV_{DD}	AV_{REF} ≤ AV_{DD} + 0.3 V		V
	AV_{REF}	AV_{REF} ≤ V_{DD} + 0.3 V		V
	V_{PP}	**Note**	–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P50 to P53, P23, P24	–0.3 to V_{DD} + 0.3	V
	V_{I2}	P23, P24	–0.3 to +5.5	V
	V_{I3}	P50 to P53	–0.3 to +13	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	–4	mA
		Total for all pins	–14	mA
Output current, low	I_{OL}	Per pin	5	mA
		Total for all pins	80	mA
Operating ambient temperature	T_A	In normal operation mode	–40 to +105	°C
		During flash memory programming	10 to 40	°C
Storage temperature	T_{stg}		–40 to +125	°C

Note Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

- **When supply voltage rises**
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (4.5 V) of the operating voltage range (see **a** in the figure below).
- **When supply voltage drops**
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (4.5 V) of the operating voltage range of V_{DD} (see **b** in the figure below).

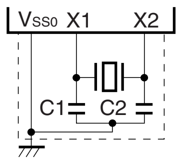
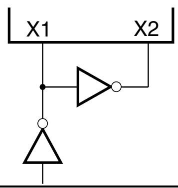
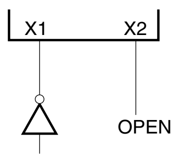


Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +105°C)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

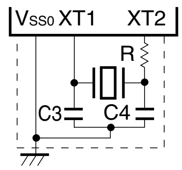
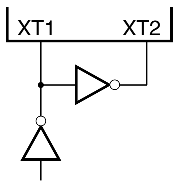
2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

3. For ceramic resonator, use the part number for which the resonator manufacturer guarantees operation under the condition of T_A = 105°C.

Remark For the resonator selection and oscillator constant, users are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +105°C)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2			1.2	2	s
External clock		XT1 input frequency (f_{XT})Note 1		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, users are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +105°C) (1/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–7	mA
Output current, low	I_{OL}	Per pin				1.6	mA
		Total for all pins				40	mA
Input voltage, high	V_{IH1}	P00 to P05, P10, P11, P60 to P67		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	P50 to P53		$0.7V_{DD}$		10	V
	V_{IH3}	$\overline{RESET}$, P20 to P26, P30 to P33		$0.8V_{DD}$		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P05, P10, P11, P60 to P67		0		$0.3V_{DD}$	V
	V_{IL2}	P50 to P53		0		$0.3V_{DD}$	V
	V_{IL3}	$\overline{RESET}$, P20 to P26, P30 to P33		0		$0.2V_{DD}$	V
	V_{IL4}	X1, X2, XT1, XT2		0		0.1	V
Output voltage, high	V_{OH}	Pins other than P23, P24, P50 to P53	I_{OH} = –1 mA	V_{DD} – 2.0			V
			I_{OH} = –100 μA	V_{DD} – 1.0			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	I_{OL} = 1.6 mA			2.0	V
			I_{OL} = 400 μA			1.0	V
	V_{OL2}	P50 to P53	I_{OL} = 1.6 mA			1.0	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +105°C) (2/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_I = V_{DD}$	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			10	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 10 V	P50 to P53 (N-ch open drain)			80	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			–10	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–10[Note]	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–10	μA
Software pull-up resistor	R_1	V_I = 0 V, for pins other than P23, P24, and P50 to P53		50	100	300	kΩ

Note A low-level input leakage current of –60 μA (MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 when P50 to P53 are set to input mode. At times other than this, a –10 μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +105°C) (3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1} Note 1	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		7.5	20.0	mA
	I_{DD2} Note 1	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		3.0	6.0	mA
	I_{DD3} Note 1	32.768 kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ±10%		30	3000	μA
	I_{DD4} Note 1	32.768 kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ±10%		25	2500	μA
	I_{DD5} Note 1	32.768 kHz crystal stop STOP mode	V_{DD} = 5.0 V ± 10%		1.0	1000	μA
	I_{DD6} Note 2	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		8.7	22.3	mA

Notes 1. The AV_{REF}ON (ADCS0 (bit 7 of ADM0; A/D converter mode register 0) = 1), AV_{DD}, and port current (including the current flowing through the internal pull-up resistors) is not included.

2. The AV_{REF}ON (ADCS0 =1) and port current (including the current flowing through the internal pull-up resistors) is not included. Refer to the A/D converter characteristics for the current flowing through AV_{REF}.

3. When the main system clock is stopped.

4. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H.)

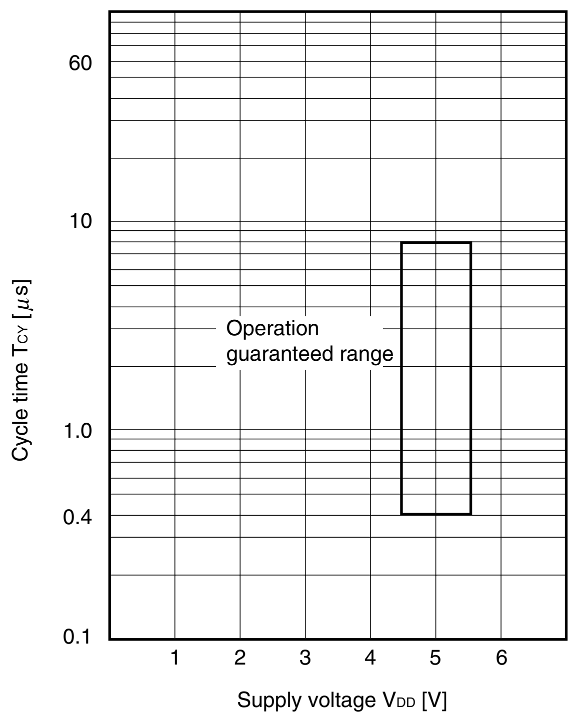
Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operation based on the main system clock	0.4		8	μs
		Operation based on the subsystem clock	114	122	125	μs
TI80 and TI81 input frequency	f_{TI}		0		4	MHz
TI80 and TI81 input high-/low-level width	t_{TIH}, t_{TIL}		0.1			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3	10			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}		10			μs
CPT90 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs. V_{DD} (main system clock)



(2) Serial interface 20 (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +105°C)

(a) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 – 50			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK1}		150			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI1}		400			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	0		250	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode ($\overline{SCK20}$...External clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}		900			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK2}		100			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI2}		400			ns
SO20 output delay time from $\overline{SCK20}$ ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns
SO20 setup time (when using $\overline{SS20}$, to $\overline{SS20}$ ↓)	t_{KAS2}				120	ns
SO20 disable time (when using $\overline{SS20}$, from $\overline{SS20}$ ↑)	t_{KDS2}				240	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

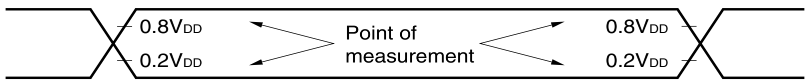
(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					78125	bps

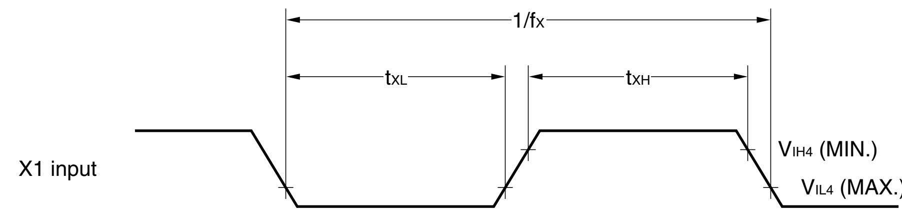
(d) UART mode (external clock input)

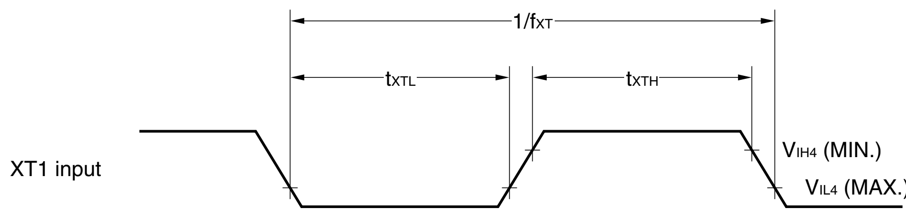
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}		900			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}		400			ns
Transfer rate					39063	bps
ASCK20 rise time, fall time	t_R, t_F				1	μs

AC Timing Measurement Points (Excluding X1 and XT1 Inputs)

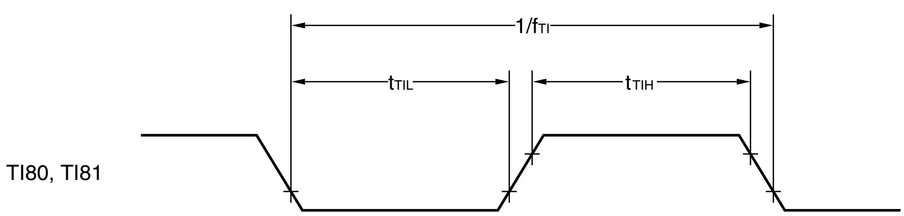


Clock Timing

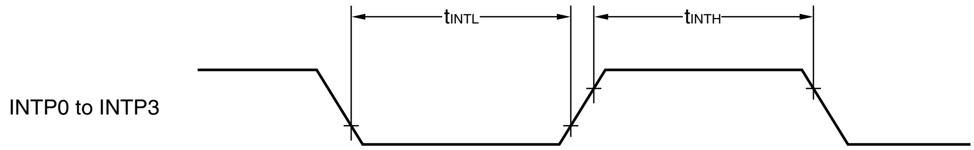




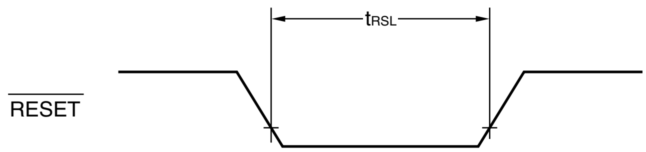
TI Timing



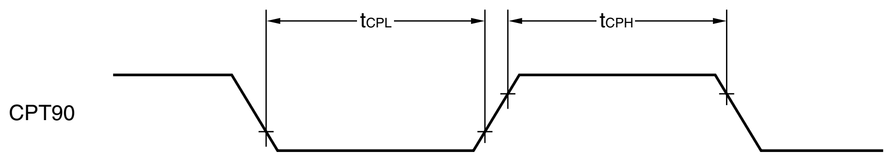
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing

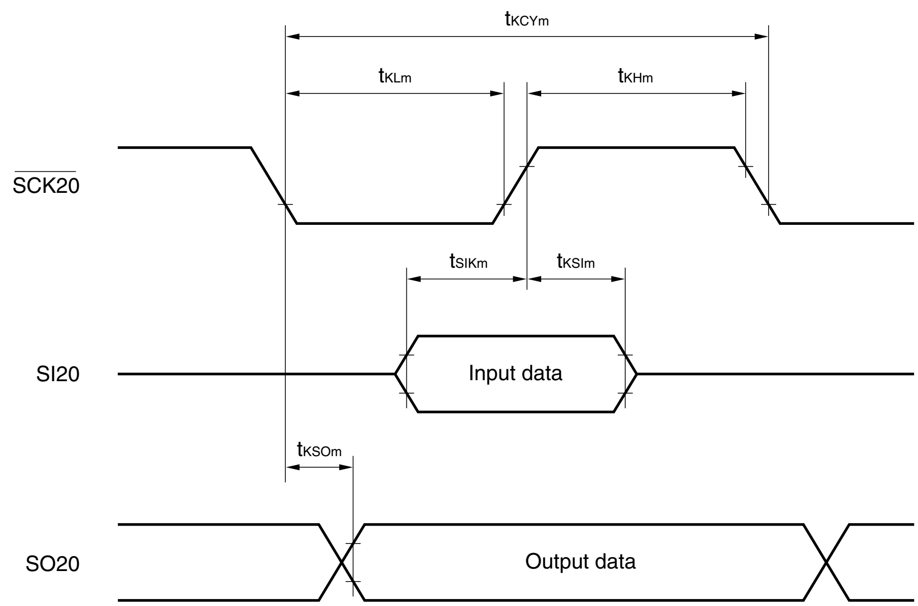


CPT90 Input Timing



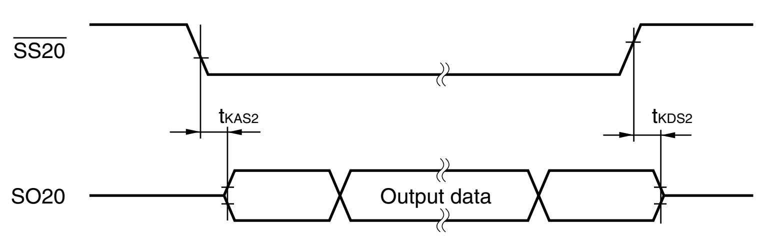
Serial Transfer Timing

3-wire serial I/O mode:

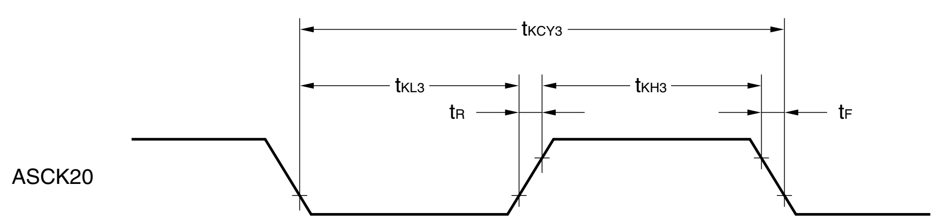


Remark m = 1, 2

3-wire serial I/O mode (when using $\overline{SS20}$):



UART mode (external clock input):



10-Bit A/D Converter Characteristics (T_A = –40 to +105°C, 4.5 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]				±0.2	±0.6	%FSR
Conversion time	t_{CONV}		14		28	μs
Zero-scale error[Note]					±0.6	%FSR
Full-scale error[Note]					±0.6	%FSR
Integral linearity error[Note]	INL				±4.5	LSB
Differential linearity error[Note]	DNL				±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full scale range

Flash Memory Write/Erase Characteristics (T_A = 10 to 40°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin)[Note 1]	I_{DDW}	When V_{PP} supply voltage = V_{PP1} (5.0 MHz operation)			23	mA
Write current (V_{PP} pin)	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			20	mA
Erase current[Note 1] (V_{DD} pin)	I_{DDE}	When V_{PP} supply voltage = V_{PP1} (5.0 MHz operation)			23	mA
Erase current (V_{PP} pin)	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			100	mA
Unit erase time[Note 2]	t_{er}		0.2	0.2	0.2	s
Total erase time	t_{era}				20	s
Write count[Note 3]		Erase/write is regarded as 1 cycle	20	20	20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation mode	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

Notes 1. The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) and AV_{DD} current are not included.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. When a product is first written after shipment, "erase → write" is taken as one rewrite.

Data Memory STOP Mode Low Power Supply Voltage Data Retention Characteristics (T_A = –40 to +105°C)

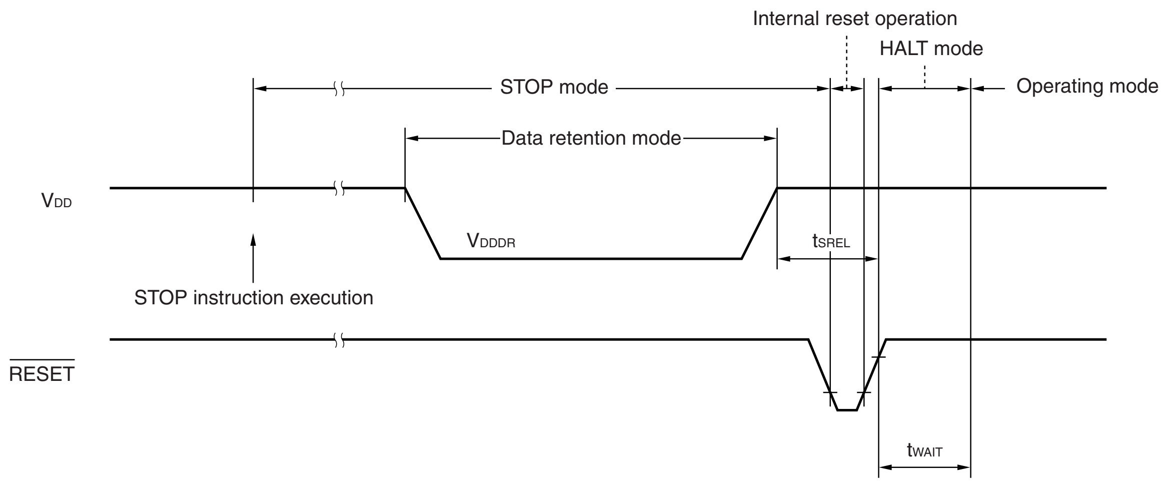
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		4.5		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.

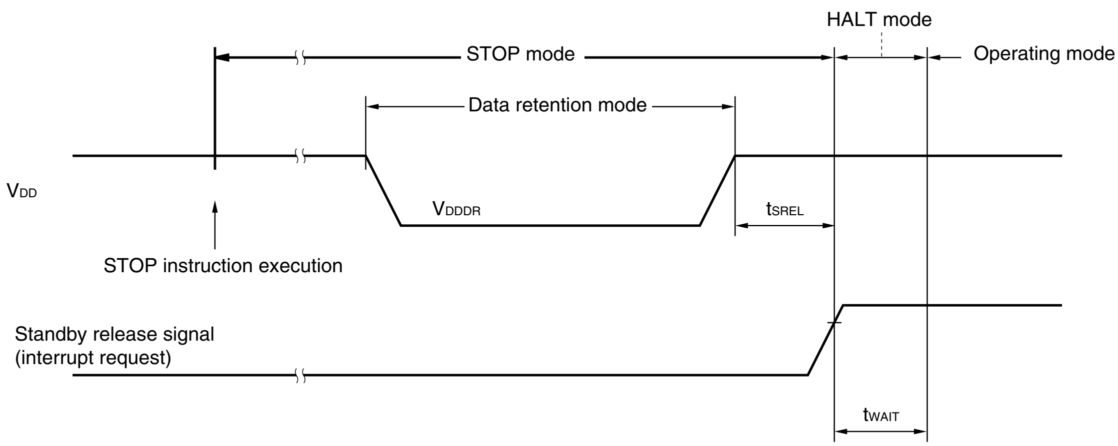
2. $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected by using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

Remark f_X: Main system clock oscillation frequency

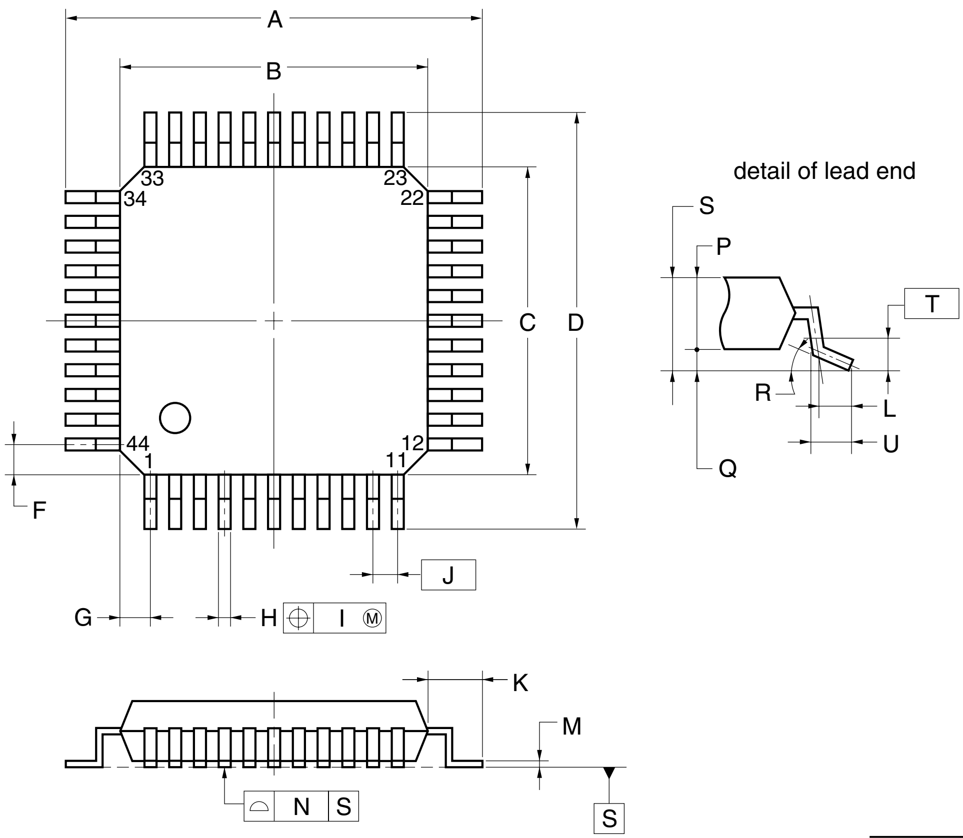
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



44 PIN PLASTIC LQFP (10x10)



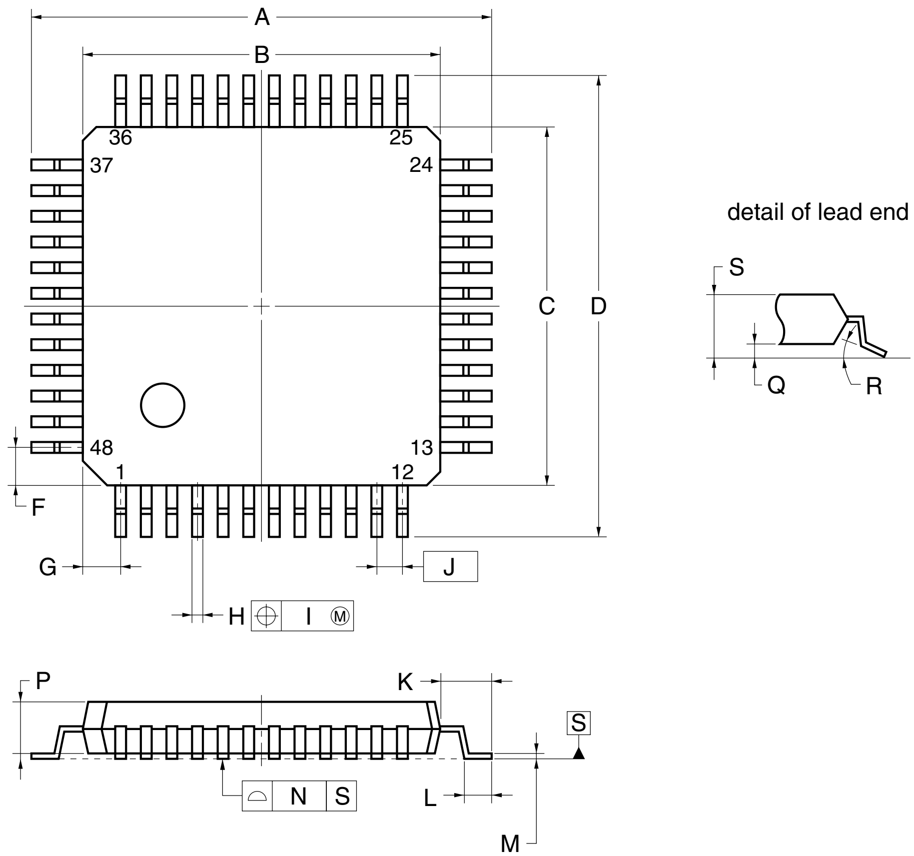
NOTE

Each lead centerline is located within 0.20 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.20
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3°^{+4°}_{-3°}$
S	1.6 MAX.
T	0.25 (T.P.)
U	0.6±0.15

S44GB-80-8ES-2

48-PIN PLASTIC TQFP (FINE PITCH) (7x7)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.0±0.2
B	7.0±0.2
C	7.0±0.2
D	9.0±0.2
F	0.75
G	0.75
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.0±0.1
Q	0.1±0.05
R	$3°^{+7°}_{-3°}$
S	1.27 MAX.

S48GA-50-9EU-2

CHAPTER 32 RECOMMENDED SOLDERING CONDITIONS

The μPD789167, 789177, 789167Y, and 789177Y Subseries should be soldered and mounted under the following recommended conditions.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html).

Table 32-1. Surface Mounting Type Soldering Conditions (1/4)

μPD789166GB-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789167GB-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789176GB-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789177GB-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789166YGB-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789167YGB-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789176YGB-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789177YGB-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789166GB(A)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789167GB(A)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789176GB(A)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789177GB(A)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789166GB(A1)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789167GB(A1)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789176GB(A1)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789177GB(A1)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789166GB(A2)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789167GB(A2)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789176GB(A2)-×××-8ES: 44-pin plastic LQFP (10 × 10)
μPD789177GB(A2)-×××-8ES: 44-pin plastic LQFP (10 × 10)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

Remark For soldering methods and conditions other than those recommended above, contact an NEC Electronics sales representative.

Table 32-1. Surface Mounting Type Soldering Conditions (2/4)

μPD78F9177GB-8ES: 44-pin plastic LQFP (10 × 10)
μPD78F9177YGB-8ES: 44-pin plastic LQFP (10 × 10)
μPD78F9177AGB-8ES: 44-pin plastic LQFP (10 × 10)
μPD78F9177AYGB-8ES: 44-pin plastic LQFP (10 × 10)
μPD78F9177AGB(A)-8ES: 44-pin plastic LQFP (10 × 10)
μPD78F9177AYGB(A)-8ES: 44-pin plastic LQFP (10 × 10)
μPD78F9177AGB(A1)-8ES: 44-pin plastic LQFP (10 × 10)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 3 days Note (After that, prebaking is necessary at 125°C for 10 to 72 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 3 days Note (After that, prebaking is necessary at 125°C for 10 to 72 hours)	VP15-103-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 3 days Note (After that, prebaking is necessary at 125°C for 10 to 72 hours)	WS60-103-1
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note The number of days for storage at 25°C, 65% RH MAX after the dry pack has been opened.

Caution Do not use different soldering methods together (except for partial heating).

Remark For soldering methods and conditions other than those recommended above, contact an NEC Electronics sales representative.

Table 32-1. Surface Mounting Type Soldering Conditions (3/4)

μPD789166GA-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789167GA-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789176GA-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789177GA-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789166YGA-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789167YGA-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789176YGA-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789177YGA-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789166YGA(A)-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789167YGA(A)-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789176YGA(A)-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789177YGA(A)-×××-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD78F9177YGA-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD78F9177AGA-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD78F9177AYGA-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD78F9177AYGA(A)-9EU: 48-pin plastic TQFP (fine pitch) (7 × 7)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 3 days Note (After that, prebaking is necessary at 125°C for 10 to 72 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 3 days Note (After that, prebaking is necessary at 125°C for 10 to 72 hours)	VP15-103-2
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note The number of days for storage at 25°C, 65% RH MAX after the dry pack has been opened.

Caution Do not use different soldering methods together (except for partial heating).

Remark For soldering methods and conditions other than those recommended above, contact an NEC Electronics sales representative.

★ **Table 32-1. Surface Mounting Type Soldering Conditions (4/4)**

μPD789166GB-××× -8ES-A: 44-pin plastic LQFP (10 × 10)
μPD789167GB-××× -8ES-A: 44-pin plastic LQFP (10 × 10)
μPD789176GB-××× -8ES-A: 44-pin plastic LQFP (10 × 10)
μPD789177GB-××× -8ES-A: 44-pin plastic LQFP (10 × 10)
μPD789166YGB-××× -8ES-A: 44-pin plastic LQFP (10 × 10)
μPD789167YGB-××× -8ES-A: 44-pin plastic LQFP (10 × 10)
μPD789176YGB-××× -8ES-A: 44-pin plastic LQFP (10 × 10)
μPD789177YGB-××× -8ES-A: 44-pin plastic LQFP (10 × 10)
μPD78F9177GB-8ES-A: 44-pin plastic LQFP (10 × 10)
μPD78F9177AGB-8ES-A: 44-pin plastic LQFP (10 × 10)
μPD789166GA-××× -9EU-A: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789167GA-××× -9EU-A: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789176GA-××× -9EU-A: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789177GA-××× -9EU-A: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789166YGA-××× -9EU-A: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789167YGA-××× -9EU-A: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789176YGA-××× -9EU-A: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD789177YGA-××× -9EU-A: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD78F9177YGA-9EU-A: 48-pin plastic TQFP (fine pitch) (7 × 7)
μPD78F9177YAGA-9EU-A: 48-pin plastic TQFP (fine pitch) (7 × 7)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days [Note] (After that, prebaking is necessary at 125°C for 20 to 72 hours)	IR60-207-3
Wave soldering	When the pin pitch of the package is 0.65 mm or more, wave soldering can also be performed. For details, ask an NEC Electronics sales representative.	–
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

Remarks 1. Products that have the part numbers suffixed by "-A" are lead-free products.

2. For soldering methods and conditions other than those recommended above, contact an NEC Electronics sales representative.

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for development of systems using the μPD789167, 789177, 789167Y, and 789177Y Subseries. Figure A-1 shows the development tools.

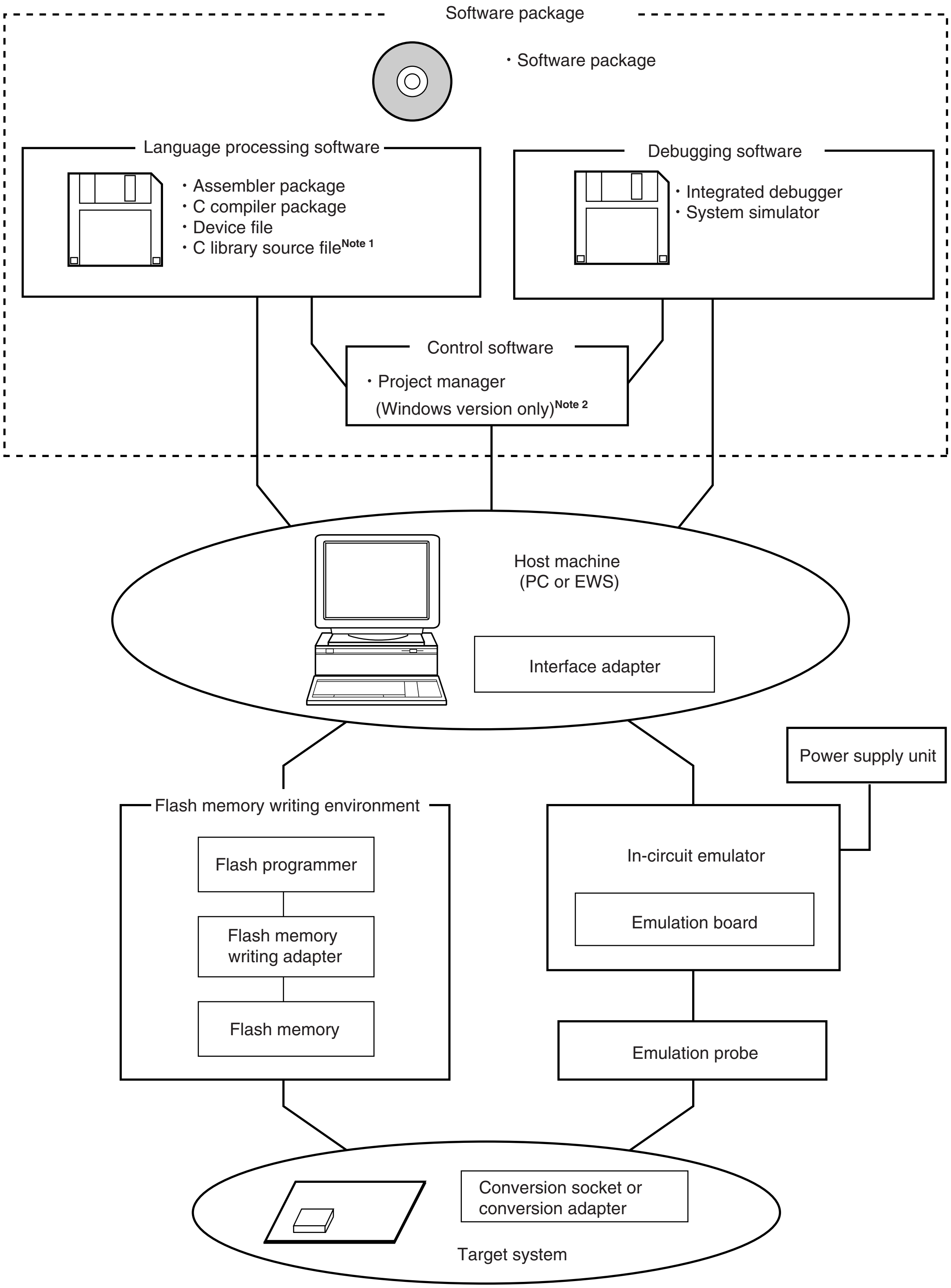
- Support to PC98-NX Series

  Unless specified otherwise, the products supported by IBM PC/AT™ compatibles can be used in PC98-NX Series. When using the PC98-NX Series, refer to the explanation of IBM PC/AT compatibles.

- Windows™

  Unless specified otherwise, "Windows" indicates the following operating systems.
  - Windows 3.1
  - Windows 95
  - Windows 98
  - Windows 2000
  - Windows NT™ Ver. 4.0
  - Windows XP

Figure A-1. Development Tools



Notes 1. The C library source file is not included in the software package.

2. The project manager is included in the assembler package.
The project manager is used only in the Windows environment.

A.1 Software Package

SP78K0S Software package	Software tools for development of the 78K/0S Series are combined in this package. The following tools are included. RA78K0S, CC78K0S, ID78K0S-NS, SM78K0S, and device files	
	Part number: μS××××SP78K0S	

Remark ×××× in the part number differs depending on the OS used

μS××××SP78K0S

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatible	Japanese Windows	CD-ROM
BB17		English Windows	

A.2 Language Processing Software

RA78K0S Assembler package	Program that converts program written in mnemonic into object codes that can be executed by a microcontroller. In addition, automatic functions to generate a symbol table and optimize branch instructions are also provided. Used in combination with a device file (DF789178) (sold separately). **<Caution when used in PC environment>** The assembler package is a DOS-based application but may be used in the Windows environment by using the project manager of Windows (included in the assembler package).
	Part number: μS××××RA78K0S
CC78K0S C compiler package	Program that converts program written in C language into object codes that can be executed by a microcontroller. Used in combination with an assembler package (RA78K0S) and device file (DF789178) (both sold separately). **<Caution when used in PC environment>** The C compiler package is a DOS-based application but may be used in the Windows environment by using the project manager of Windows (included in the assembler package).
	Part number: μS××××CC78K0S
DF789178[Note 1] Device file	File containing the information inherent to the device. Used in combination with the RA78K0S, CC78K0S, ID78K0S-NS, and SM78K0S (all sold separately).
	Part number: μS××××DF789178
CC78K0S-L[Note 2] C library source file	Source file of functions for generating an object library included in the C compiler package. Necessary for changing the object library included in the C compiler package according to the customer's specifications. Since this is a source file, its working environment does not depend on any particular operating system.
	Part number: μS××××CC78K0S-L

Notes 1. DF789178 is a common file that can be used with the RA78K0S, CC78K0S, ID78K0S-NS, and SM78K0S.

2. CC78K0S-L is not included in the software package (SP78K0S).

Remark ×××× in the part number differs depending on the host machine and operating system to be used.

μS××××RA78K0S
μS××××CC78K0S

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT compatible	Japanese Windows	3.5" 2HD FD
BB13		English Windows	
AB17		Japanese Windows	CD-ROM
BB17		English Windows	
3P17	HP9000 series 700™	HP-UX™ (Rel. 10.10)	
3K17	SPARCstation™	SunOS™ (Rel. 4.1.4), Solaris™ (Rel. 2.5.1)	

μS××××DF789178
μS××××CC78K0S-L

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT compatible	Japanese Windows	3.5" 2HD FD
BB13		English Windows	
3P16	HP9000 series 700	HP-UX (Rel. 10.10)	DAT
3K13	SPARCstation	SunOS (Rel. 4.1.4), Solaris (Rel. 2.5.1)	3.5" 2HD FD
3K15			1/4-inch CGMT

A.3 Control Software

Project manager	Control software created for efficient development of the user program in the Windows environment. User program development operations such as editor startup, build, and debugger startup can be performed from the project manager. <Caution> The project manager is included in the assembler package (RA78K0S). The project manager is used only in the Windows environment.

A.4 Flash Memory Writing Tools

Flashpro III (FL-PR3, PG-FP3) Flashpro IV (FL-PR4, PG-FP4) Flash programmer	Dedicated flash programmer for microcontrollers incorporating flash memory
FA-44GB-8ES FA-48GA Flash memory writing adapter	Adapter for writing to flash memory and connected to Flashpro III or Flashpro IV. • FA-44GB-8ES: For 44-pin plastic LQFP (GB-8ES type) • FA-48GA: For 48-pin plastic TQFP (GA-9EU type)

Remark The FL-PR3, FL-PR4, FA-44GB-8ES, and FA-48GA are products made by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

A.5 Debugging Tools (Hardware)

IE-78K0S-NS In-circuit emulator		In-circuit emulator for debugging hardware and software of an application system using the 78K/0S Series. Supports the integrated debugger (ID78K0S-NS). Used in combination with an AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-78K0S-NS-A In-circuit emulator		The IE-78K0S-NS-A provides a coverage function in addition to the IE-78K0S-NS functions, thus enhancing the debug functions, including the tracer and timer functions.
IE-70000-MC-PS-B AC adapter		Adapter for supplying power from an AC 100 to 240 V outlet.
IE-70000-98-IF-C Interface adapter		Adapter necessary when using a PC-9800 series PC (except notebook type) as the host machine (C bus supported)
IE-70000-CD-IF-A PC card interface		PC card and interface cable necessary when using a notebook PC as the host machine (PCMCIA socket supported)
IE-70000-PC-IF-C Interface adapter		Interface adapter necessary when using an IBM PC/AT compatible as the host machine (ISA bus supported)
IE-70000-PCI-IF-A Interface adapter		Adapter necessary when using a personal computer incorporating a PCI bus as the host machine
IE-789177-NS-EM1 Emulation board		Board for emulating the peripheral hardware inherent to the device. Used in combination with an in-circuit emulator.
NP-44GB-TQ NP-H44GB-TQ Emulation probe		Probe to connect the in-circuit emulator and target system. Used in combination with the TGB-044SAP.
	TGB-044SAP Conversion adapter	Conversion socket to connect the NP-44GB-TQ, NP-H44GB-TQ and a target system board on which a 44-pin plastic LQFP (GB-8ES type) can be mounted.
NP-48GA Emulation probe		Cable to connect the in-circuit emulator and target system. Used in combination with the TGA-048SDP.
	TGA-048SDP Conversion adapter	Conversion adapter to connect the NP-48GA and a target system board on which a 48-pin plastic TQFP (fine pitch) (GA-9EU type) can be mounted

Remarks 1. The NP-44GB-TQ and NP-H44GB-TQ are products made by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

2. The TGB-044SAP and TGA-048SDP are products made by TOKYO ELETECH CORPORATION.
For further information, contact: Daimaru Kogyo, Ltd.
Tokyo Electronics Department (TEL +81-3-3820-7112)
Osaka Electronics Department (TEL +81-6-6244-6672)

A.6 Debugging Tools (Software)

ID78K0S-NS Integrated debugger	This debugger supports the in-circuit emulators IE-78K0S-NS and IE-78K0S-NS-A for the 78K/0S Series. The ID78K0S-NS is Windows-based software. It has improved C-compatible debugging functions and can display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. Used in combination with a device file (DF789178) (sold separately).
	Part number: μS××××ID78K0S-NS
SM78K0S System simulator	This is a system simulator for the 78K/0S Series. The SM78K0S is Windows-based software. It can be used to debug the target system at C source level or assembler level while simulating the operation of the target system on the host machine. Using SM78K0S, the logic and performance of the application can be verified independently of hardware development. Therefore, the development efficiency can be enhanced and the software quality can be improved. Used in combination with a device file (DF789178) (sold separately).
	Part number: μS××××SM78K0S
DF789178[Note] Device file	File containing the information inherent to the device. Used in combination with the RA78K0S, CC78K0S, ID78K0S-NS, and SM78K0S (all sold separately).
	Part number: μS××××DF789178

Note DF789178 is a common file that can be used with the RA78K0S, CC78K0S, ID78K0S-NS, and SM78K0S.

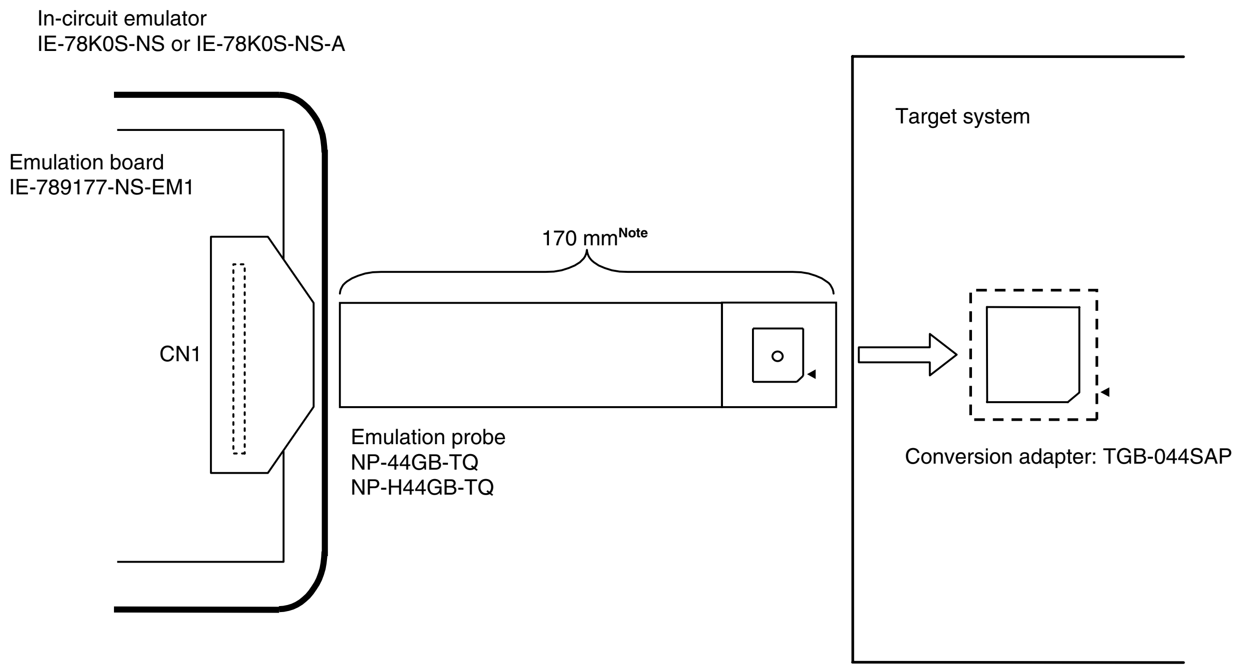
Remark ×××× in the part number differs depending on the operating system and supply medium to be used.

μS××××ID78K0S-NS
μS××××SM78K0S

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series IBM PC/AT compatible	Japanese Windows	3.5" 2HD FD
BB13		English Windows	
AB17		Japanese Windows	CD-ROM
BB17		English Windows	

The following shows the conditions when connecting the emulation probe to the conversion connector or conversion socket. Follow the configuration below and consider the shape of parts to be mounted on the target system when designing a system.

Figure B-1. Distance Between In-Circuit Emulator and Conversion Socket (NP-44GB-TQ)

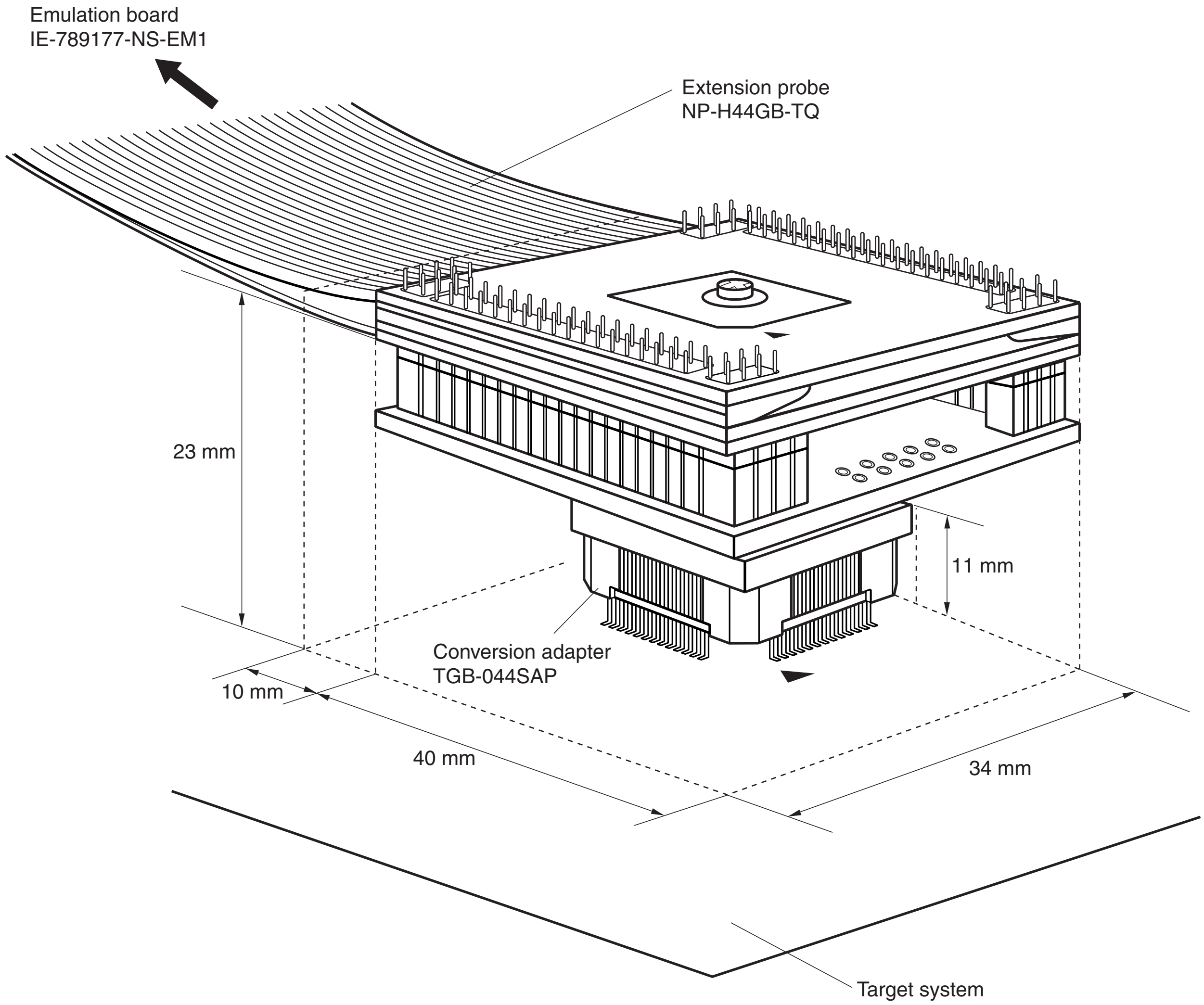


Note Distance when NP-44GB-TQ is used. When NP-H44GB-TQ is used, the distance is 370 mm.

Remarks 1. NP-44GB-TQ and NP-H44GB-TQ are products of Naito Densei Machida Mfg. Co., Ltd.

2. TGB-044SAP is a product of TOKYO ELETECH CORPORATION.

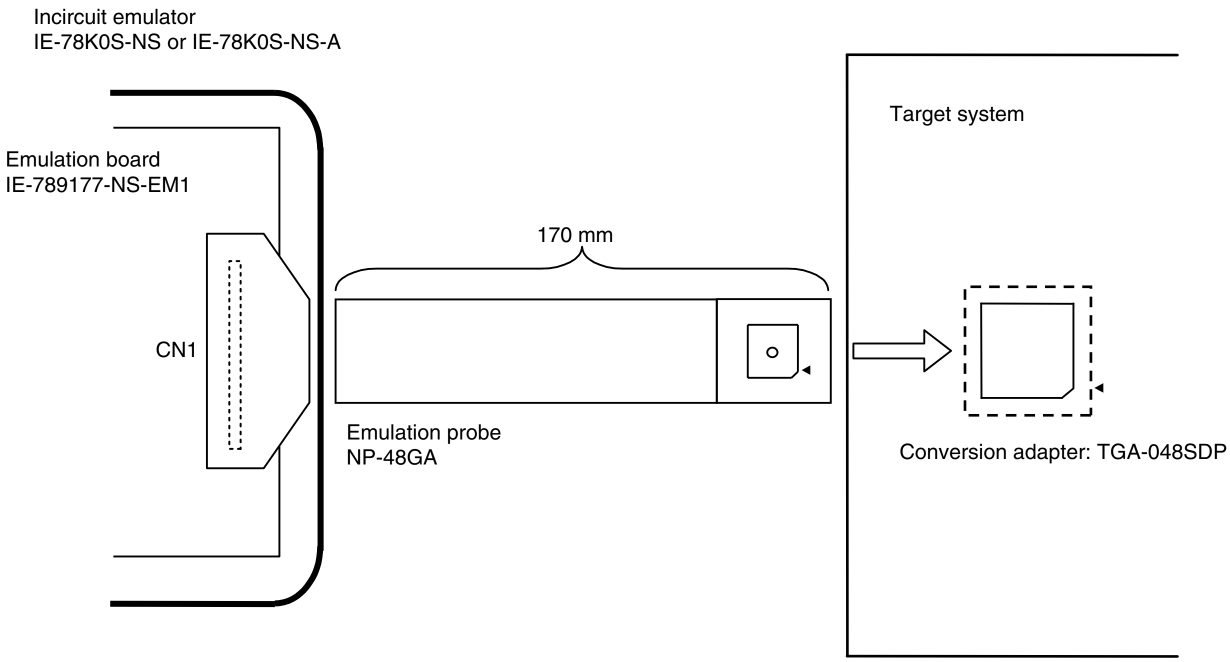
Figure B-2. Connection Condition of Target System (NP-H44GB-TQ)



Remarks **1.** NP-H44GB-TQ is a product of Naito Densei Machida Mfg. Co., Ltd.

2. TGB-044SAP is a product of TOKYO ELETECH CORPORATION.

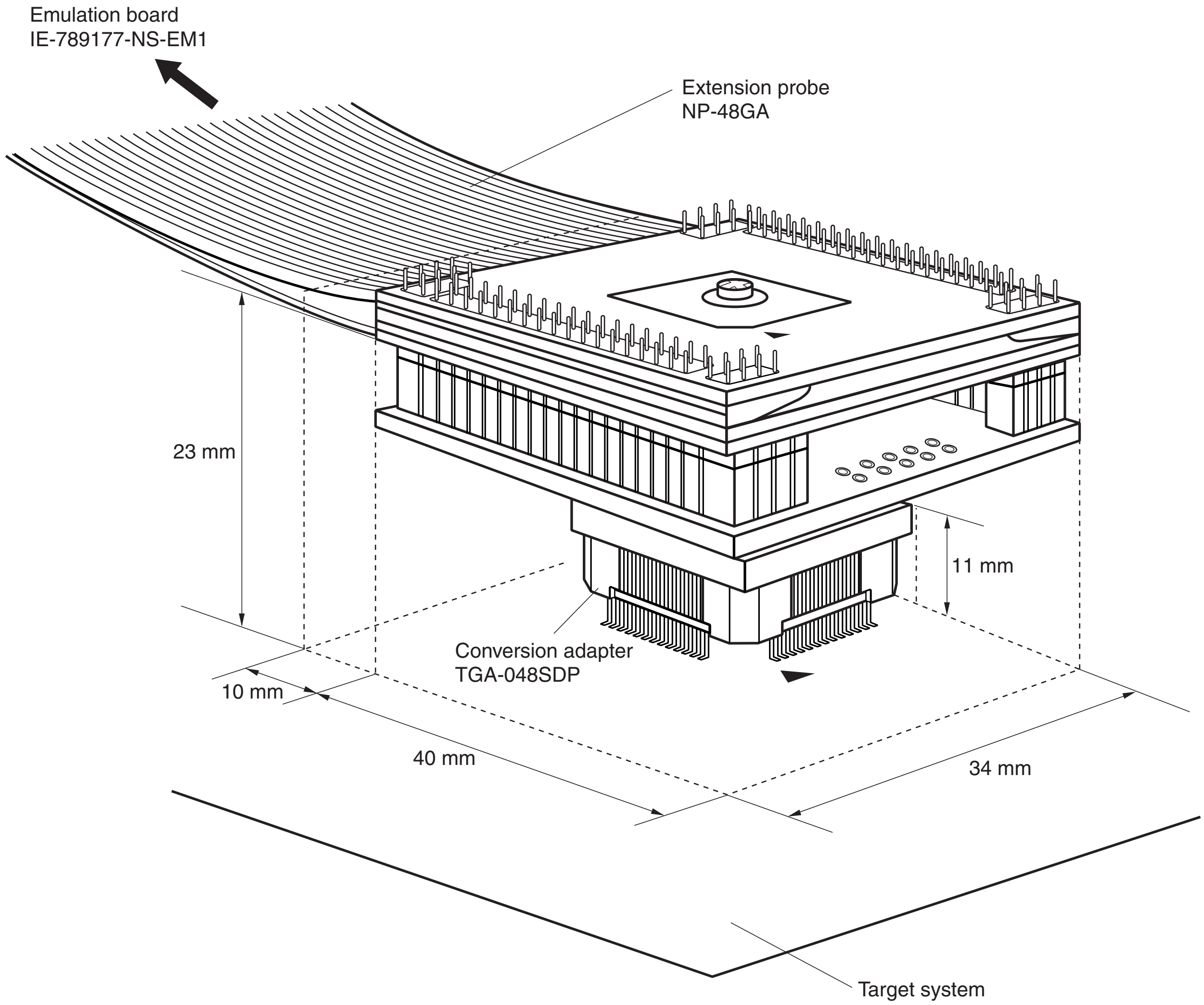
Figure B-3. Distance Between In-Circuit Emulator and Conversion Socket (NP-48GA)



Remarks **1.** NP-48GA is a product of Naito Densei Machida Mfg. Co., Ltd.

2. TGA-048SDP is a product of TOKYO ELETECH CORPORATION.

Figure B-4. Connection Condition of Target System (NP-48GA)



Remarks **1.** NP-48GA is a product of Naito Densei Machida Mfg. Co., Ltd.

2. TGA-048SDP is a product of TOKYO ELETECH CORPORATION.

APPENDIX C REGISTER INDEX

C.1 Register Name Index

C.2 Register Symbol Index

[A]

[B]

[C]

[I]

[M]

[O]

[P]

APPENDIX D REVISION HISTORY

D.1 Major Revisions in This Edition

Page	Description
	CHAPTER 1 GENERAL (μPD789167 AND 789177 SUBSERIES)
pp. 21-24	• Addition of lead-free products μPD789166GB-×××-8ES-A, μPD789166GA-×××-9EU-A, μPD789167GB-×××-8ES-A, μPD789167GA-×××-9EU-A, μPD789176GB-×××-8ES-A, μPD789176GA-×××-9EU-A, μPD789177GB-×××-8ES-A, μPD789177GA-×××-9EU-A, μPD78F9177GB-8ES-A, μPD78F9177AGB-8ES-A, μPD78F9177AGA-9EU-A
pp. 26-28	• Update of **1.5 78K/0S Series Lineup**
	CHAPTER 2 GENERAL (μPD789167Y AND 789177Y SUBSERIES)
pp. 35-38	• Addition of lead-free products μPD789166YGB-×××-8ES-A, μPD789166YGA-×××-9EU-A, μPD789167YGB-×××-8ES-A, μPD789167YGA-×××-9EU-A, μPD789176YGB-×××-8ES-A, μPD789176YGA-×××-9EU-A, μPD789177YGB-×××-8ES-A, μPD789177YGA-×××-9EU-A, μPD78F9177YGB-8ES-A, μPD78F9177AYGA-9EU-A, μPD78F9177AYGB-8ES-A, μPD78F9177AYGA-9EU-A
p. 40	• Update of **2.5 78K/0S Series Lineup**
	CHAPTER 3 PIN FUNCTIONS (μPD789167 AND 789177 SUBSERIES)
p. 51	• Addition of descriptions in **3.2.15 V_{PP} (flash memory version only)**
	CHAPTER 4 PIN FUNCTIONS (μPD789167Y AND 789177Y SUBSERIES)
p. 59	• Addition of descriptions in **4.2.15 V_{PP} (flash memory version only)**
	CHAPTER 9 8-BIT TIMER/EVENT COUNTERS 80 TO 82
p. 144	• Modification of **Figure 9-10 External Event Counter Operation Timing (with Rising Edge Specified)**
	CHAPTER 32 RECOMMENDED SOLDERING CONDITIONS
p. 444	• Addition of recommended soldering conditions for the lead-free products

The mark ★ shows major revised points.

D.2 Revision History up to Previous Edition

Revisions up to the previous edition are shown below. The "Applied to" column indicates the chapter in each edition to which the revision was applied.

(1/3)

Edition	Revision from Previous Edition	Applied to:
Second edition	Addition of description of μPD789166Y, μPD789167Y, μPD789176Y, and μPD789177Y	Throughout
	Change of status of μPD789166, μPD789167, μPD789176, and μPD789177 from "under development" to "developed"	
	Addition of description of SMB0 special function registers to Table 5-3 Special Function Registers	CHAPTER 5 CPU ARCHITECTURE
	Modification of Figure 6-5 Block Diagram of P21	CHAPTER 6 PORT FUNCTIONS
	Addition of 8.5 Notes on Using 16-Bit Timer	CHAPTER 8 16-BIT TIMER
	Addition of 15 SMB0 (μPD789167Y AND 789177Y SUBSERIES)	CHAPTER 15 SMB0 (μPD789167Y AND 789177Y SUBSERIES)
	Addition of description of SMB0 interrupt to 17 INTERRUPT FUNCTIONS	CHAPTER 17 INTERRUPT FUNCTIONS
	Addition of Figure 20-3 Flashpro III Connection in SMB Mode	CHAPTER 20 μPD78F9177 AND μPD78F9177Y
	Addition of setting with SMB mode in Table 20-4 Setting with PG-FP3	
	Addition of development tools for μPD789166Y, μPD789167Y, μPD789176Y, and μPD789177Y	APPENDIX A DEVELOPMENT TOOLS
Third edition	• Addition of μPD789166(A), 789167(A), 789176(A), 789177(A), 789166Y(A), 789167Y(A), 789176Y(A), 789177Y(A), 789166(A1), 789167(A1), 789176(A1), 789177(A1), 789166(A2), 789167(A2), 789176(A2), 789177(A2), 78F9177A, 78F9177AY, 78F9177A(A), 78F9177AY(A), and 78F9177A(A1) • Addition of description on expanded-specification products (10 MHz)	Throughout
	• Addition of description on generic terms used in this manual • Change of Related Documents	INTRODUCTION
	• Addition of 1.1 Expanded-Specification Products and Conventional Products • Addition of 1.10 Differences Between Standard Quality Grade Products and (A) Products, (A1) Products, and (A2) Products	CHAPTER 1 GENERAL (μPD789167 AND 789177 SUBSERIES)
	• Addition of 2.1 Expanded-Specification Products and Conventional Products • Addition of 2.10 Differences Between Standard Quality Grade Products and (A) Products	CHAPTER 2 GENERAL (μPD789167Y AND 789177Y SUBSERIES)
	• Modification of V_{PP} pin connection in 3.2.15 V_{PP} (flash memory version only) and Table 3-1 Types of I/O Circuits for Each Pin and Recommended Connection of Unused Pins	CHAPTER 3 PIN FUNCTIONS (μPD789167 AND 789177 SUBSERIES)
	• Addition of Note to Figure 7-3 Format of Suboscillation Mode Register	CHAPTER 7 CLOCK GENERATOR
	• Modification of description in 8.4.1 Operation as timer interrupt • Modification of description in 8.4.2 Operation as timer output	CHAPTER 8 16-BIT TIMER 90

(2/3)

Edition	Revision from Previous Edition	Applied to:
Third edition	• Addition of 9.5 (4) Cautions when set to STOP mode • Addition of 9.5 (5) Start timing of external event counter	CHAPTER 9 8-BIT TIMER/EVENT COUNTERS 80 TO 82
	• Addition of 12.5 (8) Input impedance of ANI0 to ANI7 pins	CHAPTER 12 8-BIT A/D CONVERTER (μPD789167 AND 789167Y SUBSERIES)
	• Modification of description in 13.2 (2) A/D conversion result register 0 (ADCR0) • Modification of Figure 13-4 Basic Operation of 10-Bit A/D Converter • Addition of 13.5 (8) Input impedance of ANI0 to ANI7 pins	CHAPTER 13 10-BIT A/D CONVERTER (μPD789177 AND 789177Y SUBSERIES)
	• Modification of Figure 14-1 Block Diagram of Serial Interface 20 • Modification of description on PE20 flag in Figure 14-5 Format of Asynchronous Serial Interface Status Register 20 • Addition of 14.4.2 (2) (f) Reading receive data	CHAPTER 14 SERIAL INTERFACE 20
	• Overall revision of description on flash memory programming	CHAPTER 20 FLASH MEMORY VERSION
	• Addition of electrical specifications	CHAPTER 23, 25, 27, 29, and 31 ELECTRICAL SPECIFICATIONS
	• Addition of characteristics curves	CHAPTER 24, 26, 28, 30, and 32 CHARACTERISTICS CURVES
	• Addition of package drawings	CHAPTER 33 PACKAGE DRAWINGS
	• Addition of recommended soldering conditions	CHAPTER 34 RECOMMENDED SOLDERING CONDITIONS
	• Overall revision of description on development tools • Deletion of embedded software	APPENDIX A DEVELOPMENT TOOLS
Fourth edition	Change of Related Documents	INTRODUCTION
	• Deletion of SMB from block diagram in 1.8	CHAPTER 1 GENERAL (μPD789167 AND 789177 SUBSERIES)
	• Deletion of P60 to P67 from Table 6-3 Port Mode Register and Output Latch Settings for Using Alternate Functions	CHAPTER 6 PORT FUNCTIONS
	• Modification of Figures 8-6 Timing of Timer Interrupt Operation and 8-8 Timer Output Timing	CHAPTER 8 16-BIT TIMER 90
	• Change of description of Cautions in 9.5 Notes on Using 8-Bit Timer/Event Counters 80 to 82	CHAPTER 9 8-BIT TIMER/EVENT COUNTERS 80 TO 82
	• Modification of Notes in Figure 12-2 Format of A/D Converter Mode Register 0	CHAPTER 12 8-BIT A/D CONVERTER (μPD789167 AND 789167Y SUBSERIES)
	• Modification of Notes in Figure 13-2 Format of A/D Converter Mode Register 0	CHAPTER 13 10-BIT A/D CONVERTER (μPD789177 AND 789177Y SUBSERIES)
	• Modification of Figure 14-1 Block Diagram of Serial Interface 20 • Modification of description of Cautions in Figure 14-6 Format of Baud Rate Generator Control Register 20 • Addition of 14.3 (4) (c) Generation of serial clock from system clock input to 3-wire serial I/O mode	CHAPTER 14 SERIAL INTERFACE 20

(3/3)

Edition	Revision from Previous Edition	Applied to:
Fourth edition	• Addition of description of SMBM0 to **15.4.1 Start condition** • Addition of description of **15.4.7 (7) Slave operation (after stop mode is released)** • Modification of **Table 15-3 INTSMB0 Generation Timing and Wait Control** • Addition of **15.4.8 (6) Start condition detection** • Addition and modification of description of **Notes** in **Figure 15-20 Master → Slave Communication Example (When 9-Clock Wait Is Selected for Both Master and Slave)** and **Figure 15-21. Slave → Master Communication Example (When 9-Clock Wait Is Selected for Both Master and Slave)**	CHAPTER 15 SMB0 (μPD789167Y AND 789177Y SUBSERIES)
	• Addition of **Caution** in **Figure 17-2 Format of Interrupt Request Flag Register**	CHAPTER 17 INTERRUPT FUNCTIONS
	• Modification of **Table 20-2 Communication Mode List** and **Table 20-3 Pin Connection List** • Addition of description of pseudo 3-wire mode to **Figure 20-3 Example of Connection with Dedicated Flash Programme**r and **Figure 20-9 Wiring Example for Flash Writing Adapter in 3-Wire Serial I/O Mode (SIO-ch1) or Pseudo 3-Wire Mode**	CHAPTER 20 FLASH MEMORY VERSION
	• Modification of electrical specifications	CHAPTERS 23, 25, 27, 28, 30 ELECTRICAL SPECIFICATIONS
	• Addition of chapter	APPENDIX B NOTES ON TARGET SYSTEM DESIGN
Fifth edition	Addition of 48-pin plastic TQFP (fine pitch) (7 × 7) to μPD789167, 789177 Subseries μPD789166GA-×××-9EU, μPD789167GA-×××-9EU, μPD789176GA-×××-9EU, μPD789177GA-×××-9EU, μPD78F9177AGA-9EU	Throughout
	• Addition of description on IC3 to **3.1 (2) Non-port pins** • Addition of **3.2.17 IC3** • Addition of description on IC3 to **Table 3-1 Types of I/O Circuits for Each Pin and Recommended Connection of Unused Pins**	CHAPTER 3 PIN FUNCTIONS (μPD789167 AND 789177 SUBSERIES)