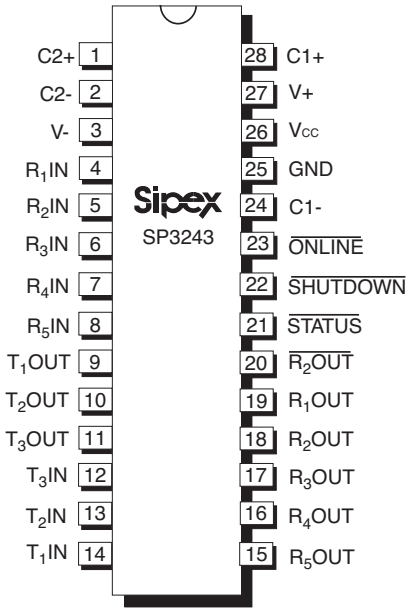
3 Driver/5 Receiver Intelligent +3.0V to +5.5V RS-232 Transceivers

FEATURES

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- ***AUTO ON-LINE®*** circuitry automatically wakes up from a 1μA shutdown
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V_{CC} Variations
- Enhanced ESD Specifications:
  ±15kV Human Body Model
  ±15kV IEC1000-4-2 Air Discharge
  ±8kV IEC1000-4-2 Contact Discharge
- 250 Kbps min. transmission rate (EB)
- 1000 Kbps min. transmission rate (EU)
- Ideal for High Speed RS-232 Applications



Now Available in Lead Free Packaging

DESCRIPTION

The SP3243 products are 3 driver/5 receiver RS-232 transceiver solutions intended for portable or hand-held applications such as notebook and palmtop computers. The SP3243 includes one complementary receiver that remains alert to monitor an external device's Ring Indicate signal while the device is shutdown. The SP3243E and EB devices feature slew-rate limited outputs for reduced crosstalk and EMI. The "U" and "H" series are optimized for high speed with data rates up to 1Mbps, easily meeting the demands of high speed RS-232 applications. The SP3243 series uses an internal high-efficiency, charge-pump power supply that requires only 0.1μF capacitors in 3.3V operation. This charge pump and Sipex's driver architecture allow the SP3243 series to deliver compliant RS-232 performance from a single power supply ranging from +3.0V to +5.5V. The AUTO ON-LINE® feature allows the device to automatically "wake-up" during a shutdown state when an RS-232 cable is connected and a connected peripheral is turned on. Otherwise, the device automatically shuts itself down drawing less than 1μA.

SELECTION TABLE

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	AUTO ON-LINE® Circuitry	TTL 3-State	# of Pins	Gauranteed Data Rate	ESD Rating
SP3243	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28	120	2kV
SP3243E	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28	120	15kV
SP3243B	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28	250	2kV
SP3243EB	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28	250	15kV
SP3243U	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28	1000	2kV
SP3243EU	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28	1000	15kV

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to +6.0V
V+ (NOTE 1).....-0.3V to +7.0V
V- (NOTE 1).....+0.3V to -7.0V
V+ + |V-| (NOTE 1).....+13V
I_{CC} (DC V_{CC} or GND current).....±100mA

Input Voltages
TxIN, $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$, ...-0.3V to Vcc +6.0V
RxIN.....±15V

Output Voltages
TxOUT.....±13.2V
RxOUT, STATUS.....-0.3V to (V_{CC} +0.3V)

Short-Circuit Duration
TxOUT.....Continuous
Storage Temperature.....-65°C to +150°C

Power Dissipation per package
28-pin SOIC (derate 12.7mW/°C above +70°C)....1000mW
28-pin SSOP (derate 11.2mW/°C above +70°C).....900mW
28-pin TSSOP (derate 13.2mW/°C above +70°C).....1059mW
32-pin MLPQ (derate 29.4mW/°C above +70°C).....2352mW

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with T_{AMB} = T_{MIN} to T_{MAX}, C1 - C4 = 0.1µF. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current,AUTO ON-LINE®		1.0	10	µA	All RxIN open, $\overline{\text{ONLINE}}$ = GND, $\overline{\text{SHUTDOWN}}$ = V_{CC}, V_{CC} = +3.3V, T_{AMB} = +25°C, TxIN = GND or V_{CC}
Supply Current, Shutdown		1.0	10	µA	$\overline{\text{SHUTDOWN}}$ = GND, V_{CC} = +3.3V, T_{AMB} = +25°C, TxIN = V_{CC} or GND
Supply Current, AUTO ON-LINE® Disabled		0.3	1.0	mA	$\overline{\text{ONLINE}}$ = $\overline{\text{SHUTDOWN}}$ = V_{CC}, no load, V_{CC} = +3.3V, T_{AMB} = +25°C, TxIN = GND or V_{CC}
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW HIGH	 2.4		 0.8	 V V	V_{CC} = +3.3V or +5.0V, TxIN, $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$
Input Leakage Current		±0.01	±1.0	µA	TxIN, $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$, T_{AMB} = +25°C, V_{IN} = 0V to V_{CC}
Output Leakage Current		±0.05	±10	µA	Receivers disabled, V_{OUT} = 0V to V_{CC}
Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
Output Voltage HIGH	V_{CC} - 0.6	V_{CC} - 0.1		V	I_{OUT} = -1.0mA
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±5.4		V	All driver outputs loaded with 3KΩ to GND, T_{AMB} = +25°C
Output Resistance	300			Ω	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V
Output Short-Circuit Current		±35	±60	mA	V_{OUT} = 0V
Output Leakage Current			±25	µA	V_{CC} = 0V or 3.0V to 5.5V, V_{OUT} = ±12V, Drivers disabled

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with $T_{AMB} = T_{MIN}$ to T_{MAX}, C1 - C4 = 0.1µF. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER INPUTS					
Input Voltage Range	-15		15	V	
Input Threshold LOW	0.6	1.2		V	V_{CC} = 3.3V
Input Threshold LOW	0.8	1.5		V	V_{CC} = 5.0V
Input Threshold HIGH		1.5	2.4	V	V_{CC} = 3.3V
Input Threshold HIGH		1.8	2.4	V	V_{CC} = 5.0V
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	kΩ	
AUTO ON-LINE® CIRCUITRY CHARACTERISTICS ($\overline{ONLINE}$ = GND, $\overline{SHUTDOWN}$ = V_{CC}) 25°C					
$\overline{STATUS}$ Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
$\overline{STATUS}$ Output Voltage HIGH	V_{CC} - 0.6			V	I_{OUT} = -1.0mA
Receiver Threshold to Drivers Enabled (t_{ONLINE})		350		µS	Figure 20
Receiver Positive or Negative Threshold to $\overline{STATUS}$ HIGH (t_{STSH})		0.2		µS	Figure 20
Receiver Positive or Negative Threshold to $\overline{STATUS}$ LOW (t_{STSL})		30		µS	Figure 20
TIMING CHARACTERISTICS					
Maximum Data Rate (U) (H) (B) (-)	1000 460 250 120			Kbps	R_L = 3KΩ, C_L = 250pF, one driver active R_L = 3KΩ, C_L = 1000pF, one driver active R_L = 3KΩ, C_L = 1000pF, one driver active. R_L = 3KΩ, C_L = 1000pF, one driver active
Receiver Propagation Delay t_{PHL} t_{PLH}		 0.15 0.15		µs	Receiver input to Receiver output, C_L = 150pF
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew (E, EB) (EU)		100 50	500 100	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Receiver Skew		50		ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Transition-Region Slew Rate (U) (EB)	 6	90	 30	V/µs	V_{CC} = 3.3V, R_L = 3KΩ, T_{AMB} = 25°C, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 1000kbps data rate, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

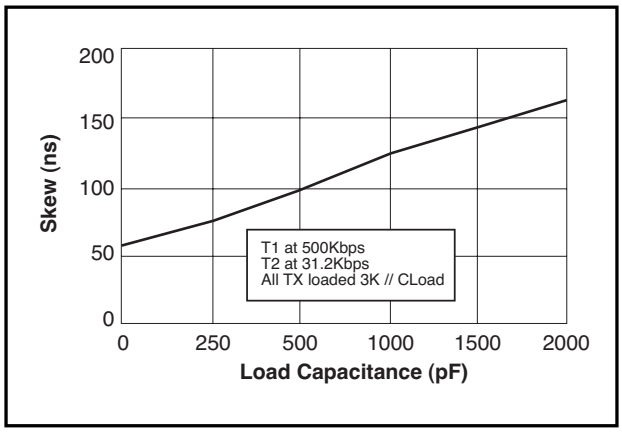


Figure 1. Transmitter Skew VS. Load Capacitance

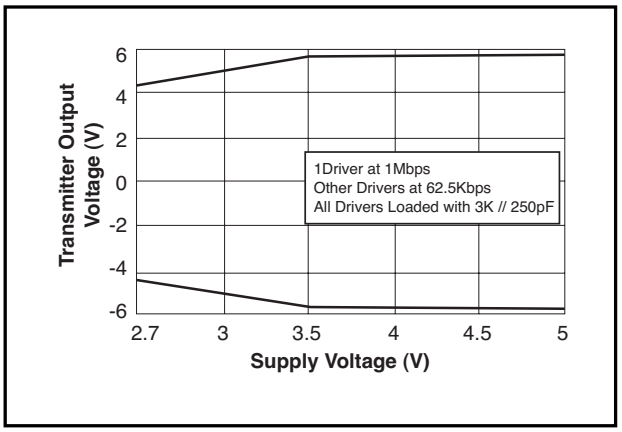


Figure 2. Transmitter Output Voltage VS. Supply Voltage for the SP3243EU

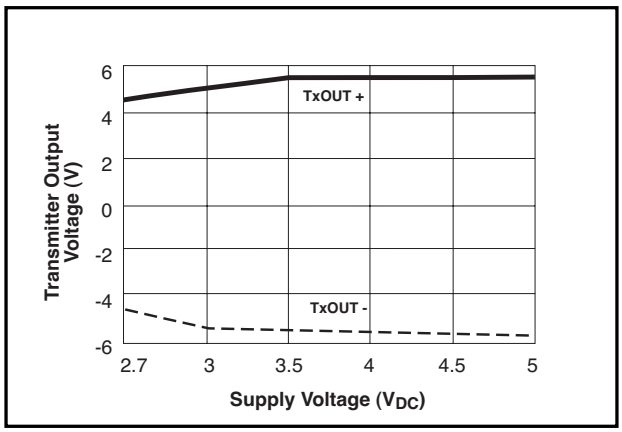


Figure 3. Transmitter Output Voltage VS. Load Capacitance for the SP3243EU

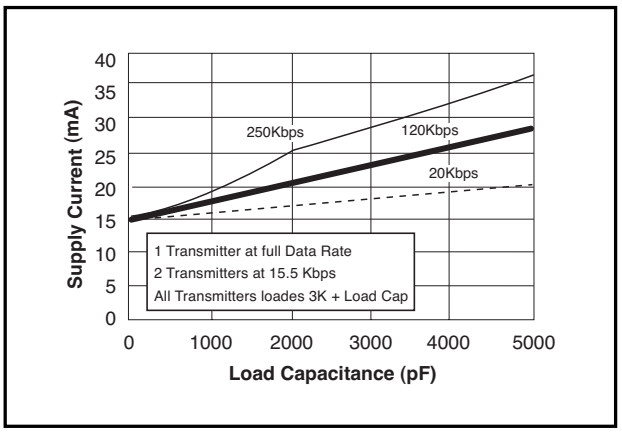


Figure 4. Supply Current VS. Load Capacitance for the SP3243EU

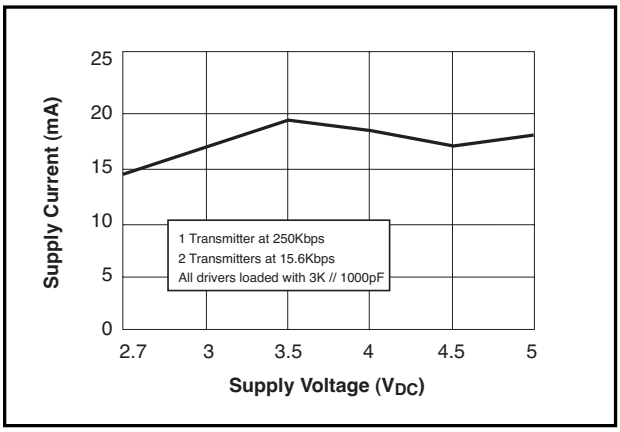


Figure 5. Supply Current VS. Supply Voltage for the SP3243EU

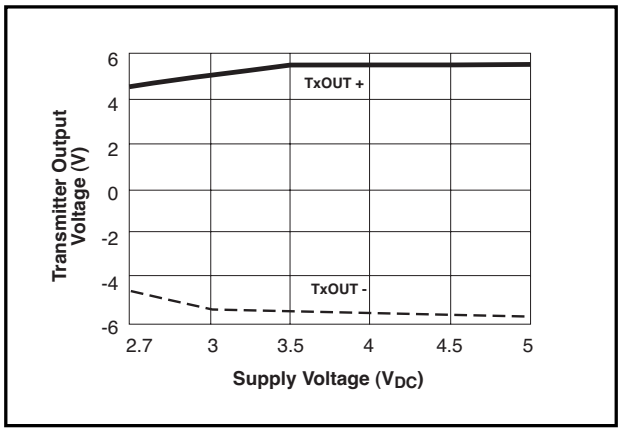


Figure 6. Transmitter Output Voltage VS. Supply Voltage for the SP3243EU

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 1000kbps data rate, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

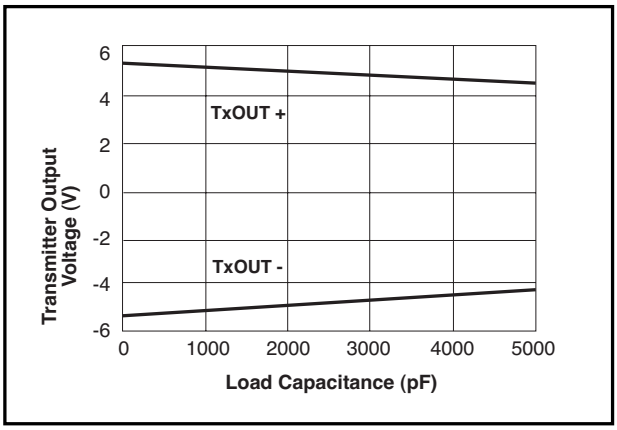


Figure 7. Transmitter Output Voltage VS. Load Capacitance

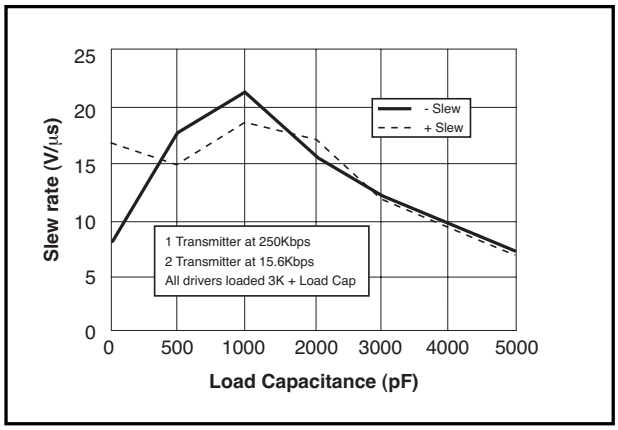


Figure 8. Slew Rate VS. Load Capacitance

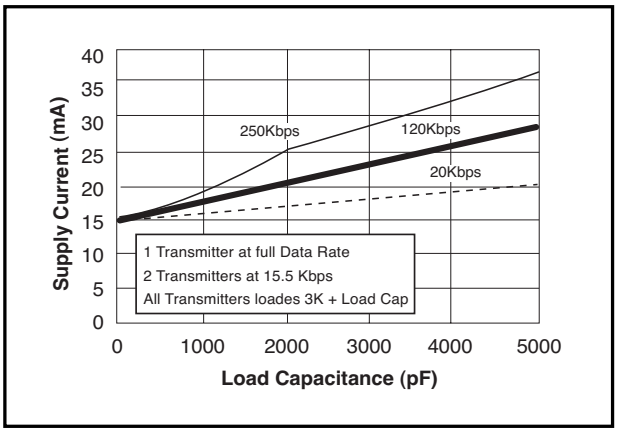


Figure 9. Supply Current VS. Load Capacitance

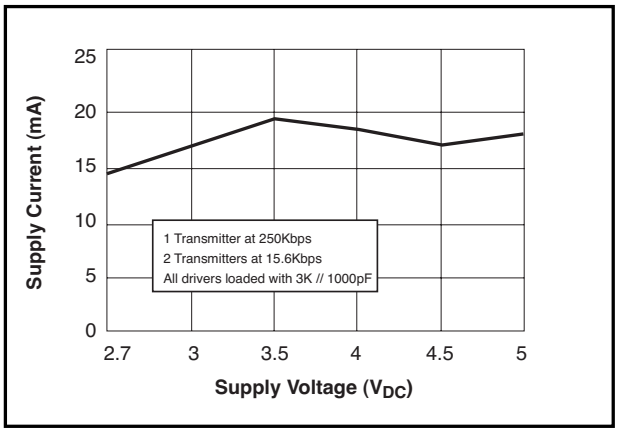


Figure 10. Supply Current VS. Supply Voltage

NAME	FUNCTION	PIN NUMBER	
		SP3243EU	SP3243EUCR MLPQ
$\overline{EN}$	Receiver Enable. Apply logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state).	-	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	28	28
V+	Regulated +5.5V output generated by the charge pump.	27	26
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	24	22
C2+	Positive terminal of the inverting charge-pump capacitor.	1	29
C2-	Negative terminal of the inverting charge-pump capacitor.	2	31
V-	Regulated -5.5V output generated by the charge pump.	3	32
R_1IN	RS-232 receiver input.	4	2
R_2IN	RS-232 receiver input.	5	3
R_3IN	RS-232 receiver input.	6	4
R_4IN	RS-232 receiver input.	7	5
R_5IN	RS-232 receiver input.	8	6
R_1OUT	TTL/CMOS receiver output.	19	17
R_2OUT	TTL/CMOS receiver output.	18	16
$\overline{R_2OUT}$	Non-inverting receiver-2 output, active in shutdown.	20	18
R_3OUT	TTL/CMOS receiver output.	17	15
R_4OUT	TTL/CMOS receiver output.	16	14
R_5OUT	TTL/CMOS receiver output.	15	13
$\overline{STATUS}$	TTL/CMOS Output indicating online and shutdown status.	21	19
T_1IN	TTL/CMOS driver input.	14	12
T_2IN	TTL/CMOS driver input.	13	11
T_3IN	TTL/CMOS driver input.	12	10
$\overline{ONLINE}$	Apply logic HIGH to override Auto-Online circuitry keeping drivers active ($\overline{SHUTDOWN}$ must also be logic HIGH, refer to Table 2).	23	21
T_1OUT	RS-232 driver output.	9	7
T_2OUT	RS-232 driver output.	10	8
T_3OUT	RS-232 driver output.	11	9
GND	Ground.	25	23
V_{CC}	+3.0V to +5.5V supply voltage.	26	25
$\overline{SHUTDOWN}$	Apply logic LOW to shut down drivers and charge pump. This overrides all AUTO ON-LINE® circuitry and $\overline{ONLINE}$ (refer to Table 2).	22	20
NC	No Connection	-	1,24,27,30

Table 1. Device Pin Description

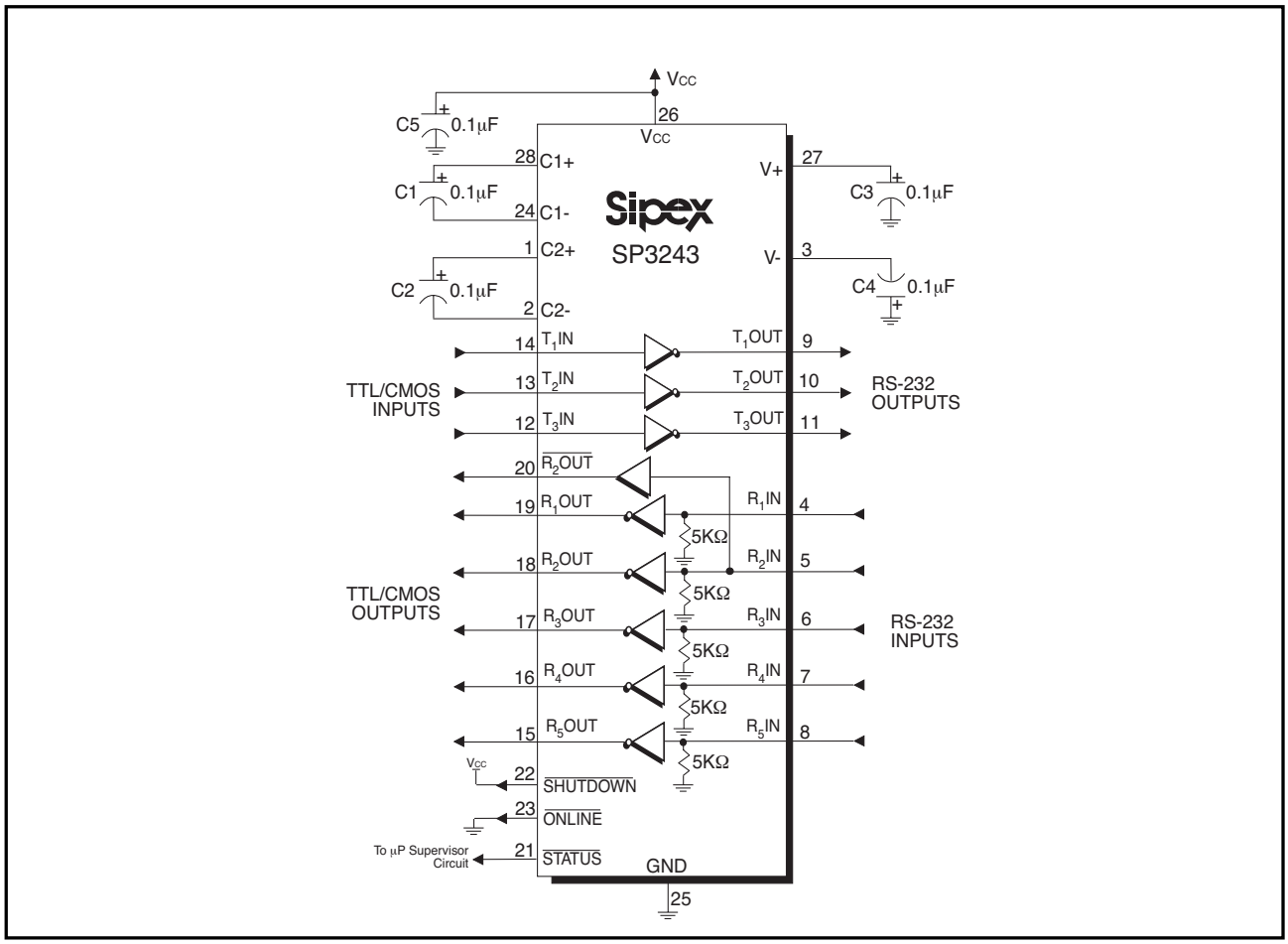


Figure 15. SP3243 Typical Operating Circuit

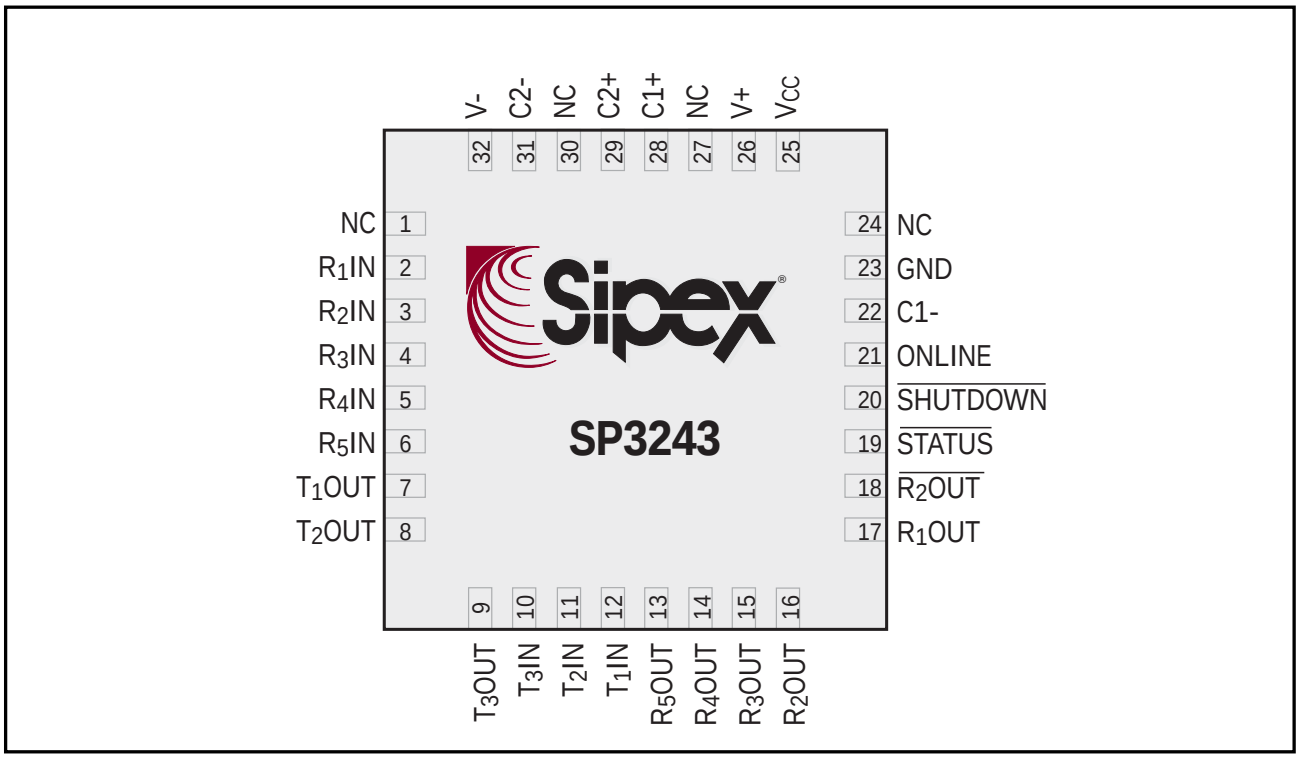


Figure 13. SP3243 QFN Pinout Configuration

DESCRIPTION

The SP3243 transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The SP3243 devices feature Sipex's proprietary and patented (U.S.-- 5,306,954) on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.0V to +5.5V power supply. The SP3243EU devices can operate at a data rate of 1000kbps fully loaded.

The SP3243 is a 3-driver/5-receiver device, ideal for portable or hand-held applications. The SP3243 includes one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown. This aids in protecting the UART or serial controller IC by preventing forward biasing of the protection diodes where V_{CC} may be disconnected.

The SP3243 series is an ideal choice for power sensitive designs. The SP3243 devices feature

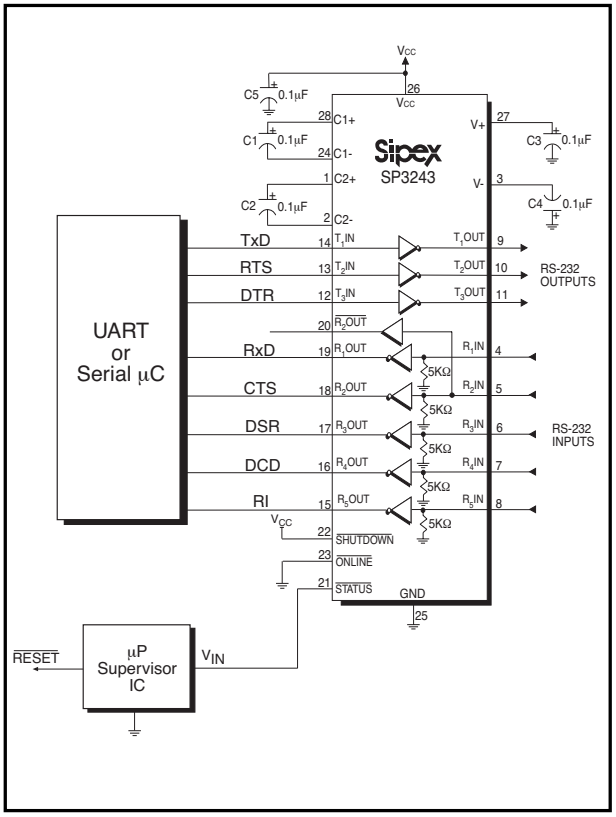


Figure 16. Interface Circuitry Controlled by Microprocessor Supervisory Circuit

AUTO ON-LINE® circuitry which reduces the power supply drain to a 1µA supply current. In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

THEORY OF OPERATION

The SP3243 series is made up of four basic circuit blocks:

1. Drivers
2. Receivers
3. the Sipex proprietary charge pump, and
4. AUTO ON-LINE® circuitry.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232-F and all previous RS-232 versions. Unused drivers inputs should be connected to GND or V_{CC}.

The drivers have a minimum data rate of 250kbps (EB) or 1000kbps (EU) fully loaded.

Figure 17 shows a loopback test circuit used to test the RS-232 Drivers. Figure 18 shows the test results where one driver was active at 1Mbps and all three drivers loaded with an RS-232 receiver in parallel with a 250pF capacitor. Figure 19

DEVICE: SP3243EU			
$\overline{SHUTDOWN}$	T_xOUT	R_xOUT	$\overline{R_2OUT}$
0	High Z	High Z	Active
1	Active	Active	Active

Table 2. $\overline{SHUTDOWN}$ Truth Tables
Note: In AUTO ON-LINE® Mode where $\overline{ONLINE}$ = GND and $\overline{SHUTDOWN}$ = V_{CC}, the device will shut down if there is no activity present at the Receiver inputs.

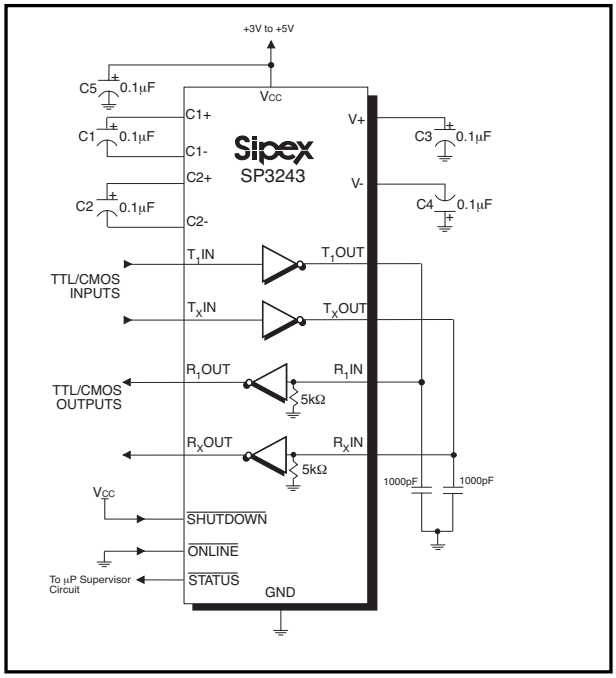


Figure 17. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

shows the test results of the loopback circuit with all drivers active at 250kbps with typical RS-232 loads in parallel with 1000pF capacitors. A superior RS-232 data transmission rate of 1Mbps makes the SP3243EU an ideal match for high speed LAN and personal computer peripheral applications.

Receivers

The receivers convert ±5.0V EIA/TIA-232 levels to TTL or CMOS logic output levels. Receivers are active when the AUTO ON-LINE® circuitry is enabled or when in shutdown. During the shutdown, the receivers will continue to be active. If there is no activity present at the receivers for a period longer than 100µs or when SHUTDOWN is enabled, the device goes into a standby mode where the circuit draws 1µA. The

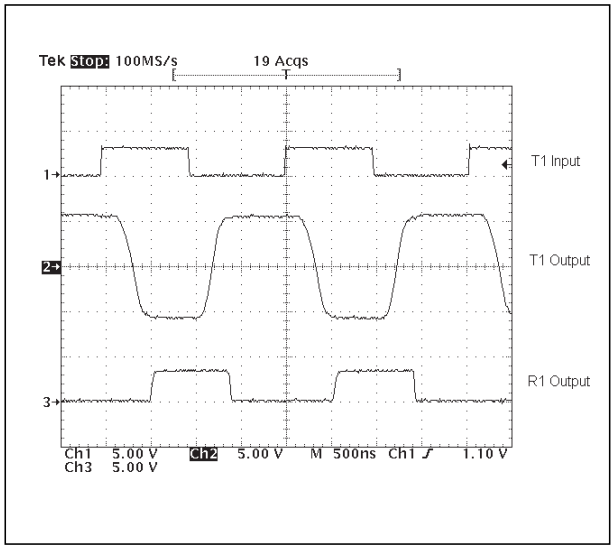


Figure 18. Loopback Test results at 1Mbps

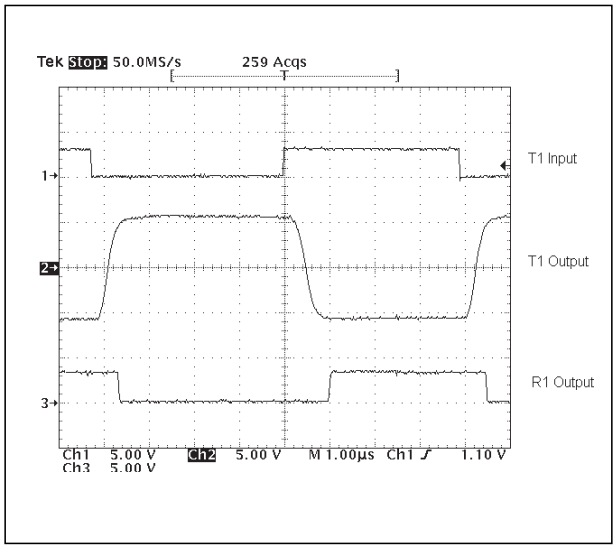


Figure 19. Loopback Test results at 250Kbps

truth table logic of the SP3243 driver and receiver outputs can be found in Table 2.

The SP3243 includes an additional non-inverting receiver with an output R_2OUT. R_2OUT is an extra output that remains active and monitors activity while the other receiver outputs are forced into high impedance. This allows Ring Indicator (RI) from a peripheral to be monitored without forward biasing the TTL/CMOS inputs of the other devices connected to the receiver outputs.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5KΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is a Sipex–patented design (U.S. 5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_4. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $–V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_3, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and $V^–$ are separately generated from V_{CC}, in a no–load condition V^+ and $V^–$ will be symmetrical. Older charge pump approaches that generate $V^–$ from V^+ will show a decrease in the magnitude of $V^–$ compared to V^+ due to the inherent inefficiencies in the design. The clock rate for the charge pump typically operates at greater than 250kHz. The external capacitors can be as low as 0.1μF with a 16V breakdown voltage rating.

Minimum recommended charge pump capacitor value	
Input Voltage V_{CC}	**Charge pump capacitor value for SP32XX**
3.0V to 3.6V	C1 – C4 = 0.1uF
4.5V to 5.5V	C1 = 0.047uF, C2-C4 = 0.33uF
3.0V to 5.5V	C1 – C4 = 0.22uF

The Sipex-patented charge pumps are designed to operate reliably with a range of low cost capacitors. Either polarized or non polarized capacitors may be used. If polarized capacitors are used they should be oriented as shown in the Typical Operating Circuit. The V+ capacitor may be connected to either ground or Vcc.

The charge pump operates with 0.1µF capacitors for 3.3V operation. For other supply voltages, see the table for required capacitor values. Do not use values smaller than those listed. Increasing the capacitor values (e.g., by doubling in value) reduces ripple on the transmitter outputs and may slightly reduce power consumption. C2, C3, and C4 can be increased without changing C1's value.

For best charge pump efficiency locate the charge pump and bypass capacitors as close as possible to the IC. Surface mount capacitors are best for this purpose. Using capacitors with lower equivalent series resistance (ESR) and self-inductance, along with minimizing parasitic PCB trace inductance will optimize charge pump operation. Designers are also advised to consider that capacitor values may shift over time and operating temperature.

AUTO ONLINE CIRCUITRY

The SP3243 devices have a patent pending AUTO ON-LINE® circuitry on board that saves power in applications such as laptop computers, palmtop (PDA) computers and other portable systems.

The SP3243 devices incorporate an AUTO ON-LINE® circuit that automatically enables itself when the external transmitters are enabled and the cable is connected. Conversely, the AUTO ON-LINE® circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1mA. This function can also be externally controlled by the $\overline{\text{ONLINE}}$ pin. When this pin is tied to a logic LOW, the AUTO ON-LINE® function is active. Once active, the device is enabled until there is no activity on the receiver inputs. The receiver input typically sees at least ±3V, which are generated from the transmitters at the other end of the cable with a ±5V minimum. When the external transmitters are disabled or the cable is disconnected, the receiver inputs will be pulled down by their internal 5kΩ resistors to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standy mode. When $\overline{\text{ONLINE}}$ is HIGH, the AUTO ON-LINE® mode is disabled.

The AUTO ON-LINE® circuit has two stages:

1) Inactive Detection
2) Accumulated Delay

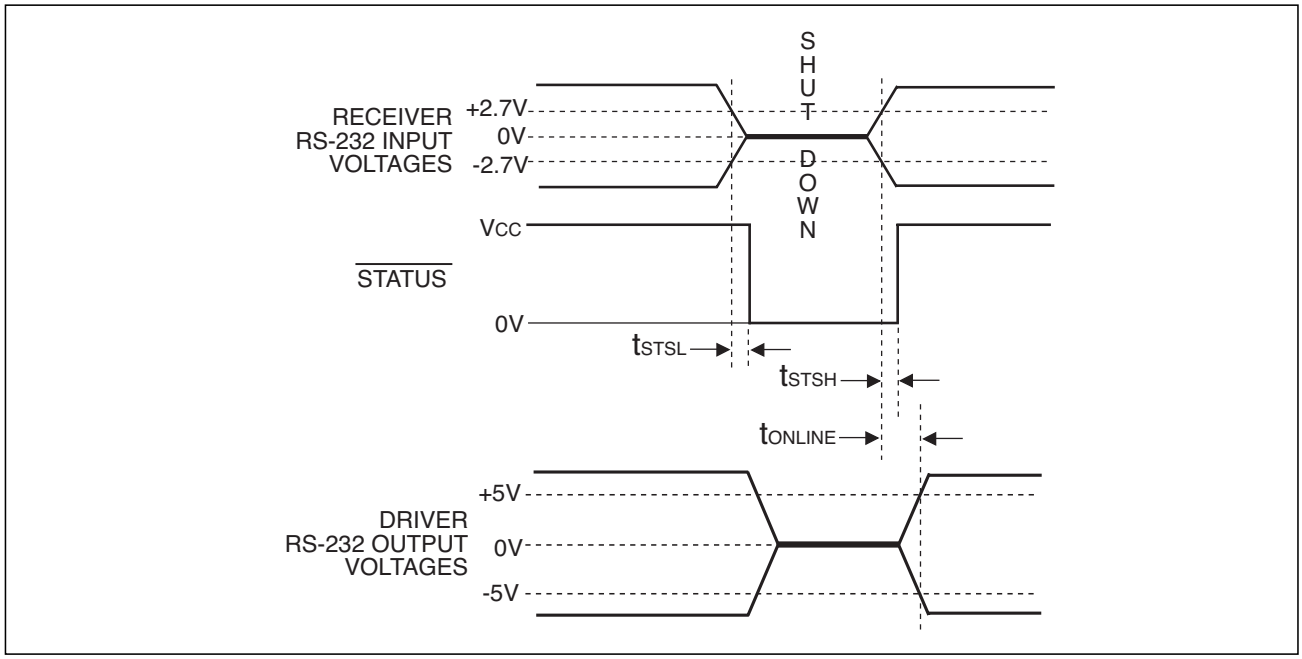


Figure 20. AUTO ON-LINE® Timing Waveforms

The first stage, shown in Figure 28, detects an inactive input. A logic HIGH is asserted on R_XINACT if the cable is disconnected or the external transmitters are disabled. Otherwise, R_XINACT will be at a logic LOW. This circuit is duplicated for each of the other receivers.

The second stage of the AUTO ON-LINE® circuitry, shown in Figure 29, processes all the receiver's R_XINACT signals with an accumulated delay that disables the device to a 1µA supply current.

The $\overline{\text{STATUS}}$ pin goes to a logic LOW when the cable is disconnected, the external transmitters are disabled, or the $\overline{\text{SHUTDOWN}}$ pin is invoked. The typical accumulated delay is around 20µs.

When the SP3243 drivers or internal charge pump are disabled, the supply current is reduced to 1µA. This can commonly occur in hand-held or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are turned off.

The AUTO ON-LINE® mode can be disabled by the $\overline{\text{SHUTDOWN}}$ pin. If this pin is a logic LOW, the AUTO ON-LINE® function will not operate regardless of the logic state of the $\overline{\text{ONLINE}}$ pin. Table 3 summarizes the logic of the AUTO ON-LINE® operating modes. The truth table logic of the SP3243 driver and receiver outputs can be found in Table 2.

The $\overline{\text{STATUS}}$ pin outputs a logic LOW signal if the device is shutdown. This pin goes to a logic HIGH when the external transmitters are enabled and the cable is connected.

When the SP3243 devices are shut down, the charge pumps are turned off. V+ charge pump output decays to V_{CC}, the V- output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V+ and V- levels is typically 200µs.

For easy programming, the $\overline{\text{STATUS}}$ can be used to indicate DSR or a Ring Indicator signal. Tying $\overline{\text{ONLINE}}$ and $\overline{\text{SHUTDOWN}}$ together will bypass the AUTO ON-LINE® circuitry so this connection acts like a shutdown input pin.

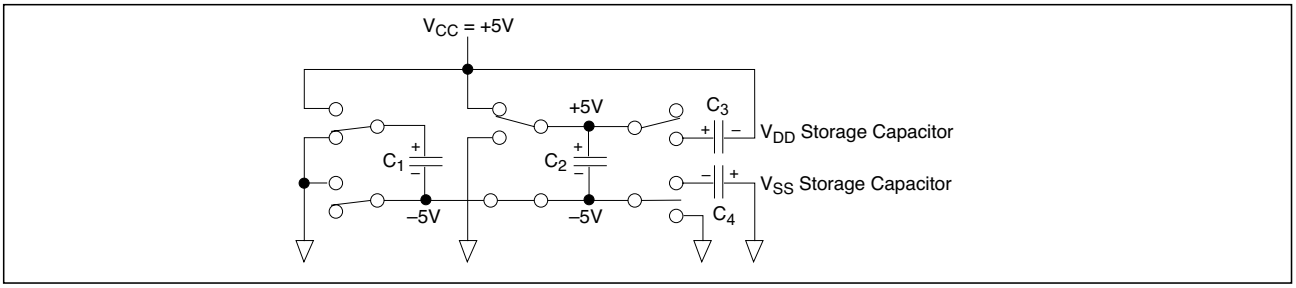


Figure 21. Charge Pump — Phase 1

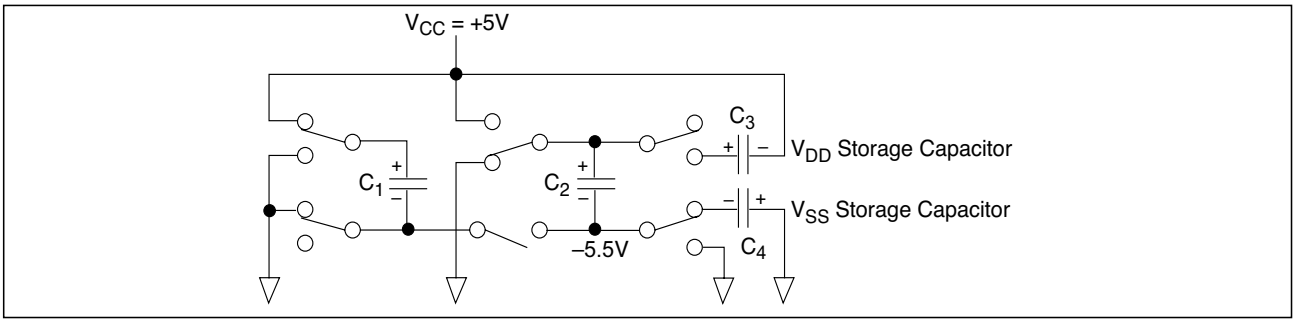


Figure 22. Charge Pump — Phase 2

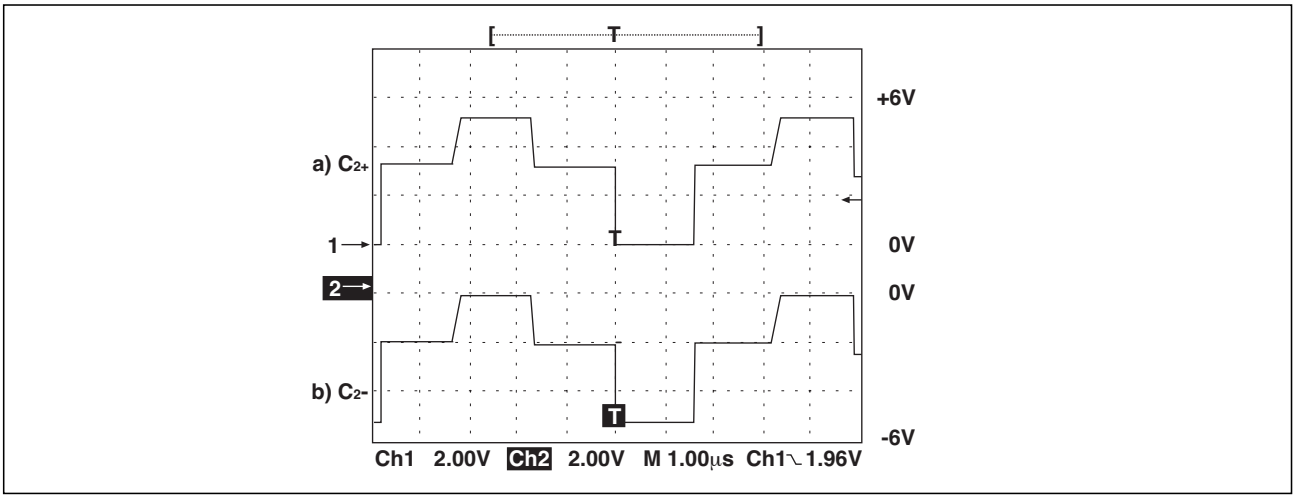


Figure 23. Charge Pump Waveforms

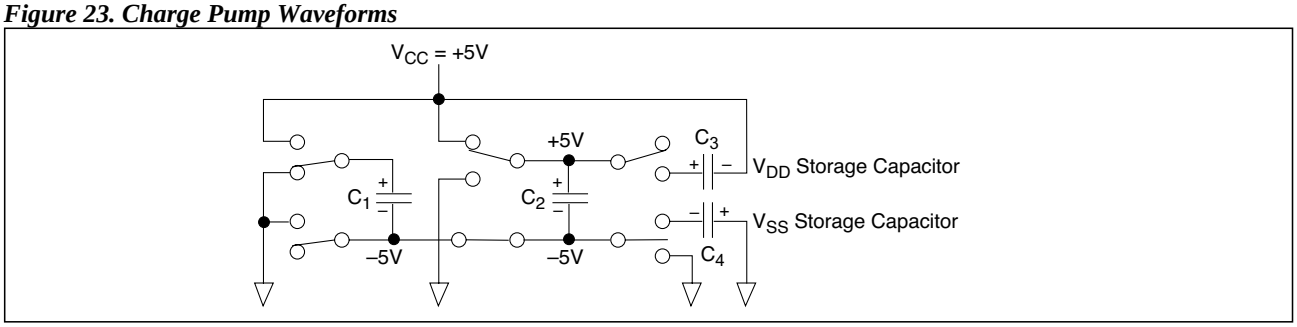


Figure 24. Charge Pump — Phase 3

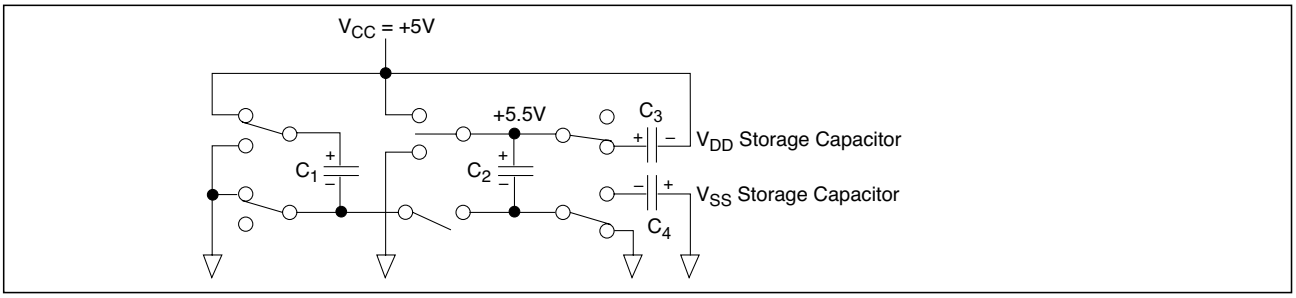


Figure 25. Charge Pump — Phase 4

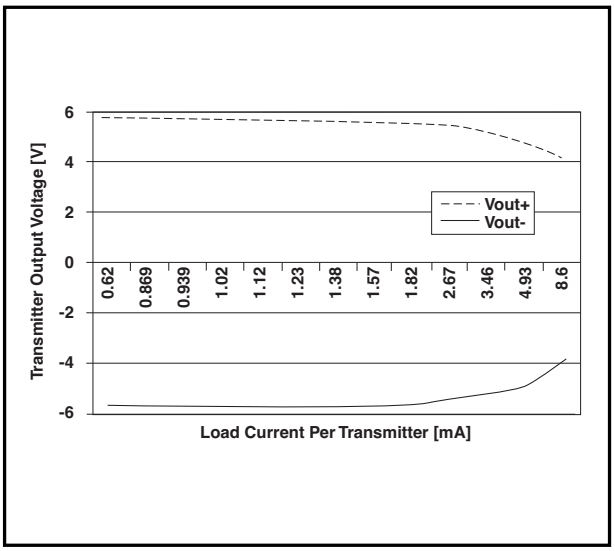
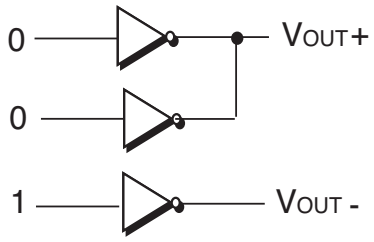


Figure 26. SP3243 Driver Output Voltages vs. Load Current per Transmitter

The SP3243 driver outputs are able to maintain voltage under loading of up to 2.5mA per driver, ensuring sufficient output for mouse-driving applications.



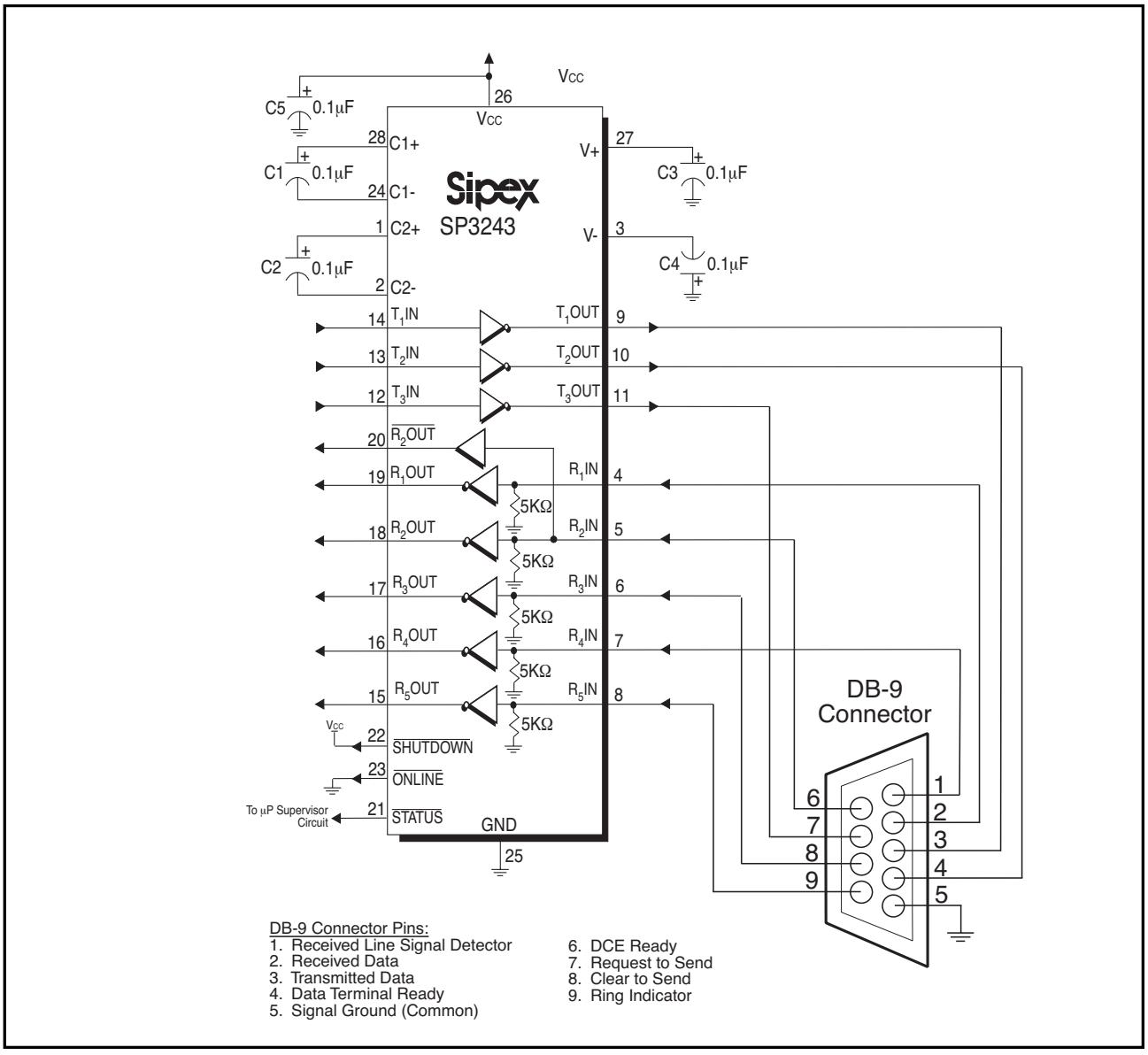


Figure 27. Circuit for the connectivity of the SP3243 with a DB-9 connector

RS-232 SIGNAL AT RECEIVER INPUT	$\overline{\text{SHUTDOWN}}$ INPUT	$\overline{\text{ONLINE}}$ INPUT	$\overline{\text{STATUS}}$ OUTPUT	TRANSCEIVER STATUS
YES	HIGH	LOW	HIGH	Normal Operation ***(Auto-Online)***
NO	HIGH	HIGH	LOW	Normal Operation
NO	HIGH	LOW	LOW	Shutdown (***Auto-Online***)
YES	LOW	HIGH / LOW	HIGH	Shutdown
NO	LOW	HIGH / LOW	LOW	Shutdown

Table 3. AUTO ON-LINE® Logic

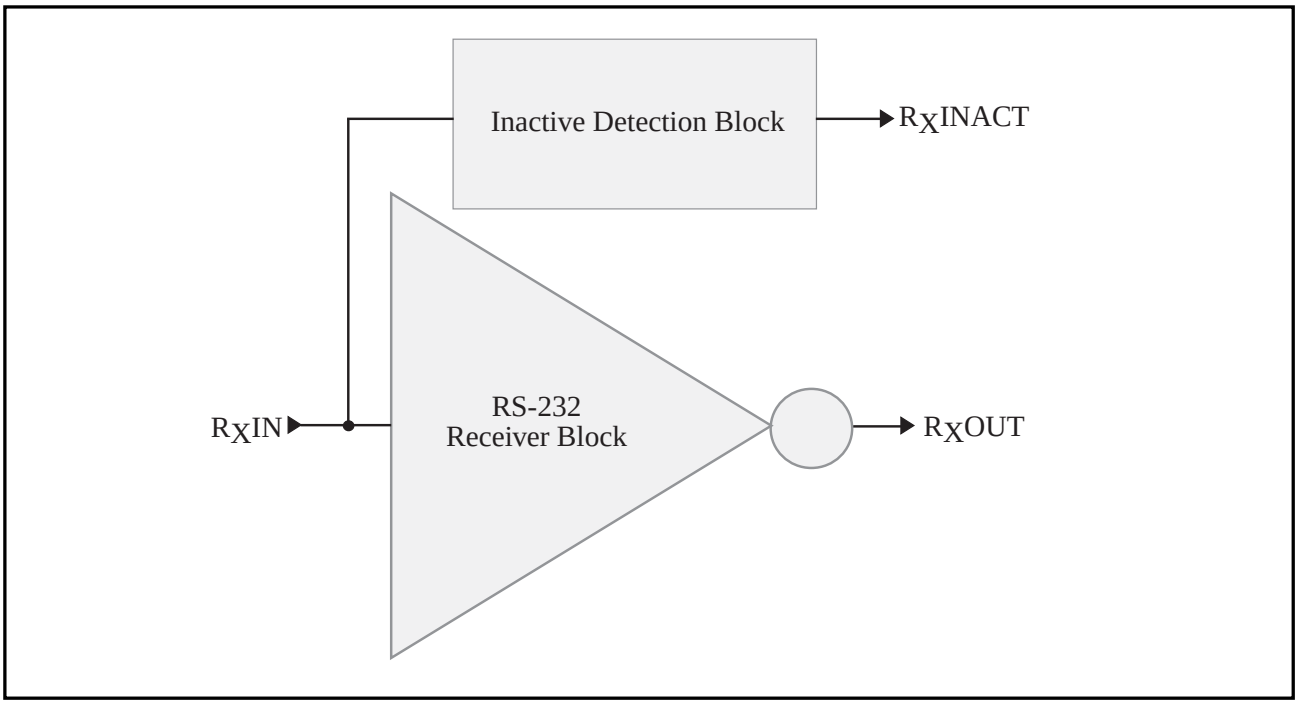


Figure 28. Stage I of AUTO ON-LINE® Circuitry

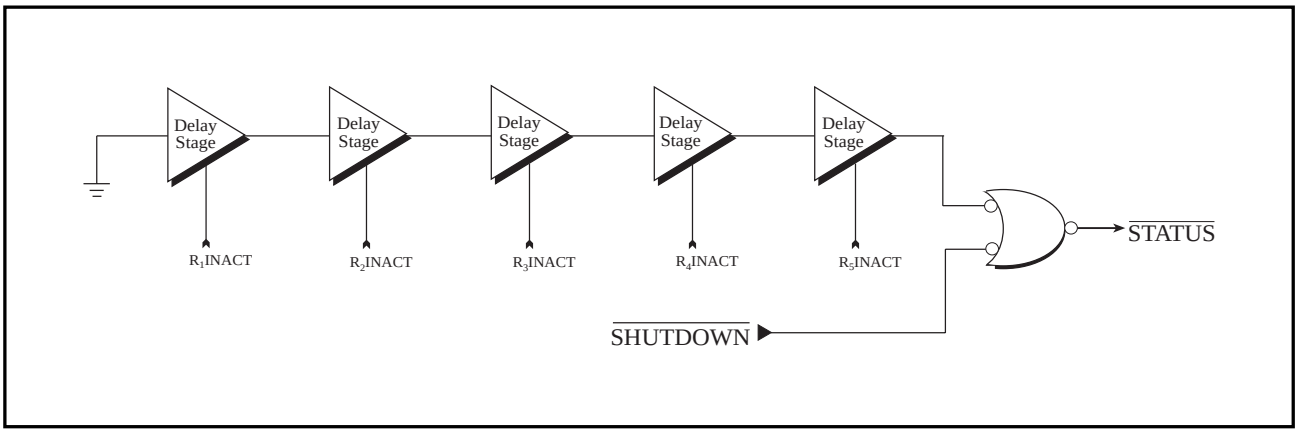


Figure 29. Stage II of AUTO ON-LINE® Circuitry

ESD TOLERANCE

The SP3243 series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC1000-4-2 Air-Discharge
c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 30. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on Figure 31. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

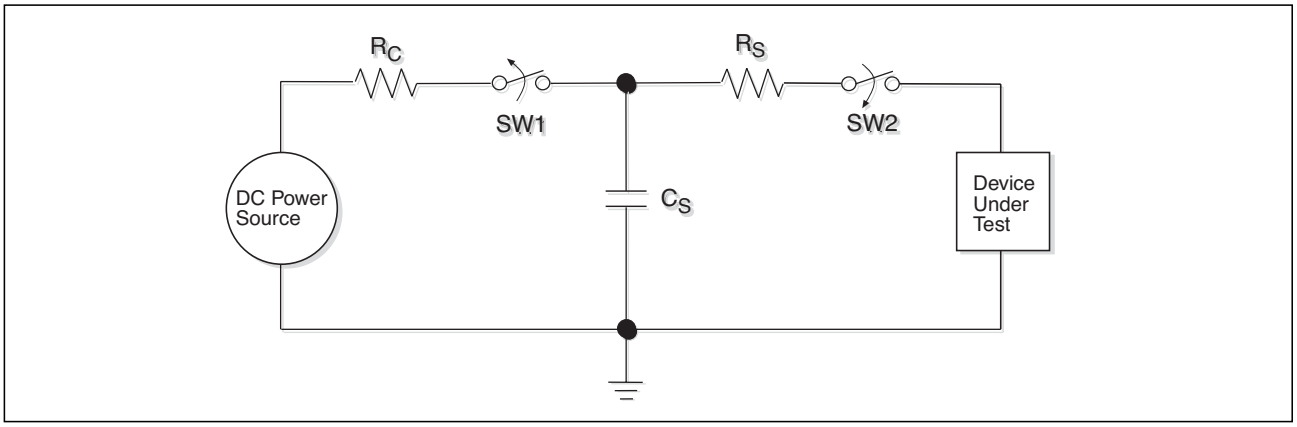


Figure 30. ESD Test Circuit for Human Body Model

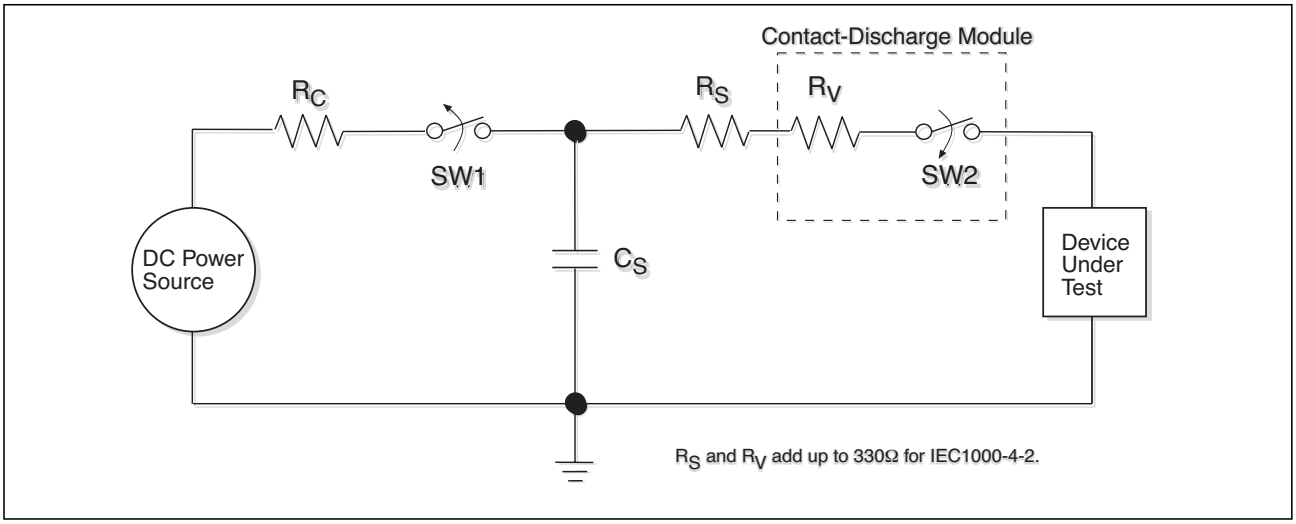


Figure 31. ESD Test Circuit for IEC1000-4-2

The circuit models in Figures30 and 31 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

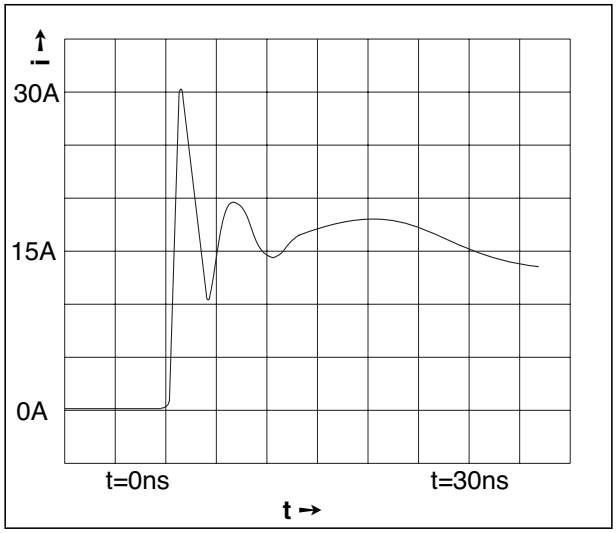
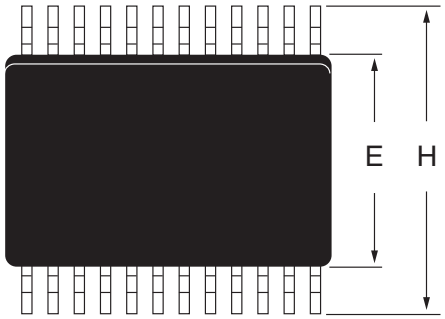


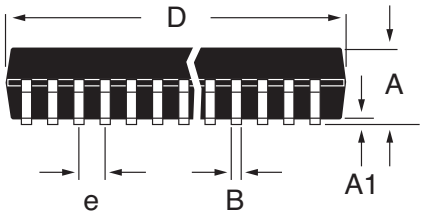
Figure 32. ESD Test Waveform for IEC1000-4-2

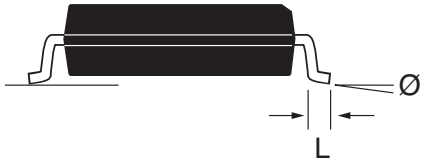
DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

Table 4. Transceiver ESD Tolerance Levels

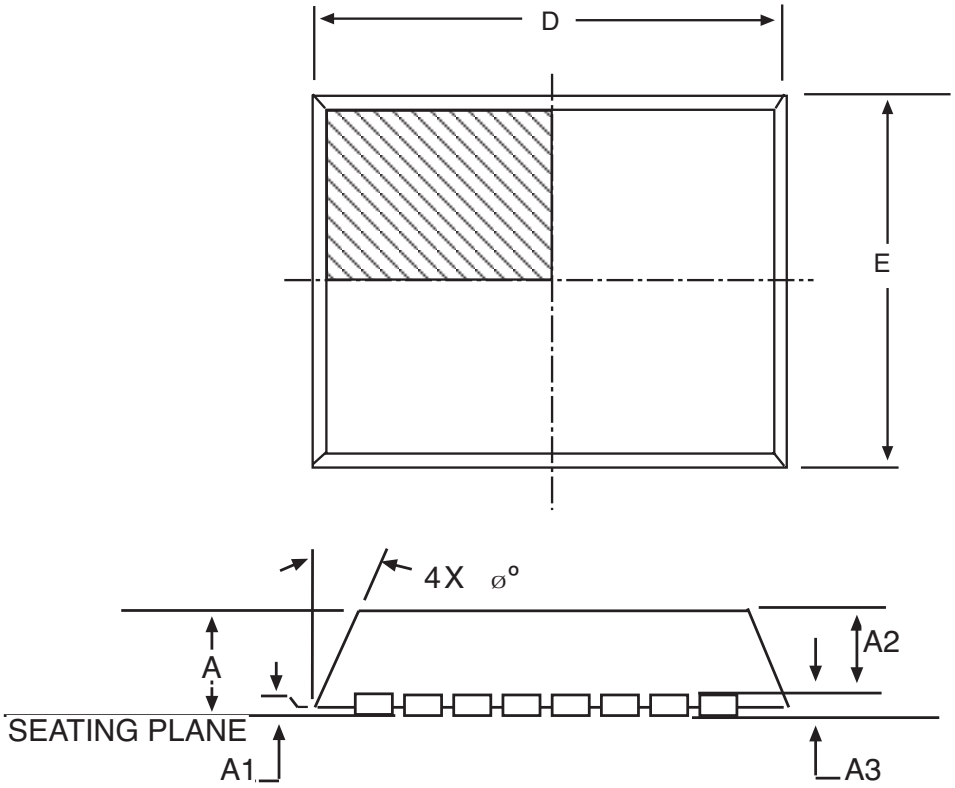
PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (WIDE)

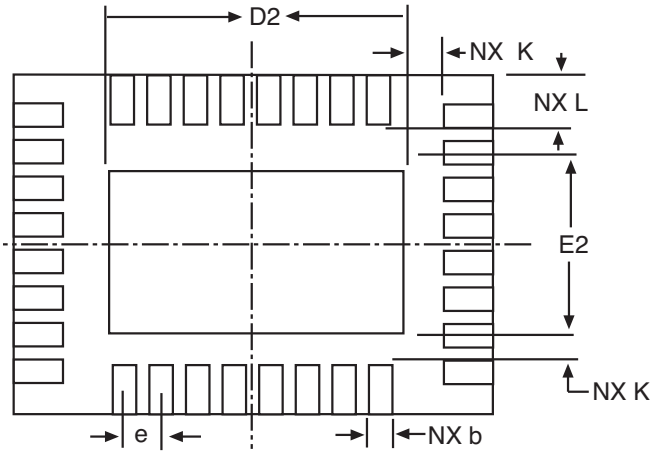






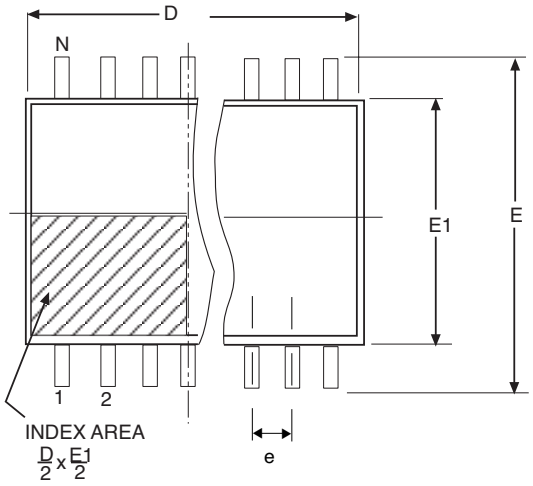
DIMENSIONS (Inches) Minimum/Maximum (mm)	28–PIN
A	0.090/0.104 (2.29/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

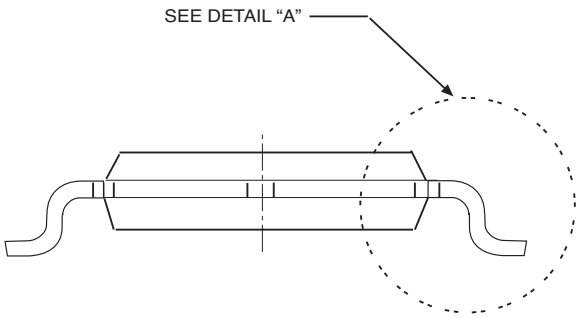


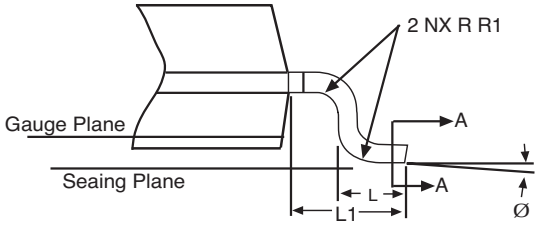


32 PIN QFN JEDECMO220 (VHHD-4)	Dimensions in (mm)		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3		0.20 REF	
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
b	0.18	0.25	0.30
Ø	0°	-	14°
D2	3.50	3.65	3.80
E2	3.50	3.65	3.80
L	0.35	0.40	0.45
K	0.20	-	-
N		32	
ND		8	
NE		8	

32 PIN QFN



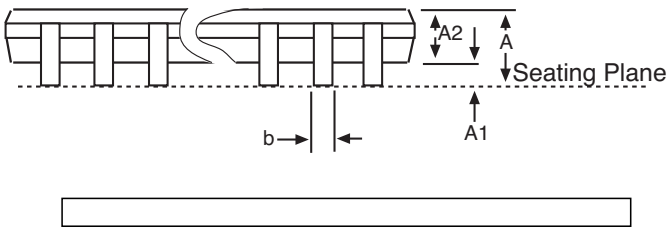


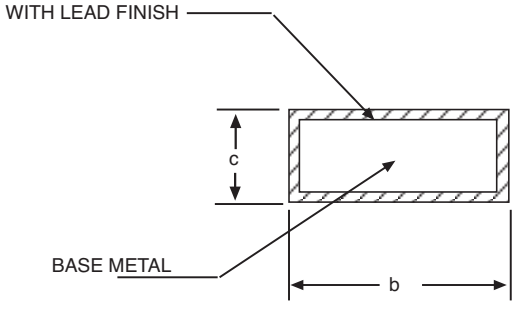


DETAIL A

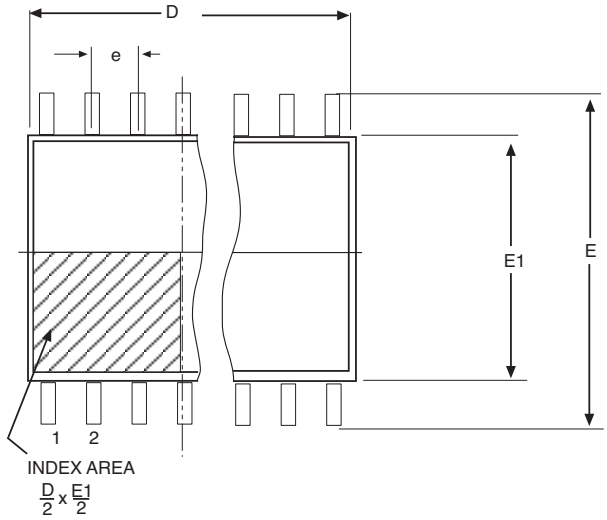
28 Pin SSOP JEDEC MO-150 (AH) Variation			
SYMBOL	MIN	NOM	MAX
A	-	-	2
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	9.9	10.2	10.5
E	7.4	7.8	8.2
E1	5	5.3	5.6
L	0.55	0.75	0.95
L1	1.25 REF		
ø	0º	4º	8º
e	0.65 BSC		

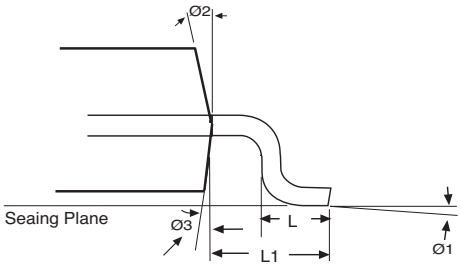
Note: Dimensions in (mm)



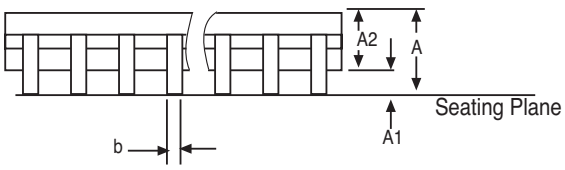


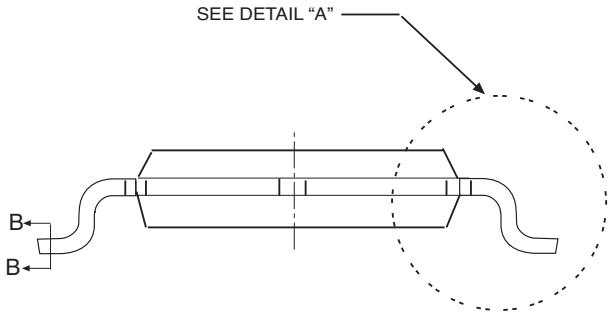
Section A-A





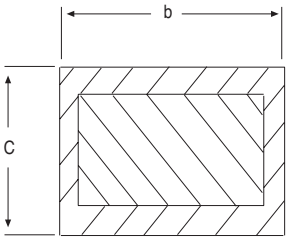
DETAIL A





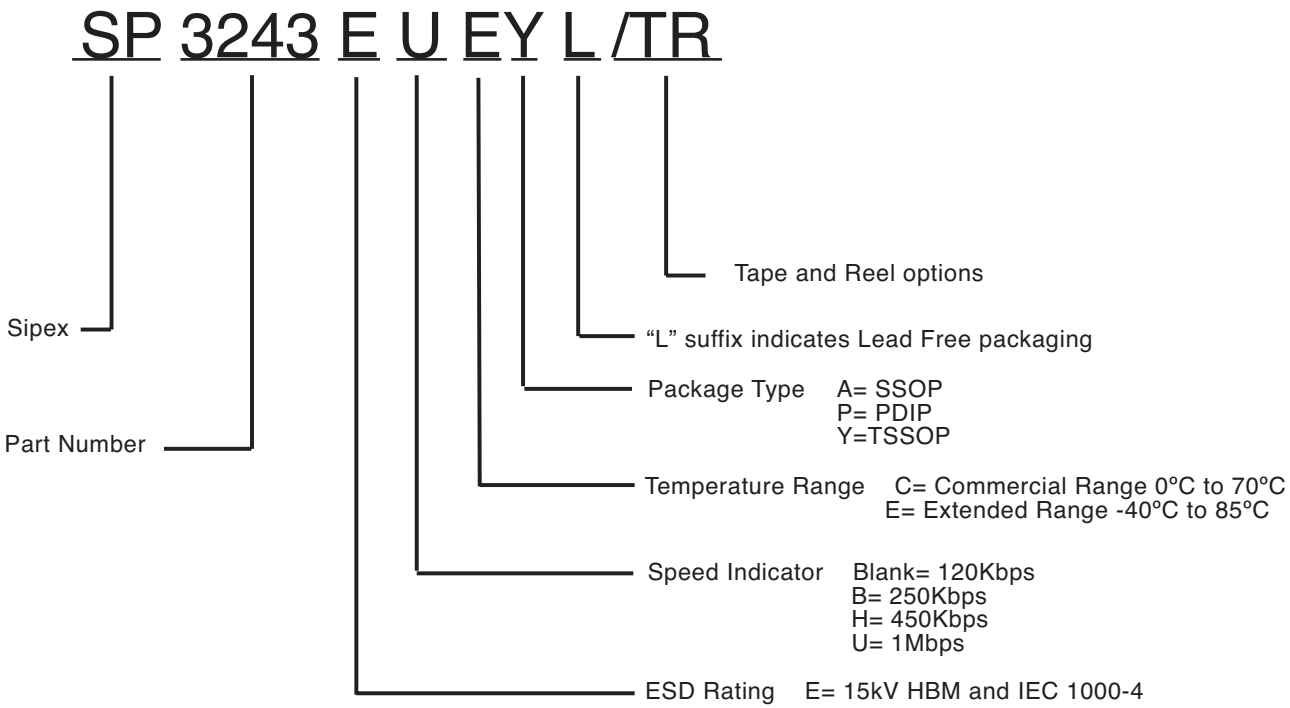
28 Pin TSSOP JEDEC MO-153 (AE) Variation			
SYMBOL	MIN	NOM	MAX
A	-	-	1.2
A1	0.05	-	0.15
A2	0.8	1	1.05
b	0.19	-	0.3
c	0.09	-	0.2
D	9.6	9.7	9.8
e	0.65 BSC		
E	6.40 BSC		
E1	4.3	4.4	4.5
L	0.45	0.6	0.75
L1	1.00 REF		
Ø1	0º	-	8º
Ø2	12º REF		
Ø3	12º REF		

Note: Dimensions in (mm)



Section B-B

PRODUCT NOMENCLATURE



Solved by Sipex™

Sipex Corporation

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Milpitas, CA 95035
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FAX: (408) 935-7600

ORDERING INFORMATION

Part Number	Speed (kbps)	Temp Range	Package
SP3243EBCA	250	-0 to 70C	28 Pin SSOP
SP3243EBCA/TR	250	-0 to 70C	28 Pin SSOP
SP3243EBCR	250	-0 to 70C	32 Pin QFN: see Note 2
SP3243EBCR/TR	250	-0 to 70C	32 Pin QFN: see Note 2
SP3243EBCT	250	-0 to 70C	28 Pin WSOIC
SP3243EBCT/TR	250	-0 to 70C	28 Pin WSOIC
SP3243EBCY	250	-0 to 70C	28 Pin TSSOP
SP3243EBCY/TR	250	-0 to 70C	28 Pin TSSOP
SP3243EBEA	250	-40 to 85C	28 Pin SSOP
SP3243EBEA/TR	250	-40 to 85C	28 Pin SSOP
SP3243EBET	250	-40 to 85C	28 Pin WSOIC
SP3243EBET/TR	250	-40 to 85C	28 Pin WSOIC
SP3243EBEY	250	-40 to 85C	28 Pin TSSOP
SP3243EBEY/TR	250	-40 to 85C	28 Pin TSSOP
SP3243ECA	120	-0 to 70C	28 Pin SSOP
SP3243ECA/TR	120	-0 to 70C	28 Pin SSOP
SP3243ECT	120	-0 to 70C	28 Pin WSOIC
SP3243ECT/TR	120	-0 to 70C	28 Pin WSOIC
SP3243ECY	120	-0 to 70C	28 Pin TSSOP
SP3243ECY/TR	120	-0 to 70C	28 Pin TSSOP
SP3243EEA	120	-40 to 85C	28 Pin SSOP
SP3243EEA/TR	120	-40 to 85C	28 Pin SSOP
SP3243EET	120	-40 to 85C	28 Pin WSOIC
SP3243EET/TR	120	-40 to 85C	28 Pin WSOIC
SP3243EEY	120	-40 to 85C	28 Pin TSSOP
SP3243EEY/TR	120	-40 to 85C	28 Pin TSSOP
SP3243EUCA	1000	-0 to 70C	28 Pin SSOP
SP3243EUCA/TR	1000	-0 to 70C	28 Pin SSOP
SP3243EUCR	1000	-0 to 70C	32 Pin QFN: see Note 2
SP3243EUCR/TR	1000	-0 to 70C	32 Pin QFN: see Note 2
SP3243EUCT	1000	-0 to 70C	28 Pin WSOIC
SP3243EUCT/TR	1000	-0 to 70C	28 Pin WSOIC
SP3243EUCY	1000	-0 to 70C	28 Pin TSSOP
SP3243EUCY/TR	1000	-0 to 70C	28 Pin TSSOP
SP3243EUEA	1000	-40 to 85C	28 Pin SSOP
SP3243EUEA/TR	1000	-40 to 85C	28 Pin SSOP
SP3243EUER	1000	-40 to 85C	32 Pin QFN: see Note 2
SP3243EUER/TR	1000	-40 to 85C	32 Pin QFN: see Note 2
SP3243EUET	1000	-40 to 85C	28 Pin WSOIC
SP3243EUET/TR	1000	-40 to 85C	28 Pin WSOIC
SP3243EUEY	1000	-40 to 85C	28 Pin TSSOP
SP3243EUEY/TR	1000	-40 to 85C	28 Pin TSSOP

Available in lead free packaging. To order add “-L” suffix to part number.

Example: SP3243EUEA/TR = standard; SP3243EUEA-L/TR = lead free

/TR = Tape and Reel. Pack quantity is 1,500 for SSOP, TSSOP and WSOIC.

Note 2: Not recommended for New Designs in QFN Package. See Factory for Availability.

ORDERING INFORMATION

Contact factory for availability of the following legacy part numbers. For long term availability Sipex recommends upgrades as listed below. All upgrade part numbers shown are fully pinout and function compatible with legacy part numbers. Upgrade part numbers may contain feature and/or performance enhancements or other changes to datasheet parameters.

Legacy Part Number	Recommended Upgrade
SP3243BCA	SP3243EBCA
SP3243BCA/TR	SP3243EBCA/TR
SP3243BCA-L	SP3243EBCA-L
SP3243BCA-L/TR	SP3243EBCA-L/TR
SP3243BCR	SP3243EBCR
SP3243BCR/TR	SP3243EBCR/TR
SP3243BCR-L	SP3243EBCR-L
SP3243BCR-L/TR	SP3243EBCR-L/TR
SP3243BCT	SP3243EBCT
SP3243BCT/TR	SP3243EBCT/TR
SP3243BCT-L	SP3243EBCT-L
SP3243BCT-L/TR	SP3243EBCT-L/TR
SP3243BCY	SP3243EBCY
SP3243BCY/TR	SP3243EBCY/TR
SP3243BCY-L	SP3243EBCY-L
SP3243BCY-L/TR	SP3243EBCY-L/TR
SP3243BEA	SP3243EBEA
SP3243BEA/TR	SP3243EBEA/TR
SP3243BEA-L	SP3243EBEA-L
SP3243BEA-L/TR	SP3243EBEA-L/TR
SP3243BET	SP3243EBET
SP3243BET/TR	SP3243EBET/TR
SP3243BET-L	SP3243EBET-L
SP3243BET-L/TR	SP3243EBET-L/TR
SP3243BEY	SP3243EBEY
SP3243BEY/TR	SP3243EBEY/TR
SP3243BEY-L	SP3243EBEY-L
SP3243BEY-L/TR	SP3243EBEY-L/TR
SP3243CA	SP3243ECA
SP3243CA/TR	SP3243ECA/TR
SP3243CA-L	SP3243ECA-L
SP3243CA-L/TR	SP3243ECA-L/TR
SP3243CT	SP3243ECT
SP3243CT/TR	SP3243ECT/TR
SP3243CT-L	SP3243ECT-L
SP3243CT-L/TR	SP3243ECT-L/TR
SP3243EA	SP3243EEA
SP3243EA/TR	SP3243EEA/TR
SP3243EA-L	SP3243EEA-L
SP3243EA-L/TR	SP3243EEA-L/TR
SP3243ET	SP3243EET
SP3243ET/TR	SP3243EET/TR
SP3243ET-L	SP3243EET-L
SP3243ET-L/TR	SP3243EET-L/TR

Legacy Part Number	Recommended Upgrade
SP3243EHCA	SP3243EUCA
SP3243EHCA/TR	SP3243EUCA/TR
SP3243EHCT	SP3243EUCT
SP3243EHCT/TR	SP3243EUCT/TR
SP3243HCA	SP3243EUCA
SP3243HCA/TR	SP3243EUCA/TR
SP3243HCA-L	SP3243EUCA-L
SP3243HCA-L/TR	SP3243EUCA-L/TR
SP3243HCT	SP3243EUCT
SP3243HCT/TR	SP3243EUCT/TR
SP3243HCT-L	SP3243EUCT-L
SP3243HCT-L/TR	SP3243EUCT-L/TR
SP3243UCA	SP3243EUCA
SP3243UCA/TR	SP3243EUCA/TR
SP3243UCA-L	SP3243EUCA-L
SP3243UCA-L/TR	SP3243EUCA-L/TR
SP3243UCR	SP3243EUCR
SP3243UCR/TR	SP3243EUCR/TR
SP3243UCR-L	SP3243EUCR-L
SP3243UCR-L/TR	SP3243EUCR-L/TR
SP3243UCT	SP3243EUCT
SP3243UCT/TR	SP3243EUCT/TR
SP3243UCT-L	SP3243EUCT-L
SP3243UCT-L/TR	SP3243EUCT-L/TR
SP3243UCY	SP3243EUCY
SP3243UCY/TR	SP3243EUCY/TR
SP3243UCY-L	SP3243EUCY-L
SP3243UCY-L/TR	SP3243EUCY-L/TR
SP3243UEA	SP3243EUEA
SP3243UEA/TR	SP3243EUEA/TR
SP3243UEA-L	SP3243EUEA-L
SP3243UEA-L/TR	SP3243EUEA-L/TR
SP3243UER	SP3243EUER
SP3243UER/TR	SP3243EUER/TR
SP3243UER-L	SP3243EUER-L
SP3243UER-L/TR	SP3243EUER-L/TR
SP3243UET	SP3243EUET
SP3243UET/TR	SP3243EUET/TR
SP3243UET-L	SP3243EUET-L
SP3243UET-L/TR	SP3243EUET-L/TR
SP3243UEY	SP3243EUEY
SP3243UEY/TR	SP3243EUEY/TR
SP3243UEY-L	SP3243EUEY-L
SP3243UEY-L/TR	SP3243EUEY-L/TR