



W49F002U

256K × 8 CMOS FLASH MEMORY

GENERAL DESCRIPTION

The W49F002U is a 2-megabit, 5-volt only CMOS flash memory organized as 256K × 8 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt VPP is not required. The unique cell architecture of the W49F002U results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

FEATURES

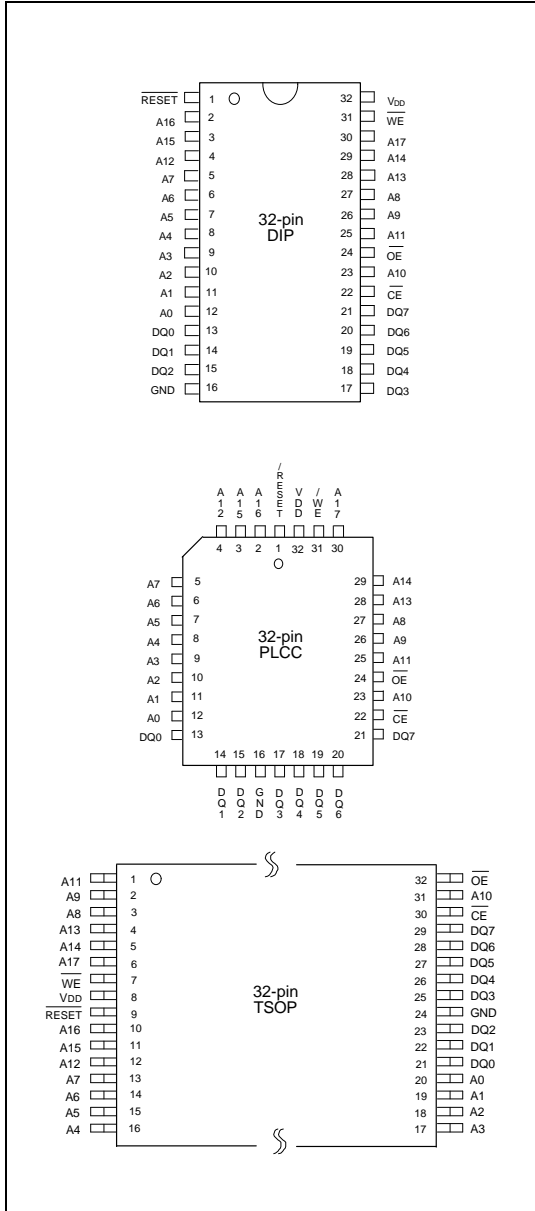
- Single 5-volt operations:
 - 5-volt Read
 - 5-volt Erase
 - 5-volt Program
- Fast Program operation:
 - Byte-by-Byte programming: 35 μS (typ.)
- Fast Erase operation: 100 mS (typ.)
- Fast Read access time: 70/90/120 nS
- Endurance: 10K cycles (typ.)
- Ten-year data retention
- Hardware data protection
- One 16K byte Boot Block with Lockout protection
- Two 8K byte Parameter Blocks
- Two Main Memory Blocks (96K, 128K) Bytes
- Low power consumption
 - Active current: 25 mA (typ.)
 - Standby current: 20 μA (typ.)
- Automatic program and erase timing with internal VPP generation
- End of program or erase detection
 - Toggle bit
 - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard byte-wide pinouts
- Available packages: 32-pin DIP and 32-pin TSOP and 32-pin-PLCC

Publication Release Date: April 2000

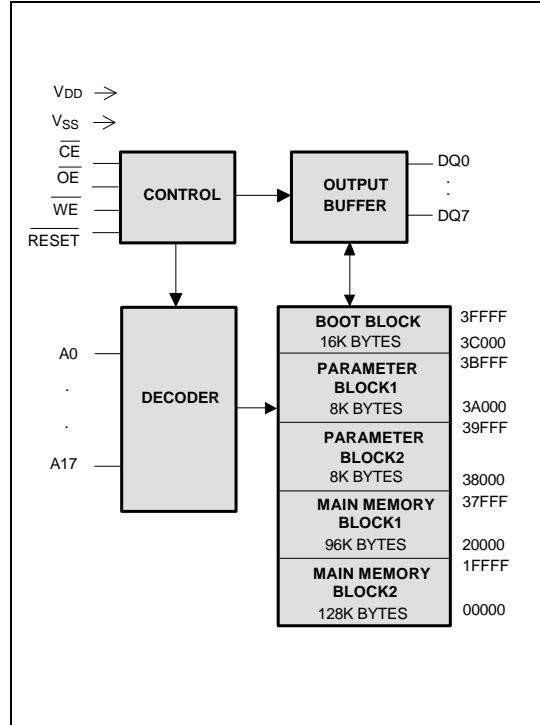
Revision A2



PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

| SYMBOL | PIN NAME |
|--------------------|---------------------|
| \overline{RESET} | Reset |
| A0-A17 | Address Inputs |
| DQ0-DQ7 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |
| \overline{WE} | Write Enable |
| VDD | Power Supply |
| GND | Ground |



FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W49F002U is controlled by \overline{CE} and \overline{OE} , both of which have to be low for the host to obtain data from the outputs. \overline{CE} is used for device selection. When \overline{CE} is high, the chip is de-selected and only standby power will be consumed. \overline{OE} is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either \overline{CE} or \overline{OE} is high. Refer to the timing waveforms for further details.

Reset Operation

The reset input pin can be used in some application. When \overline{RESET} pin is at high state, the device is in normal operation mode. When \overline{RESET} pin is at low state, it will halts the device and all outputs are at high impedance state. As the high state re-asserted to the \overline{RESET} pin, the device will return to read or standby mode, it depends on the control signals. When the system drives the \overline{RESET} pin low for at least a period of 500 nS, the device immediately terminates any operation in progress duration of the \overline{RESET} pulse. The other function for \overline{RESET} pin is temporary reset the boot block. By applying the 12V to \overline{RESET} pin, the boot block can be reprogrammed even though the boot block lockout function is enabled.

Boot Block Operation

There is one 16K-byte boot block in this device, which can be used to store boot code. It is located in the last 16K bytes with the address range of the boot block is 3C000(hex) to 3FFFF(hex). See Command Code sequence for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout); other memory locations can be changed with the regular programming method. Once the boot block programming lockout feature is activated, the chip erase function can no longer erase the boot block.

There is one condition that the lockout feature can be overridden. Just apply 12V to \overline{RESET} pin, the lockout feature will temporarily be inactivated and the block can be erased/programmed. Once the \overline{RESET} pin return to TTL level, the lockout feature will be activated again.

In order to detect whether the boot block feature is set on the 16K-bytes block, users can perform software command code sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "0002 (hex)". If the DQ0 of output data is "1," the boot block programming lockout feature is activated; if the DQ0 of output data is "0," the lockout feature is inactivated and the block can be erased/programmed.

To return to normal operation, perform a three-byte command code sequence (or an alternate single-byte command) to exit the identification mode. For the specific code, see Command Code for Identification/Boot Block Lockout Detection.

Chip Erase Operation

The chip-erase mode can be initiated by a six-byte command code sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed as fast as 100 mS (typical). The host system is not required to provide any control or timing during this operation. The entire memory array will be erased to FF hex. by the chip erase



operation if the boot block programming lockout feature is not activated. Once the boot block lockout feature is activated, the whole chip erase function will erase the two main memory blocks and the two parameter blocks but not the boot block. The device will automatically return to normal read mode after the erase operation. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Sector Erase Operation

There are four sectors: two main memory blocks and two parameters blocks which can be erased individually by initiating a six-byte command code sequence. Sector address is latched on the falling edge of \overline{WE} signal in the sixth cycle while the data input "30(hex)" is latched at the rising edge of \overline{WE} in this cycle. After the command loading cycle, the device enters the internal sector erase mode, which is automatically timed and will be completed as fast as 100 mS (typical). The host system does not require to provide any control or timing during this operation. The device will automatically return to normal read mode after the erase operation. Data polling and/or Toggle Bits can be used to detect the end of erase cycle.

When different sector address is loaded in the sixth cycle for sector erase command, the correspondent sectors will be erased automatically; that these sections will be erased independently. For detail sector to be erased information, please refer to the **Table of Command Definition**.

Program Operation

The W49F002U is programmed on a byte-by-byte basis. Program operation can only change logical data "1" to logical data "0". The erase operation (changed entire data in two main memory blocks and two parameter blocks and/or boot block from "0" to "1") is needed before programming.

The program operation is initiated by a 4-byte command code sequence (see Command Codes for Byte Programming). The device will internally enter the program operation immediately after the byte-program command is entered. The internal program timer will automatically time-out (50 μ S max. - TBP). Once completed, the device returns to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

Hardware Data Protection

The integrity of the data stored in the W49F002U is also hardware protected in the following ways:

- (1) Noise/Glitch Protection: A \overline{WE} pulse of less than 15 nS in duration will not initiate a write cycle.
- (2) VDD Power Up/Down Detection: The programming operation is inhibited when VDD is less than 2.5V typical.
- (3) Write Inhibit Mode: Forcing \overline{OE} low, \overline{CE} high, or \overline{WE} high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.
- (4) VDD power-on delay: When VDD has reached its sense level, the device will automatically time-out 5 mS before any write (erase/program) operation.

Data Polling (DQ7)- Write Status Detection

The W49F002U includes a data polling feature to indicate the end of a program or erase cycle. When the W49F002U is in the internal program or erase cycle, any attempt to read DQ7 of the last byte loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ7 will show the true data. Note that DQ7 will show logical "0" during the erase cycle, and become logical "1" or true data when the erase cycle has been completed.



Toggle Bit (DQ6)- Write Status Detection

In addition to data polling, the W49F002U provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a three-byte (or JEDEC 3-byte) command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code DA(hex). A read from address 0001H outputs the device code 0B(hex). The product ID operation can be terminated by a three-byte command code sequence or an alternate one-byte command code sequence (see Command Definition table).

In the hardware access mode, access to the product ID is activated by forcing \overline{CE} and \overline{OE} low, \overline{WE} high, and raising A9 to 12 volts.

TABLE OF OPERATING MODES

Operating Mode Selection

($V_{HH} = 12V \pm 5\%$)

| MODE | PINS | | | | | |
|----------------|--------------------|-----------------|-----------------|-----------------|---|----------------------------|
| | \overline{RESET} | \overline{CE} | \overline{OE} | \overline{WE} | ADDRESS | DQ. |
| Read | V _{IH} | V _{IL} | V _{IL} | V _{IH} | A _{IN} | Dout |
| Write | V _{IH} | V _{IL} | V _{IH} | V _{IL} | A _{IN} | Din |
| Standby | V _{IH} | V _{IH} | X | X | X | High Z |
| Write Inhibit | V _{IH} | X | V _{IL} | X | X | High Z/DOUT |
| | V _{IH} | X | X | V _{IH} | X | High Z/DOUT |
| Output Disable | V _{IH} | X | V _{IH} | X | X | High Z |
| Reset Mode | V _{IL} | X | X | X | X | High Z |
| Product ID | V _{IH} | V _{IL} | V _{IL} | V _{IH} | A0 = V _{IL} ; A1–A17 = V _{IL} ; A9 = V _{HH} | Manufacturer Code DA (Hex) |
| | V _{IH} | V _{IL} | V _{IL} | V _{IH} | A0 = V _{IH} ; A1–A17 = V _{IL} ; A9 = V _{HH} | Device Code 0B (Hex) |



TABLE OF COMMAND DEFINITION⁽¹⁾

| COMMAND | NO. OF | 1ST CYCLE | 2ND CYCLE | 3RD CYCLE | 4TH CYCLE | 5TH CYCLE | 6TH CYCLE |
|--------------------------------|--------|------------|------------|------------|------------|------------|----------------------|
| DESCRIPTION | Cycles | Addr. Data | Addr. Data | Addr. Data | Addr. Data | Addr. Data | Addr. Data |
| Read | 1 | AIN DOUT | | | | | |
| Chip Erase | 6 | 5555 AA | 2AAA 55 | 5555 80 | 5555 AA | 2AAA 55 | 5555 10 |
| Sector Erase | 6 | 5555 AA | 2AAA 55 | 5555 80 | 5555 AA | 2AAA 55 | SA ⁽³⁾ 30 |
| Byte Program | 4 | 5555 AA | 2AAA 55 | 5555 A0 | AIN DIN | | |
| Boot Block Lockout | 6 | 5555 AA | 2AAA 55 | 5555 80 | 5555 AA | 2AAA 55 | 5555 40 |
| Product ID Entry | 3 | 5555 AA | 2AAA 55 | 5555 90 | | | |
| Product ID Exit ⁽²⁾ | 3 | 5555 AA | 2AAA 55 | 5555 F0 | | | |
| Product ID Exit ⁽²⁾ | 1 | XXXX F0 | | | | | |

Notes:

1. Address Format: A14–A0 (Hex); Data Format: DQ7-DQ0 (Hex)
2. Either one of the two Product ID Exit commands can be used.
3. SA means: Sector Address
 - If SA is within 3C000 to 3FFFF (Boot Block address range), and the Boot Block programming lockout feature is activated, nothing will happen and the device will go back to read mode after 100nS.
 - If the Boot Block programming lockout feature is not activated, this command will erase Boot Block.
 - If SA is within 3A000 to 3BFFF (Parameter Block1 address range), this command will erase PB1.
 - If SA is within 38000 to 39FFF (Parameter Block2 address range), this command will erase PB2.
 - If SA is within 20000 to 37FFF (Main Memory Block1 address range), this command will erase MMB1.
 - If SA is within 00000 to 1FFFF (Main Memory Block2 address range), this command will erase MMB2.

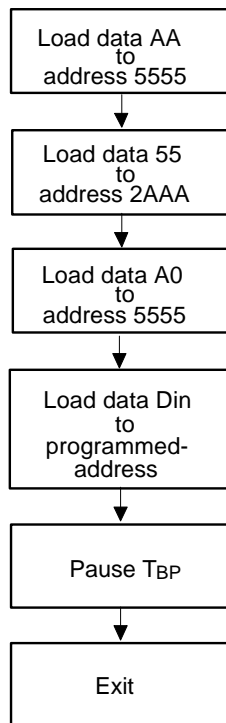


Command Codes for Byte Program

| COMMAND SEQUENCE | ADDRESS | DATA |
|------------------|--------------------|-----------------|
| 0 Write | 5555H | AAH |
| 1 Write | 2AAAH | 55H |
| 2 Write | 5555H | A0H |
| 3 Write | Programmed-address | Programmed-data |

Byte Program Flow Chart

Byte Program Command Flow



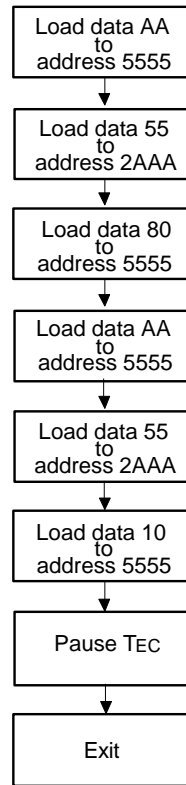
Notes for software program code:
 Data Format: DQ7–DQ0 (Hex)
 Address Format: A14–A0 (Hex)



Command Codes for Chip Erase

| BYTE SEQUENCE | ADDRESS | DATA |
|---------------|---------|------|
| 1 Write | 5555H | AAH |
| 2 Write | 2AAAH | 55H |
| 3 Write | 5555H | 80H |
| 4 Write | 5555H | AAH |
| 5 Write | 2AAAH | 55H |
| 6 Write | 5555H | 10H |

Chip Erase Acquisition Flow



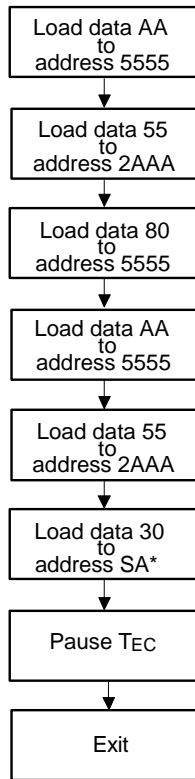
Notes for chip erase:
 Data Format: DQ7–DQ0 (Hex)
 Address Format: A14–A0 (Hex)



Command Codes for Sector Erase

| BYTE SEQUENCE | ADDRESS | DATA |
|---------------|---------|------|
| 1 Write | 5555H | AAH |
| 2 Write | 2AAAH | 55H |
| 3 Write | 5555H | 80H |
| 4 Write | 5555H | AAH |
| 5 Write | 2AAAH | 55H |
| 6 Write | SA* | 30H |

Sector Erase Acquisition Flow



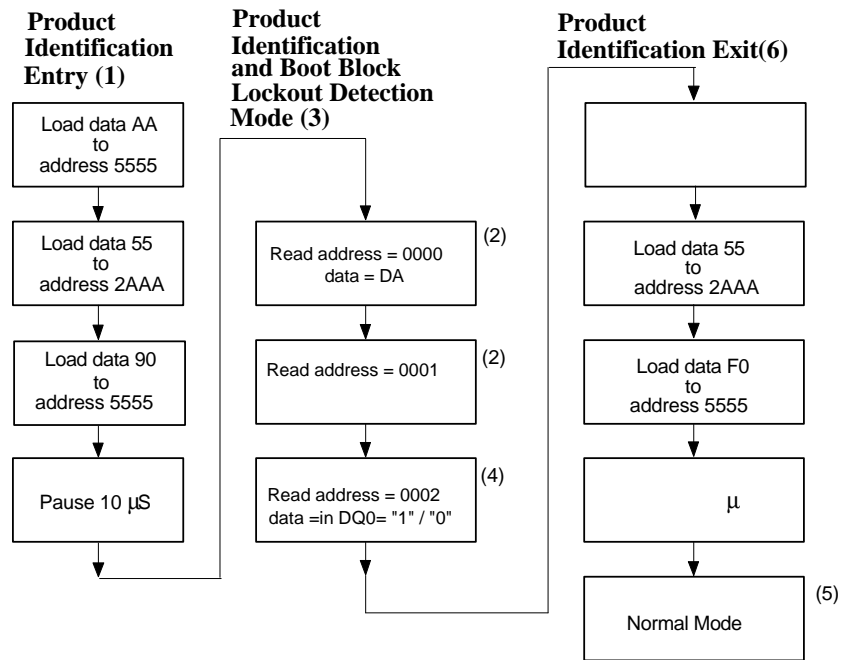
Notes for chip erase:
 Data Format: DQ7–DQ0 (Hex)
 Address Format: A14–A0 (Hex)
 SA : For details, see the page 6 .



Command Codes for Product Identification and Boot Block Lockout Detection

| BYTE SEQUENCE | SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY | | SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION EXIT(6) | |
|---------------|--|------|--|------|
| | ADDRESS | DATA | ADDRESS | DATA |
| 1 Write | 5555 | AA | 5555H | AAH |
| 2 Write | 2AAA | 55 | 2AAAH | 55H |
| 3 Write | 5555 | 90 | 5555H | F0H |
| Pause 10 μS | | | Pause 10 μS | |

Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

- (1) Data Format: DQ7–DQ0 (Hex); Address Format: A14–A0 (Hex)
- (2) A1–A17 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.
- (3) The device does not remain in identification and boot block lockout detection mode if power down.
- (4) If the output data in DQ0= " 1 " the boot block programming lockout feature is activated; if the output data in DQ0 = " 0 ," the lockout feature is inactivated and the boot block can be programmed.
- (5) The device returns to standard operation mode.
- (6) Optional 1-byte cycle (write F0 hex at XXXX address) can be used to exit the product identification/boot block lockout detection.

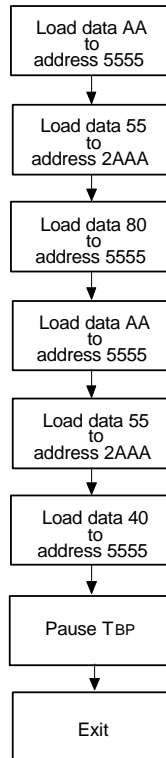


Command Codes for Boot Block Lockout Enable

| BYTE SEQUENCE | ADDRESS | DATA |
|---------------|---------|------|
| 0 Write | 5555H | AAH |
| 1 Write | 2AAAH | 55H |
| 2 Write | 5555H | 80H |
| 3 Write | 5555H | AAH |
| 4 Write | 2AAAH | 55H |
| 5 Write | 5555H | 40H |
| Pause TBP | | |

Boot Block Lockout Enable Acquisition Flow

Boot Block Lockout Feature Set Flow



Notes for boot block lockout enable:
 Data Format: DQ7–DQ0 (Hex)
 Address Format: A14–A0 (Hex)



DC CHARACTERISTICS

Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|--|------------------------------|------|
| Power Supply Voltage to V _{SS} Potential | -0.5 to +7.0 | V |
| Operating Temperature | 0 to +70 | °C |
| Storage Temperature | -65 to +150 | °C |
| D.C. Voltage on Any Pin to Ground Potential except \overline{OE} | -0.5 to V _{DD} +1.0 | V |
| Transient Voltage (<20 nS) on Any Pin to Ground Potential | -1.0 to V _{DD} +1.0 | V |
| Voltage on \overline{OE} Pin to Ground Potential | -0.5 to 12.5 | V |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Operating Characteristics

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

| PARAMETER | SYM. | TEST CONDITIONS | LIMITS | | | UNIT |
|--|-----------------|--|--------|------|----------------------|------|
| | | | MIN. | TYP. | MAX. | |
| Power Supply Current | ICC | $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all DQs open Address inputs = V _{IL} /V _{IH} , at f = 5 MHz | - | 25 | 50 | mA |
| Standby V _{DD} Current (TTL input) | ISB1 | $\overline{CE} = V_{IH}$, all DQs open Other inputs = V _{IL} /V _{IH} | - | 2 | 3 | mA |
| Standby V _{DD} Current (CMOS input) | ISB2 | $\overline{CE} = V_{DD} - 0.3V$, all DQs open Other inputs = V _{DD} - 0.3V/GND | - | 20 | 100 | μA |
| Input Leakage Current | ILI | V _{IN} = GND to V _{DD} | - | - | 10 | μA |
| Output Leakage Current | ILO | V _{OUT} = GND to V _{DD} | - | - | 10 | μA |
| Input Low Voltage | V _{IL} | - | -0.3 | - | 0.8 | V |
| Input High Voltage | V _{IH} | - | 2.0 | - | V _{DD} +0.5 | V |
| Output Low Voltage | V _{OL} | I _{OL} = 2.1 mA | - | - | 0.45 | V |
| Output High Voltage | V _{OH} | I _{OH} = -0.4 mA | 2.4 | - | - | V |



Power-up Timing

| PARAMETER | SYMBOL | TYPICAL | UNIT |
|-----------------------------|------------|---------|------|
| Power-up to Read Operation | TPU. READ | 100 | μS |
| Power-up to Write Operation | TPU. WRITE | 5 | mS |

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

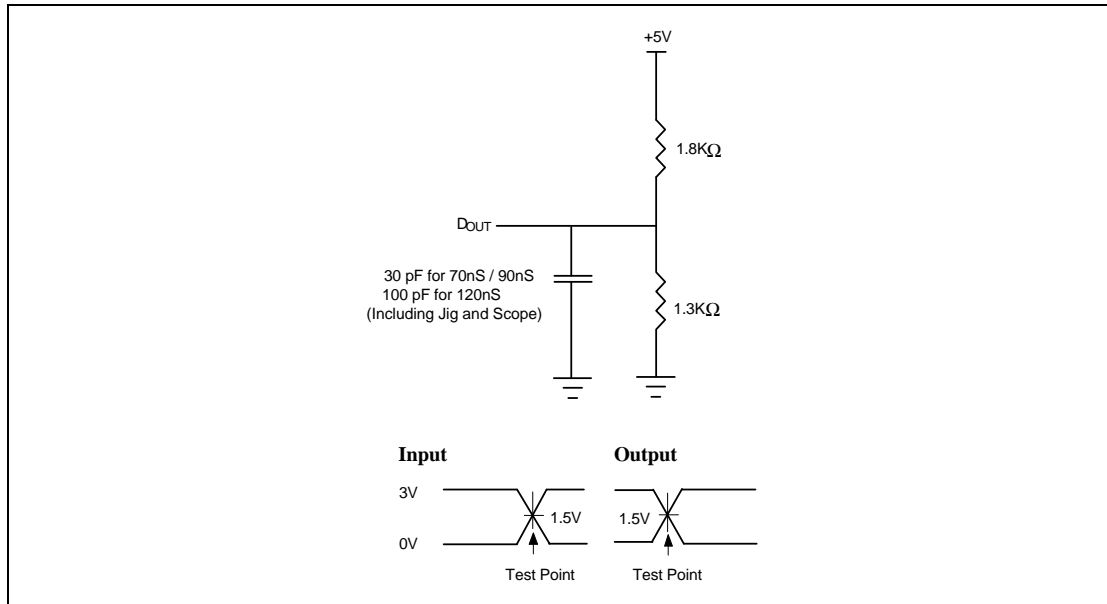
| PARAMETER | SYMBOL | CONDITIONS | MAX. | UNIT |
|---------------------|------------------|-----------------------|------|------|
| I/O Pin Capacitance | C _{I/O} | V _{I/O} = 0V | 12 | pf |
| Input Capacitance | C _{IN} | V _{IN} = 0V | 6 | pf |

AC CHARACTERISTICS

AC Test Conditions

| PARAMETER | CONDITIONS |
|---------------------------|---|
| Input Pulse Levels | 0V to 3.0V |
| Input Rise/Fall Time | < 5 nS |
| Input/Output Timing Level | 1.5V/1.5V |
| Output Load | 1 TTL Gate and C _L = 100 pF for 120 nS; C _L = 30 pF for 70 nS /90 nS |

AC Test Load and Waveform





AC Characteristics, continued

Read Cycle Timing Parameters

(V_{CC} = 5.0V ±10%, V_{CC} = 0V, T_A = 0 to 70° C)

| PARAMETER | SYM. | W49F002U-70 | | W49F002U-90 | | W49F002U-120 | | UNIT |
|---------------------------------------|------|-------------|------|-------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | TRC | 70 | - | 90 | - | 120 | - | nS |
| Chip Enable Access Time | TCE | - | 70 | - | 90 | - | 120 | nS |
| Address Access Time | TAA | - | 70 | - | 90 | - | 120 | nS |
| Output Enable Access Time | TOE | - | 35 | - | 40 | - | 50 | nS |
| \overline{CE} Low to Active Output | TCLZ | 0 | - | 0 | - | 0 | - | nS |
| \overline{OE} Low to Active Output | TOLZ | 0 | - | 0 | - | 0 | - | nS |
| \overline{CE} High to High-Z Output | TCHZ | - | 25 | - | 25 | - | 30 | nS |
| \overline{OE} High to High-Z Output | TOHZ | - | 25 | - | 25 | - | 30 | nS |
| Output Hold from Address Change | TOH | 0 | - | 0 | - | 0 | - | nS |

Write Cycle Timing Parameters

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--|--------|------|------|------|------|
| Address Setup Time | TAS | 0 | - | - | nS |
| Address Hold Time | TAH | 50 | - | - | nS |
| \overline{WE} and \overline{CE} Setup Time | TCS | 0 | - | - | nS |
| \overline{WE} and \overline{CE} Hold Time | TCH | 0 | - | - | nS |
| \overline{OE} High Setup Time | TOES | 0 | - | - | nS |
| \overline{OE} High Hold Time | TOEH | 0 | - | - | nS |
| \overline{CE} Pulse Width | TCP | 100 | - | - | nS |
| \overline{WE} Pulse Width | TWP | 100 | - | - | nS |
| \overline{WE} High Width | TWPH | 100 | - | - | nS |
| Data Setup Time | TDS | 50 | - | - | nS |
| Data Hold Time | TDH | 10 | - | - | nS |
| Byte Programming Time | TBP | - | 35 | 50 | μS |
| Erase Cycle Time | TEC | - | 0.1 | 0.2 | S |

Note: All AC timing signals observe the following guidelines for determining setup and hold times:

(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.



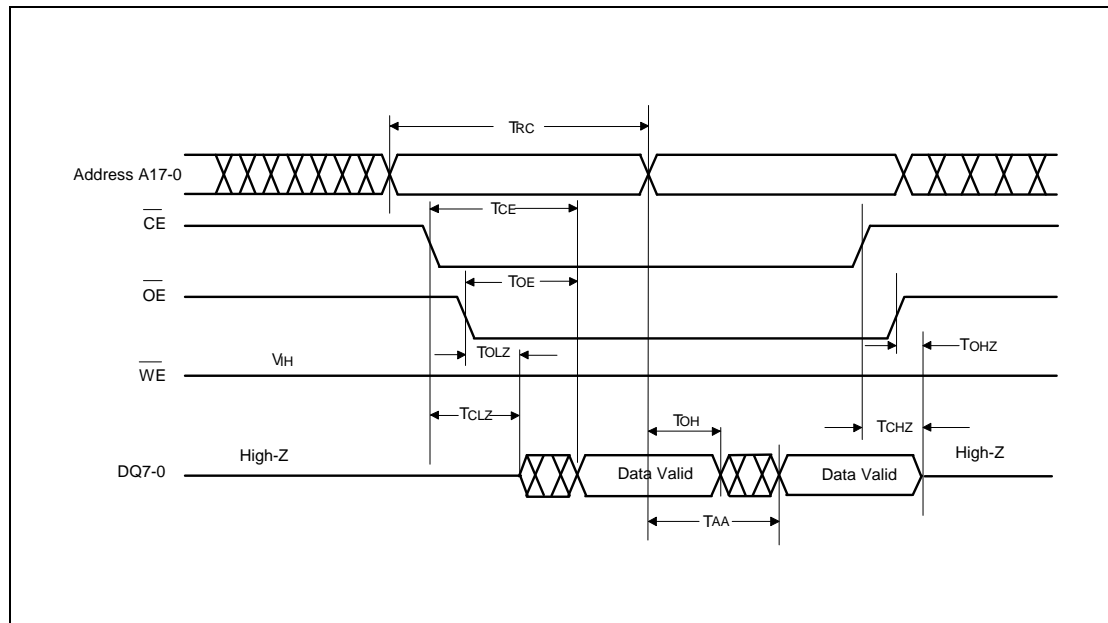
AC Characteristics, continued

Data Polling and Toggle Bit Timing Parameters

| PARAMETER | SYM. | W49F002U-70 | | W49F002U-90 | | W49F002U-120 | | UNIT |
|---|------|-------------|------|-------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $\overline{\text{OE}}$ to Data Polling Output Delay | TOEP | - | 35 | - | 40 | - | 50 | nS |
| $\overline{\text{CE}}$ to Data Polling Output Delay | TCEP | - | 70 | - | 90 | - | 120 | nS |
| $\overline{\text{OE}}$ to Toggle Bit Output Delay | TOET | - | 35 | - | 40 | - | 50 | nS |
| $\overline{\text{CE}}$ to Toggle Bit Output Delay | TCET | - | 70 | - | 90 | - | 120 | nS |

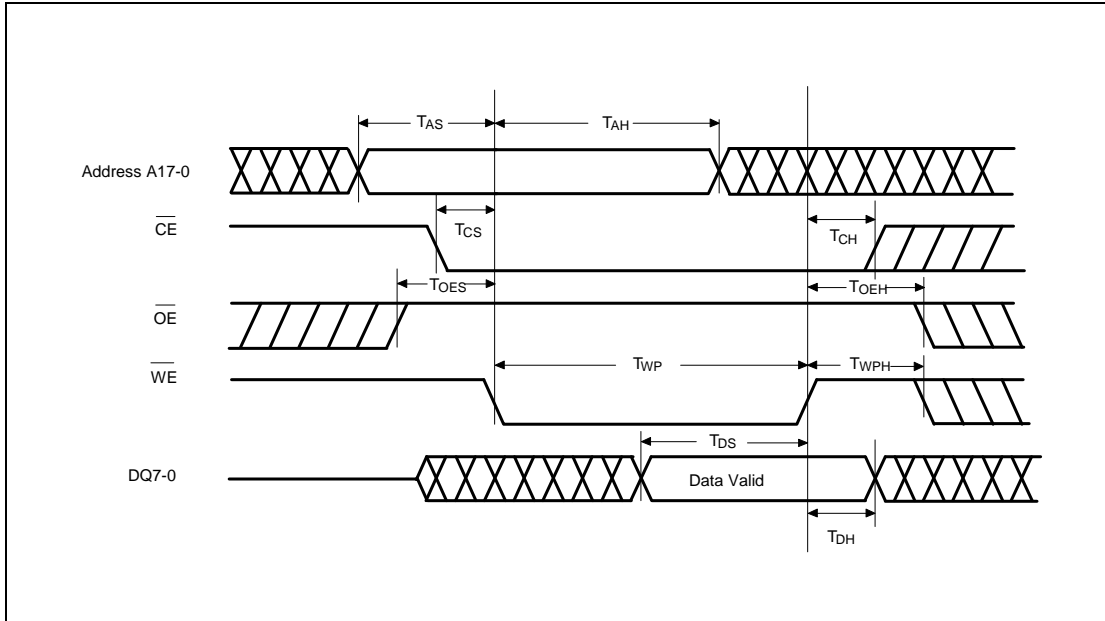
TIMING WAVEFORMS

Read Cycle Timing Diagram

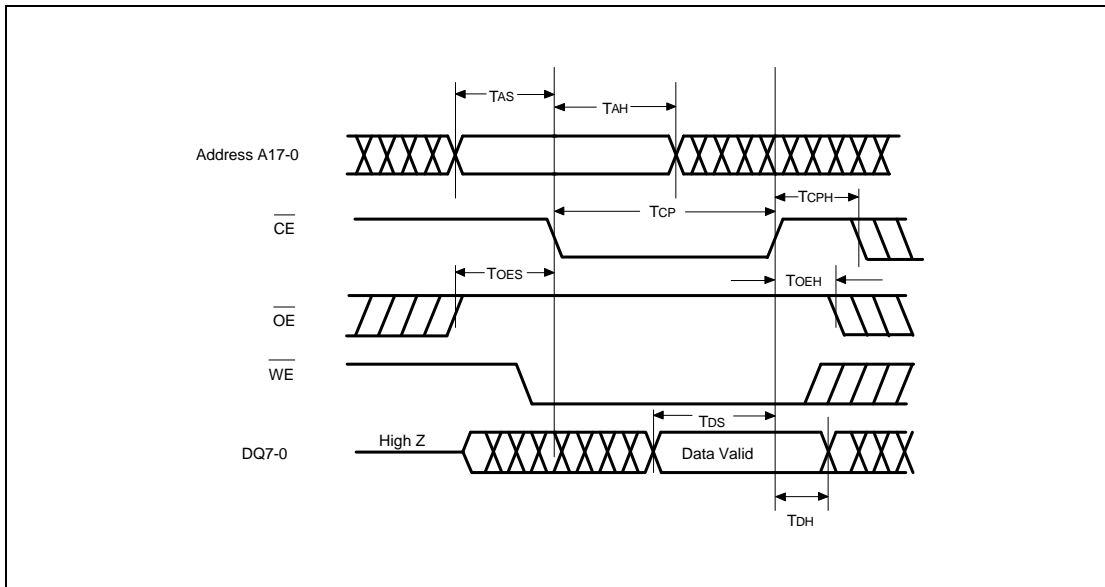


Timing Waveforms, continued

WE Controlled Command Write Cycle Timing Diagram



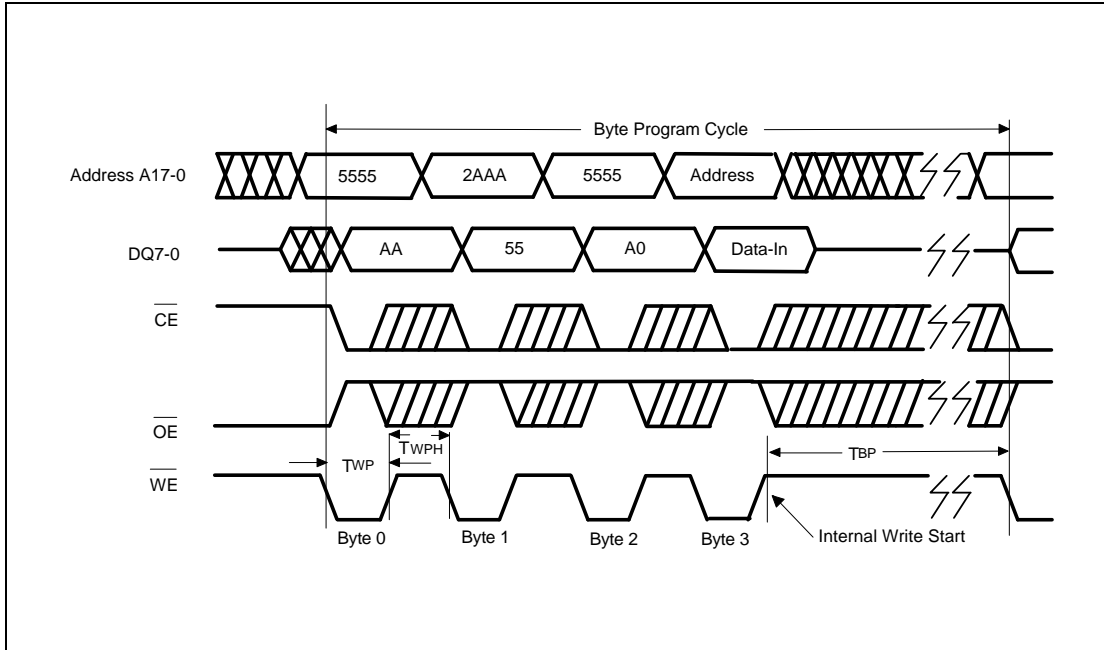
CE Controlled Command Write Cycle Timing Diagram



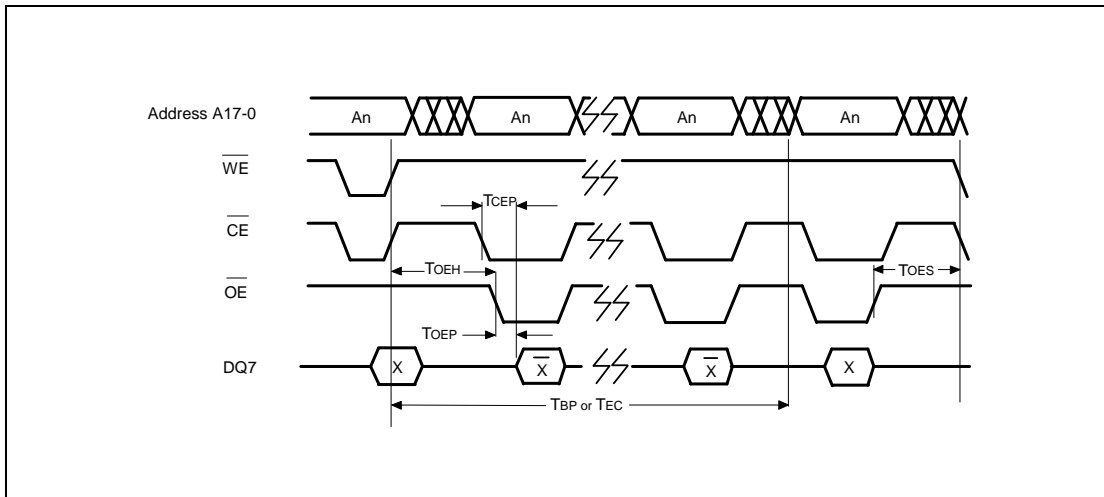


Timing Waveforms, continued

Program Cycle Timing Diagram

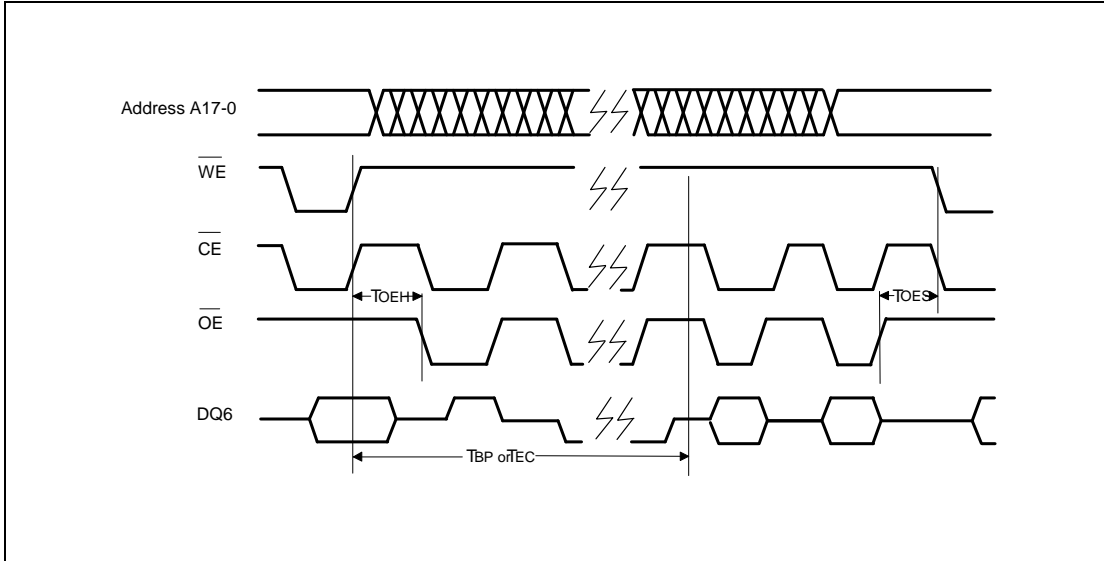


DATA Polling Timing Diagram

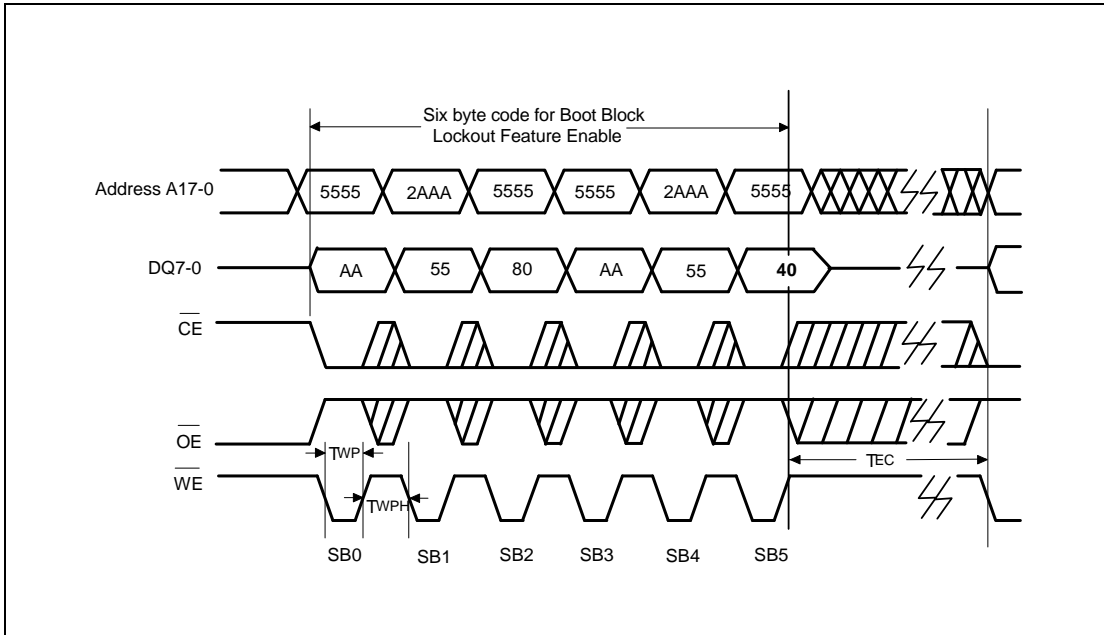


Timing Waveforms, continued

Toggle Bit Timing Diagram



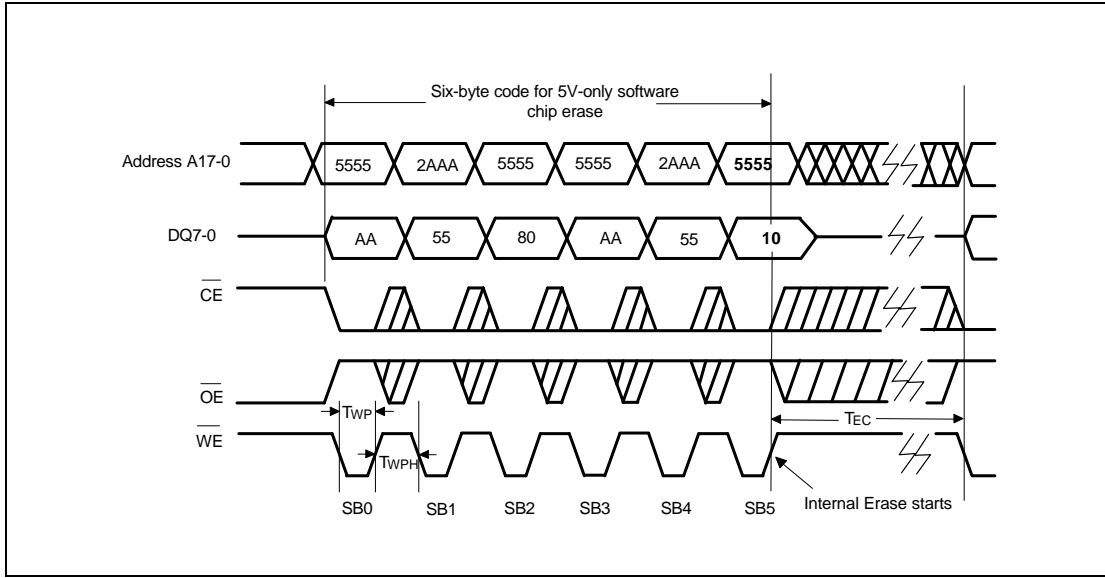
Boot Block Lockout Enable Timing Diagram



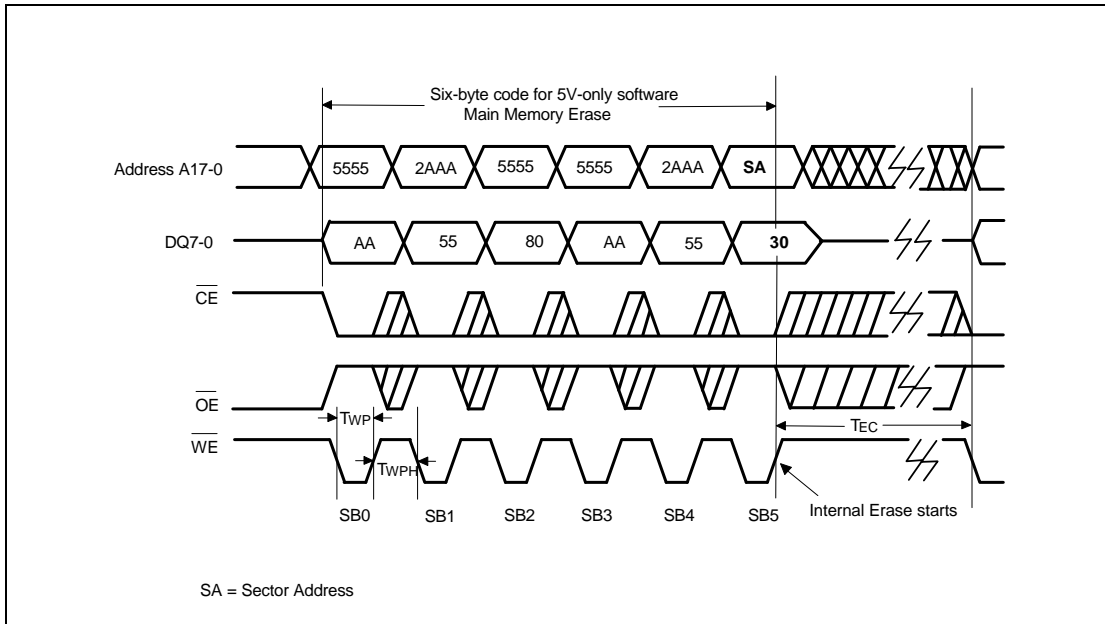


Timing Waveforms, continued

Chip Erase Timing Diagram



Sector Erase Timing Diagram





ORDERING INFORMATION

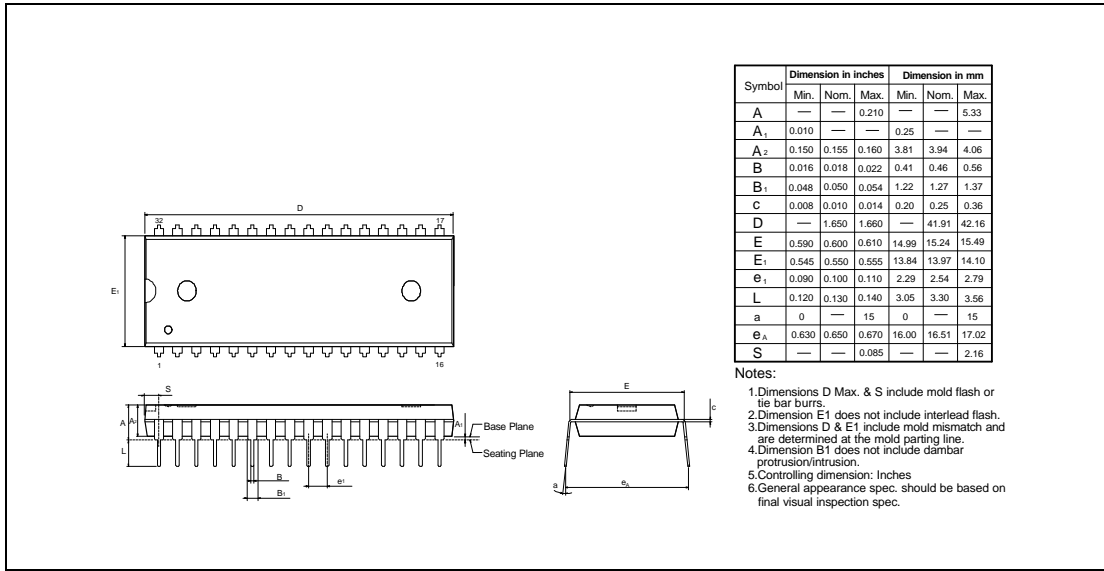
| PART NO. | ACCESS TIME (nS) | POWER SUPPLY CURRENT MAX. (mA) | STANDBY V_{DD} CURRENT MAX. (μ A) | PACKAGE | CYCLE |
|--------------|---------------------|-----------------------------------|---|-----------------------------------|-------|
| W49F002U-70B | 70 | 50 | 100 (CMOS) | 32-pin DIP | 10K |
| W49F002U-90B | 90 | 50 | 100 (CMOS) | 32-pin DIP | 10K |
| W49F002U-12B | 120 | 50 | 100 (CMOS) | 32-pin DIP | 10K |
| W49F002UT70B | 70 | 50 | 100 (CMOS) | 32-pin TSOP (8 mm \times 20 mm) | 10K |
| W49F002UT90B | 90 | 50 | 100 (CMOS) | 32-pin TSOP (8 mm \times 20 mm) | 10K |
| W49F002UT12B | 120 | 50 | 100 (CMOS) | 32-pin TSOP (8 mm \times 20 mm) | 10K |
| W49F002UP70B | 70 | 50 | 100 (CMOS) | 32-pin PLCC | 10K |
| W49F002UP90B | 90 | 50 | 100 (CMOS) | 32-pin PLCC | 10K |
| W49F002UP12B | 120 | 50 | 100 (CMOS) | 32-pin PLCC | 10K |

Notes:

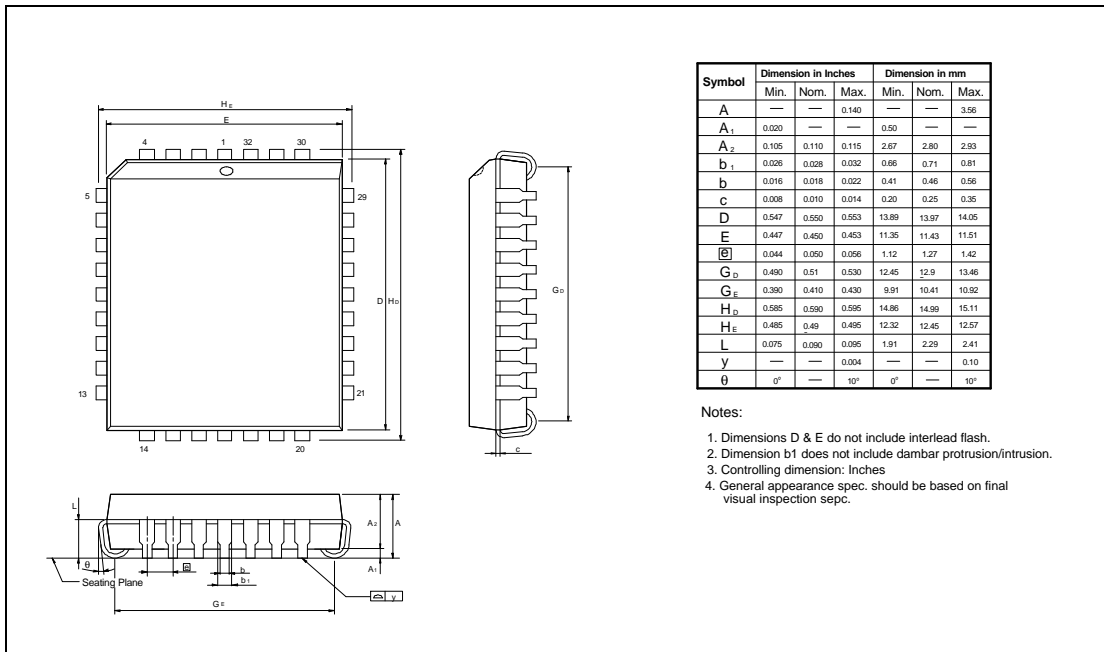
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.
3. Winbond withholds a Boot Block options for Bottom Boot use. Please contact Winbond FAEs for detail information.

PACKAGE DIMENSIONS

32-pin P-DIP

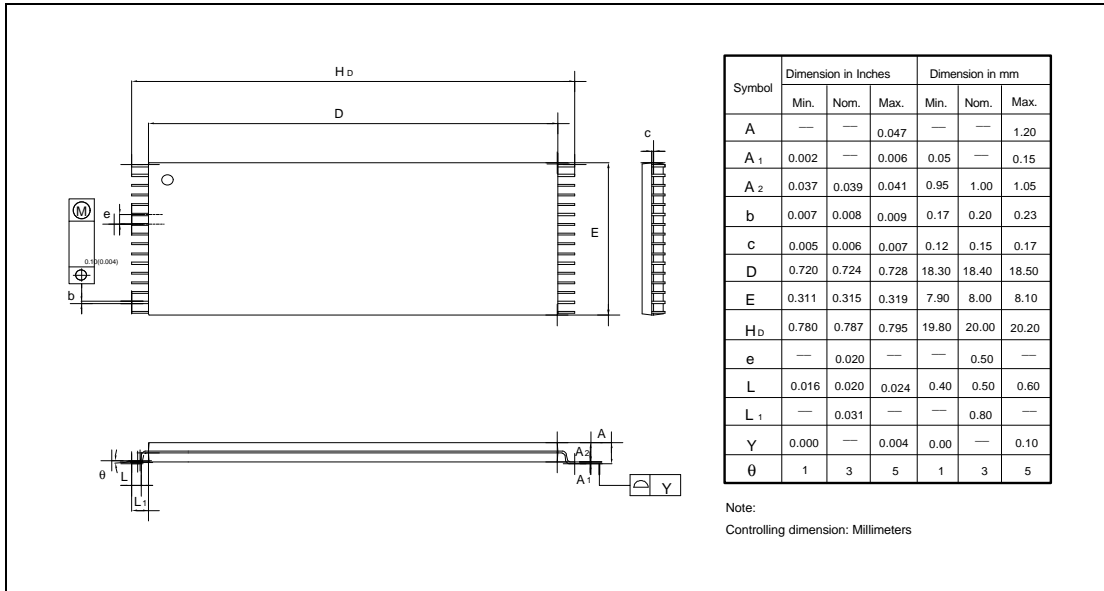


32-pin PLCC



Package Dimensions, continued

32-pin TSOP





VERSION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---------|-----------|--------------|--|
| A1 | Nov. 1999 | - | Renamed from W49F002/B/U/N |
| A2 | Apr. 2000 | 1, 13-15, 20 | Add the 120 nS bin |
| | | 14 | Change Tbp(typ.) from 10 μ S to 35 μ S Change Tec(max.) from 1 Sec to 0.2 Sec |



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Note: All data and specifications are subject to change without notice.

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Revision A2