

N-channel TrenchMOS™ transistor

PHP18NQ20T, PHB18NQ20T

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

| |
|--------------------------------------|
| $V_{DSS} = 200\text{ V}$ |
| $I_D = 16\text{ A}$ |
| $R_{DS(ON)} \leq 180\text{ m}\Omega$ |

GENERAL DESCRIPTION

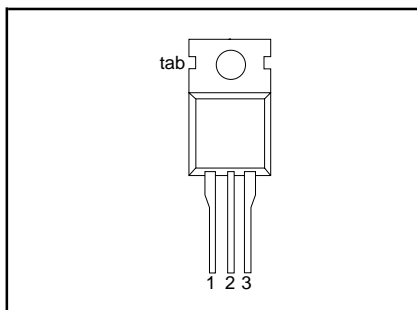
N-channel, enhancement mode field-effect power transistor using **Trench** technology, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP18NQ20T is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB18NQ20T is supplied in the SOT404 (D²PAK) surface mounting package.

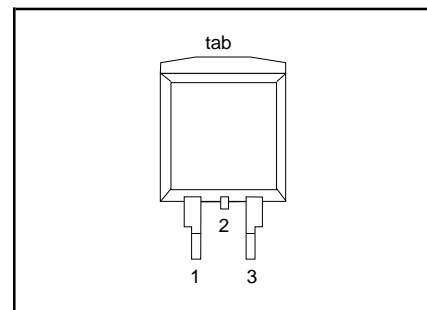
PINNING

| PIN | DESCRIPTION |
|-----|--------------------|
| 1 | gate |
| 2 | drain ¹ |
| 3 | source |
| tab | drain |

SOT78 (TO220AB)



SOT404 (D²PAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------------|--|---|------|----------|------------------|
| V_{DSS} | Drain-source voltage | $T_j = 25\text{ }^\circ\text{C to }175\text{ }^\circ\text{C}$ | - | 200 | V |
| V_{DGR} | Drain-gate voltage | $T_j = 25\text{ }^\circ\text{C to }175\text{ }^\circ\text{C}; R_{GS} = 20\text{ k}\Omega$ | - | 200 | V |
| V_{GS} | Gate-source voltage | | - | ± 20 | V |
| I_D | Continuous drain current | $T_{mb} = 25\text{ }^\circ\text{C}; V_{GS} = 10\text{ V}$ | - | 16 | A |
| | | $T_{mb} = 100\text{ }^\circ\text{C}; V_{GS} = 10\text{ V}$ | - | 11 | A |
| I_{DM} | Pulsed drain current | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 64 | A |
| P_D | Total power dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 136 | W |
| T_j, T_{stg} | Operating junction and storage temperature | | -55 | 175 | $^\circ\text{C}$ |

¹ It is not possible to make connection to pin:2 of the SOT404 package

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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------|---------------------------------------|--|------|------|------|
| E_{AS} | Non-repetitive avalanche energy | Unclamped inductive load, $I_{AS} = 14$ A; $t_p = 100$ μ s; T_j prior to avalanche = 25°C; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; refer to fig;15 | - | 180 | mJ |
| I_{AS} | Peak non-repetitive avalanche current | | - | 16 | A |

THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------|--|--|------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base | SOT78 package, in free air SOT404 and SOT428 packages, pcb mounted, minimum footprint | - | - | 1.1 | K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | | - | 60 | - | K/W |
| | | | - | 50 | - | K/W |

ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------|----------------------------------|---|-------------|--------|--------|--------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0$ V; $I_D = 0.25$ mA; $T_j = -55^\circ\text{C}$ | 200 178 | - | - | V V |
| $V_{GS(TO)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$ | 2 1 - | 3 - | 4 - | V V V |
| $R_{DS(ON)}$ | Drain-source on-state resistance | $V_{GS} = 10$ V; $I_D = 8$ A $T_j = 175^\circ\text{C}$ | - | 130 | 180 | m Ω m Ω |
| I_{GSS} | Gate source leakage current | $V_{GS} = \pm 10$ V; $V_{DS} = 0$ V | - | 10 | 100 | nA |
| I_{DSS} | Zero gate voltage drain current | $V_{DS} = 200$ V; $V_{GS} = 0$ V; $T_j = 175^\circ\text{C}$ | - | 0.05 | 10 | μ A μ A |
| $Q_{g(tot)}$ | Total gate charge | $I_D = 16$ A; $V_{DD} = 160$ V; $V_{GS} = 10$ V | - | 47 | - | nC |
| Q_{gs} | Gate-source charge | | - | 9 | - | nC |
| Q_{gd} | Gate-drain (Miller) charge | | - | 22 | - | nC |
| t_{don} | Turn-on delay time | $V_{DD} = 100$ V; $R_D = 5.6$ Ω ; $V_{GS} = 10$ V; $R_G = 5.6$ Ω Resistive load | - | 12 | - | ns |
| t_r | Turn-on rise time | | - | 45 | - | ns |
| t_{doff} | Turn-off delay time | | - | 54 | - | ns |
| t_f | Turn-off fall time | | - | 38 | - | ns |
| L_d | Internal drain inductance | Measured tab to centre of die | - | 3.5 | - | nH |
| L_d | Internal drain inductance | Measured from drain lead to centre of die (SOT78 package only) | - | 4.5 | - | nH |
| L_s | Internal source inductance | Measured from source lead to source bond pad | - | 7.5 | - | nH |
| C_{iss} | Input capacitance | $V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz | - | 1850 | - | pF |
| C_{oss} | Output capacitance | | - | 170 | - | pF |
| C_{rss} | Feedback capacitance | | - | 91 | - | pF |

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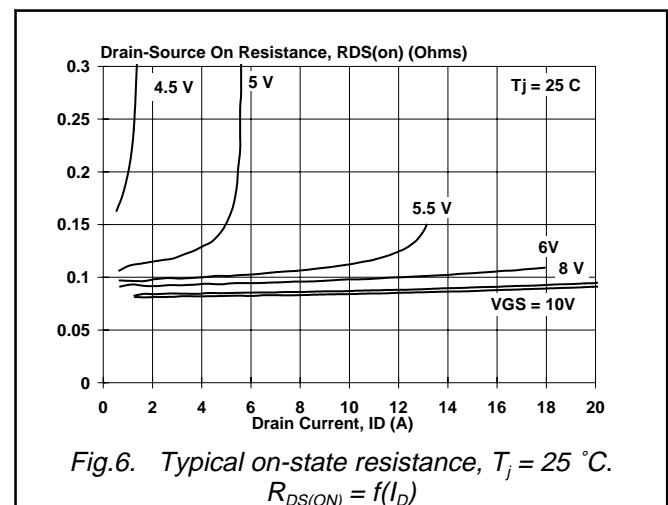
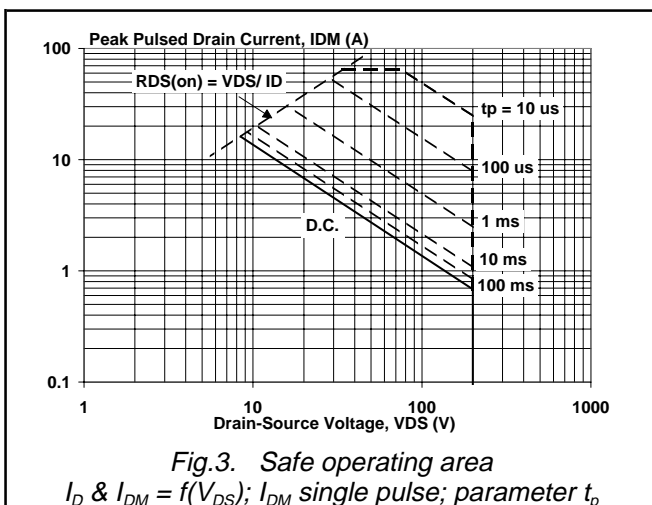
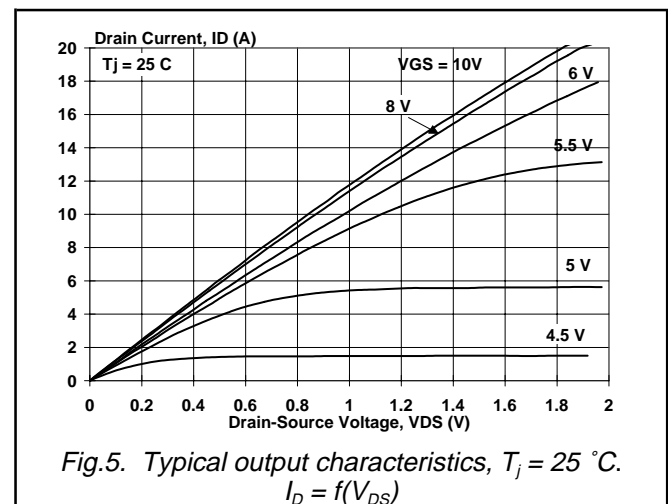
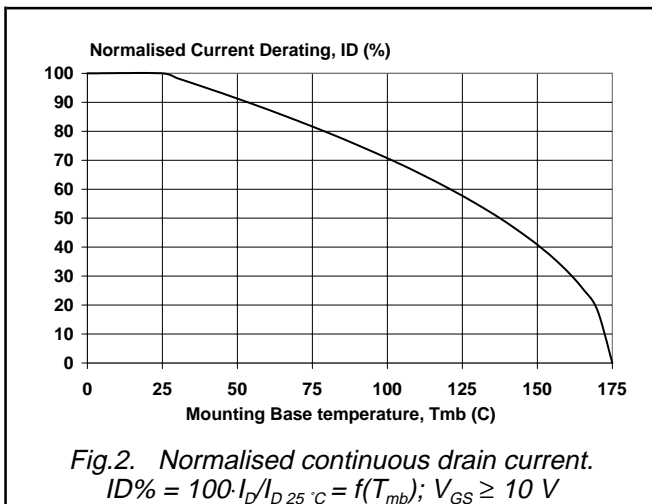
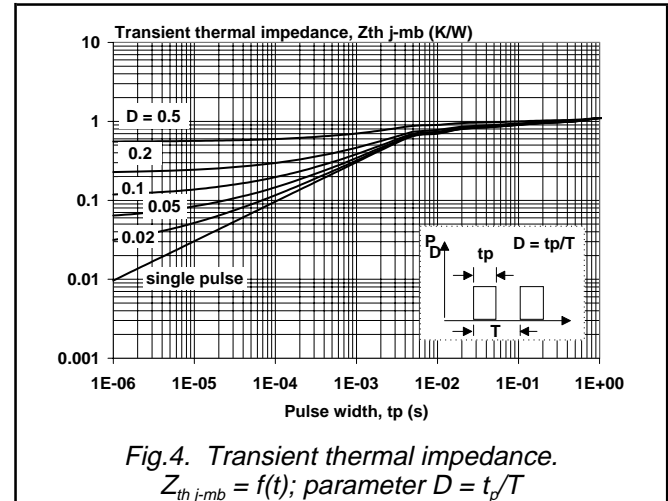
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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------|--|---|------|------|------|---------------|
| I_S | Continuous source current (body diode) | | - | - | 16 | A |
| I_{SM} | Pulsed source current (body diode) | | - | - | 64 | A |
| V_{SD} | Diode forward voltage | $I_F = 16\text{ A}; V_{GS} = 0\text{ V}$ | - | 0.9 | 1.2 | V |
| t_{rr} | Reverse recovery time | $I_F = 16\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $V_{GS} = 0\text{ V}; V_R = 25\text{ V}$ | - | 130 | - | ns |
| Q_{rr} | Reverse recovery charge | | - | 0.8 | - | μC |

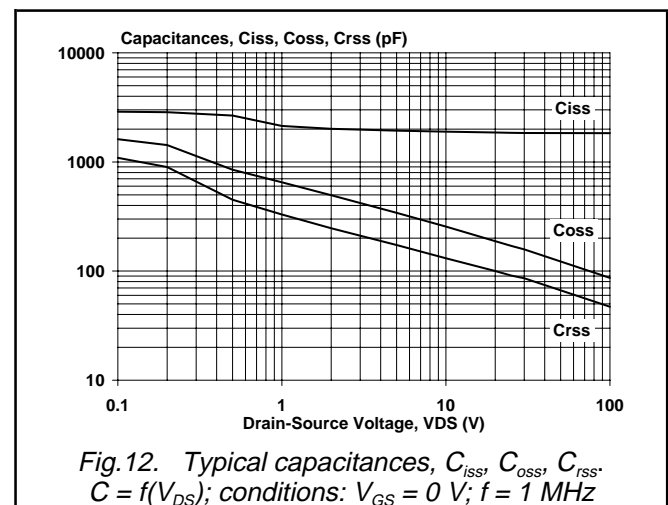
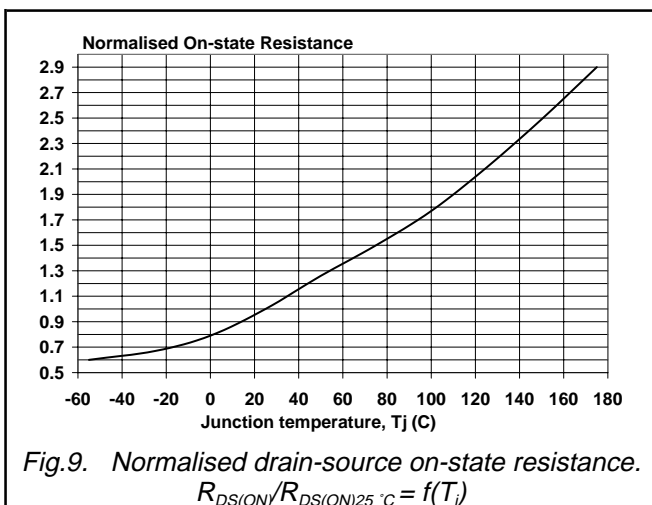
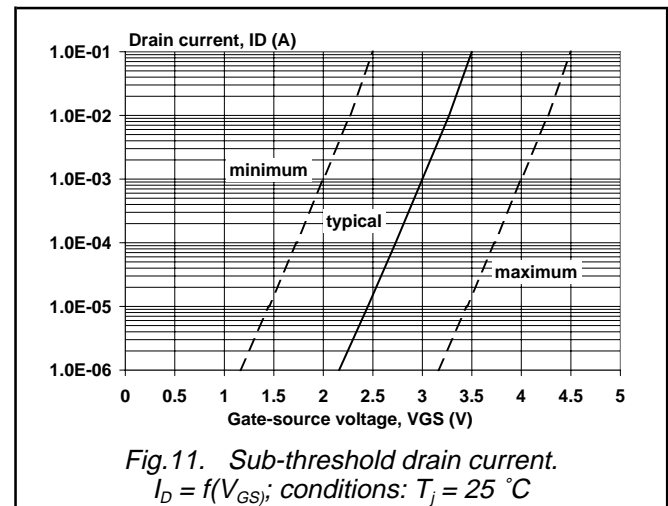
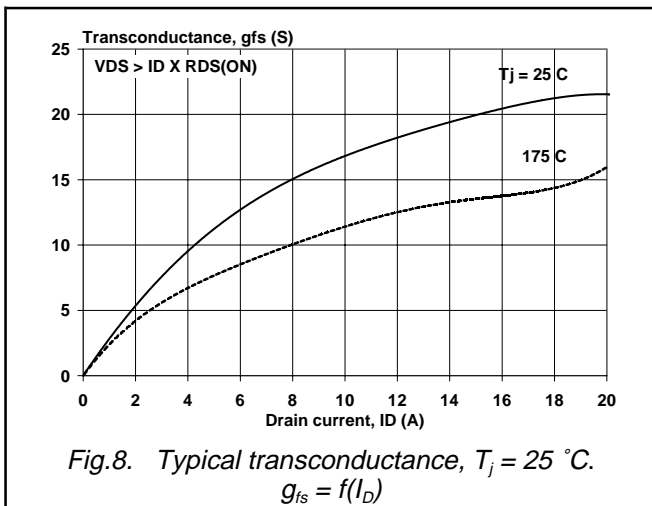
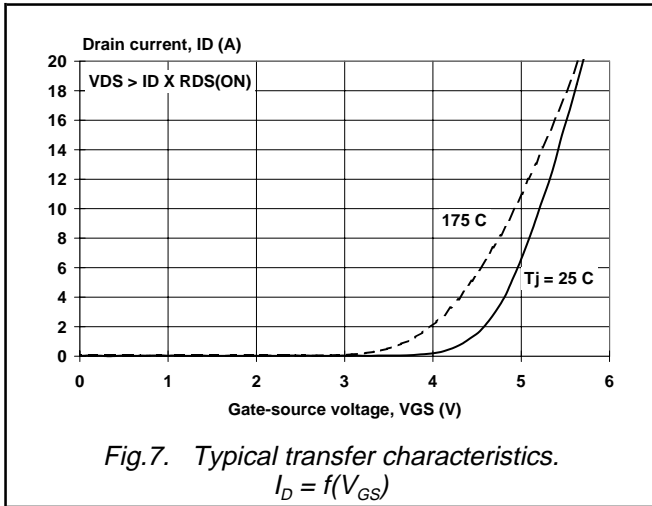
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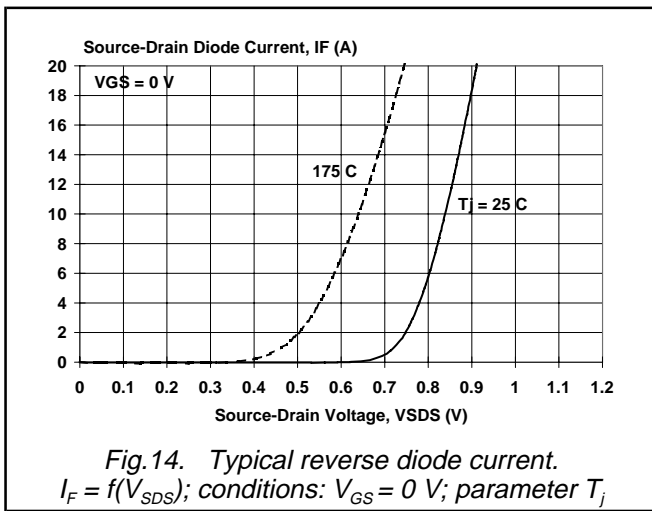
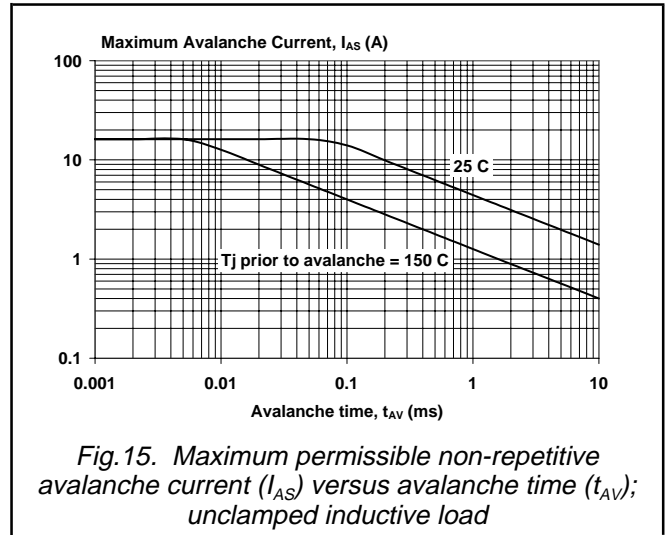
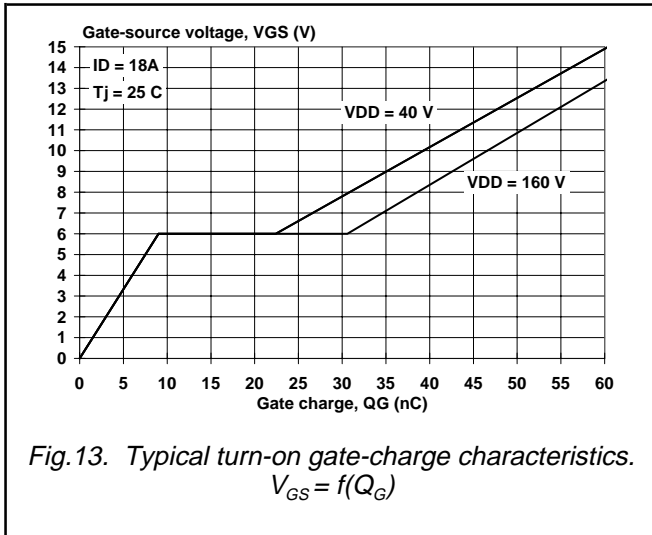
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MECHANICAL DATA

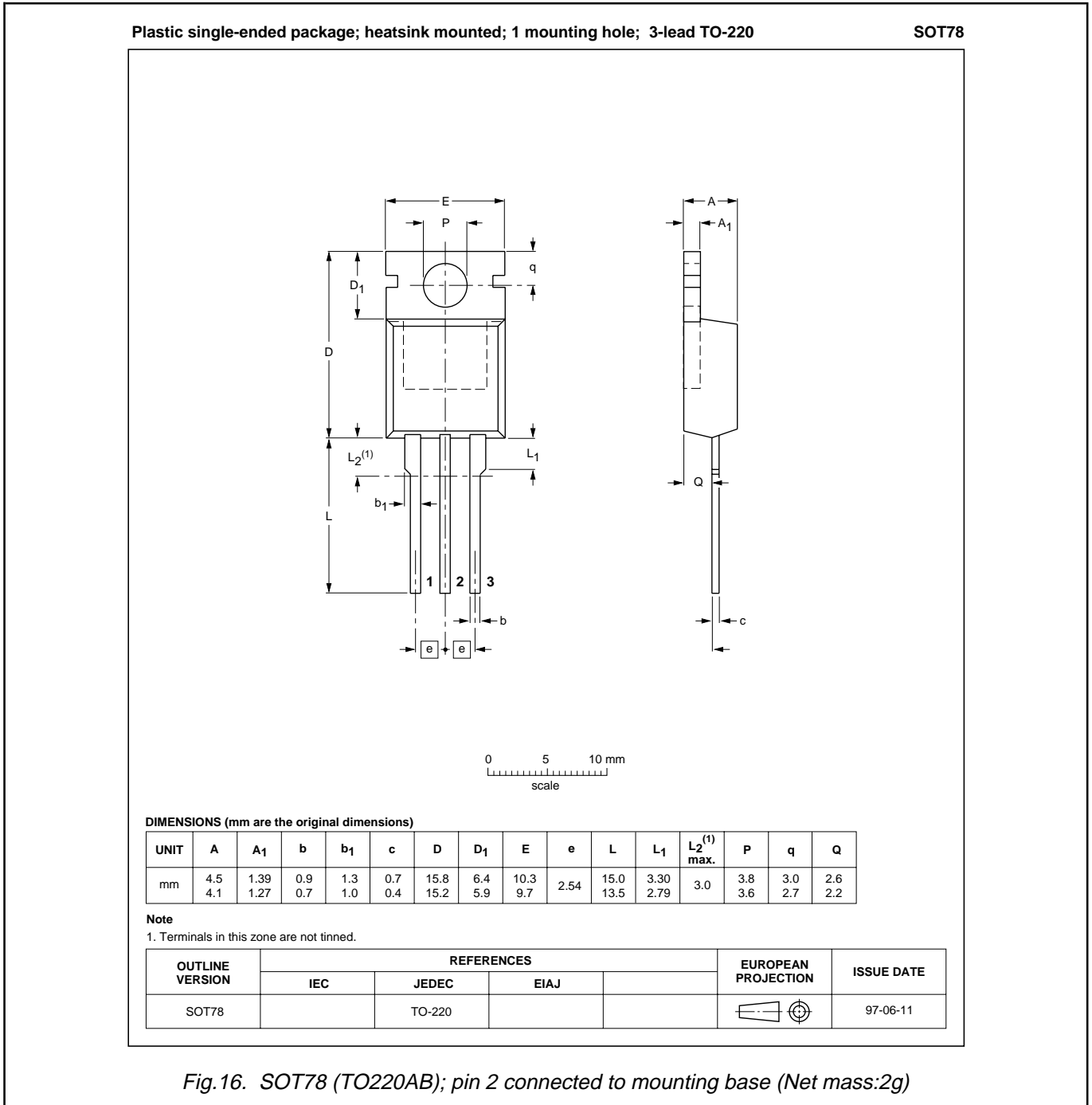


Fig. 16. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

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MECHANICAL DATA



Fig.17. SOT404 surface mounting package. Centre pin connected to mounting base.

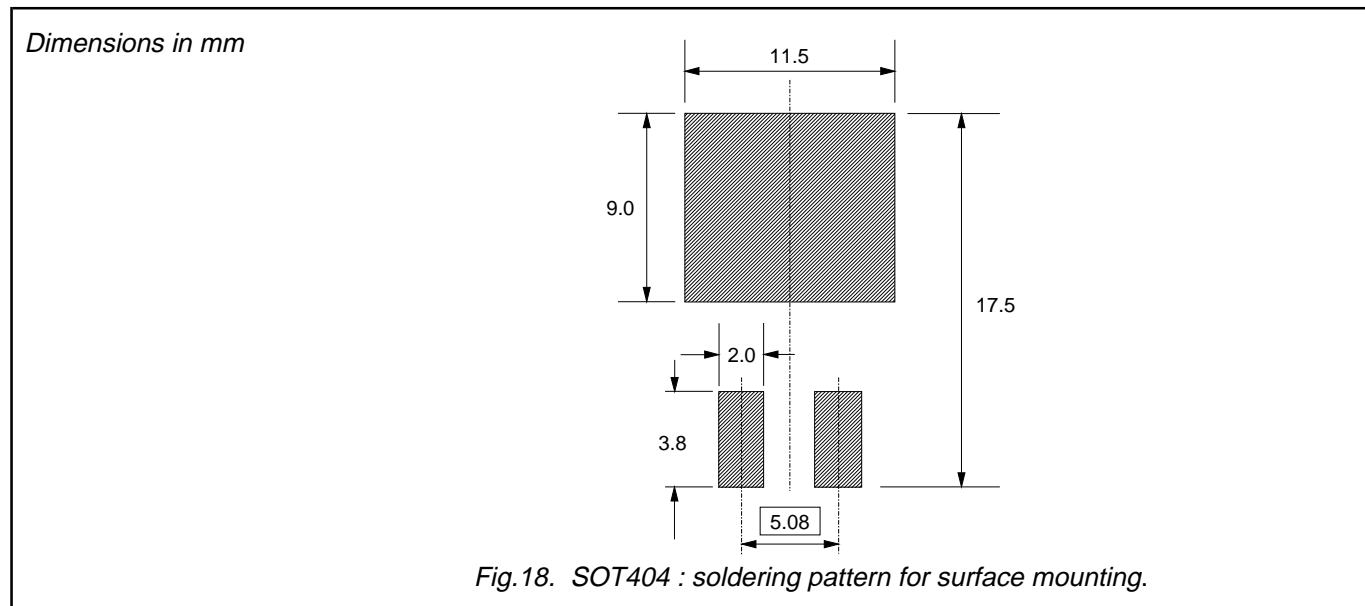
Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

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MOUNTING INSTRUCTIONS



DEFINITIONS

| | |
|--|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
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