HD74LS195A

4-bit Parallel-Access Shift Register

REJ03D0457–0300
Rev.3.00
Jul.15.2005

This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift / load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

- Parallel (broadside) load
- Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift / load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shifting is accomplished synchronously when the shift / load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

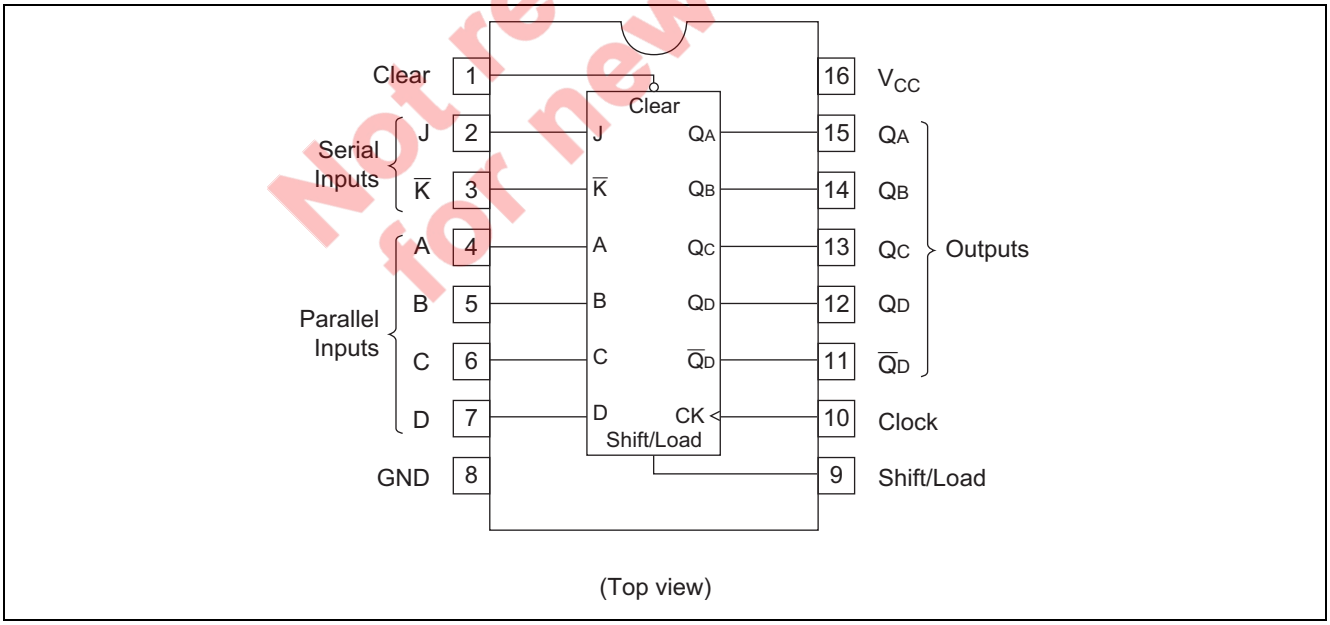
Not recommend for new design

Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS195AFPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Pin Arrangement



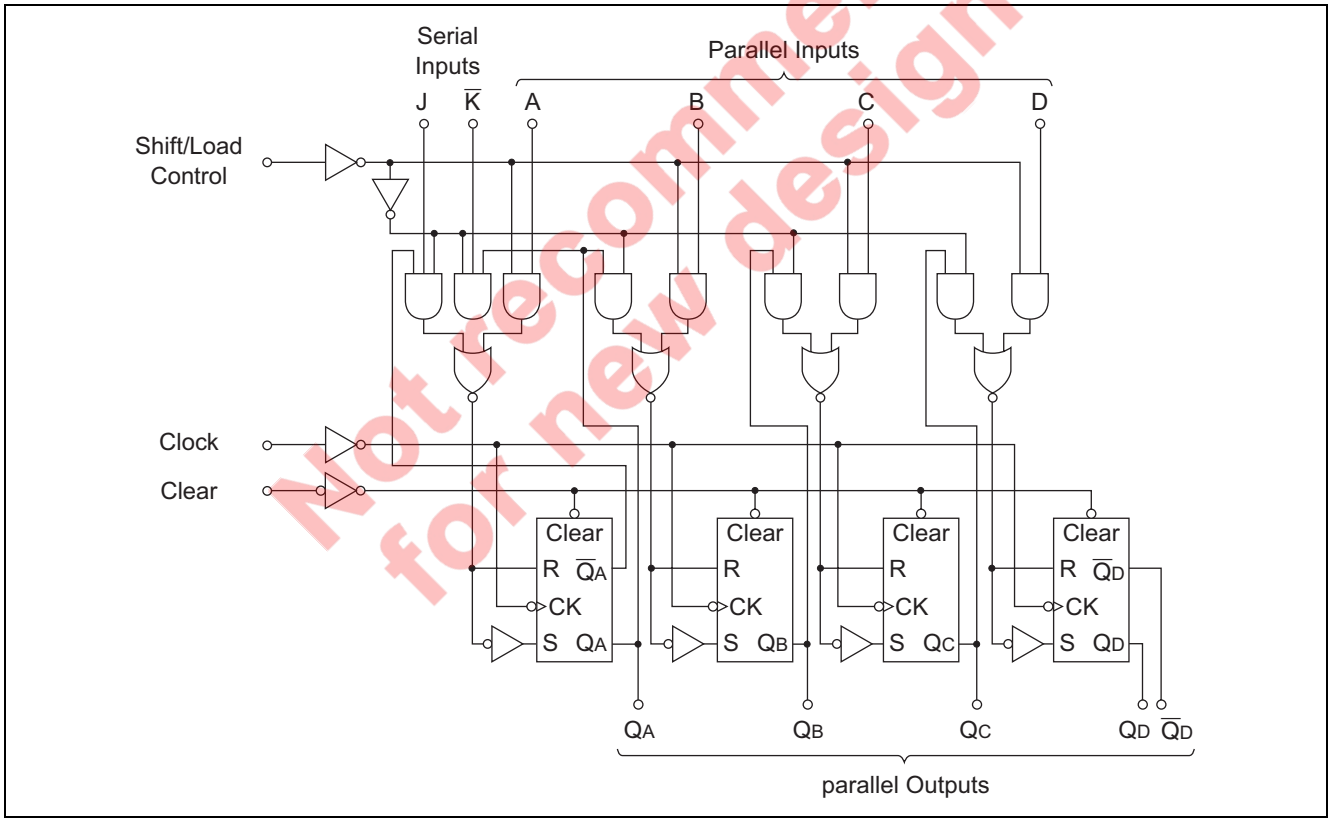
(Top view)

Function Table

Inputs									Outputs				
Clear	Shift / Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Notes: 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. a to d; the level of steady-state input at inputs A, B, C, or D, respectively
4. Q_{A0} to Q_{D0}; the level of Q_A, Q_B, Q_C, or Q_D, respectively before the indicated steady-state input conditions were established.
5. Q_{An} to Q_{Cn}; the level of Q_A, Q_B, Q_C, respectively before the most-recent ↑ transition of the clock.

Block Diagram



Not recommend for new design

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	–20	25	75	°C
Clock frequency		f_{clock}	0	—	30	MHz
Clock pulse width		$t_{w\,(CK)}$	16	—	—	ns
Clear pulse width		$t_{su\,(CLR)}$	12	—	—	ns
Setup time	Shift / load	t_{su}	25	—	—	ns
	Serial and parallel data		15	—	—	ns
	Clear inactive-state		25	—	—	ns
Release time		$t_{release}$	—	—	5	ns
Hold time		t_h	0	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA; V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
		—	—	0.5		I_{OL} = 8 mA
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
Short-circuit output current	I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**	I_{CC}	—	14	21	mA	V_{CC} = 5.25 V
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

** With all outputs open, shift / load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

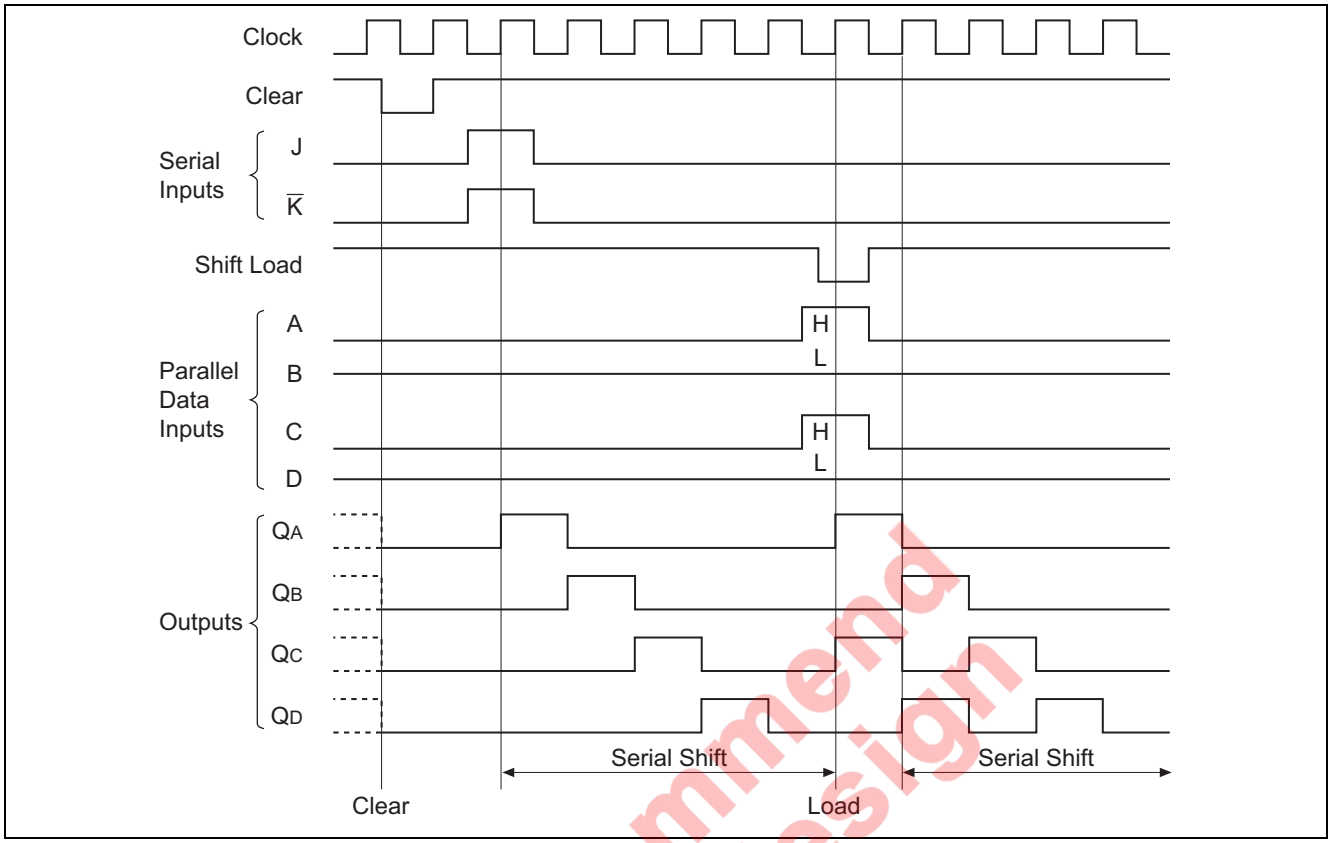
Not recommend for new design

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}	Clock	Q_A to Q_D	30	39	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PHL}	Clear	Q_A to Q_D	—	19	30	ns	
	t_{PLH}	Clock	Q_A to Q_D	—	14	22	ns	
	t_{PHL}		$\overline{Q}_D$	—	17	26	ns	

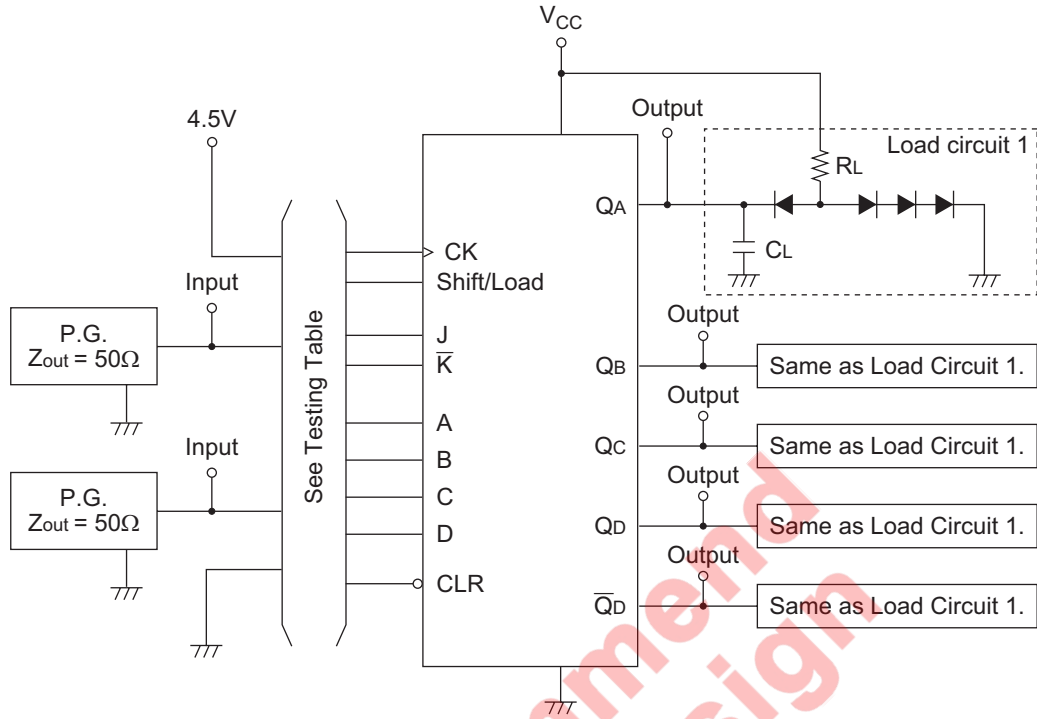
Count Sequence



Not recommend for new design

Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

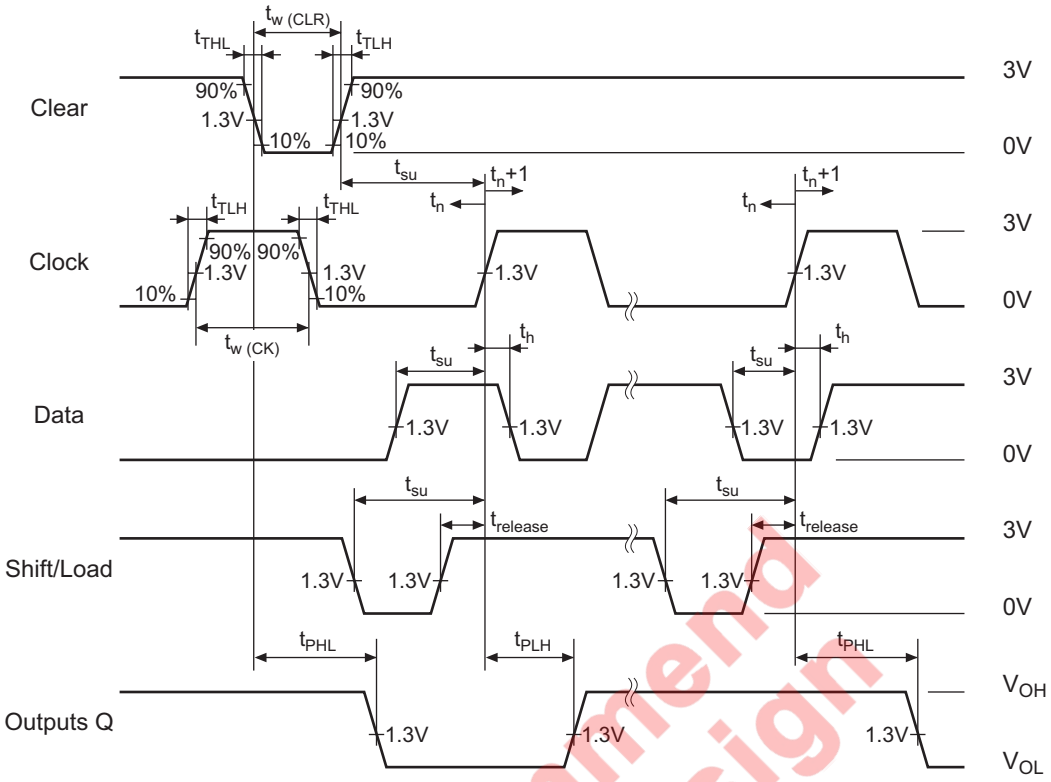
Not recommend for new design

Testing Table

Item	From input to output	Inputs								
		CLR	Shift / Load	J	$\overline{K}$	CK	A	B	C	D
f_{max}		4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V
t_{PLH} t_{PHL}	Clear→ Q_A to Q_D	IN	GND	4.5V	4.5V	IN	4.5V	4.5V	4.5V	4.5V
	Clock→ Q_A to Q_D, $\overline{Q}_D$	4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V
		4.5V	GND	4.5V	4.5V	IN	IN	IN	IN	IN

Item	From input to output	Outputs				
		Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
f_{max}		OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	Clear→ Q_A to Q_D	OUT	OUT	OUT	OUT	—
	Clock→ Q_A to Q_D, $\overline{Q}_D$	OUT	OUT	OUT	OUT	OUT
		OUT	OUT	OUT	OUT	OUT

Waveform

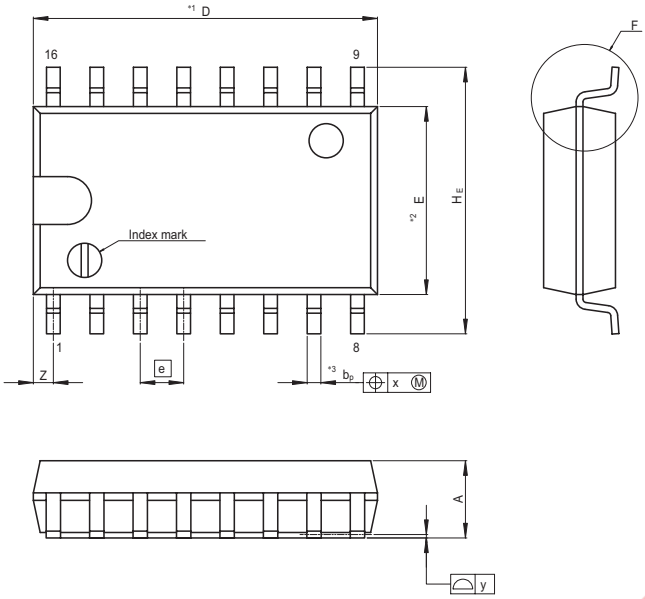


Notes:
1. Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%
2. A clear pulse is applied prior to each test.
3. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.
4. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift / load input remains high.
5. t_n; bit time beroer clocking transition.
6. t_{n+1}; bit time after one clocking transition.
7. t_{n+4}; bit time after four clocking transition.

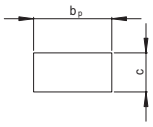
Not recommend for new design

Package Dimensions

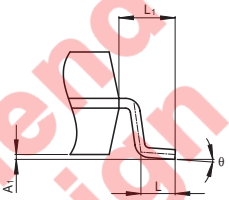
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A_2	——	——	——
A_1	0.00	0.10	0.20
A	——	——	2.20
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L_1	——	1.15	——

Not recommend for new design

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!
1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials
1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.

Not recommend for new design

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

© 2005. Renesas Technology Corp., All rights reserved. Printed in Japan.

Colophon .3.0