

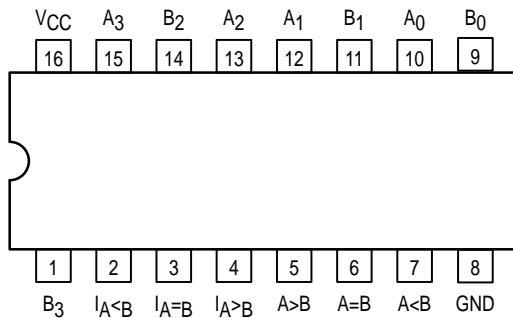


4-BIT MAGNITUDE COMPARATOR

The MC54/74F85 is a 4-Bit Magnitude Comparator which compares two 4-Bit words (A_0-A_3, B_0-B_3), A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes; the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($0_A > B$), "A less than B" ($0_A < B$), "A equal to B" ($0_A = B$). Three Expander Inputs, $I_A > B, I_A < B, I_A = B$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_A < B = I_A > B = L, I_A = B = H$. For serial (ripple) expansion the $0_A > B, 0_A < B$ Outputs are connected respectively to the $I_A > B$ and $I_A = B$ inputs of the next most significant comparator, as shown in Figure 1. Refer to applications section of data sheet for high speed method of comparing large words.

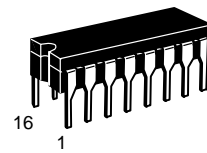
- High Impedance NPN Base Inputs for Reduced Loading (20 μ A in HIGH and LOW States)
- Magnitude Comparison of any Binary Words
- Serial or Parallel Expansion Without Extra Gating
- ESD > 4000 Volts

CONNECTION DIAGRAM

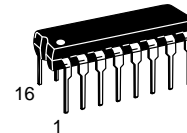


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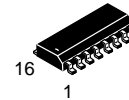
4-BIT MAGNITUDE COMPARATOR
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

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FUNCTION TABLE

Comparing Inputs				Expansion Inputs			Outputs		
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _A > B	I _A < B	I _A = B	A > B	A < B	A = B
A ₃ > B ₃	X	X	X	X	X	X	H	L	L
A ₃ < B ₃	X	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ > B ₂	X	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ < B ₂	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	L	L	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	H	L	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	X	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	H	L	L	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	L	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

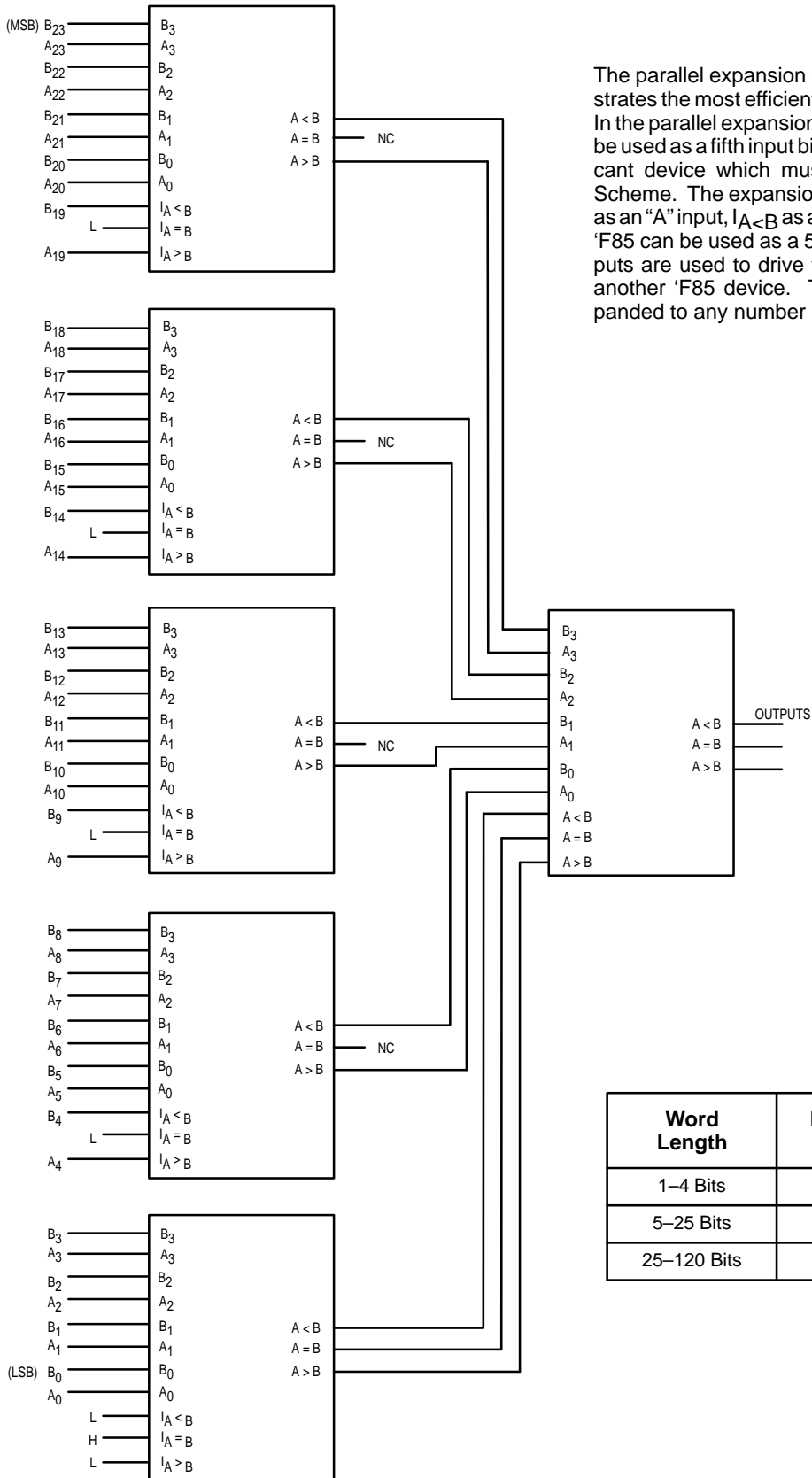
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA V _{CC} = 4.50 V
		74	2.7			
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = 0 V, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-20	μA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Total Supply Current				mA	V _{CC} = MAX
	HIGH V _{IN} = HIGH			50		
	LOW A _n = B _n = I _A -B = GND: I _A >B = I _A <B = 4.5 V			54		

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

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The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the Serial Scheme. The expansion inputs are used by labelling I_{A > B} as an "A" input, I_{A < B} as a "B" input and setting I_{A = B} low. The 'F85 can be used as a 5-bit comparator only when the outputs are used to drive the (A₀-A₃) and (B₀-B₃) inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1

Word Length	Number of Packages	Typical Speeds 74F
1-4 Bits	1	12 ns
5-25 Bits	2-6	22 ns
25-120 Bits	8-31	34 ns

Figure 1. Comparison of Two 24-Bit Words

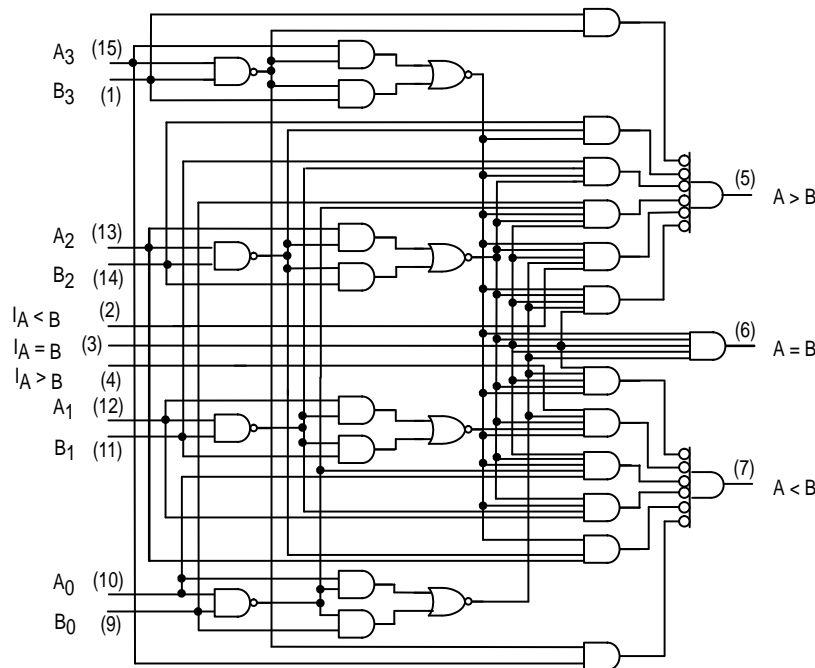
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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
t_{PLH}	A or B Input to	6.0	11	5.5	14	5.5	13	ns
t_{PHL}	A < B, A > B Output	6.0	14	5.5	16.5	5.5	15.5	
t_{PLH}	A or B Input to	5.5	11.5	5.0	15	5.0	14	ns
t_{PHL}	A = B Output	7.0	14	6.5	15.5	6.5	14.5	
t_{PLH}	$I_{A<B}$ and $I_{A=B}$ Input	3.0	7.5	2.5	10	2.5	9.0	ns
t_{PHL}	to A > B Output	3.0	9.0	2.5	11	2.5	10	
t_{PLH}	$I_{A=B}$ Input to	2.5	7.0	2.0	10	2.0	9.0	ns
t_{PHL}	A = B Output	3.5	10	2.5	13	2.5	12	
t_{PLH}	$I_{A>B}$ and $I_{A=B}$ Input	3.0	8.0	3.0	10.5	3.0	9.5	ns
t_{PHL}	to A < B Output	3.0	9.0	2.0	10.5	2.0	9.5	

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A > B, A = B, and A < B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15 ns

is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B} = \text{LOW}$, $I_{A=B} = \text{HIGH}$, and $I_{A<B} = \text{LOW}$.



NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 2. Logic Diagram