REALTEK SINGLE CHIP SINGLE PORT 10/100M FAST ETHERNET PHYCEIVER RTL8201CL

1. Features **2**
2. General Description **2**
3. Block Diagram **3**
4. Pin Assignments **4**
5. Pin Description **5**
5.1 MII Interface 5
5.2 SNI (Serial Network Interface): 10Mbps only 5
5.3 Clock Interface 6
5.4 10Mbps / 100Mbps Network Interface 6
5.5 Device Configuration Interface 6
5.6 LED Interface/PHY Address Config 7
5.7 Reset and other pins 7
5.8 Power and Ground pins 7
6. Register Descriptions **8**
6.1 Register 0 Basic Mode Control Register 8
6.2 Register 1 Basic Mode Status Register 9
6.3. Register 2 PHY Identifier Register 1 9
6.4. Register 3 PHY Identifier Register 2 9
6.5. Register 4 Auto-negotiation Advertisement Register(ANAR) 10
6.6 Register 5 Auto-Negotiation Link Partner Ability Register(ANLPAR) 10
6.7 Register 6 Auto-negotiation Expansion Register(ANER) 11
6.8 Register 16 Nway Setup Register(NSR) 11
6.9 Register 17 Loopback, Bypass, Receiver Error Mask Register(LBREMR) 12
6.10 Register 18 RX_ER Counter(REC) 12
6.11 Register 19 SNR Display Register 12
6.12 Register 25 Test Register 13
7. Functional Description **14**
7.1 MII and Management Interface 14
7.1.1 Data Transition 14
7.1.2 Serial Management 15
7.2 Auto-negotiation and Parallel Detection 16
7.3 Flow control support 17
7.4 Hardware Configuration and Auto-negotiation 17
7.5 LED and PHY Address Configuration 18
7.6 Serial Network Interface 18
7.7 Power Down, Link Down, Power Saving, and Isolation Modes 18
7.8 Media Interface 19
7.8.1 100Base TX 19
7.8.2 100Base-FX Fiber Mode Operation 19
7.8.3 10Base Tx/Rx 20
7.9 Repeater Mode Operation 20
7.10 Reset, and Transmit Bias(RTSET) 20
7.11 3.3V power supply and voltage conversion circuit 20
7.12 Far End Fault Indication (FEFI) 21
8. Electrical Characteristics **22**
8.1 D.C. Characteristics 22
8.1.1. Absolute Maximum Ratings 22
8.1.2. Operating Conditions 22
8.1.3. Power Dissipation 22
8.1.4 Supply Voltage: Vcc 22
8.2 A.C. Characteristics 23
8.2.1 MII Timing of Transmission Cycle 23
8.2.2 MII Timing of Reception Cycle 24
8.2.3 SNI Timing of Transmission Cycle 25
8.2.4 SNI Timing of Reception Cycle 26
8.2.5 MDC/MDIO timing 27
8.2.6 Transmission Without Collision 27
8.2.7 Reception Without Error 28
8.3 Crystal and Transformer Specifications 29
8.3.1 Crystal Specifications 29
8.3.2 Transformer Specifications 29
9. Mechanical Dimensions **30**
10. Revision History **31**

1. Features

The Realtek RTL8201CL is a Fast Ethernet Phyceiver with selectable MII or SNI interface to the MAC chip. It provides the following features:

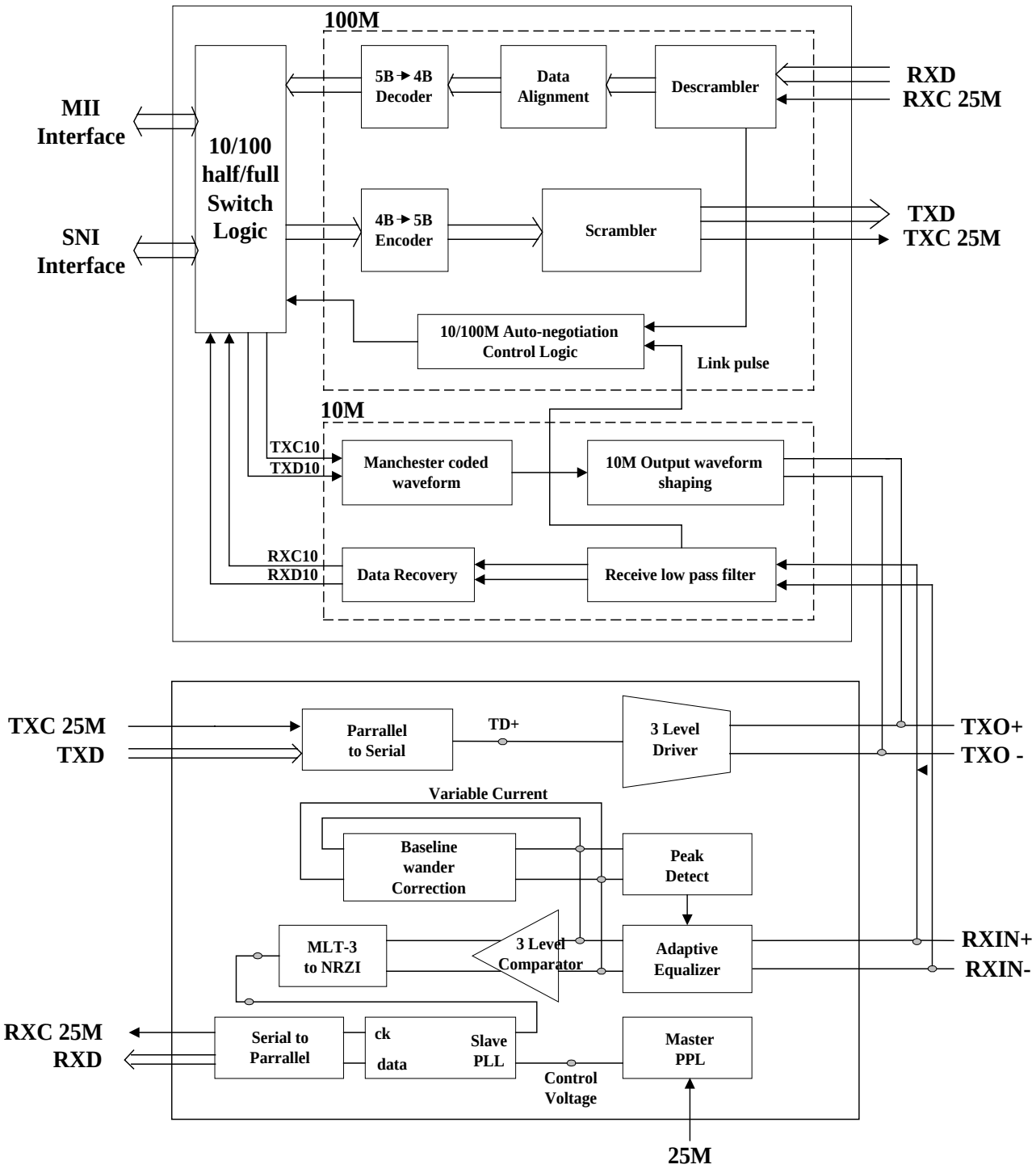
- Supports MII/7-wire SNI (Serial Network Interface) interface
- Supports 10/100Mbps operation
- Supports half/full duplex operation
- Support of twisted pair or Fiber mode output
- IEEE 802.3/802.3u compliant
- Supports IEEE 802.3u clause 28 auto negotiation
- Supports power down mode
- Supports operation under Link Down Power Saving mode
- Supports Base Line Winder (BLW) compensation
- Supports repeater mode
- Speed/duplex/auto negotiation adjustable
- 3.3V operation with 5V IO signal tolerance
- Low operation power consumption and only need single supply 3.3V
- Adaptive Equalization
- 25MHz crystal/oscillator as clock source
- Multiple network status LED support
- Flow control ability support to co-work with MAC (by MDC/MDIO)
- 48 pin LQFP package

2. General Description

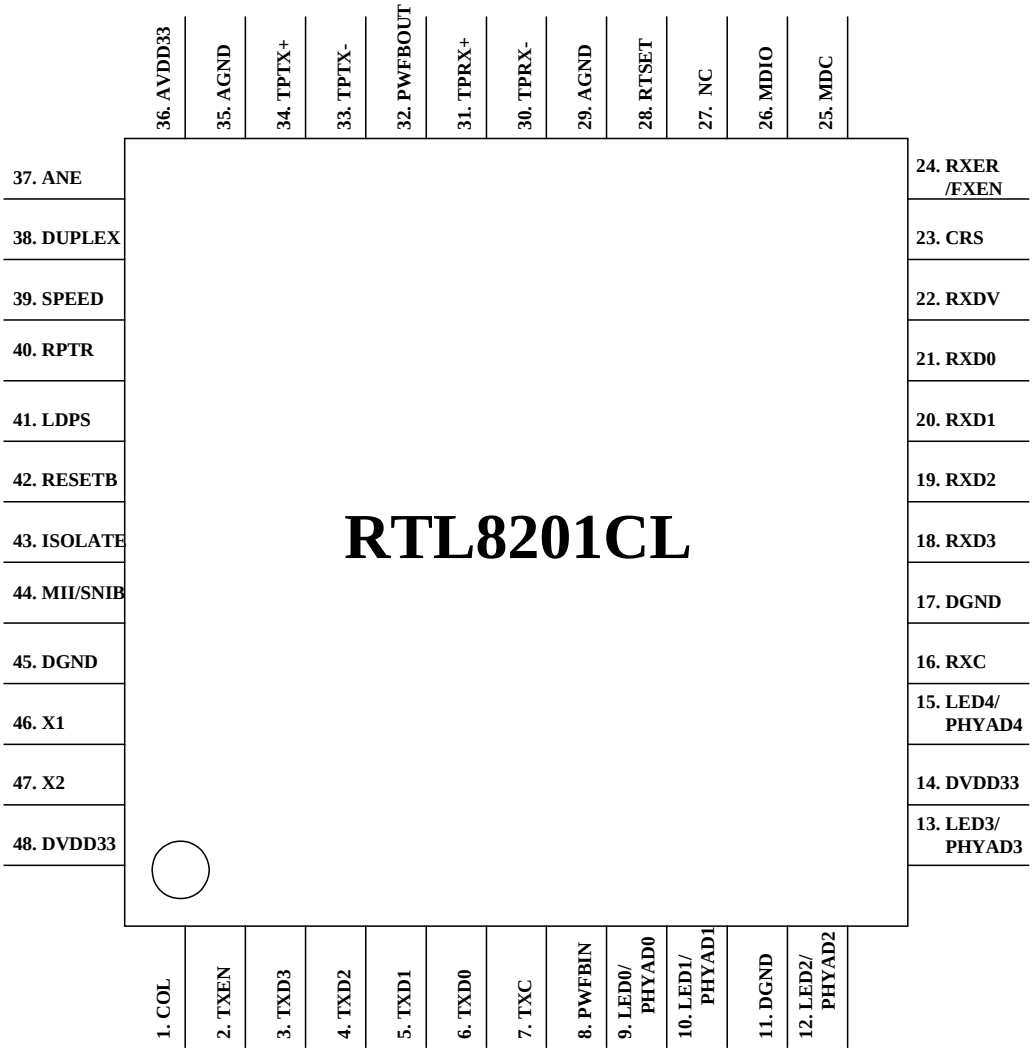
The RTL8201CL is a single-port Phyceiver with an MII (Media Independent Interface)/SNI (Serial Network Interface). It implements all 10/100M Ethernet Physical-layer functions including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), 10Base-Tx Encoder/Decoder and Twisted Pair Media Access Unit (TPMAU). A PECL interface is supported to connect with an external 100Base-FX fiber optical transceiver. The chip is fabricated with an advanced CMOS process to meet low voltage and low power requirements. Further more, it is developed with on chip Digital Signal Processing technology to ensure excellent performance under all operating conditions.

The RTL8201CL can be used as a Network Interface Adapter, MAU, CNR, ACR, Ethernet Hub, and Ethernet Switch. Additionally, it can also be used in any embedded system with an Ethernet MAC that needs a UTP physical connection or Fiber PECL interface to external 100Base-FX optical transceiver module.

3. Block Diagram



4. Pin Assignments



5. Pin Description

LI: Latched Input during Power up or Reset
I/O: Bi-directional input and output
I: Input
O: Output
P: Power

5.1 MII Interface

Symbol	Type	Pin No.	Description
TXC	O	7	**Transmit Clock:** This pin provides a continuous clock as a timing reference for TXD[3:0] and TXEN.
TXEN	I	2	**Transmit Enable:** The input signal indicates the presence of a valid nibble data on TXD[3:0].
TXD[3:0]	I	3, 4, 5, 6	**Transmit Data:** MAC will source TXD[0..3] synchronous with TXC when TXEN is asserted.
RXC	O	16	**Receive Clock:** This pin provides a continuous clock reference for RXDV and RXD[0..3] signals. RXC is 25MHz in the 100Mbps mode and 2.5Mhz in the 10Mbps mode.
COL	O	1	**Collision Detect:** COL is asserted high when a collision is detected on the media.
CRS	O	23	**Carrier Sense:** This pin's signal is asserted high if the media is not in IDEL state.
RXDV	O	22	**Receive Data Valid:** This pin's signal is asserted high when received data is present on the RXD[3:0] lines; the signal is de-asserted at the end of the packet. The signal is valid on the rising of the RXC.
RXD[3:0]	O	18, 19, 20, 21	**Receive Data:** These are the four parallel receive data lines aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY).
RXER/ FXEN	O/LI	24	**Receive Error:** if any 5B decode error occurs, such as invalid J/K, T/R, invalid symbol, this pin will go high. **Fiber/UTP Enable:** During power on reset, this pin status is latched to determine at which media mode to operate: 1: Fiber mode 0: UTP mode An internal weak pull low resistor, sets this to the default of UTP mode. It is possible to use an external 5.1KΩ pull high resistor to enable fiber mode. After power on, the pin operates as the Receive Error pin.
MDC	I	25	**Management Data Clock:** This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks. The clock rate can be up to 2.5MHz.
MDIO	I/O	26	**Management Data Input/Output:** This pin provides the bi-directional signal used to transfer management information.

5.2 SNI (Serial Network Interface): 10Mbps only

Symbol	Type	Pin No.	Description
COL	O	1	**Collision Detect**
RXD0	O	21	**Received Serial Data**
CRS	O	23	**Carrier Sense**
RXC	O	16	**Receive Clock:** Resolved from received data
TXD0	I	6	**Transmit Serial Data**
TXC	O	7	**Transmit Clock:** Generate by PHY
TXEN	I	2	**Transmit Enable:** For MAC to indicate transmit operation

5.3 Clock Interface

Symbol	Type	Pin No.	Description
X2	O	47	**25MHz Crystal Output:** This pin provides the 25MHz crystal output. It must be left open when an external 25MHz oscillator drives X1.
X1	I	46	**25MHz Crystal Input:** This pin provides the 25MHz crystal input. If a 25MHz oscillator is used, connect X1 to the oscillator's output. Refer to section 8.3 to obtain clock source specifications.

5.4 10Mbps / 100Mbps Network Interface

Symbol	Type	Pin No.	Description
TPTX+ TPTX-	O O	34 33	**Transmit Output:** Differential transmit output pair shared by 100Base-TX, 100Base-FX and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 100Base-FX, the output is pseudo-ECL level.
RTSET	I	28	**Transmit Bias Resistor Connection:** This pin should be pulled to GND by a 5.9KΩ (1%) resistor to define driving current for transmit DAC. The resistance value may be changed, depending on experimental results of the RTL8201CL.
TPRX+ TPRX-	I I	31 30	**Receive Input:** Differential receive input pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes.

5.5 Device Configuration Interface

Symbol	Type	Pin No.	Description
ISOLATE	I	43	Set high to isolate the RTL8201CL from the MAC. This will also isolate the MDC/MDIO management interface. In this mode, the power consumption is minimum. This pin can be directly connected to GND or VCC.
RPTR	I	40	Set high to put the RTL8201CL into repeater mode. This pin can be directly connected to GND or VCC.
SPEED	LI	39	This pin is latched to input during a power on or reset condition. Set high to put the RTL8201CL into 100Mbps operation. This pin can be directly connected to GND or VCC.
DUPLEX	LI	38	This pin is latched to input during a power on or reset condition. Set high to enable full duplex. This pin can be directly connected to GND or VCC.
ANE	LI	37	This pin is latched to input during a power on or reset condition. Set high to enable Auto-negotiation mode, set low to force mode. This pin can be directly connected to GND or VCC.
LDPS	I	41	Set high to put the RTL8201CL into LDPS mode. This pin can be directly connected to GND or VCC. Refer to Section 7.7 for more information.
MII/SNIB	LI/O	44	This pin is latched to input during a power on or reset condition. Pull high to set the RTL8201CL into MII mode operation. Set low for SNI mode. This pin can be directly connected to GND or VCC.

5.6 LED Interface/PHY Address Config

These five pins are latched into the RTL8201CL during power up reset to configure PHY address [0:4] used for MII management register interface. And then, in normal operation after initial reset, they are used as driving pins for status indication LED. The driving polarity, active low or active high, is determined by each latched status of the PHY address [4:0] during power-up reset. If latched status is High then it will be active low, and if latched status is Low then it will be active high. Refer to Section 7.5 for more information.

Symbol	Type	Pin No.	Description
PHYAD0/ LED0	LI/O	9	**PHY Address [0]** **Link LED:** Active when linked.
PHYAD1/ LED1	LI/O	10	**PHY Address [1]** **Full Duplex LED:** Active when in Full Duplex operation.
PHYAD2/ LED2	LI/O	12	**PHY Address [2]** **Link 10/ACT LED:** Active when linked in 10Base-T mode, and blinking when transmitting or receiving data.
PHYAD3/ LED3	LI/O	13	**PHY Address [3]** **Link 100/ACT LED:** Active when linked in 100Base-TX and blinking when transmitting or receiving data.
PHYAD4/ LED4	LI/O	15	**PHY Address [4]** **Collision LED:** Active when collisions occur.

5.7 Reset and other pins

Symbol	Type	Pin No.	Description
RESETB	I	42	**RESETB:** Set low to reset the chip. For a complete reset function, this pin must be asserted low for at least 10ms.
PWFBOUT	O	32	**Power Feedback Output:** Be sure to connect a 22uF tantalum capacitor for frequency compensation and a 0.1uF capacitor for noise de-coupling. Then connect this pin through a ferrite bead to PWFBIN(pin8). The connection method is figured in section 7.11.
PWFBIN	I	8	**Power Feedback Input:** see the description of PWFBOUT.
NC		27	**Not connection**

5.8 Power and Ground pins

Symbol	Type	Pin No.	Description
AVDD33	P	36	**3.3V Analog power input:** 3.3V power supply for analog circuit; should be well decoupled.
AGND	P	29,35	**Analog Ground:** Should be connected to a larger GND plane
DVDD33	P	14,48	**3.3V Digital Power input:** 3.3V power supply for digital circuit.
DGND	P	11,17,45	**Digital Ground:** Should be connected to a larger GND plane.

6. Register Descriptions

This section will describe definitions and usage for each of the registers available in the RTL8201CL.

6.1 Register 0 Basic Mode Control Register

Address	Name	Description/Usage	Default/Attribute
0:<15>	Reset	This bit sets the status and control registers of the PHY in a default state. This bit is self-clearing. 1 = software reset 0 = normal operation	0, RW
0:<14>	Loopback	This bit enables loopback of transmit data nibbles TXD<3:0> to the receive data path. 1 = enable loopback 0 = normal operation	0, RW
0:<13>	Spd_Set	This bit sets the network speed. 1 = 100Mbps 0 = 10Mbps After completing auto negotiation, this bit will reflect the duplex status.(1: Full duplex, 0: Half duplex) *When 100Base-FX mode is enabled, this bit=1 and is read only.*	1, RW
0:<12>	Auto Negotiation Enable	This bit enables/disables the Nway auto-negotiation function. 1 = enable auto-negotiation; bits 0:<13> and 0:<8> will be ignored. 0 = disable auto-negotiation; bits 0:<13> and 0:<8> will determine the link speed and the data transfer mode, respectively. *When 100Base-FX mode is enabled, this bit=0 and is read only*.	1, RW
0:<11>	Power Down	This bit turns down the power of the PHY chip including internal crystal oscillator circuit. The MDC, MDIO is still alive for accessing the MAC. 1 = power down 0 = normal operation	0, RW
0:<10>	Reserved		
0:<9>	Restart Auto Negotiation	This bits allows the Nway auto-negotiation function to be reset. 1 = re-start auto-negotiation 0 = normal operation	0, RW
0:<8>	Duplex Mode	This bit sets the duplex mode if auto negotiation is disabled (bit 0:<12>=0) 1 = full duplex 0 = half duplex After completing auto negotiation, this bit will reflect the duplex status.(1: Full duplex, 0: Half duplex)	1, RW
0:<7:0>	Reserved		

6.2 Register 1 Basic Mode Status Register

Address	Name	Description/Usage	Default/Attribute
1:<15>	100Base-T4	1 = enable 100Base-T4 support 0 = suppress 100Base-T4 support	0, RO
1:<14>	100Base_TX_FD	1 = enable 100Base-TX full duplex support 0 = suppress 100Base-TX full duplex support	1, RO
1:<13>	100BASE_TX_HD	1 = enable 100Base-TX half duplex support 0 = suppress 100Base-TX half duplex support	1, RO
1:<12>	10Base_T_FD	1 = enable 10Base-T full duplex support 0 = suppress 10Base-T full duplex support	1, RO
1:<11>	10_Base_T_HD	1 = enable 10Base-T half duplex support 0 = suppress 10Base-T half duplex support	1, RO
1:<10:7>	Reserved		
1:<6>	MF Preamble Suppression	The RTL8201CL will accept management frames with preamble suppressed. The RTL8201CL accepts management frames without preamble. A Minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE802.3u specifications	1, RO
1:<5>	Auto Negotiation Complete	1 = auto-negotiation process completed 0 = auto-negotiation process not completed	0, RO
1:<4>	Remote Fault	1 = remote fault condition detected (cleared on read) 0 = no remote fault condition detected When in 100Base-FX mode, this bit means an in-band signal Far-End-Fault is detected. Refer to Section 7.11.	0, RO
1:<3>	Auto Negotiation	1 = Link had not been experienced fail state 0 = Link had been experienced fail state	1, RO
1:<2>	Link Status	1 = valid link established 0 = no valid link established	0, RO
1:<1>	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	0, RO
1:<0>	Extended Capability	1 = extended register capability 0 = basic register capability only	1, RO

6.3. Register 2 PHY Identifier Register 1

Address	Name	Description/Usage	Default/Attribute
2:<15;0>	PHYID1	PHY identifier ID for software recognize RTL8201CL	0000, RO

6.4. Register 3 PHY Identifier Register 2

Address	Name	Description/Usage	Default/Attribute
3:<15;0>	PHYID2	PHY identifier ID for software recognize RTL8201	8201, RO

6.5. Register 4 Auto-negotiation Advertisement Register(ANAR)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during Auto-negotiation.

Address	Name	Description/Usage	Default/Attribute
4:<15>	NP	Next Page bit. 0 = transmitting the primary capability data page 1 = transmitting the protocol specific data page	0, RO
4:<14>	ACK	1 = acknowledge reception of link partner capability data word 0 = do not acknowledge reception	0, RO
4:<13>	RF	1 = advertise remote fault detection capability 0 = do not advertise remote fault detection capability	0, RW
4:<12>	Reserved		
4:<11>	TFC	1 = TX flow control is supported by local node 0 = TX flow control is NOT supported by local node	0, RW
4:<10>	Pause	1 = RX flow control is supported by local node 0 = RX flow control is NOT supported by local node	0, RW
4:<9>	T4	1 = 100Base-T4 is supported by local node 0 = 100Base-T4 not supported by local node	0, RO
4:<8>	TXFD	1 = 100Base-TX full duplex is supported by local node 0 = 100Base-TX full duplex not supported by local node	1, RW
4:<7>	TX	1 = 100Base-TX is supported by local node 0 = 100Base-TX not supported by local node	1, RW
4:<6>	10FD	1 = 10Base-T full duplex supported by local node 0 = 10Base-T full duplex not supported by local node	1, RW
4:<5>	10	1 = 10Base-T is supported by local node 0 = 10Base-T not supported by local node	1, RW
4:<4:0>	Selector	Binary encoded selector supported by this node. Currently only CSMA/CD <00001> is specified. No other protocols are supported.	<00001>, RW

6.6 Register 5 Auto-Negotiation Link Partner Ability Register(ANLPAR)

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. The content changes after the successful Auto-negotiation if Next-pages are supported.

Address	Name	Description/Usage	Default/Attribute
5:<15>	NP	Next Page bit. 0 = transmitting the primary capability data page 1 = transmitting the protocol specific data page	0, RO
5:<14>	ACK	1 = link partner acknowledges reception of local node's capability data word 0 = no acknowledgement	0, RO
5:<13>	RF	1 = link partner is indicating a remote fault 0 = link partner does not indicate a remote fault	0, RO
5:<12>	Reserved		
5:<11>	TFC	1 = TX flow control is supported by Link partner 0 = TX flow control is NOT supported by Link partner	0, RO
5:<10>	Pause	1 = RX flow control is supported by Link partner 0 = RX flow control is NOT supported by Link partner	0, RO
5:<9>	T4	1 = 100Base-T4 is supported by link partner 0 = 100Base-T4 not supported by link partner	0, RO

5:<8>	TXFD	1 = 100Base-TX full duplex is supported by link partner 0 = 100Base-TX full duplex not supported by link partner	0, RO
5:<7>	100BASE-TX	1 = 100Base-TX is supported by link partner 0 = 100Base-TX not supported by link partner This bit will also be set after the link in 100Base is established by parallel detection.	1, RO
5:<6>	10FD	1 = 10Base-T full duplex is supported by link partner 0 = 10Base-T full duplex not supported by link partner	0, RO
5:<5>	10Base-T	1 = 10Base-T is supported by link partner 0 = 10Base-T not supported by link partner This bit will also be set after the link in 10Base is established by parallel detection.	0, RO
5:<4:0>	Selector	Link Partner's binary encoded node selector Currently only CSMA/CD <00001> is specified	<00000>, RO

6.7 Register 6 Auto-negotiation Expansion Register(ANER)

This register contains additional status for NWay auto-negotiation.

Address	Name	Description/Usage	Default/Attribute
6:<15:5>	Reserved	This bit is always set to 0.	
6:<4>	MLF	Status indicating if a multiple link fault has occurred. 1 = fault occurred 0 = no fault occurred	0, RO
6:<3>	LP_NP_ABLE	Status indicating if the link partner supports Next Page negotiation. 1 = supported 0 = not supported	0, RO
6:<2>	NP_ABLE	This bit indicates if the local node is able to send additional Next Pages.	0, RO
6:<1>	PAGE_RX	This bit is set when a new Link Code Word Page has been received. It is automatically cleared when the auto-negotiation link partner's ability register (register 5) is read by management.	0, RO
6:<0>	LP_NW_ABLE	1 = link partner supports Nway auto-negotiation.	0, RO

6.8 Register 16 Nway Setup Register(NSR)

Address	Name	Description/Usage	Default/Attribute
16:<15:12>	Reserved		
16:<11>	ENNWLE	1 = LED4 Pin indicates linkpulse	0, RW
16:<10>	Testfun	1 = Auto-neg speeds up internal timer	0, RW
16:<9>	NWLPBK	1 = set Nway to loopback mode.	0, RW
16:<8;3>	Reserved		
16:<2>	FLAGABD	1 = Auto-neg experienced ability detect state	0, RO
16:<1>	FLAGPDF	1 = Auto-neg experienced parallel detection fault state	0, RO
16:<0>	FLAGLSC	1 = Auto-neg experienced link status check state	0, RO

6.9 Register 17 Loopback, Bypass, Receiver Error Mask Register(LBREMR)

Address	Name	Description/Usage	Default/Attribute
17:<15>	RPTR	Set to 1 to put the RTL8201CL into repeater mode	0, RW
17:<14>	BP_4B5B	Assertion of this bit allows bypassing of the 4B/5B & 5B/4B encoder.	0, RW
17:<13>	BP_SCR	Assertion of this bit allows bypassing of the scrambler/descrambler.	0, RW
17:<12>	LDPS	Set to 1 to enable Link Down Power Saving mode	0, RW
17:<11>	AnalogOFF	Set to 1 to power down analog function of transmitter and receiver.	0, RW
17:<10>	Reserve	Reserve	
17:<9>	LB	Set to 1 to enablePCS Loopback	0, RW
17:<8>	F_Link_10B	Used to logic force good link in 10Mbps for diagnostic purposes. (Assert 0 to active)	1, RW
17:<7>	F_Link_100B	Used to logic force good link in 100Mbps for diagnostic purposes. (Assert 1 to active)	1, RW
17:<6>	JBEN	Set to 1 to enable Jabber Function in 10BT	0, RW
17:<5>	CODE_err	Assertion of this bit causes a code error detection to be reported.	0, RW
17:<4>	PME_err	Assertion of this bit causes a pre-mature end error detection to be reported.	0, RW
17:<3>	LINK_err	Assertion of this bit causes a link error detection to be reported.	0, RW
17:<2>	PKT_err	Assertion of this bit causes a detection of packet errors due to 722 ms time-out to be reported.	0, RW
17:<1>	FXMODE	This bit indicates status whether Fiber Mode is Enabled	0, R
17:<0>	RMIIMODE	This bit indicates status whether RMII mode is Enabled	0, R

6.10 Register 18 RX_ER Counter(REC)

Address	Name	Description/Usage	Default/Attribute
18:<15:0>	RXERCNT	This 16-bit counter increments by 1 for each valid packet received.	H'[0000], RW

6.11 Register 19 SNR Display Register

Address	Name	Description/Usage	Default/Attribute
19:<15:4>	Reserved	Please do not alternate this field with Realtek's approval. (Test Mode Purpose for Realtek Only)	
19:<3:0>	SNR	This 4-bit shows SNR value	[000], RW

6.12 Register 25 Test Register

Address	Name	Description/Usage	Default/ Attribute
25<15:12>	Test	Reserved for internal testing	R/W
25:<11:7>	PHYAD[4:0]	Reflects the PHY address defined by external PHY address configuration pins	RO
25<6:2>	Test	Reserved for internal testing	RO
25<1>	LINK10	1: Link established in 10Base OK 0: No link established in 10Base	RO
25<0>	LINK100	1: Link established in 100Base OK 0: No link established in 100Base	RO

7. Functional Description

The RTL8201CL Phyceiver is a physical layer device that integrates 10Base-T and 100Base-TX functions and some extra power manage features into a 48 pin single chip which is used in 10/100 Fast Ethernet applications. This device supports the following functions:

- MII interface with MDC/MDIO SMI management interface to communicate with MAC
- IEEE 802.3u clause 28 Auto-Negotiation ability
- Flow control ability support to cooperate with MAC
- Speed, duplex, auto-negotiation ability configurable by hard wire or MDC/MDIO.
- Flexible LED configuration.
- 7-wire SNI(Serial Network Interface) support, works only on 10Mbps mode.
- Power Down mode support
- 4B/5B transform
- Scrambling/De-scrambling
- NRZ to NRZI, NRZI to MLT3
- Manchester Encode and Decode for 10 BaseT operation
- Clock and Data recovery
- Adaptive Equalization
- Far End Fault Indication (FEFI) in fiber mode

7.1 MII and Management Interface

7.1.1 Data Transition

To set the RTL8201CL for MII mode operation, pull MII/SNIB pin high and properly set the ANE, SPEED, and DUPLEX pins.

The MII (Media Independent Interface) is an 18-signal interface which is described in IEEE 802.3u supplying a standard interface between PHY and MAC layer. This interface operates in two frequencies – 25Mhz and 2.5Mhz to support 100Mbps/10Mbps bandwidth for both transmit and receive functions. While transmitting packets, the MAC will first assert the TXEN signal and change byte data into 4 bits nibble and pass to the PHY by TXD[0..3]. PHY will sample TXD[0..3] synchronously with TXC — the transmit clock signal supplied by PHY – during the interval TXEN is asserted. While receiving a packet, the PHY will assert the RXEN signal, pass the received nibble data RXD[0..3] clocked by RXC, which is recovered from the received data. CRS and COL signals are used for collision detection and handling.

In 100Base-TX mode, when decoded signal in 5B is not IDLE, the CRS signal will assert and when 5B is recognized as IDLE it will be de-asserted. In 10Base-T mode, CRS will assert when the 10M preamble been confirmed and will be de-asserted when the IDLE pattern been confirmed.

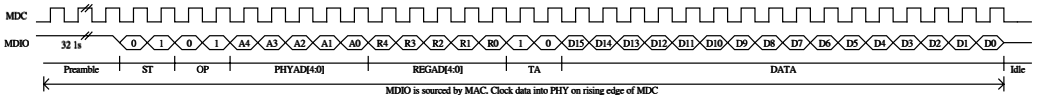
The RXDV signal will be asserted when decoded 5B are /J/K/and will be de-asserted if the 5B are /T/R/or IDLE in 100Mbps mode. In 10Mbps mode, the RXDV signal is the same as the CRS signal.

The RXER (Receive Error) signal will be asserted if any 5B decode errors occur such as invalid J/K, T/R, invalid symbol, this pin will go high for one or more clock period to indicate to the reconciliation sublayer that an error was detected somewhere in the frame.

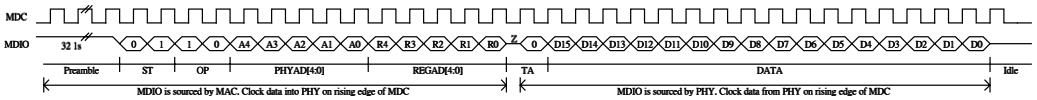
The RTL8201CL does not use the TXER signal and will not affect the transmit function.

7.1.2 Serial Management

The MAC layer device can use the MDC/MDIO management interface to control a maximum of 31 RTL8201CL devices, configured with different PHY addresses (00001b to 11111b). During a hardware reset, the logic levels of pins 9,10,12,13,15 are latched into the RTL8201CL to be set as the PHY address for serial management interface communication. Setting the PHY address to 00000b will put the RTL8201CL into power down mode. The read and write frame structure for the management interface follows.



Write Cycle



Read Cycle

Preamble	32 contiguous logic '1's sent by the MAC on MDIO along with 32 corresponding cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 01 pattern.
OP	Operation code. Read = 10. Write = 01.
PHYAD	PHY Address. Up to 31 PHYs can be connected to one MAC. This 5 bit field selects which PHY the frame is directed to.
REGAD	Register Address. This is a 5 bit field that selects which one of the 32 registers of the PHY this operation refers to.
TA	Turnaround. This is a two bit time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY shall remain in a high-impedance state for the first bit time of the turnaround. The PHY shall drive a zero bit during the second bit time of the turnaround of a read transaction.
DATA	Data. These are the 16 bits of Data.
IDLE	Idle Condition, not actually part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logic one.

7.2 Auto-negotiation and Parallel Detection

The RTL8201CL supports IEEE 802.3u clause 28 Auto-negotiation operation which can cooperate with other transceivers supporting auto-negotiation. By this mechanism, the RTL8201CL can auto detect the link partner's ability and determine the highest speed/duplex configuration and transmit/receive in this configuration. If the link partner does not support Auto-negotiation, then the RTL8201CL will enable half duplex mode and enter parallel detection. The RTL8201CL will default to transmit FLP and wait for the link partner to respond. If the RTL8201CL receives FPL, then the auto-negotiation process will go on. If it receives NLP, then the RTL8201CL will change to 10Mbps and half duplex mode. If it receives a 100Mbps IDLE pattern, it will change to 100Mbps and half duplex mode.

To enable the auto-negotiation mode operation on the RTL8201CL, just pull the ANE pin high. And the SPEED pin and DUPLEX pin will set the ability content of auto-negotiation register. The auto-negotiation mode can be externally disabled by pulling the ANE pin low. In this case, the SPEED pin and DUXPLEX pin will change the media configuration of the RTL8201CL.

Below is a list for all configurations of the ANE/SPEED/DUPLEX pins and their operation in Fiber or UTP mode.

Select Medium type and interface mode to MAC

FX (pin 24)	**MII/SNIB** (pin 44)	**Operation mode**
L	H	UTP mode and MII interface
L	L	UTP mode and SNI interface
H	X	Fiber mode and MII interface

UTP mode and MII interface

ANE (Pin 37)	**SPEED** (Pin 39)	**DUPLEX** (Pin 38)	**Operation**
H	L	L	Auto-negotiation enable, the ability field does not support 100Mbps and full duplex mode operation
H	L	H	Auto-negotiation enable, the ability field does not support 100Mbps operation
H	H	L	Auto-negotiation enable, the ability field does not support full duplex mode operation
H	H	H	Default setup, auto-negotiation enable, the RTL8201CL will support 10BaseT /100BaseTX, half/full duplex mode operation
L	L	L	Auto-negotiation disable, force the RTL8201CL into 10BaseT and half duplex mode
L	L	H	Auto-negotiation disable, force the RTL8201CL into 10BaseT and full duplex mode
L	H	L	Auto-negotiation disable, force the RTL8201CL into 100BaseTX and half duplex mode
L	H	H	Auto-negotiation disable, force the RTL8201CL into 100BaseTX and full duplex mode

UTP mode and SNI interface

SNI interface to MAC. It only works in 10Base-T when the SNI interface is enabled.

ANE (Pin 37)	**SPEED** (Pin 39)	**DUPLEX** (Pin 38)	**Operation**
X	X	L	The duplex pin is pulled low to support the 10Base-T half duplex function.10Base-T half duplex is the specified default mode in the SNI interface.
X	X	H	The RTL8201CL also supports full duplex in SNI mode. The duplex pin is pulled high to support 10Base-T full duplex function.

Fiber mode and MII interface
The RTL8201CL only supports 100Base-FX when Fiber mode is enabled. Ignore ANE and Speed hardwire configuration.

ANE (Pin 37)	SPEED (Pin 39)	DUPLEX (Pin 38)	Operation
X	X	H	The duplex pin is pulled high to support 100Base-FX full duplex function.
X	X	L	The duplex pin is pulled low to support 100Base-FX half duplex function.

7.3 Flow control support

The RTL8201CL supports flow control indications. The MAC can program the MII register to indicate to the PHY that flow control is supported. When MAC supports the Flow Control mechanism, setting bit 10 of the ANAR register by MDC/MDIO SMI interface, then the RTL8201CL will add the ability to its N-Way ability. If the Link partner also supports Flow Control, then the RTL8201CL can recognize the Link partner's N-Way ability by examining bit 10 of ANLPAR (register 5).

7.4 Hardware Configuration and Auto-negotiation

This section describes methods to configure the RTL8201CL and set the auto-negotiation mode. This list will show the various pins and their setting to provide the desired result.

1) **Isolate pin**: Set high to isolate the RTL8201CL from the MAC. This will also isolate the MDC/MDIO management interface. In this mode, power consumption is minimum. Please refer to the section covering Isolation mode and Power Down mode.

2) **RPTR pin**: Pull high to set the RTL8201CL into repeater mode. This pin is pulled low by default. Please refer to the section covering Repeater mode operation.

3) **LDPS pin**: Pull high to set the RTL8201CL into LDPS mode. This pin is pulled low by default. Please refer to the section covering Power Down mode and Link Down Power Saving.

4) **MII/SNIB**: Pull high to set RTL8201CL into MII mode operation, which is the default mode for the RTL8201. This pin pulled low will set the RTL8201CL into SNI mode operation. When set to SNI mode, the RTL8201CL will work at 10Mbps. Please refer to the section covering Serial Network Interface for more detail information.

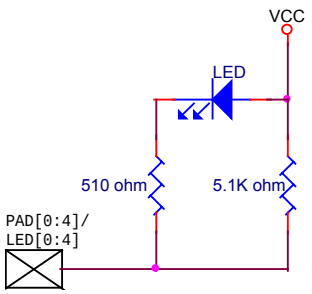
5) **ANE pin**: Pull high to enable Auto-negotiation (default). Pull low to disable auto-negotiation and activate the parallel detection mechanism. Please refer to the section covering Auto-negotiation and Parallel Detection

6) **Speed pin**: When ANE is pulled high, the ability to adjust speed is setup. When ANE is pulled low, pull this pin low to force 10Mbps operation and high to force 100Mbps operation. Please refer to the section on Auto-negotiation and Parallel Detection.

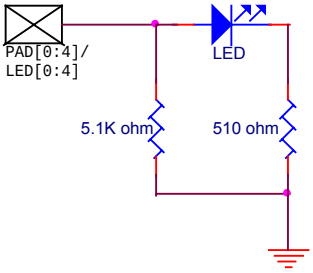
7) **DUPLEX pin**: When ANE is pulled high, the ability to adjust the DUPLEX pin will be setup. When ANE is pulled low, pull this pin low to force half duplex and high to force full duplex operation. Please refer to the section covering Auto-negotiation and Parallel Detection.

7.5 LED and PHY Address Configuration

In order to reduce the pin count on the RTL8201CL, the LED pins are duplexed with the PHY address pins. Because the PHYAD strap options share the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset. For example, as following left figure shows, if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. As right figure shows, if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. The PHY address configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (ex 5.1KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.



PHY address[:] = logic 1
LED indication = active low



PHY address[:] = logic 0
LED indication = active High

LED0	Link
LED1	Full Duplex
LED2	Link 10-Activity
LED3	Link 100-Activity
LED4	Collision

LED Definitions

7.6 Serial Network Interface

The RTL8201CL also supports the traditional 7-wire serial interface to cooperate with legacy MACs or embedded systems. To setup for this mode of operation, pull the MII/SNIB pin low and by doing so, the RTL8201CL will ignore the setup of the ANE and SPEED pins. In this mode, the RTL8201CL will set the default to work in 10Mbps and Half-duplex mode. But the RTL8201CL may also support full duplex mode operation if the DUPLEX pin has been pulled high.

This interface consists of 10Mbps transmit and receive clock generated by PHY, 10Mbps transmit and receive serial data, transmit enable, collision detect, and carry sense signals.

7.7 Power Down, Link Down, Power Saving, and Isolation Modes

The RTL8201CL supplies 4 kinds of Power Saving mode operation. This section will discuss all four, including how to implement each mode. The first three modes are configured through software, and the fourth through hardware.

1) **Analog off**: Setting bit 11 of register 17 to 1 will put the RTL8201CL into analog off state. In analog off state, the RTL8201CL will power down all analog functions such as transmit, receive, PLL, etc. However, the internal 25MHz crystal oscillator will not be powered down. The digital functions in this mode are still available which

allows reacquisition of analog functions.

2) **LDPS mode**: Setting bit 12 of register 17 to 1 or pulling the LDPS pin high will put the RTL8201CL into LDPS (Link Down Power Saving) mode. In LDPS mode, the RTL8201CL will detect the link status to decide whether or not to turn off the transmit function. If the link is off, FLP or 100Mbps IDLE/10Mbps NLP will not be transmitted. However, some signals similar to NLP will be transmitted. Once the receiver detects any leveled signals, it will stop the signal and transmit FLP or 100Mbps IDLE/10Mbps NLP again. This may save about 60%~80% power when the link is down.

3) **PWD mode**: Setting bit 11 of register 0 to 1 will put the RTL8201CL into power down mode. This is the maximum power saving mode while the RTL8201CL is still alive. In PWD mode, the RTL8201CL will turn off all analog/digital functions except the MDC/MDIO management interface. Therefore, if the RTL8201CL is put into PWD mode and the MAC wants to recall the PHY, it must create the MDC/MDIO timing by itself (this is done by software).

4) **Isolation mode**: This mode is different from the three previous software configured power saving modes. This mode is configured by hardware pin 43. Setting pin 43 high will isolate the RTL8201CL from the Media Access Controller (MAC) and the MDC/MDIO management interface. In this mode, power consumption is minimum.

7.8 Media Interface

7.8.1 100Base TX

1) **100Base-TX Transmit Function:** The 100Base-TX transmit function is performed as follows: First the transmit data in 4 bit nibbles (TXD[3:0]), clocked in 25MHz (TXC) will be transformed into 5B symbol code, called 4B/5B encoding. Scrambling, serializing and conversion to 125Mhz, and NRZ to NRZI will then take place. After this process, the NRZI signal will pass to the MLT3 encoder, then to the transmit line driver. The transmitter will first assert TXEN. Before transmitting the data pattern, it will send a /J/K/ symbol (Start-of-frame delimiter), the data symbol, and finally a /T/R/ symbol known as the End-Of-Frame delimiter. The 4B/5B and the scramble process can be bypassed by setting the PHY register. For better EMI performance consideration, the seed of the scrambler is related to the PHY address. Therefore in a hub/switch environment, every RTL8201CL will be set into a different PHY address so that they will use different scrambler seeds, which will spread the output of the MLT3 signals.

2) **100Base-TX Receive Function:** The 100Base-TX receive function is performed as follows: The received signal will first be compensated by the adaptive equalizer to make up for the signal loss due to cable attenuation and ISI. The Baseline Wander Corrector will monitor the process and dynamically apply corrections to the process of signal equalization. The PLL will then recover the timing information from the signals and form the receive clock. With this, the received signal may be sampled to form NRZI data. The next steps are the NRZI to NRZ process, unscrambling of the data, serial to parallel and 5B to 4B conversion and passing of the 4B nibble to the MII interface.

7.8.2 100Base-FX Fiber Mode Operation

RTL8201CL can be configured as 100Base-FX by hardware configuration. The priority of setting 100Base-FX is greater than Nway. Scrambler is not needed in 100Base-FX.

1) **100Base-FX Transmit Function:** The 100Base-FX transmit function is performed as follows: Di-bits of TXD are processed as 100Base-TX, except without scrambler before the NRZI stage. Instead of converting to MLT-3 signals, as in 100Base-TX, the serial data stream is driven out as NRZI PECL signals, which enter the fiber transceiver in differential-pairs form.

2) **In 100Base-FX Receive Function:** The 100Base-FX receive function is performed as follows: The signal is received through PECL receiver inputs from the fiber transceiver, and directly passed to the clock recovery circuit for data/clock recovery. The scrambler/de-scrambler is bypassed in 100Base-FX.

7.8.3 10Base Tx/Rx

1) **10Base Transmit Function:** The 10Base transmit function is performed as follows: The transmit 4 bits nibbles(TXD[0:3]) clocked in 2.5MHz(TXC) is first feed to parallel to serial converter, then put the 10Mbps NRZ signal to Manchester coding. The Manchester encoder converts the 10 Mbps NRZ data into a Manchester Encoded data stream for the TP transmitter and adds a start of idle pulse (SOI) at the end of the packet as specified in IEEE 802.3. Then, the encoded data stream is shaped by band- limited filter embedded in RTL8201CL and then transmitted to TP line.

2) **10Base Receive function:** The 10Base receive function is performed as follows: In 10Base receive mode, The Manchester decoder in RTL8201CL converts the Manchester encoded data stream from the TP receiver into NRZ data by decoding the data and stripping off the SOI pulse. Then, the serial NRZ data stream is converted to parallel 4 bit nibble signal(RXD[0:3]).

7.9 Repeater Mode Operation

Setting bit 15 of register 17 to 1 or pulling the RPTR pin high will set the RTL8201CL into repeater mode. In repeater mode, the RTL8201CL will assert CRS high only when receiving a packet. In NIC mode, the RTL8201CL will assert CRS high both in transmitting and receiving packets. If using the RTL8201CL in a repeater, please set the RTL8201CL to Repeater mode, and if using the RTL8201CL in a NIC or switch application, please set the default mode. NIC/Switch mode is the default setting and has the RPTR pin pulled low or bit 15 of register 17 is set to 0.

7.10 Reset, and Transmit Bias(RTSET)

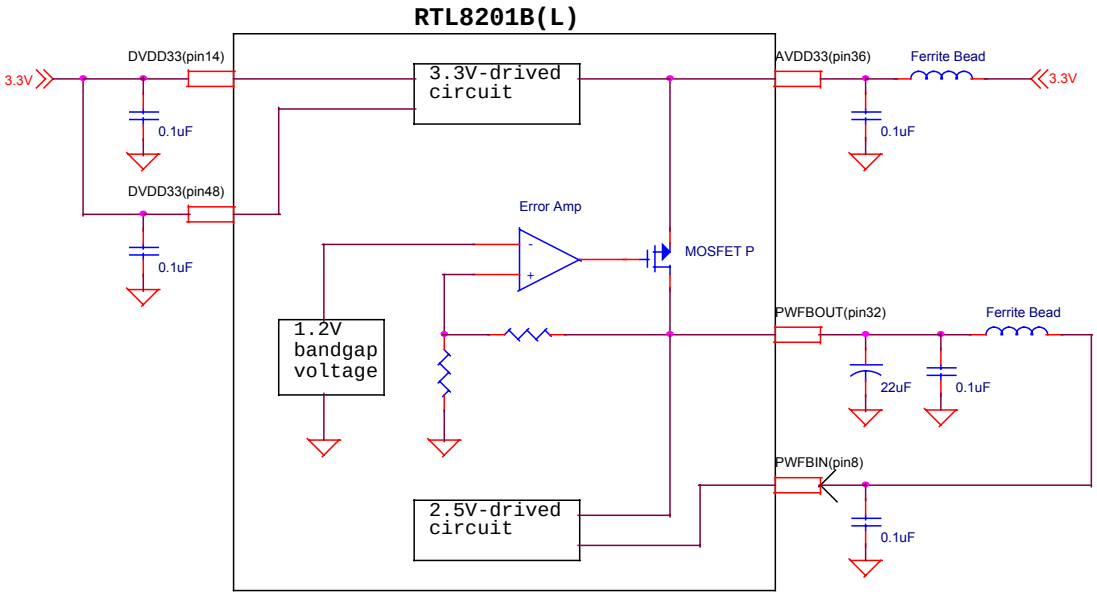
The RTL8201CL can be reset by pulling the RESETB pin low for about 10ms, then pulling the pin high. It can also be reset by setting bit 15 of register 0 to 1, and then setting it back to 0. Reset will clear the registers and re-initialize them, and the media interface will first disconnect and restart the auto-negotiation/parallel detection process.

The RTSET pin must be pulled low by a 5.9KΩ resister with 1% accuracy to establish an accurate transmit bias, this will affect the signal quality of the transmit waveform. Keep the circuitry away from other clock traces or transmit/receive paths to avoid signal interference.

7.11 3.3V power supply and voltage conversion circuit

RTL8201CL is fabricated in 0.18um process. The core circuit needs to be powered by 1.8V , however, the circuit of digital IO and DAC need 3.3V power supply. RTL8201CL has embedded a regulator to convert 3.3V to 1.8V. Just like many commercial voltage conversion devices, the 1.8V output pin (PWFBOUT) of this circuit requires the use of an output capacitor (22uF tantalum capacitor) as part of the device frequency compensation and another small capacitor (0.1uF) for high frequency noise de-coupling. And PWFBIN is fed with the 1.8V power externally from PWFBOUT through a ferrite bead as below figure shown. Strongly emphasize here, do not provide any extra external 1.8V produced by any other power device other than PWFBOUT and PWFBIN.

The analog and digital Ground planes should be as large and intact as possible. If the ground plane is large enough, the analog and digital grounds can be separated, which is a more ideal configuration. However, if the total ground plane is not sufficiently large, partition of the ground plane is not a good idea. In this case, all the ground pins can be connected together to a larger single and intact ground plane.



7.12 Far End Fault Indication (FEFI)

The MII Reg.1.4 (Remote Fault) is the FEFI bit when 100FX mode is enabled which indicates that FEFI has been detected. FEFI is an alternative in-band signaling method which is composed of 84 consecutive '1' followed by one '0'. From the point of view of the RTL8201CL, when this pattern is detected three times, Reg.1.4 is set, which means the transmit path (the Remote side's receive path) has a problem. On the other hand, the incoming signal failure in causing a link OK will force the RTL8201CL to start sending this pattern, which in turn causes the remote side to detect a Far-End-Fault. This means that the receive path has a problem from the point of view of the RTL8201CL. The FEFI mechanism is used only in 100Base-FX mode.

8. Electrical Characteristics

8.1 D.C. Characteristics

8.1.1. Absolute Maximum Ratings

Symbol	Conditions	Minimum	Typical	Maximum
Supply Voltage		3.0V	3.3V	3.6V
Storage Temp.		-55°C		125°C

8.1.2. Operating Conditions

Symbol	Conditions	Minimum	Typical	Maximum
Vcc 3.3V	3.3V Supply voltage	3.0V	3.3V	3.6V
TA	Operating Temperature	0°C		70°C

8.1.3. Power Dissipation

Test condition: VCC=3.3V

Symbol	Condition	Total Current Consumption
P_{LDPS}	Link down power saving mode	
P_{AnaOff}	Analog off mode	
P_{PWD}	Power down mode	
$P_{Isolate}$	Isolate mode	
P_{100F}	100Base full duplex	
P_{10F}	10Base full duplex	
P_{10TX}	10Base transmit	
P_{10RX}	10Base receive	
P_{10IDLE}	10Base idle	

8.1.4 Supply Voltage: Vcc

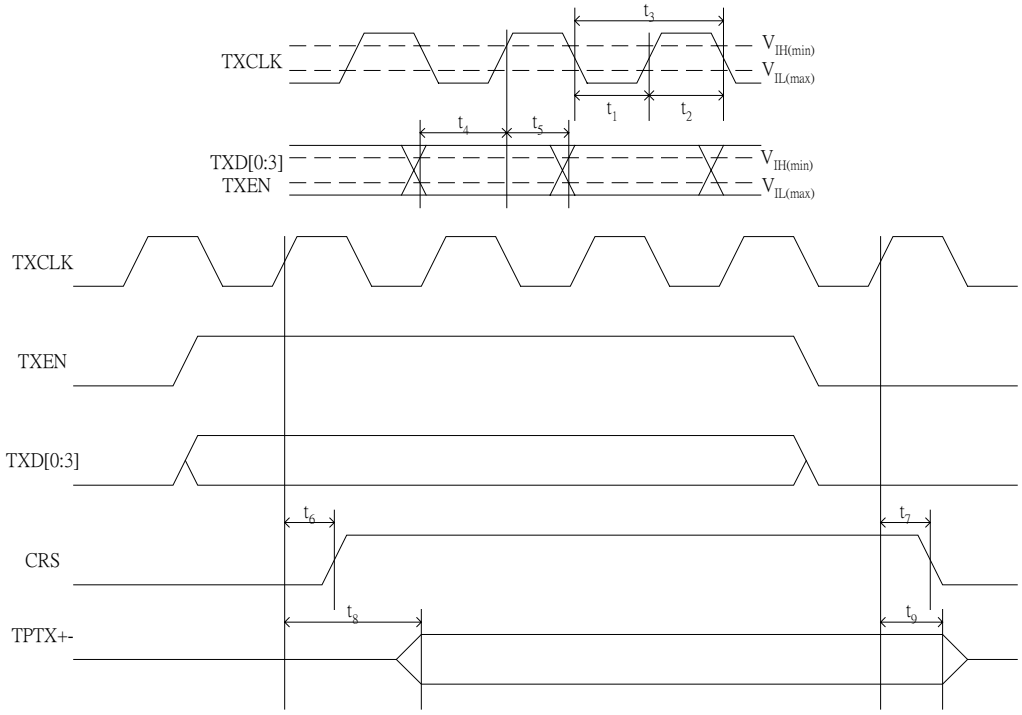
Symbol	Conditions		Minimum	Typical	Maximum
TTL V_{IH}	Input High Vol.		0.5*Vcc		Vcc+0.5V
TTL V_{IL}	Input Low Vol.		-0.5V		0.3*Vcc
TTL V_{OH}	Output High Vol.	IOH=-8mA	0.9*Vcc		Vcc
TTL V_{OL}	Output Low Vol.	IOL=8mA			0.1*Vcc
TTL I_{OZ}	Tri-state Leakage	Vout=Vcc or GND	-10uA		10uA
I_{IN}	Input Current	Vin=Vcc or GND	-1.0uA		1.0uA
Icc	Average Operating Supply Current	Iout=0mA			200mA
PECL V_{IH}	PECL Input High Vol		Vdd-1.16V		Vdd-0.88V
PECL V_{IL}	PECL Input Low Vol.		Vdd-1.81V		Vdd-1.47V
PECL V_{OH}	PECL Output High Vol.		Vdd-1.02V		
PECL V_{OL}	PECL Output Low Vol.				Vdd-1.62V

8.2 A.C. Characteristics

8.2.1 MII Timing of Transmission Cycle

Shown is an example transfer of a packet from MAC to PHY in MII interface.

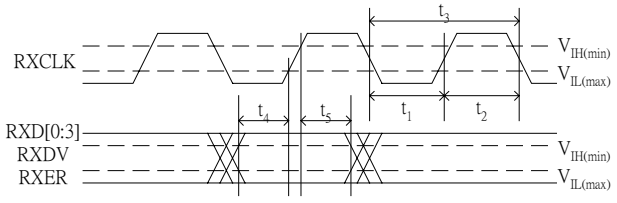
Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	TXCLK high pulse width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	TXCLK low pulse width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	TXCLK period	100Mbps		40		ns
		10Mbps		400		ns
t_4	TXEN, TXD[0:3] setup to TXCLK rising edge	100Mbps	10	24		ns
		10Mbps	5			ns
t_5	TXEN, TXD[0:3] hold after TXCLK rising edge	100Mbps		10	25	ns
		10Mbps	5			ns
t_6	TXEN sampled to CRS high	100Mbps			40	ns
		10Mbps			400	ns
t_7	TXEN sampled to CRS low	100Mbps			160	ns
		10Mbps			2000	ns
t_8	Transmit latency	100Mbps	60	70	140	ns
		10Mbps			400	ns
t_9	Sampled TXEN inactive to end of frame	100Mbps		100	170	ns
		10Mbps				ns

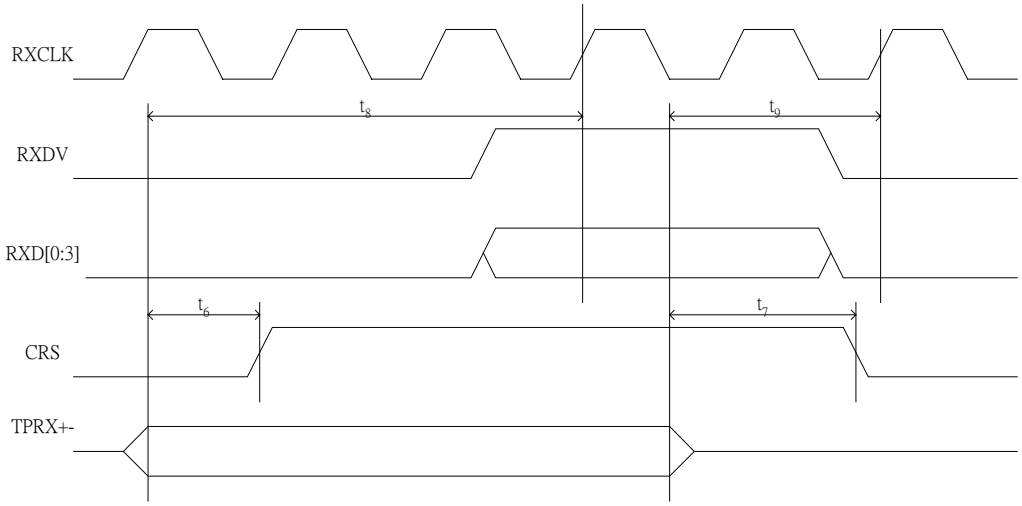


8.2.2 MII Timing of Reception Cycle

Shown is an example of transfer of a packet from PHY to MAC in MII interface

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	RXCLK high pulse width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	RXCLK low pulse width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	RXCLK period	100Mbps		40		ns
		10Mbps		400		ns
t_4	RXER, RXDV, RXD[0:3] setup to RXCLK rising edge	100Mbps	10			ns
		10Mbps	6			ns
t_5	RXER, RXDV, RXD[0:3] hold after RXCLK rising edge	100Mbps	10			ns
		10Mbps	6			ns
t_6	Receive frame to CRS high	100Mbps			130	ns
		10Mbps			600	ns
t_7	End of receive frame to CRS low	100Mbps			240	ns
		10Mbps			600	ns
t_8	Receive frame to sampled edge of RXDV	100Mbps			150	ns
		10Mbps			3200	ns
t_9	End of receive frame to sampled edge of RXDV	100Mbps			120	ns
		10Mbps			800	ns

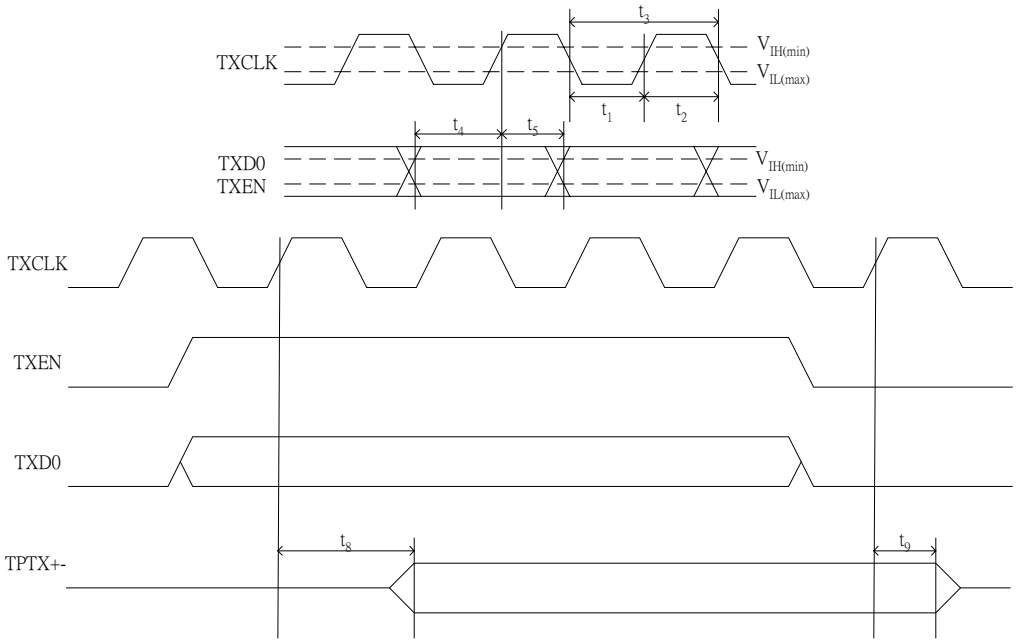




8.2.3 SNI Timing of Transmission Cycle

Shown is an example transfer of a packet from MAC to PHY in SNI interface. SNI mode only runs in 10Mbps.

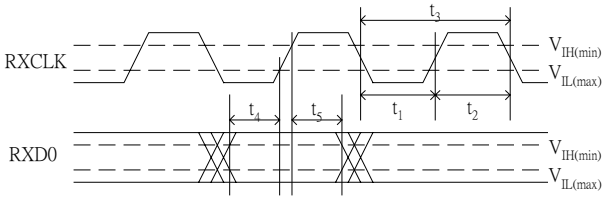
Symbol	Description	Minimum	Typical	Maximum	Unit
t_1	TXCLK high pulse width	36			ns
t_2	TXCLK low pulse width	36			ns
t_3	TXCLK period	80		120	ns
t_4	TXEN, TXD0 setup to TXCLK rising edge	20			ns
t_5	TXEN, TXD0 hold after TXCLK rising edge	10			ns
t_8	Transmit latency			50	ns

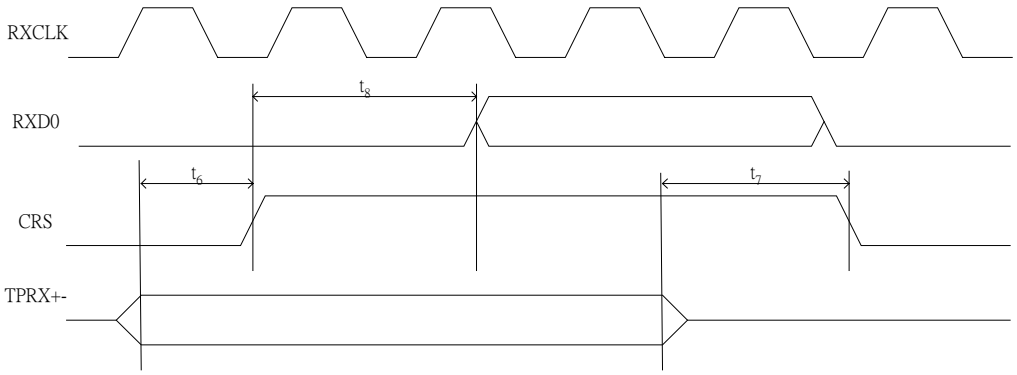


8.2.4 SNI Timing of Reception Cycle

Shown is an example of transfer of a packet from PHY to MAC in SNI interface. SNI mode only runs in 10Mbps.

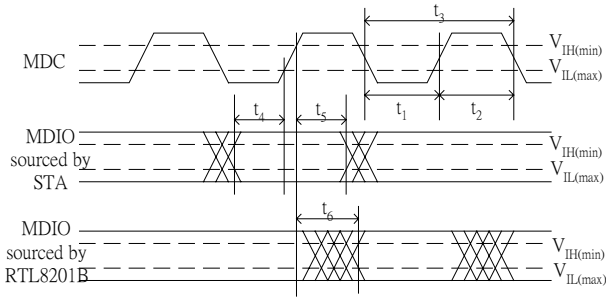
Symbol	Description	Minimum	Typical	Maximum	Unit
t_1	RXCLK high pulse width	36			ns
t_2	RXCLK low pulse width	36			ns
t_3	RXCLK period	80		120	ns
t_4	RXD0 setup to RXCLK rising edge	40			ns
t_5	RXD0 hold after RXCLK rising edge	40			ns
t_6	Receive frame to CRS high			50	ns
t_7	End of receive frame to CRS low			160	ns
t_8	Decoder acquisition time		600	1800	ns





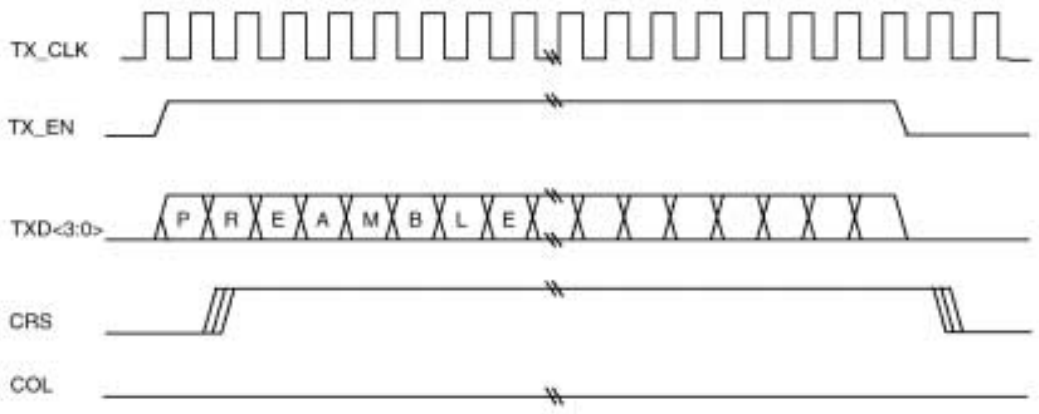
8.2.5 MDC/MDIO timing

Symbol	Description	Minimum	Typical	Maximum	Unit
t_1	MDC high pulse width	160			ns
t_2	MDC low pulse width	160			ns
t_3	MDC period	400			ns
t_4	MDIO setup to MDC rising edge	10			ns
t_5	MDIO hold time from MDC rising edge	10			ns
t_6	MDIO valid from MDC rising edge	0		300	ns



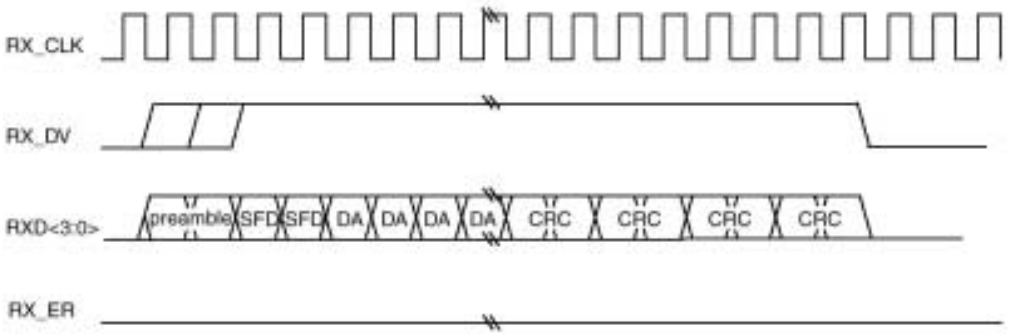
8.2.6 Transmission Without Collision

Shown is an example transfer of a packet from MAC to PHY.



8.2.7 Reception Without Error

Shown is an example of transfer of a packet from PHY to MAC



8.3 Crystal and Transformer Specifications

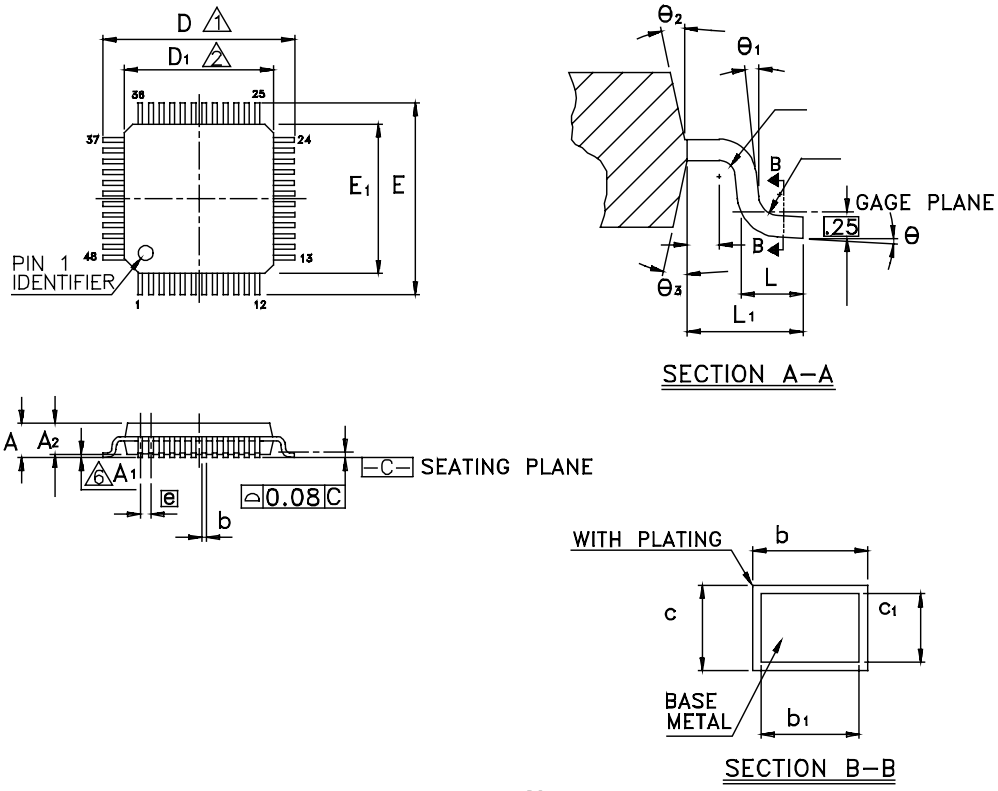
8.3.1 Crystal Specifications

Item	Parameter	Range
1	Nominal Frequency	25.000 MHz
2	Oscillation Mode	Base wave
3	Frequency Tolerance at 25℃	±50 ppm
4	Temperature Characteristics	±50 ppm
5	Operating Temperature Range	-10℃ ~ +70℃
6	Equivalent Series Resistance	30 ohm Max.
7	Drive Level	0.1 mV
8	Load Capacitance	20 pF
9	Shunt Capacitance	7 pF Max.
10	Insulation Resistance	Mega ohm Min./DC 100V
11	Test Impedance Meter	Saunders 250A
12	Aging Rate A Year	±0.0003%

8.3.2 Transformer Specifications

Parameter	Transmit End	Receive End
Turn ratio	1:1 CT	1:1
Inductance (min.)	350 uH @ 8mA	350 uH @ 8mA
Leakage inductance	0.05-0.15 uH	0.05-0.15 uH
Capacitance (max)	15 pF	15 pF
DC resistance (max)	0.4 ohm	0.4 ohm

9. Mechanical Dimensions



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.067	-	-	1.70
A1	0.000	0.004	0.008	0.00	**0.1**	0.20
A2	0.051	0.055	0.059	1.30	**1.40**	1.50
b	0.006	0.009	0.011	0.15	**0.22**	0.29
b1	0.006	0.008	0.010	0.15	**0.20**	0.25
c	0.004	-	0.008	0.09	-	0.20
c1	0.004	-	0.006	0.09	-	0.16
D	0.354 BSC			9.00 BSC		
D1	0.276 BSC			7.00 BSC		
E	0.354 BSC			9.00 BSC		
E1	0.276 BSC			7.00 BSC		
e	0.020 BSC			0.50 BSC		
L	0.016	0.024	0.031	0.40	0.60	0.80
L1	0.039 REF			1.00 REF		
θ	0°	3.5°	9°	0°	3.5°	9°
θ1	0°	-	-	0°	-	-
θ2	12° TYP			12° TYP		
θ3	12° TYP			12° TYP		

Notes:

1. To be determined at seating plane -c-
2. Dimensions D1 and E1 do not include mold protrusion.
   D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion.
   Dambar can not be located on the lower radius of the
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating plane t lowest point of the package body.
7. Controlling dimension: millimeter.
8. Reference document: JEDEC MS-026, BBC

TITLE: 48LD LQFP (7x7x1.4mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	SS048 - P1
		DATE	Sept. 25.2000
REALTEK SEMI-CONDUCTOR CORP.			

10. Revision History

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