M37281MAH–XXXSP,M37281MFH–XXXSP,M37281MKH–XXXSP, M37281EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER
with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

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1. DESCRIPTION

The M37281MAH–XXXSP, M37281MFH–XXXSP and M37281MKH-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. They have a OSD function and a data slicer function, so it is useful for a channel selection system for TV with a closed caption decoder.

The feautures of the M37281EKSP is similar to those of the M37281MKH-XXXSP except that the chip has a built-in PROM which can be written electrically. The difference between M37281MAH–XXXSP, M37281MKH-XXXSP and M37281MFH-XXXSP are the ROM size and RAM size. Accordingly, the following descriptions will be for the M37281MKH-XXXSP.

2. FEATURES

- Number of basic instructions 71
- Memory size
  - ROM .... 40K bytes (M37281MAH-XXXSP)
    60K bytes (M37281MFH-XXXSP)
    80K bytes (M37281MKH-XXXSP, M37281EKSP)
  - RAM .... 1088 bytes (M37281MAH-XXXSP, M37281MFH-XXXSP)
    1536 bytes (M37281MKH-XXXSP, M37281EKSP)
  - (*ROM correction memory included)
- Minimum instruction execution time
  .... 0.5 µs (at 8 MHz oscillation frequency)
- Power source voltage .... 5 V ± 10 %
- Subroutine nesting .... 128 levels (Max.)
- Interrupts .... 19 types, 16 vectors
- 8-bit timers 6
- Programmable I/O ports (Ports P0, P1, P2, $P3_0$, $P3_1$) 26
- Input ports (Ports $P4_0$–$P4_6$, $P6_3$, $P6_4$, $P7_0$–$P7_2$) 12
- Output ports (Ports $P5_2$–$P5_5$) 4
- LED drive ports 2
- Serial I/O .... 8-bit × 1 channel
- Multi-master I^2C-BUS interface .... 1 (2 systems)
- A-D converter (8-bit resolution) .... 8 channels
- PWM output circuit .... 8-bit × 8
- Power dissipation
  - In high-speed mode .... 165 mW
    (at V_{CC} = 5.5V, 8 MHz oscillation frequency, OSD on, and Data slicer on)
  - In low-speed mode .... 0.33 mW
    (at V_{CC} = 5.5V, 32 kHz oscillation frequency)
- ROM correction function .... 2 vectors
- Closed caption data slicer
- OSD function
  - Display characters .... 32 characters × 16 lines + RAM font (1 character)
  - Kinds of characters .... 510 kinds (CC/OSD mode) + 62 kinds (CDOSD mode) + 1 kind (RAM font)
  - (Coloring unit) (a character) (a dot) (a dot)
  - Triple layer function ....
    2 layers selected from CC/CDOSD/OSD mode + RAM font layer
  - Character display area .... CC/CDOSD mode: 16 × 26 dots
    OSD mode/RAM font: 16 × 20 dots
  - Kinds of character sizes .... CC mode/RAM font: 4 kinds
    OSD/CDOSD mode: 14 kinds
  - Kinds of character colors ....
    64 colors (4 adjustment levels for each R, G, B)
  - Coloring unit .... dot, character, character background, raster
  - Blanking output OUT1, OUT2
  - Display position
    Horizontal: 256 levels Vertical :1024 levels
    (RAM font can be set independently)
  - Attribute ....
    CC mode: smooth italic, underline, flash, automatic solid space
    OSD mode: border, shadow
  - Window/Blank function

3. APPLICATION

TV with a closed caption decoder

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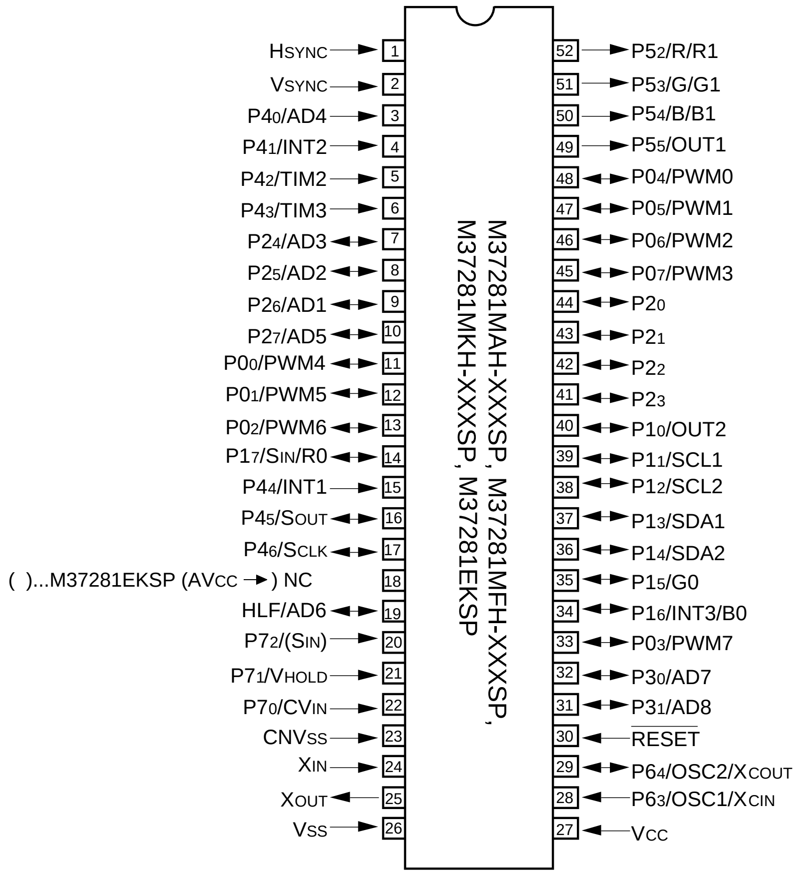
4. PIN CONFIGURATION



Outline 52P4B

Note: Only 18th pin is NC pin of M37281MAH/MFH/MKH-XXXSP. This pin is AVcc pin of M37281EKSP. But NC pin of M37281MAH/MFH/MKH-XXXSP is not connect in the IC. You can apply to Vcc.

Fig. 4.1 Pin Configuration (Top View)

5. FUNCTIONAL BLOCK DIAGRAM

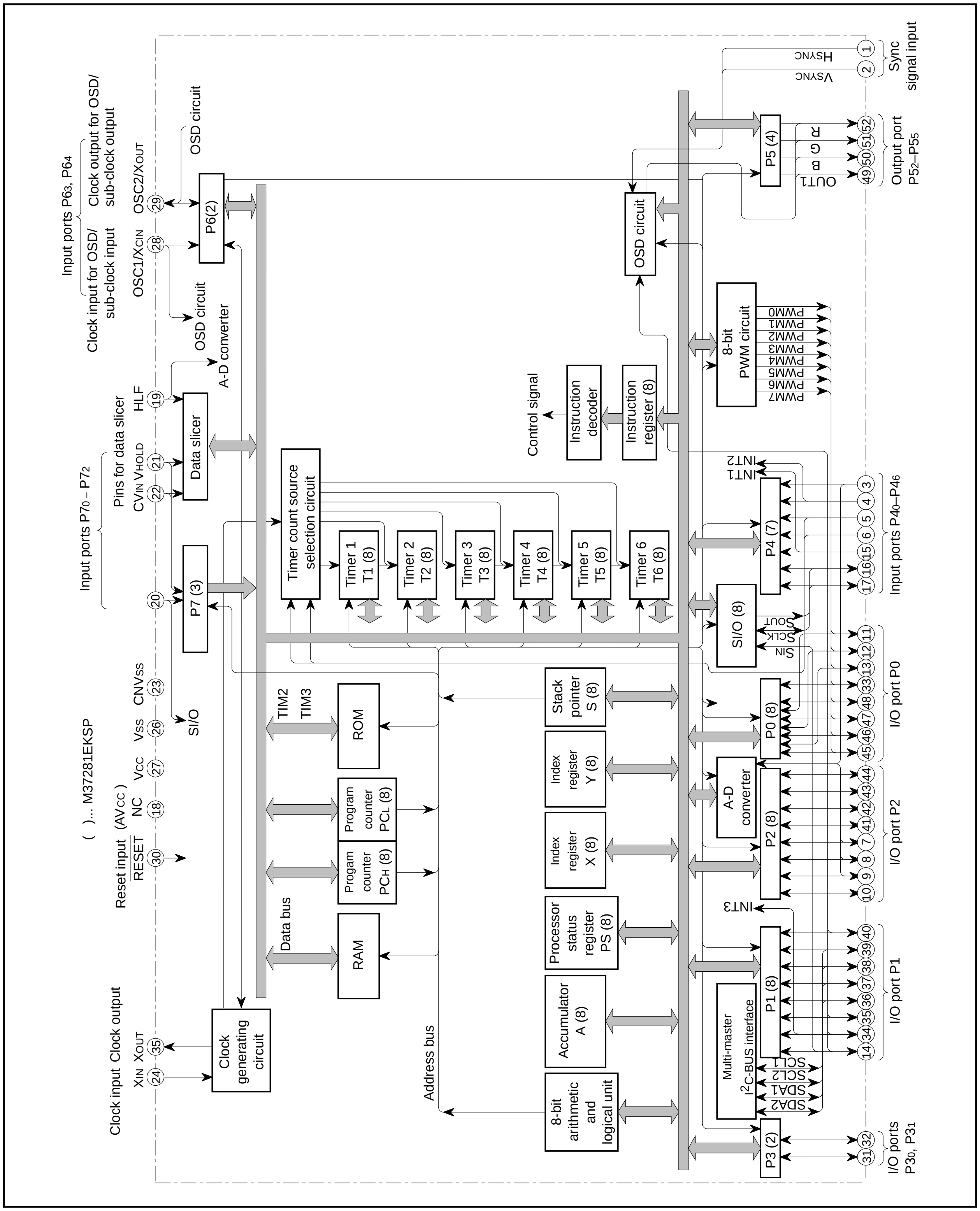


Fig. 5.1 Functional Block Diagram of M37281

6. PERFORMANCE OVERVIEW

Table 6.1 Performance Overview

Parameter			Functions
Number of basic instructions			71
Instruction execution time			0.5 µs (the minimum instruction execution time, at 8 MHz oscillation frequency)
Clock frequency			8 MHz (maximum)
Memory size	ROM	M37281MAH-XXXSP	40K bytes
		M37281MFH-XXXSP	60K bytes
		M37281MKH-XXXSP, M37281EKSP	80K bytes
	RAM	M37281MAH-XXXSP,M37281MFH-XXXSP	1088 bytes (ROM correction memory included)
		M37281MKH-XXXSP, M37281EKSP	1536 bytes (ROM correction memory included)
	OSD ROM (character font)		20400 bytes
	OSD ROM (color dot font)		9672 bytes
	OSD RAM (SPRITE)		120 bytes
	OSD RAM (character)		1536 bytes
Input/Output ports	P00–P02, P04–P07	I/O	7-bit × 1 (N-channel open-drain output structure, can be used as PWM output pins)
	P03	I/O	1-bit × 1 (CMOS input/output structure, can be used as PWM output pin)
	P10, P15–P17	I/O	4-bit × 1 (CMOS input/output structure, can be used as OSD output pin, INT input pin, serial input pin)
	P11–P14	I/O	4-bit × 1 (N-channel open-drain output structure, can be used as multi-master I²C-BUS interface)
	P2	I/O	8-bit × 1 (CMOS input/output structure, can be used as A-D input pins)
	P30, P31	I/O	2-bit × 1 (CMOS input/output structure, can be used as A-D input pins)
	P40–P44	Input	5-bit × 1 (can be used as A-D input pins, INT input pins, external clock input pins for timer)
	P45, P46	Input	2-bit × 1 (N-channel open-drain output structure when serial I/O is used, can be used as serial I/O pins)
	P52–P55	Output	4-bit × 1 (CMOS output structure, can be used as OSD output pins)
	P63	Input	1-bit × 1 (can be used as sub-clock input pin, OSD clock input pin)
	P64	Input	1-bit × 1 (CMOS output structure when LC is oscillating, can be used as sub-clock output pin, OSD clock output pin)
	P70–P72	Input	3-bit × 1 (can be used as data slicer input/output, serial input pin)
Serial I/O			8-bit × 1
Multi-master I²C-BUS interface			1 (2 systems)
A-D converter			8 channels (8-bit resolution)
PWM output circuit			8-bit × 8
Timers			8-bit timer × 6
ROM correction function			2 vectors
Subroutine nesting			128 levels (maximum)
Interrupt			<19 types> INT external interrupt × 3, Internal timer interrupt × 6, Serial I/O interrupt × 1, OSD interrupt × 1, Multi-master I²C-BUS interface interrupt × 1, Data slicer interrupt × 1, f(XIN)/4096 interrupt × 1, SPRITE OSD interrupt × 1, VSYNC interrupt × 1, A-D conversion interrupt × 1, BRK instruction interrupt × 1, Reset × 1
Clock generating circuit			2 built-in circuits (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Data slicer			Built in

Table 6.2 Performance Overview

Parameter				Functions
OSD function		Number of display characters		32 characters ✕ 16 lines
		Dot structure		CC mode: 16 ✕ 26 dots (Character display area: 16 ✕ 20 dots) OSD mode: 16 ✕ 20 dots EXOSD mode: 16 ✕ 26 dots SPRITE display: 16 ✕ 20 dots
		Kinds of characters		CC/OSD mode: 510 kinds CDOSD mode: 62 kinds SPRITE display: 1 kind
		Kinds of character sizes		CC mode: 4 kinds OSD/CDOSD mode: 14 kinds SPRITE display: 8 kinds
		Character font coloring		<CC mode> 1 screen : 8 kinds (per character unit) <OSD mode> 1 screen : 15 kinds (per character unit) <CDOSD mode> 1 screen : 8 kinds (per dot unit) <SPRITE display> 1 screen : 8 kinds (per dot unit)
		Display position		Horizontal: 256 levels, Vertical: 1024 levels <SPRITE display> Horizontal: 2048 levels, Vertical: 1024 levels
Power source voltage				5V ± 10%
Power dissipation	In high-speed mode	OSD ON (Analog output)	Data slicer ON	275 mW typ. (at oscillation frequency $f(X_{IN})$ = 8 MHz, f_{OSC} = 27 MHz)
		OSD ON (Digital output)	Data slicer OFF	165 mW typ. (at oscillation frequency $f(X_{IN})$ = 8 MHz, f_{OSC} = 27 MHz)
		OSD OFF	Data slicer OFF	82.5 mW typ. (at oscillation frequency $f(X_{IN})$ = 8 MHz)
	In low-speed mode	OSD OFF	Data slicer OFF	0.33 mW typ. (at oscillation frequency $f(X_{CIN})$ = 32 kHz, $f(X_{IN})$ = stop)
	In stop mode			0.055 mW (maximum)
Operating temperature range				–10 °C to 70 °C
Device structure				CMOS silicon gate process
Package				52-pin shrink plastic molded DIP

7. PIN DESCRIPTION

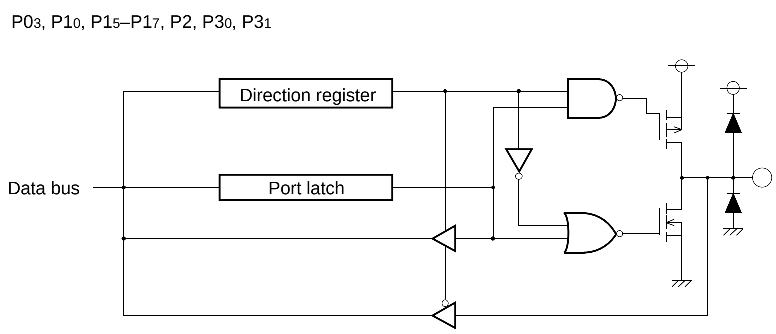
Table 7.1 Pin Description

Pin	Name	Input/ Output	Functions
VCC, (AVCC,) VSS	Power source		Apply voltage of 5 V ± 10 % (typical) to VCC (AVCC) , and 0 V to VSS. ( ) ...M37281EKSP
CNVSS	CNVSS		Connected to VSS.
RESET (overlined)	Reset input	Input	To enter the reset state, the reset input pin must be kept at a LOW for 2 µs or more (under normal VCC conditions). If more time is needed for the quartz-crystal oscillator to stabilize, this LOW condition should be maintained for the required time.
XIN	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins XIN and XOUT. If an external clock is used, the clock source should be connected to the XIN pin and the XOUT pin should be left open.
XOUT	Clock output	Output	
P0$_0$/ PWM4– P0$_2$/PWM6, P0$_3$/PWM7, P0$_4$/ PWM0– P0$_7$/PWM3	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure of P0$_3$ is CMOS output, that of P0$_0$–P0$_2$ and P0$_4$–P0$_7$ are N-channel open-drain output (See note.)
	8-bit PWM output	Output	Pins P0$_0$–P0$_3$ and P0$_4$–P0$_7$ are also used as 8-bit PWM output pins PWM4–PWM7 and PWM0–PWM3 respectively. The output structure of PWM0–PWM6 is N-channel open-drain output. And the output structure of PWM7 is CMOS output.
P1$_0$/OUT2, P1$_1$/SCL1, P1$_2$/SCL2, P1$_3$/SDA1, P1$_4$/SDA2, P1$_5$/G0, P1$_6$/INT3/ B0, P1$_7$/SIN/R0	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure of P1$_0$ and P1$_5$–P1$_7$ is CMOS output, that of P1$_1$–P1$_4$ is N-channel open-drain output (See note.)
	OSD output	Output	Pin P1$_0$, P1$_5$–P1$_7$ are also used as OSD output pins OUT2, G0, B0, R0, respectively. The output structure is CMOS output.
	Multi-master I^{2}C-BUS interface	I/O	Pin P1$_1$–P1$_4$ are used as SCL1, SCL2, SDA1 and SDA2 respectively, when multi-master I^{2}C-BUS interface is used. The output structure is N-channel open-drain output.
	External interrupt input	Input	Pin P1$_6$ is also used as INT extemal interrupt input pin INT3.
	Serial I/O data input	Input	Pin P1$_7$ is also used as serial I/O data input pin SIN.
P2$_0$–P2$_3$ P2$_4$/AD3– P2$_6$/AD1, P2$_7$/AD5	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output (See note.)
	Analog input	Input	Pins P2$_4$–P2$_6$, P2$_7$ are also used as analog input pins AD3–AD1, AD5 respectively.
P3$_0$/AD7, P3$_1$/AD8	I/O port P3	I/O	Ports P3$_0$ and P3$_1$ are 2-bit I/O ports and have basically the same functions as port P0. The output structure is CMOS output (See note.)
	Analog input	Input	Pins P3$_0$, P3$_1$ are also used as analog input pins AD7, AD8 respectively.
P4$_0$/AD4, P4$_1$/INT2, P4$_2$/TIM2, P4$_3$/TIM3, P4$_4$/INT1, P4$_5$/SOUT, P4$_6$/SCLK	Input port P4	Input	Ports P4$_0$–P4$_6$ are a 7-bit input port.
	Analog input	Input	Pin P4$_0$ is also used as analog input pin AD4.
	External interrupt input	Input	Pins P4$_1$, P4$_4$ are also used as INT external interrupt input pins INT2, INT1.
	External clock input for timer	Input	Pins P4$_2$ and P4$_3$ are also used as INT external clock input pins TIM2, TIM3 for timer respectively.
	Serial I/O data output	Output	Pin P4$_5$ is used as serial I/O data output pin SOUT. The output structure is N-channel open-drain output.
	Serial I/O synchronous clock input/output	I/O	Pin P4$_6$ is used as serial I/O synchronous clock input/output pin SCLK. The output structure is N-channel open-drain output.

Table 7.2 Pin Description (continued)

Pin	Name	Input/ Output	Functions
$P5_2$/R/R1, $P5_3$/G/G1, $P5_4$/B/B1, $P5_5$/OUT1	Output port P5	Output	Port P5 is a 4-bit output port. The output structure is CMOS output.
	OSD output	Output	Pins $P5_2$–$P5_5$ are also used as OSD output pins R/R1, G/G1, B/B1, OUT1 respectively. At R, G, B output, the output structure is analog output. At R1, G1, B1 and OUT1 output, the output structure is CMOS output.
$P6_3$/OSC1/ X_{CIN}, $P6_4$/OSC2/ X_{COUT}	Input port P6	Input	Ports $P6_3$ and $P6_4$ are 2-bit input port.
	Clock input for OSD	Input	Pin $P6_3$ is also used as OSD clock input pin OSC1.
	Clock output for OSD	Output	Pin $P6_4$ is also used as OSD clock output pin OSC2. The output structure is CMOS output.
	Sub-clock input	Input	Pin $P6_3$ is also used as sub-clock input pin X_{CIN}.
	Sub-clock output	Output	Pin $P6_4$ is also used as sub-clock output pin X_{COUT}. The output structure is CMOS output.
$P7_0$/CV_{IN}, $P7_1$/V_{HOLD}, $P7_2$/(S_{IN})	Input port P7	Input	Ports $P7_0$–$P7_2$ are 3-bit input port.
	Input for data slicer	Input	Pins $P7_0$, $P7_1$ are also used as data slicer input pins CV_{IN}, V_{HOLD} respectively. When using data slicer, input composite video signal through a capacitor. Connect a capacitor between V_{HOLD} and V_{SS}.
	Serial I/O data input	Input	Pins $P7_2$ is also used as serial I/O data input pin S_{IN}.
HLF/AD6	I/O for data slicer	I/O	When using data slicer, connect a filter using of a capacitor and a resistor between HLF and V_{SS}.
	Analog input	Input	This is an analog input pin AD6 .
H_{SYNC}	H_{SYNC} input	Input	This is a horizontal synchronous signal input for OSD.
V_{SYNC}	V_{SYNC} input	Input	This is a vertical synchronous signal input for OSD.

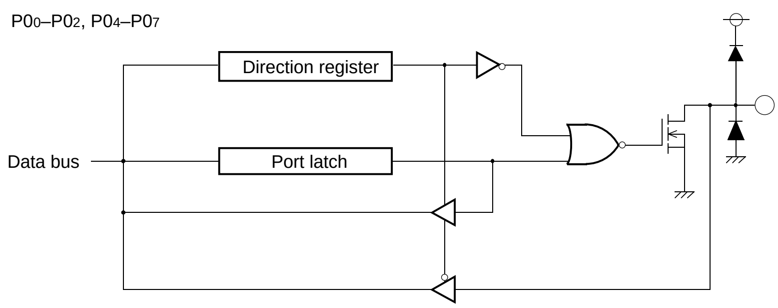
Note : Port Pi (i = 0 to 3) has the port Pi direction register (address $00C1_{16}$ of zero page) which can be used to program each bit as an input ("0") or an output ("1"). The pins programmed as "1" in the direction register are output pins. When pins are programmed as "0," they are input pins. When pins are programmed as output pins, the output data are written into the port latch and then output. When data is read from the output pins, the output pin level is not read but the data of the port latch is read. This allows a previously-output value to be read correctly even if the output "L" voltage has risen, for example, because a light emitting diode was directly driven. The input pins float, so the values of the pins can be read. When data is written into the input pin, it is written only into the port latch, while the pin remains in the floating state.



CMOS output

Ports $P0_3$, $P1_0$, $P1_5$–$P1_7$,
P2, $P3_0$, $P3_1$

Note : Each port is also used as follows :
$P0_0$: PWM7
$P1_0$: OUT2
$P1_5$: G0
$P1_6$: INT3/B0
$P1_7$: SIN/R0
$P2_4$–$P2_6$: AD3–AD1
$P2_7$: AD5
$P3_0$: AD7
$P3_1$: AD8

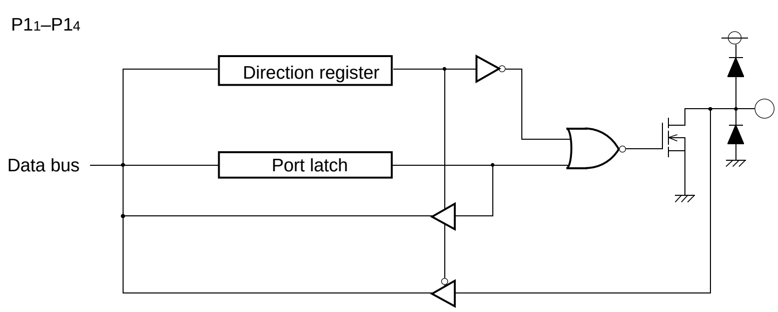


N-channel open-drain output

Ports $P0_0$–$P0_2$, $P0_4$–$P0_7$

Note1 : Each port is also used as follows :
$P0_0$–$P0_2$: PWM4–PWM6
$P0_4$–$P0_7$: PWM0–PWM3

2 : M37281EKSP, does not have the diode side with V_{CC}.



N-channel open-drain output

Port $P1_1$-$P1_4$

Note : Each port is also used as follows :
$P1_1$: SCL1
$P1_2$: SCL2
$P1_3$: SDA1
$P1_4$: SDA2

Fig. 7.1 I/O Pin Block Diagram (1)

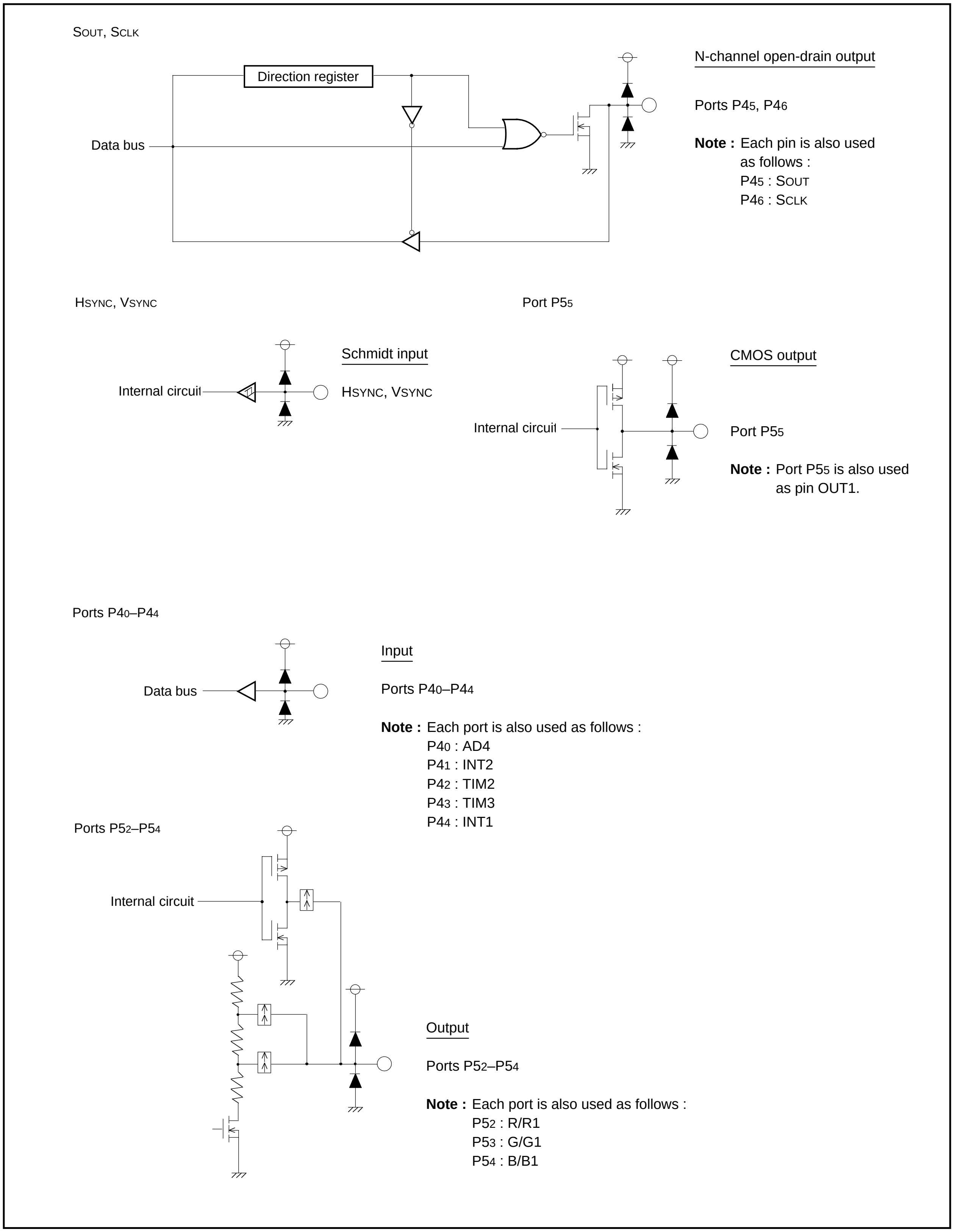


Fig. 7.2 I/O Pin Block Diagram (2)

8. FUNCTIONAL DESCRIPTION
8.1. CENTRAL PROCESSING UNIT (CPU)

This microcomputer uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the SERIES 740 <Software> User’s Manual for details on the instruction set.
Machine-resident 740 Family instructions are as follows:
The FST, SLW instruction cannot be used.
The MUL, DIV, WIT and STP instructions can be used.

8.1.1 CPU Mode Register

The CPU mode register contains the stack page selection bit and internal system clock selection bit. The CPU mode register is allocated at address $00FB_{16}$.

CPU Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
			1	1		0	0

CPU mode register (CM) [Address $00FB_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: Not available 1 0: Not available 1 1: Not available	0	R	W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R	W
3, 4	Fix these bits to “1.”		1	R	W
5	XCOUT drivability selection bit (CM5)	0: LOW drive 1: HIGH drive	1	R	W
6	Main Clock (XIN–XOUT) stop bit (CM6)	0: Oscillating 1: Stopped	0	R	W
7	Internal system clock selection bit (CM7)	0: XIN–XOUT selected (high-speed mode) 1: XCIN–XCOUT selected (low-speed mode)	0	R	W

Note: This bit is set to “1” after the reset release.

Fig. 8.1.1 CPU Mode Register

8.2 MEMORY

8.2.1 Special Function Register (SFR) Area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

8.2.2 RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

8.2.3 ROM

The M37281MAH-XXXSP has 40K-byte program area and M37281MFH-XXXSP has 60K-byte program area. The M37281MKH -XXXSP has 56K-byte program area and 24K-byte data-dedicated area. For the M37281EKSP, the two area (60K, 24K + 56K) can be swithed each other by setting the bank control register.

8.2.4 OSD RAM

RAM for display is used for specifying the character codes and colors to display.

8.2.5 OSD ROM

ROM for display is used for storing character data.

8.2.6 Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

8.2.7 Zero Page

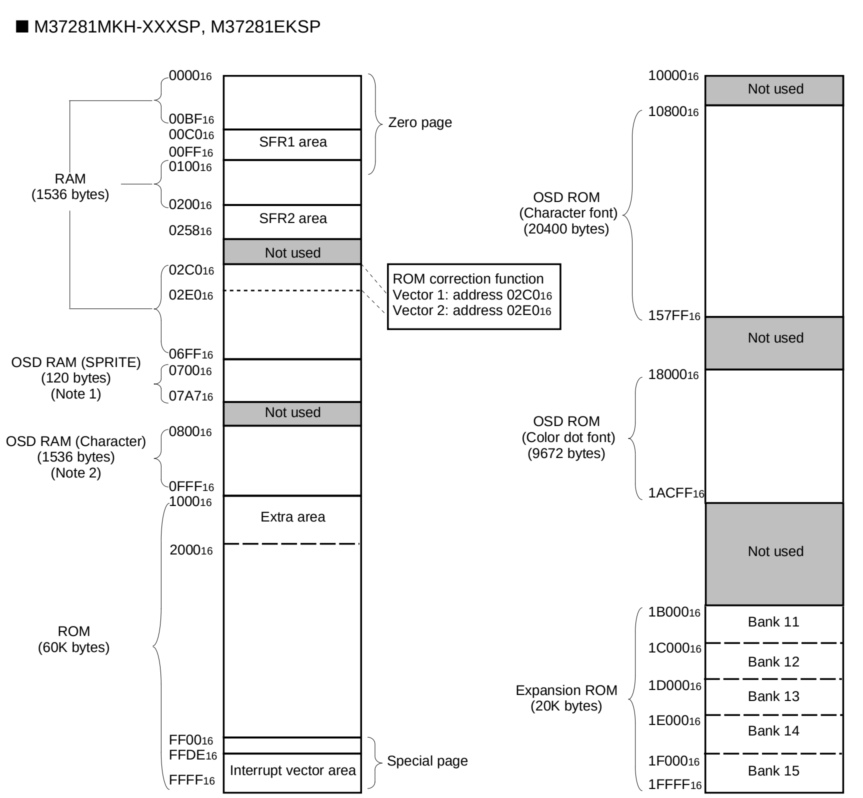
The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

8.2.8 Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

8.2.9 ROM Correction Vector

This is used as the program jump destination addresses for ROM correction.



Notes 1: Refer to Table 8.11.6 OSD RAM (SPRITE).
2: Tables 8.11.4 and 8.11.5 OSD RAM (Character).

Fig. 8.2.1 Memory Map (M37281MKH-XXXSP, M37281EKSP)

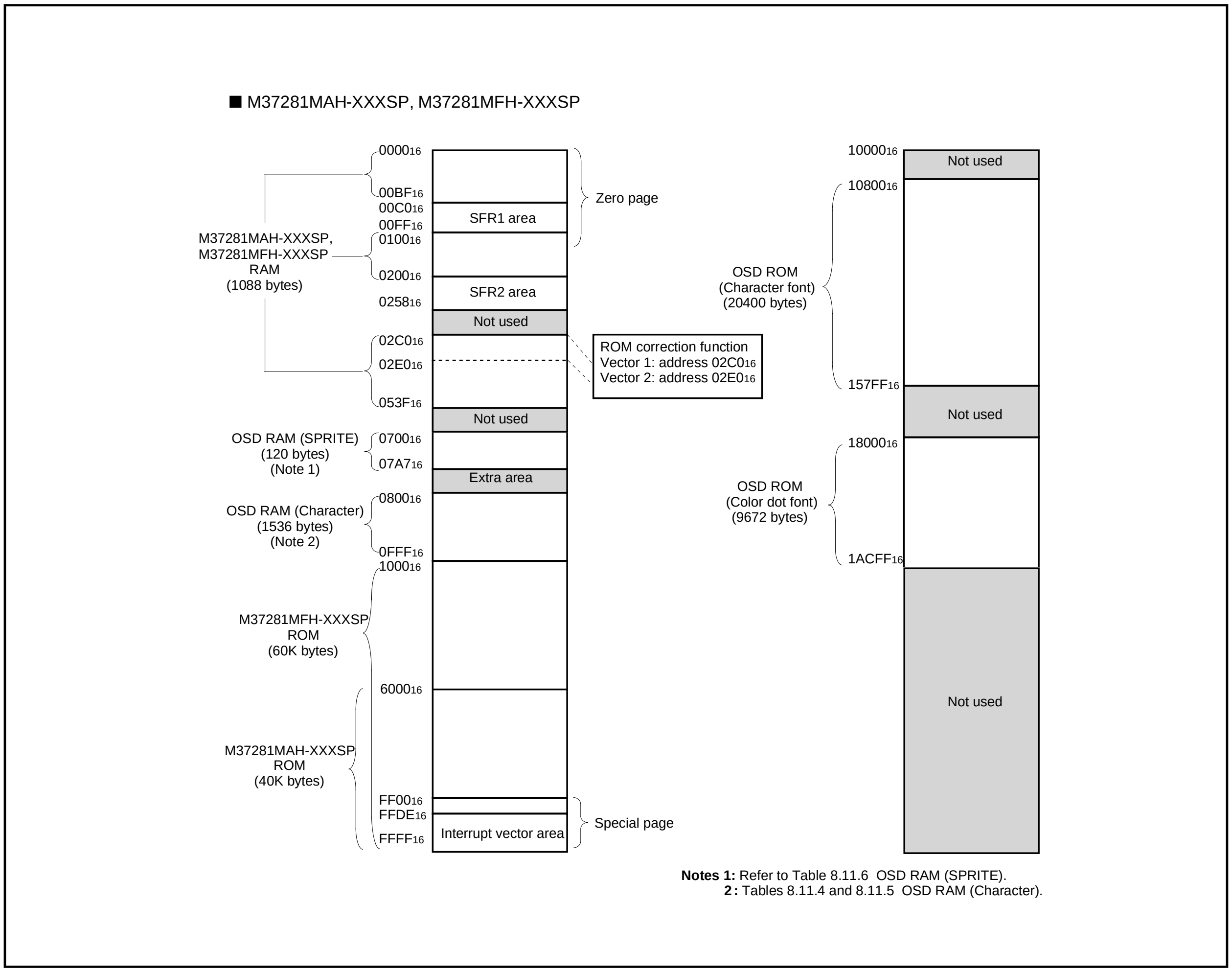


Fig. 8.2.2 Memory Map (M37281MAH-XXXSP,M37281MFH-XXXSP)

8.2.10 Expansion ROM (only M37281MKH-XXXSP/M37281EKSP)

The M37281MKH-XXXSP/M37281EKSP can use 5-bank (total 20K bytes) expansion ROM (4K bytes each bank) by setting the bank register.

The expansion ROM is assigned to address $1B000_{16}$ to $1FFFF_{16}$. The contents of each bank in the expansion ROM are read by setting the bank register and accessing addresses 1000_{16} to $1FFF_{16}$. As the expansion ROM is not programmable, use it as data-dedicated area. When using the expansion ROM area, the internal ROM at addresses 1000_{16} to $1FFF_{16}$ (extra area) is not also programmable.

Notes 1: When using the expansion ROM (BK7 = "1"), the ROM correction function do not operate for addresses 1000_{16} to $1FFF_{16}$.

2: When using the emulator MCU (M37281ERSS), as addresses 1000_{16} to $FFFF_{16}$ can be emulated by setting bit 7 of the bank control register to "0," the expansion ROM cannot be used. Addresses 2000_{16} to $FFFF_{16}$ can be emulated by setting it to "1." The data in specified area by the bank selection bits can be read by accessing addresses 1000_{16} to $1FFF_{16}$.

3: When using the emulator MCU, the expansion ROM and the extra area cannot be emulated by setting bit 7 of the bank control register to "1." Therefore, write the data to this area before using.

4: For the M37281MKH-XXXSP, fix bit 7 of the bank control register to "1." For M37281MAH-XXXSP and M37281MFH-XXXSP, fix the address $00ED_{16}$ to "00_{16}."

Bank Control Register

b7 b6 b5 b4 b3 b2 b1 b0

[ ][ ][0][0][ ][ ][ ][ ] Bank control register (BK) [Address $00ED_{16}$]

B	Name	Functions				After reset	R	W
0 to 3	Bank selection bits (BK0 to BK3)	Bank number is selected (bank 11 to 15)				0	R	W
4, 5	Fix these bits to "0."					0	R	W
6, 7	Bank control bits (BK6, BK7)	b7	b6	Bank ROM	Address 1000_{16} level access	0	R	W
		0	×	Not used	Read out from extra area (programmable)			
		1	0	Used	Read out the data from area specified by the bank selection bits			
		1	1	Used	Read out from extra area (data-dedicated)			

Fig. 8.2.3 Bank Control Register

■ SFR1 area (addresses $C0_{16}$ to DF_{16})

<Bit allocation>

- (blank box) : } Function bit
- (Name box) : } Function bit
- (shaded box) : No function bit
- 0 (shaded) : Fix to this bit to “0” (do not write to “1”)
- 1 (shaded) : Fix to this bit to “1” (do not write to “0”)

<State immediately after reset>

- 0 : “0” immediately after reset
- 1 : “1” immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	b7							b0	State immediately after reset (b7 … b0)
$C0_{16}$	Port P0 (P0)									?
$C1_{16}$	Port P0 direction register (D0)									00_{16}
$C2_{16}$	Port P1 (P1)									?
$C3_{16}$	Port P1 direction register (D1)									00_{16}
$C4_{16}$	Port P2 (P2)									?
$C5_{16}$	Port P2 direction register (D2)									00_{16}
$C6_{16}$	Port P3 (P3)									?
$C7_{16}$	Port P3 direction register (D3)	P6IM	T3CS							00_{16}
$C8_{16}$	Port P4 (P4)									?
$C9_{16}$	Port P4 direction register (D4)								0	00_{16}
CA_{16}	Port P5 (P5)									?
CB_{16}	OSD port control register (PF)	0	OUT2	OUT1	B	G	R	RGB 2BIT	0	00_{16}
CC_{16}	Port P6 (P6)									?
CD_{16}	Port P7 (P7)									0 0 0 0 0 ? ? ?
CE_{16}	OSD control register 1 (OC 1)	OC17	OC16	OC15	OC14	OC13	OC12	OC11	OC10	00_{16}
CF_{16}	Horizontal position register (HP)	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	00_{16}
$D0_{16}$	Block control register 1 (BC_1)		$BC_1$6	$BC_1$5	$BC_1$4	$BC_1$3	$BC_1$2	$BC_1$1	$BC_1$0	?
$D1_{16}$	Block control register 2 (BC_2)		$BC_2$6	$BC_2$5	$BC_2$4	$BC_2$3	$BC_2$2	$BC_2$1	$BC_2$0	?
$D2_{16}$	Block control register 3 (BC_3)		$BC_3$6	$BC_3$5	$BC_3$4	$BC_3$3	$BC_3$2	$BC_3$1	$BC_3$0	?
$D3_{16}$	Block control register 4 (BC_4)		$BC_4$6	$BC_4$5	$BC_4$4	$BC_4$3	$BC_4$2	$BC_4$1	$BC_4$0	?
$D4_{16}$	Block control register 5 (BC_5)		$BC_5$6	$BC_5$5	$BC_5$4	$BC_5$3	$BC_5$2	$BC_5$1	$BC_5$0	?
$D5_{16}$	Block control register 6 (BC_6)		$BC_6$6	$BC_6$5	$BC_6$4	$BC_6$3	$BC_6$2	$BC_6$1	$BC_6$0	?
$D6_{16}$	Block control register 7 (BC_7)		$BC_7$6	$BC_7$5	$BC_7$4	$BC_7$3	$BC_7$2	$BC_7$1	$BC_7$0	?
$D7_{16}$	Block control register 8 (BC_8)		$BC_8$6	$BC_8$5	$BC_8$4	$BC_8$3	$BC_8$2	$BC_8$1	$BC_8$0	?
$D8_{16}$	Block control register 9 (BC_9)		$BC_9$6	$BC_9$5	$BC_9$4	$BC_9$3	$BC_9$2	$BC_9$1	$BC_9$0	?
$D9_{16}$	Block control register 10 (BC_{10})		BC_{10}6	BC_{10}5	BC_{10}4	BC_{10}3	BC_{10}2	BC_{10}1	BC_{10}0	?
DA_{16}	Block control register 11 (BC_{11})		BC_{11}6	BC_{11}5	BC_{11}4	BC_{11}3	BC_{11}2	BC_{11}1	BC_{11}0	?
DB_{16}	Block control register 12 (BC_{12})		BC_{12}6	BC_{12}5	BC_{12}4	BC_{12}3	BC_{12}2	BC_{12}1	BC_{12}0	?
DC_{16}	Block control register 13 (BC_{13})		BC_{13}6	BC_{13}5	BC_{13}	BC_{13}3	BC_{13}2	BC_{13}1	BC_{13}0	?
DD_{16}	Block control register 14 (BC_{14})		BC_{14}6	BC_{14}5	BC_{14}4	BC_{14}3	BC_{14}2	BC_{14}1	BC_{14}0	?
DE_{16}	Block control register 15 (BC_{15})		BC_{15}6	BC_{15}5	BC_{15}4	BC_{15}3	BC_{15}2	BC_{15}1	BC_{15}0	?
DF_{16}	Block control register 16 (BC_{16})		BC_{16}6	BC_{16}5	BC_{16}4	BC_{16}3	BC_{16}2	BC_{16}1	BC_{16}0	?

Fig. 8.2.4 Memory Map of Special Function Register 1 (SFR1) (1)

■ SFR1 area (addresses $E0_{16}$ to FF_{16})

<Bit allocation>

- [ ] : } Function bit
- [Name] : } Function bit
- [shaded] : No function bit
- [0] (shaded) : Fix to this bit to “0” (do not write to “1”)
- [1] (shaded) : Fix to this bit to “1” (do not write to “0”)

<State immediately after reset>

- [0] : “0” immediately after reset
- [1] : “1” immediately after reset
- [?] : Indeterminate immediately after reset

Address	Register	b7	b6	b5	b4	b3	b2	b1	b0	State immediately after reset (b7 … b0)
$E0_{16}$	Data slicer control register 1 (DSC1)	0	0	0	0	0	DSC12	DSC11	DSC10	00_{16}
$E1_{16}$	Data slicer control register 2 (DSC2)		0	DSC25	DSC24	DSC23		0	DSC20	? 0 ? 0 ? ? 0 ?
$E2_{16}$	Caption data register 1 (CD1)	CDL17	CDL16	CDL15	CDL14	CDL13	CDL12	CDL11	CDL10	00_{16}
$E3_{16}$	Caption data register 2 (CD2)	CDH17	CDH16	CDH15	CDH14	CDH13	CDH12	CDH11	CDH10	00_{16}
$E4_{16}$	Caption data register 3 (CD3)	CDL27	CDL26	CDL25	CDL24	CDL23	CDL22	CDL21	CDL20	00_{16}
$E5_{16}$	Caption data register 4 (CD4)	CDH27	CDH26	CDH25	CDH24	CDH23	CDH22	CDH21	CDH20	00_{16}
$E6_{16}$	Caption Position register (CPS)	CPS7	CPS6	CPS5	CPS4	CPS3	CPS2	CPS1	CPS0	0 0 ? 0 0 0 0 0
$E7_{16}$	Data slicer test register 2	00_{16}								00_{16}
$E8_{16}$	Data slicer test register 1	00_{16}								00_{16}
$E9_{16}$	Sync signal counter register (HC)			HC5	HC4	HC3	HC2	HC1	HC0	0 0 ? ? ? ? ? ?
EA_{16}	Clock run-in detect register (CRD)	CRD7	CRD6	CRD5	CRD4	CRD3				00_{16}
EB_{16}	Data clock position register (DPS)	DPS7	DPS6	DPS5	DPS4	DPS3	0	0	1	09_{16}
EC_{16}										?
ED_{16}	Bank control register (BK)	BK7	BK6	0	0	BK3	BK2	BK1	BK0	00_{16}
EE_{16}	A-D conversion register (AD)									?
EF_{16}	A-D control register (ADCON)	0		0	ADVREF	ADSTR	ADIN2	ADIN1	ADIN0	0 ? 0 0 1 0 0 0
$F0_{16}$	Timer 1 (T1)									FF_{16}
$F1_{16}$	Timer 2 (T2)									07_{16}
$F2_{16}$	Timer 3 (T3)									FF_{16}
$F3_{16}$	Timer 4 (T4)									07_{16}
$F4_{16}$	Timer mode register 1 (TM1)	TM17	TM16	TM15	TM14	TM13	TM12	TM11	TM10	00_{16}
$F5_{16}$	Timer mode register 2 (TM2)	TM27	TM26	TM25	TM24	TM23	TM22	TM21	TM20	00_{16}
$F6_{16}$	I^2C data shift register (S0)	D7	D6	D5	D4	D3	D2	D1	D0	?
$F7_{16}$	I^2C address register (S0D)	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW	00_{16}
$F8_{16}$	I^2C status register (S1)	MST	TRX	BB	PIN	AL	AAS	AD0	LRB	0 0 0 1 0 0 0 ?
$F9_{16}$	I^2C control register (S1D)	BSEL1	BSEL0	10BIT SAD	ALS	ESO	BC2	BC1	BC0	00_{16}
FA_{16}	I^2C clock control register (S2)	ACK	ACK BIT	FAST MODE	CCR4	CCR3	CCR2	CCR1	CCR0	00_{16}
FB_{16}	CPU mode register (CM)	CM7	CM6	CM5	1	1	CM2	0	0	$3C_{16}$
FC_{16}	Interrupt request register 1 (IREQ1)		ADR	VSCR	OSDR	TM4R	TM3R	TM2R	TM1R	00_{16}
FD_{16}	Interrupt request register 2 (IREQ2)	0	TM56R	IICR	IN2R	CKR	SIOR	DSR	IN1R	00_{16}
FE_{16}	Interrupt control register 1 (ICON1)		ADE	VSCE	OSDE	TM4E	TM3E	TM2E	TM1E	00_{16}
FF_{16}	Interrupt control register 2 (ICON2)	TM56S	TM56E	IICE	IN2E	CKE	SIOE	DSE	IN1E	00_{16}

Fig. 8.2.5 Memory Map of Special Function Register 1 (SFR2) (2)

■ SFR2 area (addresses 200_{16} to $21F_{16}$)

<Bit allocation>

- ☐ : } Function bit
- [Name] : } Function bit
- ▒ : No function bit
- 0 : Fix to this bit to "0" (do not write to "1")
- 1 : Fix to this bit to "1" (do not write to "0")

<State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	b7	b6	b5	b4	b3	b2	b1	b0	State immediately after reset (b7–b0)
200_{16}	PWM0 register (PWM0)									?
201_{16}	PWM1 register (PWM1)									?
202_{16}	PWM2 register (PWM2)									?
203_{16}	PWM3 register (PWM3)									?
204_{16}	PWM4 register (PWM4)									?
205_{16}	PWM5 register (PWM5)									?
205_{16}	PWM6 register (PWM6)									?
207_{16}	PWM7 register (PWM7)									?
208_{16}										?
209_{16}										?
$20A_{16}$	PWM mode register 1 (PN)				PN4	PN3			PN0	00_{16}
$20B_{16}$	PWM mode register 2 (PW)	0	PW6	PW5	PW4	PW3	PW2	PW1	PW0	00_{16}
$20C_{16}$	ROM correction address 1 (high-order)									00_{16}
$20D_{16}$	ROM correction address 1 (low-order)									00_{16}
$20E_{16}$	ROM correction address 2 (high-order)									00_{16}
$20F_{16}$	ROM correction address 2 (low-order)									00_{16}
210_{16}	ROM correction enable register (RCR)					0	0	RCR1	RCR0	00_{16}
211_{16}	Test register	00_{16}								00_{16}
212_{16}	Interrupt input polarity register (IP)	AD/INT3 SEL	POL3		POL2	POL1				00_{16}
213_{16}	Serial I/O mode register (SM)		SM6	SM5	SM4	SM3	SM2	SM1	SM0	00_{16}
214_{16}	Serial I/O register (SIO)									?
215_{16}	OSD control register 2(OC2)	OC27	OC26	OC25	OC24	OC23	OC12	OC21	OC20	00_{16}
216_{16}	Clock control register (CS)		0	0	0	0	CS2	CS1	CS0	00_{16}
217_{16}	I/O polarity control register (PC)	PC7	PC6	PC5	PC4		PC2	PC1	PC0	80_{16}
218_{16}	Raster color register (RC)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	00_{16}
219_{16}	OSD control register 3(OC3)	OC37	OC36	OC35	OC34	OC33	OC32	OC31	OC30	00_{16}
$21A_{16}$	Timer 5 (TM5)									FF_{16}
$21B_{16}$	Timer 6 (TM6)									07_{16}
$21C_{16}$	Top border control register 1 (TB1)	TB17	TB16	TB15	TB14	TB13	TB12	TB11	TB10	?
$21D_{16}$	Bottom border control register 1 (BB1)	BB17	BB16	BB15	BB14	BB13	BB12	BB11	BB10	?
$21E_{16}$	Top border control register 2 (TB2)							TB21	TB20	?
$21F_{16}$	Bottom border control register 2 (BB2)							BB21	BB20	?

Fig. 8.2.6 Memory Map of Special Function Register 2 (SFR2) (1)

■ SFR2 area (addresses 220_{16} to $23F_{16}$)

<Bit allocation>

- (blank box) : } Function bit
- Name : } Function bit
- (grey box) : No function bit
- 0 (grey box) : Fix to this bit to “0” (do not write to “1”)
- 1 (grey box) : Fix to this bit to “1” (do not write to “0”)

<State immediately after reset>

- 0 : “0” immediately after reset
- 1 : “1” immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	b7							b0	State immediately after reset (b7–b0)
220_{16}	Vertical position register 1_1 ($VP1_1$)	$VP1_17$	$VP1_16$	$VP1_15$	$VP1_14$	$VP1_13$	$VP1_12$	$VP1_11$	$VP1_10$	?
221_{16}	Vertical position register 1_2 ($VP1_2$)	$VP1_27$	$VP1_26$	$VP1_25$	$VP1_24$	$VP1_23$	$VP1_22$	$VP1_21$	$VP1_20$	?
222_{16}	Vertical position register 1_3 ($VP1_3$)	$VP1_37$	$VP1_36$	$VP1_35$	$VP1_34$	$VP1_33$	$VP1_32$	$VP1_31$	$VP1_30$	?
223_{16}	Vertical position register 1_4 ($VP1_4$)	$VP1_47$	$VP1_46$	$VP1_45$	$VP1_44$	$VP1_43$	$VP1_42$	$VP1_41$	$VP1_40$	?
224_{16}	Vertical position register 1_5 ($VP1_5$)	$VP1_57$	$VP1_56$	$VP1_55$	$VP1_54$	$VP1_53$	$VP1_52$	$VP1_51$	$VP1_50$	?
225_{16}	Vertical position register 1_6 ($VP1_6$)	$VP1_67$	$VP1_66$	$VP1_65$	$VP1_64$	$VP1_63$	$VP1_62$	$VP1_61$	$VP1_60$	?
226_{16}	Vertical position register 1_7 ($VP1_7$)	$VP1_77$	$VP1_76$	$VP1_75$	$VP1_74$	$VP1_73$	$VP1_72$	$VP1_71$	$VP1_70$	?
227_{16}	Vertical position register 1_8 ($VP1_8$)	$VP1_87$	$VP1_86$	$VP1_85$	$VP1_84$	$VP1_83$	$VP1_82$	$VP1_81$	$VP1_80$	?
228_{16}	Vertical position register 1_9 ($VP1_9$)	$VP1_97$	$VP1_96$	$VP1_95$	$VP1_94$	$VP1_93$	$VP1_92$	$VP1_91$	$VP1_90$	?
229_{16}	Vertical position register 1_{10} ($VP1_{10}$)	$VP1_{10}7$	$VP1_{10}6$	$VP1_{10}5$	$VP1_{10}4$	$VP1_{10}3$	$VP1_{10}2$	$VP1_{10}1$	$VP1_{10}0$	?
$22A_{16}$	Vertical position register 1_{11} ($VP1_{11}$)	$VP1_{11}7$	$VP1_{11}6$	$VP1_{11}5$	$VP1_{11}4$	$VP1_{11}3$	$VP1_{11}2$	$VP1_{11}1$	$VP1_{11}0$	?
$22B_{16}$	Vertical position register 1_{12} ($VP1_{12}$)	$VP1_{12}7$	$VP1_{12}6$	$VP1_{12}5$	$VP1_{12}4$	$VP1_{12}3$	$VP1_{12}2$	$VP1_{12}1$	$VP1_{12}0$	?
$22C_{16}$	Vertical position register 1_{13} ($VP1_{13}$)	$VP1_{13}7$	$VP1_{13}6$	$VP1_{13}5$	$VP1_{13}4$	$VP1_{13}3$	$VP1_{13}2$	$VP1_{13}1$	$VP1_{13}0$	?
$22D_{16}$	Vertical position register 1_{14} ($VP1_{14}$)	$VP1_{14}7$	$VP1_{14}6$	$VP1_{14}5$	$VP1_{14}4$	$VP1_{14}3$	$VP1_{14}2$	$VP1_{14}1$	$VP1_{14}0$	?
$22E_{16}$	Vertical position register 1_{15} ($VP1_{15}$)	$VP1_{15}7$	$VP1_{15}6$	$VP1_{15}5$	$VP1_{15}4$	$VP1_{15}3$	$VP1_{15}2$	$VP1_{15}1$	$VP1_{15}0$	?
$22F_{16}$	Vertical position register 1_{16} ($VP1_{16}$)	$VP1_{16}7$	$VP1_{16}6$	$VP1_{16}5$	$VP1_{16}4$	$VP1_{16}3$	$VP1_{16}2$	$VP1_{16}1$	$VP1_{16}0$	?
230_{16}	Vertical position register 2_1 ($VP2_1$)							$VP2_11$	$VP2_10$	?
231_{16}	Vertical position register 2_2 ($VP2_2$)							$VP2_21$	$VP2_20$	?
232_{16}	Vertical position register 2_3 ($VP2_3$)							$VP2_31$	$VP2_30$	?
233_{16}	Vertical position register 2_4 ($VP2_4$)							$VP2_41$	$VP2_40$	?
234_{16}	Vertical position register 2_5 ($VP2_5$)							$VP2_51$	$VP2_50$	?
235_{16}	Vertical position register 2_6 ($VP2_6$)							$VP2_61$	$VP2_60$	?
236_{16}	Vertical position register 2_7 ($VP2_7$)							$VP2_71$	$VP2_70$	?
237_{16}	Vertical position register 2_8 ($VP2_8$)							$VP2_81$	$VP2_80$	?
238_{16}	Vertical position register 2_9 ($VP2_9$)							$VP2_91$	$VP2_90$	?
239_{16}	Vertical position register 2_{10} ($VP2_{10}$)							$VP2_{10}1$	$VP2_{10}0$	?
$23A_{16}$	Vertical position register 2_{11} ($VP2_{11}$)							$VP2_{11}1$	$VP2_{11}0$	?
$23B_{16}$	Vertical position register 2_{12} ($VP2_{12}$)							$VP2_{12}1$	$VP2_{12}0$	?
$23C_{16}$	Vertical position register 2_{13} ($VP2_{13}$)							$VP2_{13}1$	$VP2_{13}0$	?
$23D_{16}$	Vertical position register 2_{14} ($VP2_{14}$)							$VP2_{14}1$	$VP2_{14}0$	?
$23E_{16}$	Vertical position register 2_{15} ($VP2_{15}$)							$VP2_{15}1$	$VP2_{15}0$	?
$23F_{16}$	Vertical position register 2_{16} ($VP2_{16}$)							$VP2_{16}1$	$VP2_{16}0$	?

Fig. 8.2.7 Memory Map of Special Function Register 2 (SFR2) (2)

■ SFR2 area (addresses 240_{16} to 258_{16})

<Bit allocation>

- ☐ : / Name : } Function bit
- (grey box) : No function bit
- 0 : Fix to this bit to “0” (do not write to “1”)
- 1 : Fix to this bit to “1” (do not write to “0”)

<State immediately after reset>

- 0 : “0” immediately after reset
- 1 : “1” immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	b7	b6	b5	b4	b3	b2	b1	b0	State immediately after reset (b7–b0)
240_{16}										?
241_{16}	Color pallet register 1 (CR1)		$CR_{1}6$	$CR_{1}5$	$CR_{1}4$	$CR_{1}3$	$CR_{1}2$	$CR_{1}1$	$CR_{1}0$	?
242_{16}	Color pallet register 2 (CR2)		$CR_{2}6$	$CR_{2}5$	$CR_{2}4$	$CR_{2}3$	$CR_{2}2$	$CR_{2}1$	$CR_{2}0$	?
243_{16}	Color pallet register 3 (CR3)		$CR_{3}6$	$CR_{3}5$	$CR_{3}4$	$CR_{3}3$	$CR_{3}2$	$CR_{3}1$	$CR_{3}0$	?
244_{16}	Color pallet register 4 (CR4)		$CR_{4}6$	$CR_{4}5$	$CR_{4}4$	$CR_{4}3$	$CR_{4}2$	$CR_{4}1$	$CR_{4}0$	?
245_{16}	Color pallet register 5 (CR5)		$CR_{5}6$	$CR_{5}5$	$CR_{5}4$	$CR_{5}3$	$CR_{5}2$	$CR_{5}1$	$CR_{5}0$	?
246_{16}	Color pallet register 6 (CR6)		$CR_{6}6$	$CR_{6}5$	$CR_{6}4$	$CR_{6}3$	$CR_{6}2$	$CR_{6}1$	$CR_{6}0$	?
247_{16}	Color pallet register 7 (CR7)		$CR_{7}6$	$CR_{7}5$	$CR_{7}4$	$CR_{7}3$	$CR_{7}2$	$CR_{7}1$	$CR_{7}0$	?
248_{16}										?
249_{16}	Color pallet register 9 (CR9)		$CR_{9}6$	$CR_{9}5$	$CR_{9}4$	$CR_{9}3$	$CR_{9}2$	$CR_{9}1$	$CR_{9}0$	?
$24A_{16}$	Color pallet register10 (CR10)		$CR_{10}6$	$CR_{10}5$	$CR_{10}4$	$CR_{10}3$	$CR_{10}2$	$CR_{10}1$	$CR_{10}0$	?
$24B_{16}$	Color pallet register 11 (CR11)		$CR_{11}6$	$CR_{11}5$	$CR_{11}4$	$CR_{11}3$	$CR_{11}2$	$CR_{11}1$	$CR_{11}0$	?
$24C_{16}$	Color pallet register 12 (CR12)		$CR_{12}6$	$CR_{12}5$	$CR_{12}4$	$CR_{12}3$	$CR_{12}2$	$CR_{12}1$	$CR_{12}0$	?
$24D_{16}$	Color pallet register 13 (CR13)		$CR_{13}6$	$CR_{13}5$	$CR_{13}4$	$CR_{13}3$	$CR_{13}2$	$CR_{13}1$	$CR_{13}0$	?
$24E_{16}$	Color pallet register 14 (CR14)		$CR_{14}6$	$CR_{14}5$	$CR_{14}4$	$CR_{14}3$	$CR_{14}2$	$CR_{14}1$	$CR_{14}0$	?
$24F_{16}$	Color pallet register 15 (CR15)		$CR_{15}6$	$CR_{15}5$	$CR_{15}4$	$CR_{15}3$	$CR_{15}2$	$CR_{15}1$	$CR_{15}0$	?
250_{16}	Left border control register 1 (LB1)	LB17	LB16	LB15	LB14	LB13	LB12	LB11	LB10	01_{16}
251_{16}	Left border control register 2 (LB2)						LB22	LB21	LB20	00_{16}
252_{16}	Right border control register 1 (RB1)	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	FF_{16}
253_{16}	Right border control register 2 (RB2)						RB22	RB21	RB20	07_{16}
254_{16}	SPRITE vertical position register 1 (VS1)	VS17	VS16	VS15	VS14	VS13	VS12	VS11	VS10	?
255_{16}	SPRITE vertical position register 2 (VS2)							VS21	VS20	00_{16}
256_{16}	SPRITE horizontal position register 1 (HS1)	HS17	HS16	HS15	HS14	HS13	HS12	HS11	HS10	?
257_{16}	SPRITE horizontal position register 2 (HS2)						HS22	HS21	HS20	0 0 0 0 0 ? ? ?
258_{16}	SPRITE OSD control register (SC)			SC5	SC4	SC3	SC2	SC1	SC0	00_{16}

Fig. 8.2.8 Memory Map of Special Function Register 2 (SFR2) (3)

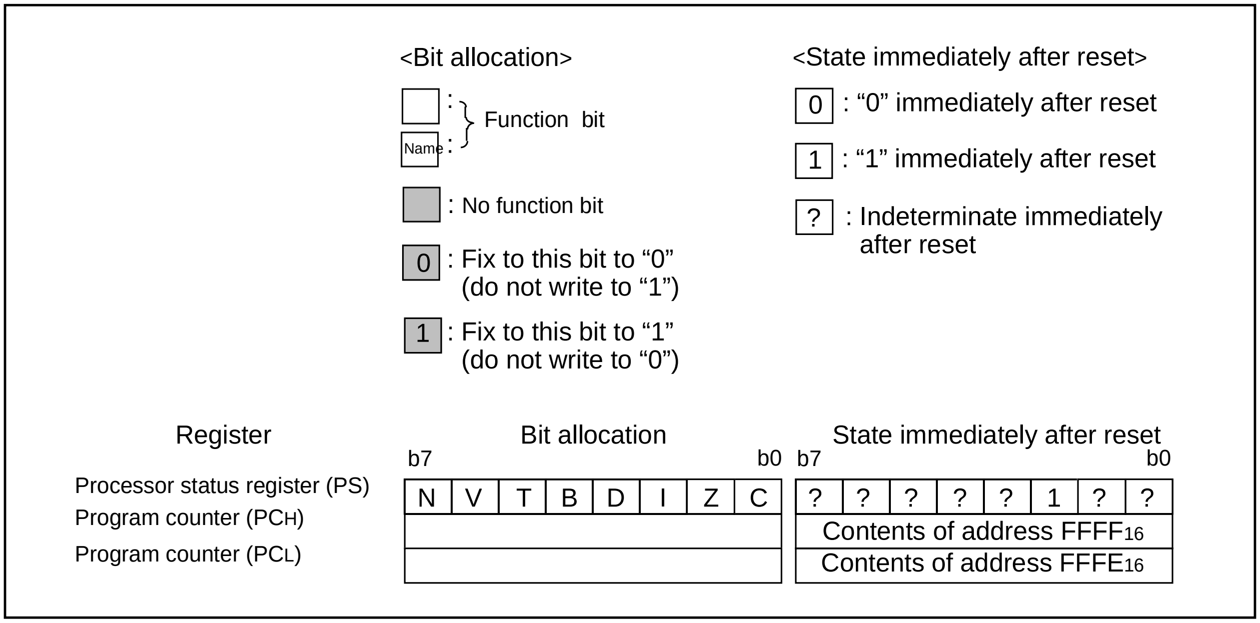


Fig. 8.2.9 Internal State of Processor Status Register and Program Counter at Reset

8.3 INTERRUPTS

Interrupts can be caused by 19 different sources consisting of 3 external, 14 internal, 1 software, and reset. Interrupts are vectored interrupts with priorities as shown in Table 8.3.1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted,

① The contents of the program counter and processor status register are automatically stored into the stack.

② The interrupt disable flag I is set to “1” and the corresponding interrupt request bit is set to “0.”

③ The jump destination address stored in the vector address enters the program counter.

Nothing to stop reset.

Other interrupts are disabled when the interrupt disable flag is set to “1.”

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figures 8.3.2 to 8.3.6 show the interrupt-related registers.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is “1,” interrupt request bit is “1,” and the interrupt disable flag is “0.” The interrupt request bit can be set to “0” by a program, but not set to “1.” The interrupt enable bit can be set to “0” and “1” by a program.

Reset is treated as a non-maskable interrupt with the highest priority.

Figure 8.3.1 shows interrupt control.

8.3.1 Interrupt Causes

(1) VSYNC and OSD Interrupts

The VSYNC interrupt is an interrupt request synchronized with the vertical sync signal.

The OSD interrupt occurs after character block display to the CRT is completed.

(2) INT1, INT2 External Interrupts

The INT1 and INT2 interrupts are external interrupt inputs, the system detects that the level of a pin changes from LOW to HIGH or from HIGH to LOW, and generates an interrupt request. The input active edge can be selected by bits 3 and 4 of the interrupt input polarity register (address 0212_{16}) : when this bit is “0,” a change from LOW to HIGH is detected; when it is “1,” a change from HIGH to LOW is detected. Note that both bits are cleared to “0” at reset.

(3) Timer 1 to 4 Interrupts

An interrupt is generated by an overflow of timer 1, 2, 3 or 4.

Table 8.3.1 Interrupt Vector Addresses and Priority

Priority	Interrupt Source	Vector Addresses	Remarks
1	Reset	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
2	OSD interrupt	$FFFD_{16}$, $FFFC_{16}$	
3	INT1 external interrupt	$FFFB_{16}$, $FFFA_{16}$	Active edge selectable
4	Data slicer interrupt	$FFF9_{16}$, $FFF8_{16}$	
5	Serial I/O interrupt	$FFF7_{16}$, $FFF6_{16}$	
6	Timer 4 interrupt	$FFF5_{16}$, $FFF4_{16}$	
7	f(XIN)/4096 • SPRITE OSD interrupt	$FFF3_{16}$, $FFF2_{16}$	Software switch by software (See note)
8	VSYNC interrupt	$FFF1_{16}$, $FFF0_{16}$	
9	Timer 3 interrupt	$FFEF_{16}$, $FFEE_{16}$	
10	Timer 2 interrupt	$FFED_{16}$, $FFEC_{16}$	
11	Timer 1 interrupt	$FFEB_{16}$, $FFEA_{16}$	
12	A-D convertion • INT3 external interrupt	$FFE9_{16}$, $FFE8_{16}$	Software switch by software (See note)/ When selecting INT3 interrupt, active edge selectable.
13	INT2 external interrupt	$FFE7_{16}$, $FFE6_{16}$	Active edge selectable
14	Multi-master I^2C-BUS interface interrupt	$FFE5_{16}$, $FFE4_{16}$	
15	Timer 5 • 6 interrupt	$FFE3_{16}$, $FFE2_{16}$	Software switch by software (See note)
16	BRK instruction interrupt	$FFDF_{16}$, $FFDE_{16}$	Non-maskable (software interrupt)

Note : Switching a source during a program causes an unnecessary interrupt occurs. Accordingly, set a source at initializing of program.

(4) Serial I/O Interrupt

This is an interrupt request from the clock synchronous serial I/O function.

(5) f(XIN)/4096 • SPRITE OSD Interrupt

The f (XIN)/4096 interrupt occurs regularly with a f(XIN)/4096 period. Set bit 0 of the PWM mode register 1 to “0.”

The SPRITE OSD interrupt occurs at the completion of SPRITE display.

Since f(XIN)/4096 interrupt and SPRITE OSD interrupt share the same vector, an interrupt source is selected by bit 5 of the SPRITE OSD control register (address 0258_{16}).

(6) Data Slicer Interrupt

An interrupt occurs when slicing data is completed.

(7) Multi-master I^2C-BUS Interface Interrupt

This is an interrupt request related to the multi-master I^2C-BUS interface.

(8) A-D Conversion • INT3 external Interrupt

The A-D conversion interrupt occurs at the completion of A-D conversion.

The INT3 is an external input,the system detects that the level of a pin changes from LOW to HIGH or from HIGH to LOW, and generates an interrupt request. The input active edge can be selected by bit 6 of the interrupt input polarity register (address 0212_{16}) : when this bit is “0,” a change from LOW to HIGH is detected; when it is “1,” a change from HIGH to LOW is detected. Note that this bit is cleared to “0” at reset.

Since A-D conversion interrupt and the INT3 external interrupt share the same vector, an interrupt source is selected by bit 7 of the interrupt interval determination control register (address 0212_{16}).

(9) Timer 5 • 6 Interrupt

An interrupt is generated by an overflow of timer 5 or 6. Their priorities are same, and can be switched by software.

(10) BRK Instruction Interrupt

This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

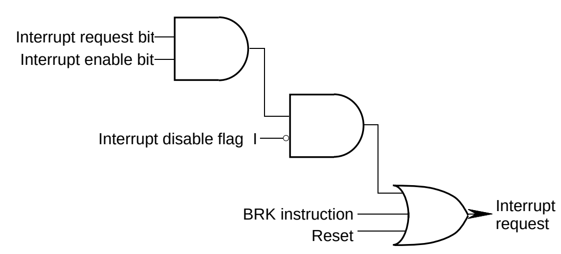


Fig. 8.3.1 Interrupt Control

Interrupt Request Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
6	A-D conversion • INT3 external interrupt request bit (ADR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

✻ : “0” can be set by software, but “1” cannot be set.

Fig. 8.3.2 Interrupt Request Register 1

Interrupt Request Register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

Interrupt request register 2 (IREQ2) [Address 00FD16]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt request bit (IN1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	Data slicer interrupt request bit (DSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Serial I/O interrupt request bit (SIOR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	f(XIN)/4096 • SPRITE OSD interrupt request bit (CKR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	INT2 external interrupt request bit (IN2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	Multi-master I2C-BUS interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
6	Timer 5 • 6 interrupt request bit (TM56R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	Fix this bit to “0.”		0	R	W

✻: “0” can be set by software, but “1” cannot be set.

Fig. 8.3.3 Interrupt Request Register 2

Interrupt Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address $00FE_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	OSD interrupt enable bit (OSDE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	A-D conversion • INT3 external interrupt enable bit (ADE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Fig. 8.3.4 Interrupt Control Register 1

Interrupt Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 2 (ICON2) [Address $00FF_{16}$]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt enable bit (IN1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Data slicer interrupt enable bit (DSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (SIOE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	$f(X_{IN})/4096$ • SPRITE OSD interrupt enable bit (CKE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	INT2 external interrupt enable bit (IN2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	Multi-master I^2C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Timer 5 • 6 interrupt enable bit (TM56E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Timer 5 • 6 interrupt switch bit (TM56S)	0 : Timer 5 1 : Timer 6	0	R	W

Fig. 8.3.5 Interrupt Control Register 2

Interrupt Input Polarity Register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt input polarity register (IP) [Address 0212_{16}]

B	Name	Functions	After reset	R	W
0 to 2	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
3	INT1 polarity switch bit (POL1)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	INT2 polarity switch bit (POL2)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is “0.”		0	R	—
6	INT3 polarity switch bit (POL3)	0 : Positive polarity 1 : Negative polarity	0	R	W
7	A-D conversion • INT3 interrupt source selection bit (AD/INT3SEL)	0 : INT3 interrupt 1 : A-D conversion interrupt	0	R	W

Fig. 8.3.6 Interrupt Input Polarity Register

8.4 TIMERS

This microcomputer has 6 timers: timer 1, timer 2, timer 3, timer 4, timer 5, and timer 6. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 8.4.3.
All of the timers count down and their divide ratio is 1/(n+1), where n is the value of timer latch. By writing a count value to the corresponding timer latch (addresses $00F0_{16}$ to $00F3_{16}$: timers 1 to 4, addresses $021A_{16}$ and $021B_{16}$: timers 5 and 6), the value is also set to a timer, simultaneously.
Down counts "nn_{16} – 1, nn_{16} – 2......., 01_{16}, 00_{16}" by the input of the count source from the right after setting to the timer. The interrupt is requested by a timer overflow at the next count source input in which the value of the timer becomes "00_{16}."
Each timers are explained below.

8.4.1 Timer 1

Timer 1 can select one of the following count sources:
- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- $f(X_{IN})/4096$ or $f(X_{CIN})/4096$
- External clock from the TIM2 pin

The count source of timer 1 is selected by setting bits 5 and 0 of timer mode register 1 (address $00F4_{16}$). Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register.
Timer 1 interrupt request occurs at timer 1 overflow.

8.4.2 Timer 2

Timer 2 can select one of the following count sources:
- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- Timer 1 overflow signal
- External clock from the TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of timer mode register 1 (address $00F4_{16}$). Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register. When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.
Timer 2 interrupt request occurs at timer 2 overflow.

8.4.3 Timer 3

Timer 3 can select one of the following count sources:
- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- $f(X_{CIN})$
- External clock from the TIM3 pin

The count source of timer 3 is selected by setting bit 0 of timer mode register 2 (address $00F5_{16}$) and bit 6 at address $00C7_{16}$. Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register.
Timer 3 interrupt request occurs at timer 3 overflow.

8.4.4 Timer 4

Timer 4 can select one of the following count sources:
- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- $f(X_{IN})/2$ or $f(X_{CIN})/2$
- $f(X_{CIN})$
- Timer 3 overflow signal

The count source of timer 4 is selected by setting bits 1 and 4 of timer mode register 2 (address $00F5_{16}$). Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register. When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.
Timer 4 interrupt request occurs at timer 4 overflow.

8.4.5 Timer 5

Timer 5 can select one of the following count sources:
- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- Timer 2 overflow signal
- Timer 4 overflow signal

The count source of timer 5 is selected by setting bit 6 of timer mode register 1 (address $00F4_{16}$) and bit 7 of timer mode register 2 (address $00F5_{16}$). When overflow of timer 2 or 4 is a count source for timer 5, either timer 2 or 4 functions as an 8-bit prescaler. Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register.
Timer 5 interrupt request occurs at timer 5 overflow.

8.4.6 Timer 6

Timer 6 can select one of the following count sources:
- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- Timer 5 overflow signal

The count source of timer 6 is selected by setting bit 7 of timer mode register 1 (address $00F4_{16}$). Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register. When timer 5 overflow signal is a count source for timer 6, timer 5 functions as an 8-bit prescaler.
Timer 6 interrupt request occurs at timer 6 overflow.

At reset, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. The $f(X_{IN})$✻ /16 is selected as the timer 3 count source. The internal reset is released by timer 4 overflow in this state and the internal clock is connected.
At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. However, the $f(X_{IN})$✻ /16 is not selected as the timer 3 count source. So set both bit 0 of timer mode register 2 (address $00F5_{16}$) and bit 6 at address $00C7_{16}$ to "0" before execution of the STP instruction ($f(X_{IN})$✻ /16 is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow in this state and the internal clock is connected.
As a result of the above procedure, the program can start under a stable clock.

✻ : When bit 7 of the CPU mode register (CM7) is "1," $f(X_{IN})$ becomes $f(X_{CIN})$.

The timer-related registers is shown in Figures 8.4.1 and 8.4.2.

Timer Mode Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 1 (TM1) [Address $00F4_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (TM10)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Count source selected by bit 5 of TM1	0	R	W
1	Timer 2 count source selection bit 1 (TM11)	0: Count source selected by bit 4 of TM1 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (TM12)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (TM13)	0: Count start 1: Count stop	0	R	W
4	Timer 2 count source selection bit 2 (TM14)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Timer 1 overflow	0	R	W
5	Timer 1 count source selection bit 2 (TM15)	0: f(XIN)/4096 or f(XCIN)/4096 (See note) 1: External clock from TIM2 pin	0	R	W
6	Timer 5 count source selection bit 2 (TM16)	0: Timer 2 overflow 1: Timer 4 overflow	0	R	W
7	Timer 6 count source selection bit (TM17)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Timer 5 overflow	0	R	W

Note: Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

Fig. 8.4.1 Timer Mode Register 1

Timer Mode Register 2

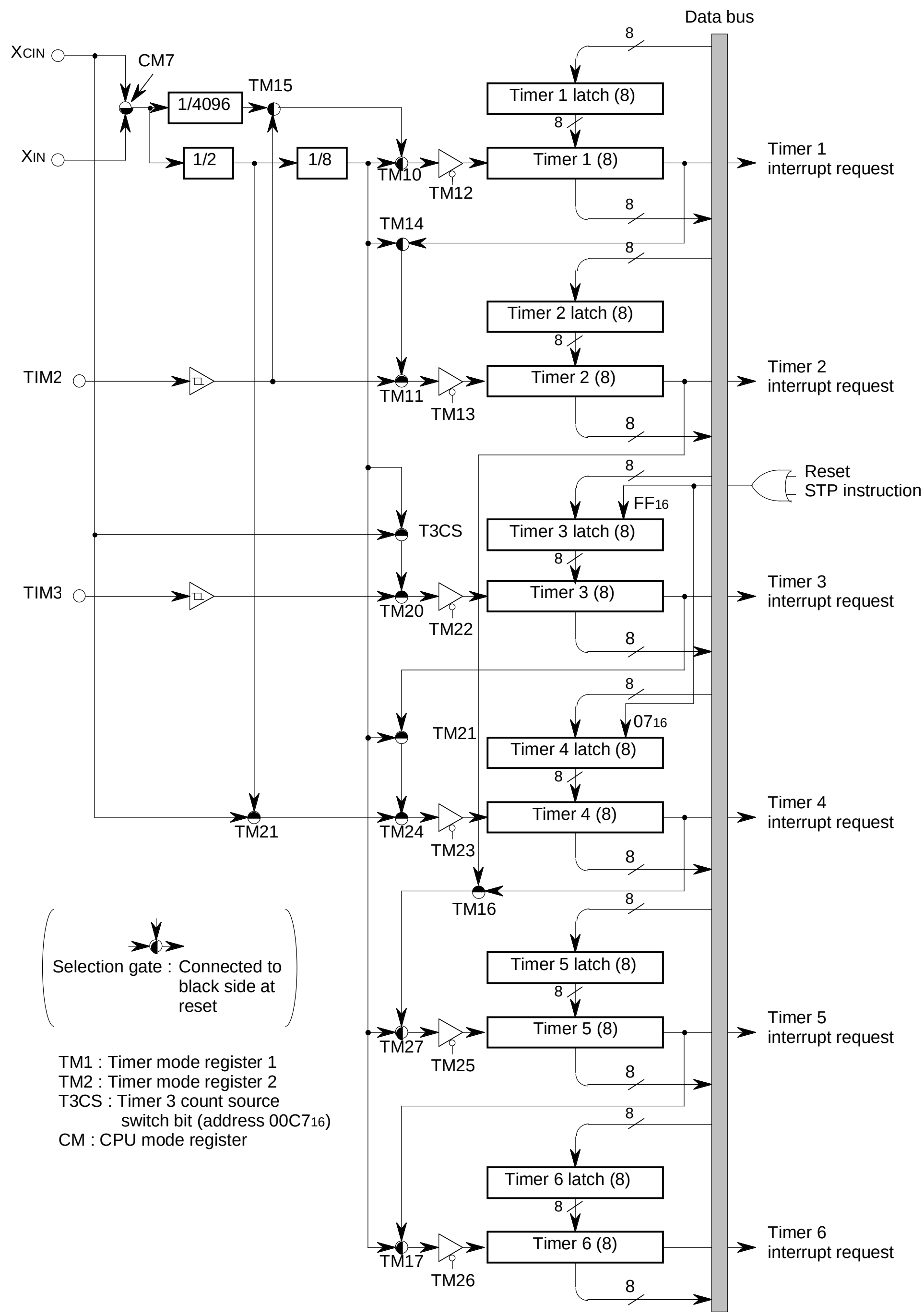
b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 2 (TM2) [Address 00F5$_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (TM20)	(b6 at address 00C7$_{16}$) ▼ b0 0 0 : f(XIN)/16 or f(XCIN)/16 (See note) 1 0 : f(XCIN) 0 1 : } External clock from TIM3 pin 1 1 : }	0	R	W
1, 4	Timer 4 count source selection bits (TM21, TM24)	b4 b1 0 0 : Timer 3 overflow signal 0 1 : f(XIN)/16 or f(XCIN)/16 (See note) 1 0 : f(XIN)/2 or f(XCIN)/2 (See note) 1 1 : f(XCIN)	0	R	W
2	Timer 3 count stop bit (TM22)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (TM23)	0: Count start 1: Count stop	0	R	W
5	Timer 5 count stop bit (TM25)	0: Count start 1: Count stop	0	R	W
6	Timer 6 count stop bit (TM26)	0: Count start 1: Count stop	0	R	W
7	Timer 5 count source selection bit 1 (TM27)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Count source selected by bit 6 of TM1	0	R	W

Note: Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

Fig. 8.4.2 Timer Mode Register 2



Notes 1: HIGH pulse width of external clock inputs TIM2 and TIM3 needs 4 machine cycles or more.

2: When the external clock source is selected, timers 1, 2, and 3 are counted at a rising edge of input signal.

3: In the stop mode or the wait mode, external clock inputs TIM2 and TIM3 cannot be used.

Fig. 8.4.3 Timer Block Diagram

8.5 SERIAL I/O

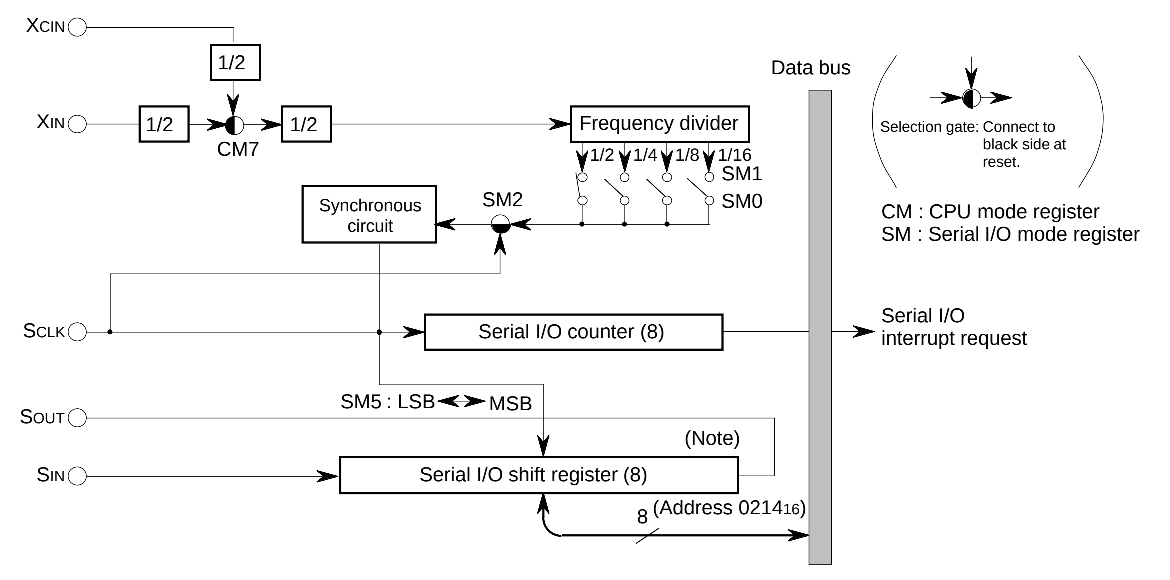
This microcomputer has a built-in serial I/O which can either transmit or receive 8-bit data serially in the clock synchronous mode.

The serial I/O block diagram is shown in Figure 8.5.1. The synchronous clock I/O pin (SCLK), and data output pin (SOUT) also function as port P4, data input pin (SIN) also functions as ports P1 and P7.

Bit 2 of the serial I/O mode register (address 0213_{16}) selects whether the synchronous clock is supplied internally or externally (from the SCLK pin). When an internal clock is selected, bits 1 and 0 select whether f(XIN) or f(XCIN) is divided by 8, 16, 32, or 64. To use the pin for servial I/O, set the bit corresponding to SCLK pin of thr port P4 direction register (address $00C9_{16}$) and the bit corresponding to SIN pin of the port P1 direction register (address $00C3_{16}$) to "0".

More over, set the bit corresponding to SOUT of rhe port P4 direction register (address $00C9_{16}$) to "1" And, to use SOUT pin for serial I/O, set the corresponding bits of the port P4 direction register (address $00C9_{16}$) to "1."

The operation of the serial I/O is described below. The operation of the serial I/O differs depending on the clock source; external clock or internal clock.



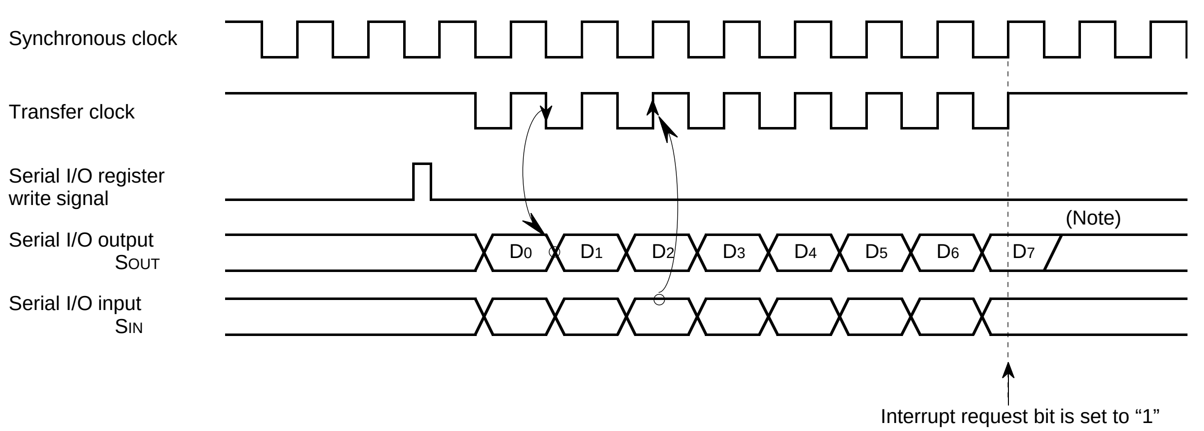
Note : When the data is set in the serial I/O register (address 0214_{16}), the register functions as the serial I/O shift register.

Fig. 8.5.1 Serial I/O Block Diagram

Internal clock : The serial I/O counter is set to “7” during the write cycle into the serial I/O register (address 0214_{16}), and the transfer clock goes “H” forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the SOUT pin. Transfer direction can be selected by bit 5 of the serial I/O mode register. At each rising edge of the transfer clock, data is input from the SIN pin and data in the serial I/O register is shifted 1 bit.
After the transfer clock has counted 8 times, the serial I/O counter becomes “0” and the transfer clock stops at HIGH. At this time the interrupt request bit is set to “1.”

External clock : The an external clock is selected as the clock source, the interrupt request is set to “1” after the transfer clock has been counted 8 counts. However, transfer operation does not stop, so the clock should be controlled externally. Use the external clock of 500 kHz or less with a duty cycle of 50 %.
The serial I/O timing is shown in Figure 8.5.2. When using an external clock for transfer, the external clock must be held at HIGH for initializing the serial I/O counter. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O counter after switching.

Notes 1: On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions, such as SEB and CLB.
2: When an external clock is used as the synchronous clock, write transmit data to the serial I/O register when the transfer clock input level is HIGH.



Note : When an internal clock is selected, the SOUT pin is at high-impedance after transfer is completed.

Fig. 8.5.2 Serial I/O Timing (for LSB first)

Serial I/O Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O mode register (SM) [Address 0213_{16}]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: $f(X_{IN})/8$ or $f(X_{CIN})/8$ 0 1: $f(X_{IN})/16$ or $f(X_{CIN})/16$ 1 0: $f(X_{IN})/32$ or $f(X_{CIN})/32$ 1 1: $f(X_{IN})/64$ or $f(X_{CIN})/64$	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Port function selection bit (SM3)	0: $P1_1$, $P1_3$ 1: SCL1, SDA1	0	R	W
4	Port function selection bit (SM4)	0: $P1_2$, $P1_4$ 1: SCL2, SDA2	0	R	W
5	Transfer direction selection bit (SM5)	0: Transfer from the last significant bit (LSB) 1: Transfer from the top significant bit (MSB)	0	R	W
6	S_{IN} pin switch bit (SM6)	0: $P1_7$ is S_{IN} pin 1: $P7_2$ is S_{IN} pin	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Fig. 8.5.3 Serial I/O Mode Register

8.6 MULTI-MASTER I^{2}C-BUS INTERFACE

The multi-master I^{2}C-BUS interface is a serial communications circuit, conforming to the Philips I^{2}C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.

Figure 8.6.1 shows a block diagram of the multi-master I^{2}C-BUS interface and Table 8.6.1 shows multi-master I^{2}C-BUS interface functions.

This multi-master I^{2}C-BUS interface consists of the I^{2}C address register, the I^{2}C data shift register, the I^{2}C clock control register, the I^{2}C control register, the I^{2}C status register and other control circuits.

Table 8.6.1 Multi-master I^{2}C-BUS Interface Functions

Item	Function
Format	In conformity with Philips I^{2}C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I^{2}C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at ϕ = 4 MHz)

ϕ : System clock = f(XIN)/2

Note : We are not responsible for any third party's infringement of patent rights or other rights attributable to the use of the control function (bits 6 and 7 of the I^{2}C control register at address 00F9$_{16}$) for connections between the I^{2}C-BUS interface and ports (SCL1, SCL2, SDA1, SDA2).

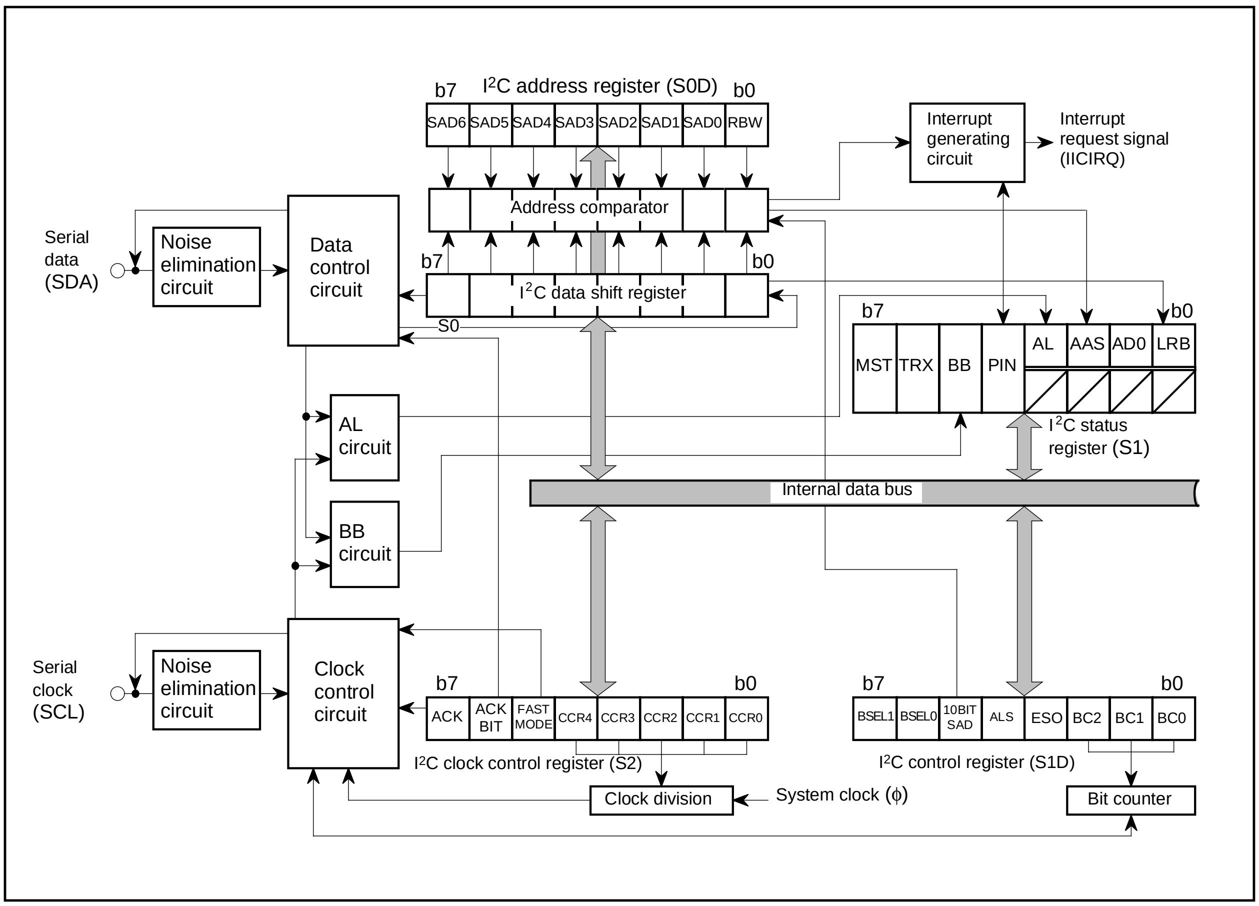


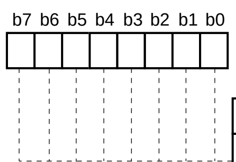
Fig. 8.6.1 Block Diagram of Multi-master I^{2}C-BUS Interface

8.6.1 I^2C Data Shift Register

The I^2C data shift register (S0 : address $00F6_{16}$) is an 8-bit shift register to store receive data and write transmit data.
When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted one bit to the left.
The I^2C data shift register is in a write enable status only when the ESO bit of the I^2C control register (address $00F9_{16}$) is “1.” The bit counter is reset by a write instruction to the I^2C data shift register. When both the ESO bit and the MST bit of the I^2C status register (address $00F8_{16}$) are “1,” the SCL is output by a write instruction to the I^2C data shift register. Reading data from the I^2C data shift register is always enabled regardless of the ESO bit value.

Note: To write data into the I^2C data shift register after setting the MST bit to “0” (slave mode), keep an interval of 8 machine cycles or more.

I^2C Data Shift Register



I^2C data shift register (S0) [Address $00F6_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	D0 to D7	This is an 8-bit shift register to store receive data and write transmit data.	Indeterminate	R	W

Note: To write data into the I^2C data shift register after setting the MST bit to “0” (slave mode), keep an interval of 8 machine cycles or more.

Fig. 8.6.2 Data Shift Register

8.6.2 I^{2}C Address Register

The I^{2}C address register (address 00F7$_{16}$) consists of a 7-bit slave address and a $\overline{\text{read}}$/write bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition are detected.

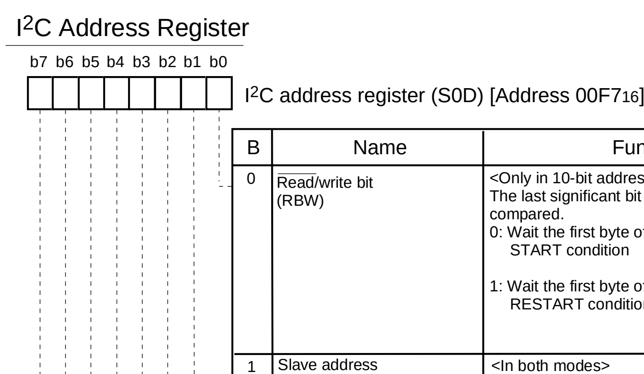
(1) Bit 0: $\overline{\text{Read}}$/Write Bit (RBW)

Not used when comparing addresses, in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RBW) of the I^{2}C address register.

The RBW bit is cleared to “0” automatically when the STOP condition is detected.

(2) Bits 1 to 7: Slave Address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.



B	Name	Functions	After reset	R	W
0	$\overline{\text{Read}}$/write bit (RBW)	<Only in 10-bit addressing (in slave) mode> The last significant bit of address data is compared. 0: Wait the first byte of slave address after START condition (read state) 1: Wait the first byte of slave address after RESTART condition (write state)	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	<In both modes> The address data is compared.	0	R	W

Fig. 8.6.3 I^{2}C Address Register

8.6.3 I²C Clock Control Register

The I²C clock control register (address 00FA16) is used to set ACK control, SCL mode and SCL frequency.

(1) Bits 0 to 4: SCL Frequency Control Bits (CCR0–CCR4)

These bits control the SCL frequency.

(2) Bit 5: SCL Mode Specification Bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to “0,” the standard clock mode is set. When the bit is set to “1,” the high-speed clock mode is set.

(3) Bit 6: ACK Bit (ACK BIT)

This bit sets the SDA status when an ACK clock✻ is generated. When this bit is set to “0,” the ACK return mode is set and SDA goes to LOW at the occurrence of an ACK clock. When the bit is set to “1,” the ACK non-return mode is set. The SDA is held in the HIGH status at the occurrence of an ACK clock.
However, when the slave address matches the address data in the reception of address data at ACK BIT = “0,” the SDA is automatically made LOW (ACK is returned). If there is a mismatch between the slave address and the address data, the SDA is automatically made HIGH (ACK is not returned).

✻ACK clock: Clock for acknowledgement

(4) Bit 7: ACK Clock Bit (ACK)

This bit specifies a mode of acknowledgment which is an acknowledgment response of data transmission. When this bit is set to “0,” the no ACK clock mode is set. In this case, no ACK clock occurs after data transmission. When the bit is set to “1,” the ACK clock mode is set and the master generates an ACK clock upon completion of each 1-byte data transmission.The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (make SDA HIGH) and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transmission. If data is written during transmission, the I²C clock generator is reset, so that data cannot be transmitted normally.

I²C Clock Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I²C clock control register (S2) [Address 00FA16]

B	Name	Functions: Register value b4 to b0	Functions: Standard clock mode	Functions: High speed clock mode	After reset	R	W
0 to 4	SCL frequency control bits (CCR0 to CCR4)	00 to 02	Setup disabled	Setup disabled	0	R	W
		03	Setup disabled	333			
		04	Setup disabled	250			
		05	100	400 (See note)			
		06	83.3	166			
		⋮	500/CCR value	1000/CCR value			
		1D	17.2	34.5			
		1E	16.6	33.3			
		1F	16.1	32.3			
		(at f = 4 MHz, unit : kHz)					
5	SCL mode specification bit (FAST MODE)	0: Standard clock mode 1: High-speed clock mode			0	R	W
6	ACK bit (ACK BIT)	0: ACK is returned. 1: ACK is not returned.			0	R	W
7	ACK clock bit (ACK)	0: No ACK clock 1: ACK clock			0	R	W

Note: At 400 kHz in the high-speed clock mode, the duty is as below .
“0” period : “1” period = 3 : 2
In the other cases, the duty is as below.
“0” period : “1” period = 1 : 1

Fig. 8.6.4 I²C Clock Control

8.6.4 I^{2}C Control Register

The I^{2}C control register (address 00F9$_{16}$) controls the data communication format.

(1) Bits 0 to 2: Bit Counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. An interrupt request signal occurs immediately after the number of bits specified with these bits are transmitted.
When a START condition is received, these bits become “000$_2$” and the address data is always transmitted and received in 8 bits.

(2) Bit 3: I^{2}C Interface Use Enable Bit (ESO)

This bit enables usage of the multimaster I^{2}C BUS interface. When this bit is set to “0,” the use disable status is provided, so the SDA and the SCL become high-impedance. When the bit is set to “1,” use of the interface is enabled.
When ESO = “0,” the following is performed.

- PIN = “1,” BB = “0” and AL = “0” are set (they are bits of the I^{2}C status register at address 00F8$_{16}$).
- Writing data to the I^{2}C data shift register (address 00F6$_{16}$) is disabled.

(3) Bit 4: Data Format Selection Bit (ALS)

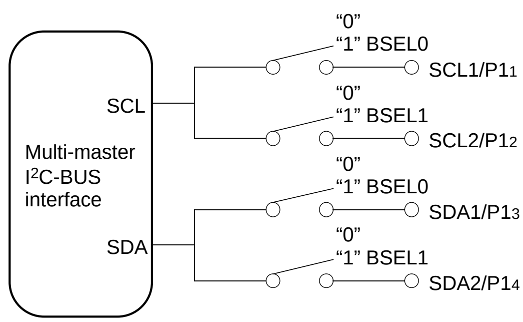
This bit decides whether or not to recognize slave addresses. When this bit is set to “0,” the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to “8.6.5 I^{2}C Status Register,” bit 1) is received, transmission processing can be performed. When this bit is set to “1,” the free data format is selected, so that slave addresses are not recognized.

(4) Bit 5: Addressing Format Selection Bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to “0,” the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I^{2}C address register (address 00F7$_{16}$) are compared with address data. When this bit is set to “1,” the 10-bit addressing format is selected, all the bits of the I^{2}C address register are compared with address data.

(5) Bits 6 and 7:Connection Control Bits between I^{2}C-BUS Interface and Ports (BSEL0, BSEL1)

These bits controls the connection between SCL and ports or SDA and ports (refer to Figure 8.6.5).



Note: When using multi-master I^{2}C-BUS interface, set bits 3 and 4 of the serial I/O mode register (address 0213$_{16}$) to “1.” Moreover, set the corresponding direction register to “1” to use the port as multi-master I^{2}C-BUS interface.

Fig. 8.6.5 Connection Port Control by BSEL0 and BSEL1

I²C Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I²C control register (S1D) [Address 00F9₁₆]

B	Name	Functions	After reset	R W
0 to 2	Bit counter (Number of transmit/recieve bits) (BC0 to BC2)	b2 b1 b0 0 0 0: 8 0 0 1: 7 0 1 0: 6 0 1 1: 5 1 0 0: 4 1 0 1: 3 1 1 0: 2 1 1 1: 1	0	R W
3	I²C-BUS interface use enable bit (ESO)	0: Disabled 1: Enabled	0	R W
4	Data format selection bit (ALS)	0: Addressing format 1: Free data format	0	R W
5	Addressing format selection bit (10BIT SAD)	0: 7-bit addressing format 1: 10-bit addressing format	0	R W
6, 7	Connection control bits between I²C-BUS interface and ports (BSEL0, BSEL1)	b7 b6 Connection port (See note) 0 0: None 0 1: SCL1, SDA1 1 0: SCL2, SDA2 1 1: SCL1, SDA1, SCL2, SDA2	0	R W

Fig. 8.6.6 I²C Control Register

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8.6.5 I²C Status Register

The I²C status register (address $00F8_{16}$) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

(1) Bit 0: Last Receive Bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address $00F6_{16}$).

(2) Bit 1: General Call Detecting Flag (AD0)

This bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition.

*General call: The master transmits the general call address "00_{16}" to all slaves.

(3) Bit 2: Slave Address Comparison Flag (AAS)

This flag indicates a comparison result of address data.

- ■ In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions.
  - The address data immediately after occurrence of a START condition matches the slave address stored in the high-order 7 bits of the I²C address register (address $00F7_{16}$).
  - A general call is received.
- ■ In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition.
  - When the address data is compared with the I²C address register (8 bits consists of slave address and RBW), the first bytes match.
- ■ The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address $00F6_{16}$).

(4) Bit 3: Arbitration Lost* detecting flag (AL)

In the master transmission mode, when a device other than the microcomputer sets the SDA to "L,", arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to receive and recognize its own slave address transmitted by another master device.

*Arbitration lost: The status in which communication as a master is disabled.

(5) Bit 4: I²C-BUS Interface Interrupt Request Bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the state of the PIN bit changes from "1" to "0." At the same time, an interrupt request signal is sent to the CPU. The PIN bit is set to "0" in synchronization with a falling edge of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling edge of the PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 8.6.8 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in any one of the following conditions.

- Executing a write instruction to the I²C data shift register (address $00F6_{16}$).
- When the ESO bit is "0"
- At reset

The conditions in which the PIN bit is set to "0" are shown below:

- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

(6) Bit 5: Bus Busy Flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. When this bit is set to "1," this bus system is busy and the occurrence of a START condition is disabled by the START condition duplication prevention function (Note).

This flag can be written by software only in the master transmission mode. In the other modes, this bit is set to "1" by detecting a START condition and set to "0" by detecting a STOP condition. When the ESO bit of the I²C control register (address $00F9_{16}$) is "0" and at reset, the BB flag is kept in the "0" state.

(7) Bit 6: Communication Mode Specification Bit (transfer direction specification bit: TRX)

This bit decides the direction of transfer for data communication. When this bit is "0," the reception mode is selected and the data of a transmitting device is received. When the bit is "1," the transmission mode is selected and address data and control data are output into the SDA in synchronization with the clock generated on the SCL.

When the ALS bit of the I²C control register (address $00F9_{16}$) is "0" in the slave reception mode is selected, the TRX bit is set to "1" (transmit) if the least significant bit (R/$\overline{W}$ bit) of the address data transmitted by the master is "1." When the ALS bit is "0" and the R/$\overline{W}$ bit is "0," the TRX bit is cleared to "0" (receive).

The TRX bit is cleared to "0" in one of the following conditions.

- When arbitration lost is detected.
- When a STOP condition is detected.
- When occurence of a START condition is disabled by the START condition duplication prevention function (Note).
- With MST = "0" and when a START condition is detected.
- With MST = "0" and when ACK non-return is detected.
- At reset

(8) Bit 7: Communication Mode Specification Bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is "0," the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is "1," the master is specified and a START condition and a STOP condition are generated, and also the clocks required for data communication are generated on the SCL.

The MST bit is cleared to "0" in one of the following conditions.

- Immediately after completion of 1-byte data transmission when arbitration lost is detected
- When a STOP condition is detected.
- When occurence of a START condition is disabled by the START condition duplication preventing function (Note).
- At reset

Note: The START condition duplication prevention function disables the START condition generation, reset of bit counter reset, and SCL output, when the following condition is satisfied:
a START condition is set by another master device.

I^2C Status Register

b7 b6 b5 b4 b3 b2 b1 b0

I^2C status register (S1) [Address $00F8_{16}$]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0" 1 : Last bit = "1" (See note)	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected (See note)	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address mismatch 1 : Address match (See note)	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected (See note)	0	R	—
4	I^2C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	1	R	W
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave recieve mode 0 1 : Slave transmit mode 1 0 : Master recieve mode 1 1 : Master transmit mode	0	R	W

Note : These bits and flags can be read out, but cannnot be written.

Fig. 8.6.7 I^2C Status Register

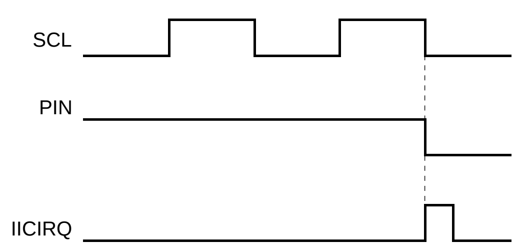

Fig. 8.6.8 Interrupt Request Signal Generation Timing

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8.6.6 START Condition Generation Method

When the ESO bit of the I2C control register (address 00F916) is "1," execute a write instruction to the I2C status register (address 00F816) to set the MST, TRX and BB bits to "1." A START condition will then be generated. After that, the bit counter becomes "0002" and an SCL for 1 byte is output. The START condition generation timing and BB bit set timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 8.6.9 for the START condition generation timing diagram, and Table 8.6.2 for the START condition/STOP condition generation timing table.

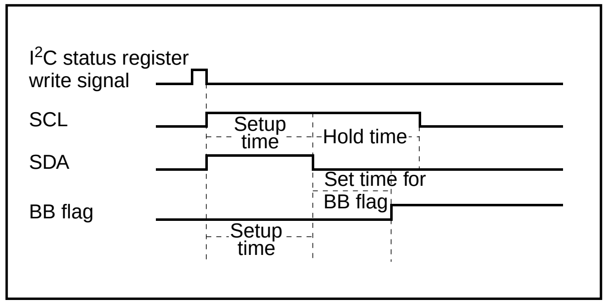

Fig. 8.6.9 START Condition Generation Timing Diagram

8.6.7 STOP Condition Generation Method

When the ESO bit of the I2C control register (address 00F916) is "1," execute a write instruction to the I2C status register (address 00F816) for setting the MST bit and the TRX bit to "1" and the BB bit to "0". A STOP condition will then be generated. The STOP condition generation timing and the BB flag reset timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 8.6.10 for the STOP condition generation timing diagram, and Table 8.6.2 for the START condition/STOP condition generation timing table.

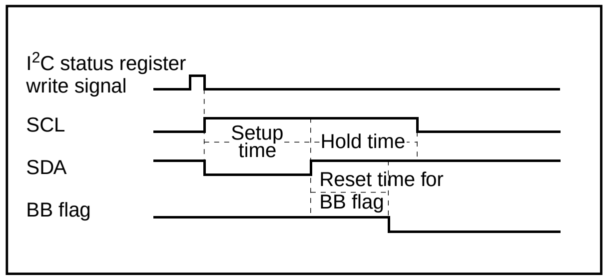

Fig. 8.6.10 STOP Condition Generation Timing Diagram

Table 8.6.2 START Condition/STOP Condition Generation Timing Table

Item	Standard Clock Mode	High-speed Clock Mode
Setup time	4.25 µs (17 cycles)	1.75 µs (7 cycles)
Hold time	5.0 µs (20 cycles)	2.5 µs (10 cycles)
Set/reset time for BB flag	3.0 µs (12 cycles)	1.5 µs (6 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

8.6.8 START/STOP Condition Detect Conditions

The START/STOP condition detect conditions are shown in Figure 8.6.11 and Table 8.6.3. Only when the 3 conditions of Table 8.6.3 are satisfied, a START/STOP condition can be detected.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "IICIRQ" is generated to the CPU.

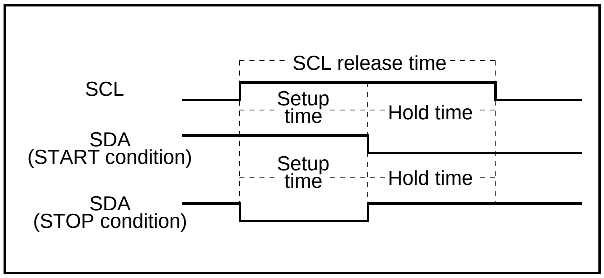

Fig. 8.6.11 START Condition/STOP Condition Detect Timing Diagram

Table 8.6.3 START Condition/STOP Condition Detect Conditions

Standard Clock Mode	High-speed Clock Mode
6.5 µs (26 cycles) < SCL release time	1.0 µs (4 cycles) < SCL release time
3.25 µs (13 cycles) < Setup time	0.5 µs (2 cycles) < Setup time
3.25 µs (13 cycles) < Hold time	0.5 µs (2 cycles) < Hold time

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

8.6.9 Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats is described below.

(1) 7-bit Addressing Format

To meet the 7-bit addressing format, set the 10BIT SAD bit of the I^{2}C control register (address $00F9_{16}$) to "0." The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I^{2}C address register (address $00F7_{16}$). At the time of this comparison, address comparison of the RBW bit of the I^{2}C address register (address $00F7_{16}$) is not made. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 8.6.12, (1) and (2).

(2) 10-bit Addressing Format

To meet the 10-bit addressing format, set the 10BIT SAD bit of the I^{2}C control register (address $00F9_{16}$) to "1." An address comparison is made between the first-byte address data transmitted from the master and the 7-bit slave address stored in the I^{2}C address register (address $00F7_{16}$). At the time of this comparison, an address comparison between the RBW bit of the I^{2}C address register (address $00F7_{16}$) and the R/$\overline{W}$ bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the R/$\overline{W}$ bit which is the last bit of the address data not only specifies the direction of communication for control data but also is processed as an address data bit.
When the first-byte address data matches the slave address, the AAS bit of the I^{2}C status register (address $00F8_{16}$) is set to "1." After the second-byte address data is stored into the I^{2}C data shift register (address $00F6_{16}$), make an address comparison between the second-byte data and the slave address by software. When the address data of the 2nd bytes matches the slave address, set the RBW bit of the I^{2}C address register (address $00F7_{16}$) to "1" by software. This processing can match the 7-bit slave address and R/$\overline{W}$ data, which are received after a RESTART condition is detected, with the value of the I^{2}C address register (address $00F7_{16}$). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 8.6.12, (3) and (4).

8.6.10 Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

① Set a slave address in the high-order 7 bits of the I^2C address register (address $00F7_{16}$) and "0" in the RBW bit.
② Set the ACK return mode and SCL = 100 kHz by setting "85_{16}" in the I^2C clock control register (address $00FA_{16}$).
③ Set "10_{16}" in the I^2C status register (address $00F8_{16}$) and hold the SCL at the HIGH.
④ Set a communication enable status by setting "48_{16}" in the I^2C control register (address $00F9_{16}$).
⑤ Set the address data of the destination of transmission in the high-order 7 bits of the I^2C data shift register (address $00F6_{16}$) and set "0" in the least significant bit.
⑥ Set "$F0_{16}$" in the I^2C status register (address $00F8_{16}$) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occurs.
⑦ Set transmit data in the I^2C data shift register (address $00F6_{16}$). At this time, an SCL and an ACK clock automatically occurs.
⑧ When transmitting control data of more than 1 byte, repeat step ⑦.
⑨ Set "$D0_{16}$" in the I^2C status register (address $00F8_{16}$). After this, if ACK is not returned or transmission ends, a STOP condition will be generated.

8.6.11 Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode, using the addressing format, is shown below.

① Set a slave address in the high-order 7 bits of the I^2C address register (address $00F7_{16}$) and "0" in the RBW bit.
② Set the no ACK clock mode and SCL = 400 kHz by setting "25_{16}" in the I^2C clock control register (address $00FA_{16}$).
③ Set "10_{16}" in the I^2C status register (address $00F8_{16}$) and hold the SCL at the HIGH.
④ Set a communication enable status by setting "48_{16}" in the I^2C control register (address $00F9_{16}$).
⑤ When a START condition is received, an address comparison is made.
⑥ •When all transmitted address are"0" (general call):
  AD0 of the I^2C status register (address $00F8_{16}$) is set to "1"and an interrupt request signal occurs.
  •When the transmitted addresses match the address set in ①:
  ASS of the I^2C status register (address $00F8_{16}$) is set to "1" and an interrupt request signal occurs.
  •In the cases other than the above:
  AD0 and AAS of the I^2C status register (address $00F8_{16}$) are set to "0" and no interrupt request signal occurs.
⑦ Set dummy data in the I^2C data shift register (address $00F6_{16}$).
⑧ When receiving control data of more than 1 byte, repeat step ⑦.
⑨ When a STOP condition is detected, the communication ends.

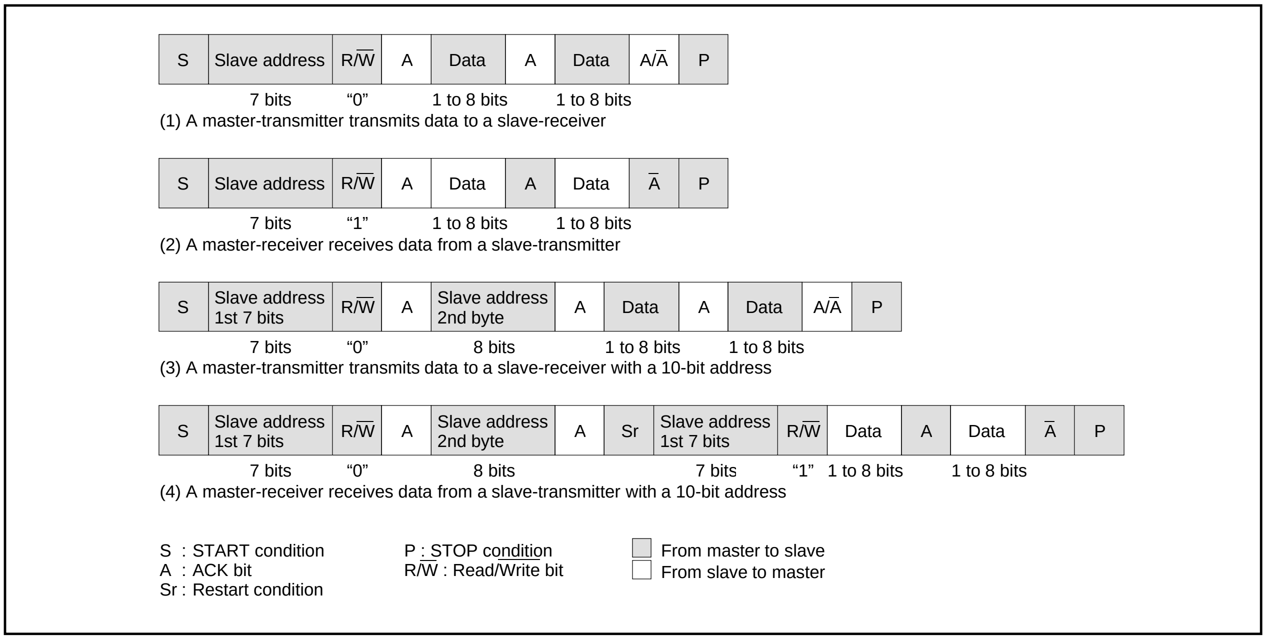

Fig. 8.6.12 Address Data Communication Format

8.6.12 Precautions when using multi-master I²C-BUS interface

(1) Read-modify-write instruction

The precautions when the read-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I²C-BUS interface are described below.

•I²C data shift register (S0)
When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.

•I²C address register (S0D)
When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because hardware changes the read/write bit (RBW) at the above timing.

•I²C status register (S1)
Do not execute the read-modify-write instruction for this register because all bits of this register are changed by hardware.

•I²C control register (S1D)
When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because hardware changes the bit counter (BC0–BC2) at the above timing.

•I²C clock control register (S2)
The read-modify-write instruction can be executed for this register.

(2) START condition generating procedure using multi-master

①Procedure example (The necessary conditions of the generating procedure are described as the following ② to ⑤).

```
                •
                •
        LDA     —               (Taking out of slave address value)
        SEI                     (Interrupt disabled)
        BBS  5,S1,BUSBUSY       (BB flag confirming and branch process)
BUSFREE:
        STA  S0                 (Writing of slave address value)
        LDM  #$F0, S1           (Trigger of START condition generating)
        CLI                     (Interrupt enabled)
                •
                •
BUSBUSY:
        CLI                     (Interrupt enabled)
                •
                •
```

②Use "STA," "STX" or "STY" of the zero page addressing instruction for writing the slave address value to the I²C data shift register.

③Use "LDM" instruction for setting trigger of START condition generating.

④Write the slave address value of above ② and set trigger of START condition generating of above ③ continuously shown the above procedure example.

⑤Disable interrupts during the following three process steps:
• BB flag confirming
• Writing of slave address value
• Trigger of START condition generating
When the condition of the BB flag is bus busy, enable interrupts immediately.

(3) RESTART condition generating procedure

①Procedure example (The necessary conditions of the generating procedure are described as the following ② to ⑥.)

Execute the following procedure when the PIN bit is "0."

```
              •
              •
LDM   #$00, S1      (Select slave receive mode)
LDA   —             (Taking out of slave address value)
SEI                 (Interrupt disabled)
STA   S0            (Writing of slave address value)
LDM   #$F0, S1      (Trigger of RESTART condition generating)
CLI                 (Interrupt enabled)
              •
              •
```

②Select the slave receive mode when the PIN bit is "0." Do not write "1" to the PIN bit. Neither "0" nor "1" is specified for the writing to the BB bit.
The TRX bit becomes "0" and the SDA pin is released.

③The SCL pin is released by writing the slave address value to the I^{2}C data shift register. Use "STA," "STX" or "STY" of the zero page addressing instruction for writing.

④Use "LDM" instruction for setting trigger of RESTART condition generating.

⑤Write the slave address value of above ③ and set trigger of RESTART condition generating of above ④ continuously shown the above procedure example.

⑥Disable interrupts during the following two process steps:
- Writing of slave address value
- Trigger of RESTART condition generating

(4) STOP condition generating procedure

①Procedure example (The necessary conditions of the generating procedure are described as the following ② to ④.)

```
              •
              •
SEI                 (Interrupt disabled)
LDM   #$C0, S1      (Select master transmit mode)
NOP                 (Set NOP)
LDM   #$D0, S1      (Trigger of STOP condition generating)
CLI                 (Interrupt enabled)
              •
              •
```

②Write "0" to the PIN bit when master transmit mode is select.

③Execute "NOP" instruction after setting of master transmit mode. Also, set trigger of STOP condition generating within 10 cycles after selecting of master trasmit mode.

④Disable interrupts during the following two process steps:
- Select of master transmit mode
- Trigger of STOP condition generating

(5) Writing to I^{2}C status register

Do not execute an instruction to set the PIN bit to "1" from "0" and an instruction to set the MST and TRX bits to "0" from "1" simultaneously. It is because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to "0" from "1" simultaneously when the PIN bit is "1." It is because it may become the same as above.

(6) Process of after STOP condition generating

Do not write data in the I^{2}C data shift register S0 and the I^{2}C status register S1 until the bus busy flag BB becomes "0" after generating the STOP condition in the master mode. It is because the STOP condition waveform might not be normally generated. Reading to the above registers do not have the problem.

8.7 PWM OUTPUT CIRCUIT

This microcomputer is equipped with eight 8-bit PWMs (PWM0–PWM7). PWM0–PWM7 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of 4 µs and repeat period of 1024 µs (for $f(X_{IN})$ = 8 MHz) .

Figure 8.7.1 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to PWM0–PWM7 using $f(X_{IN})$ divided by 2 as a reference signal.

8.7.1 Data Setting

When outputting PWM0–PWM7, set 8-bit output data to the PWMi register (i means 0 to 7; addresses 0200_{16} to 0207_{16}).

8.7.2 Transmitting Data from Register to PWM circuit

Data transfer from the PWM register to the PWM circuit is executed at writing data to the register.

The signal output from the PWM output pin corresponds to the contents of this register.

8.7.3 PWM Operation

The following explains PWM operation.

First, set the bit 0 of PWM mode register 1 (address $020A_{16}$) to “0” (at reset, bit 0 is already set to “0” automatically), so that the PWM count source is supplied.

PWM0–PWM3 are also used as pins $P0_4$–$P0_7$, PWM4–PWM6 are also used as pins $P0_0$–$P0_2$, and PWM7 is also used as pin $P0_3$ respectively. Set the corresponding bits of the port P0 direction register to “1” (output mode). And select each output polarity by bit 3 of PWM mode register 1 (address $020A_{16}$). Then, set bits 7 to 0 of PWM mode register 2 to “1” (PWM output).

The PWM waveform is output from the PWM output pins by setting these registers.

Figure 8.7.2 shows the PWM timing. One cycle (T) is composed of 256 (2^8) segments. The 8 kinds of pulses, relative to the weight of each bit (bits 0 to 7), are output inside the circuit during 1 cycle. Refer to Figure 8.7.2 (a). The PWM outputs waveform which is the logical sum (OR) of pulses corresponding to the contents of bits 0 to 7 of the PWM register. Several examples are shown in Figure 8.7.2 (b). 256 kinds of output (HIGH area: 0/256 to 255/256) are selected by changing the contents of the PWM register. A length of entirely HIGH cannot be output, i.e. 256/256.

8.7.4 Output after Reset

At reset, the output of port P0 is in the high-impedance state, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

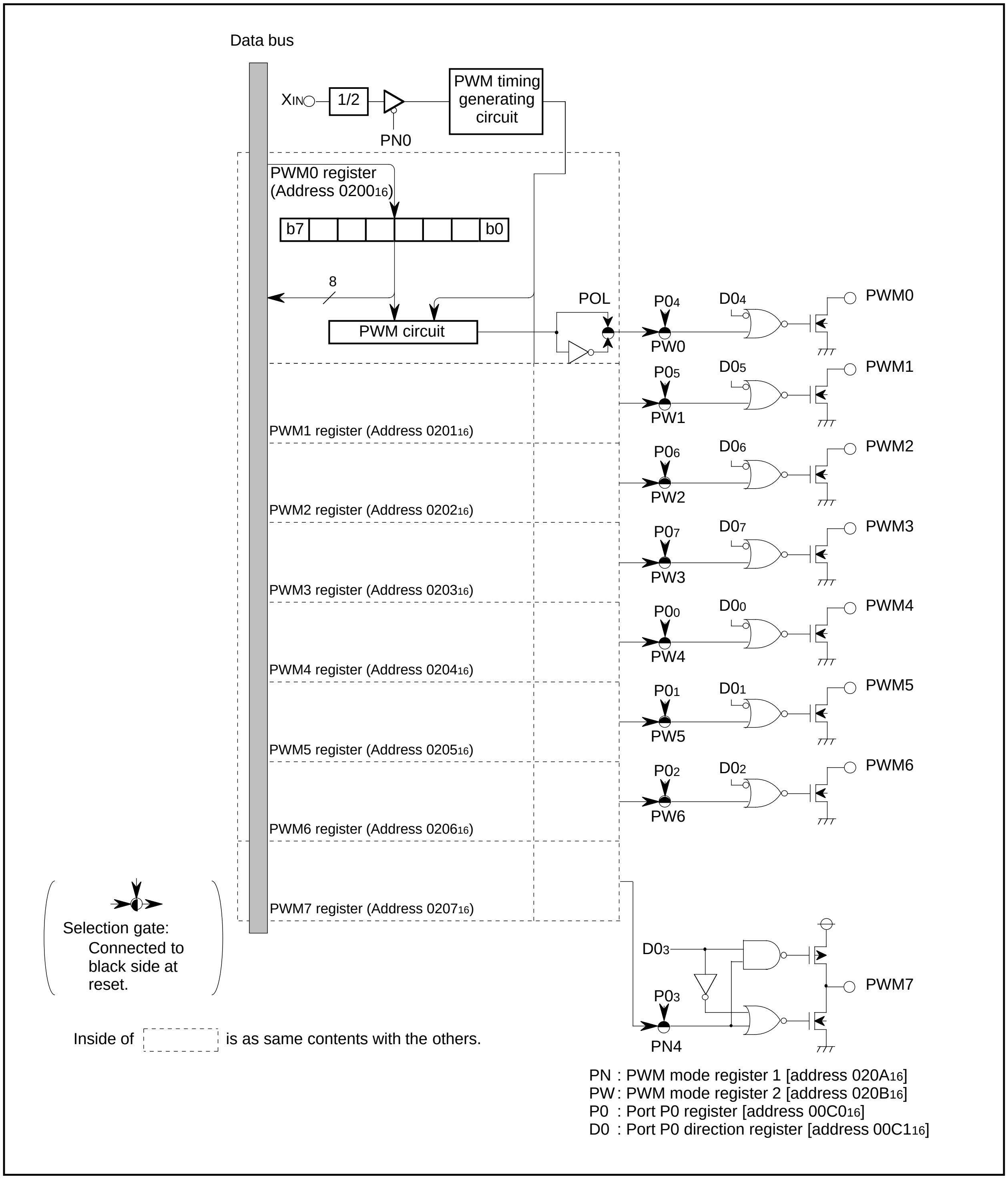

Fig. 8.7.1 PWM Block Diagram

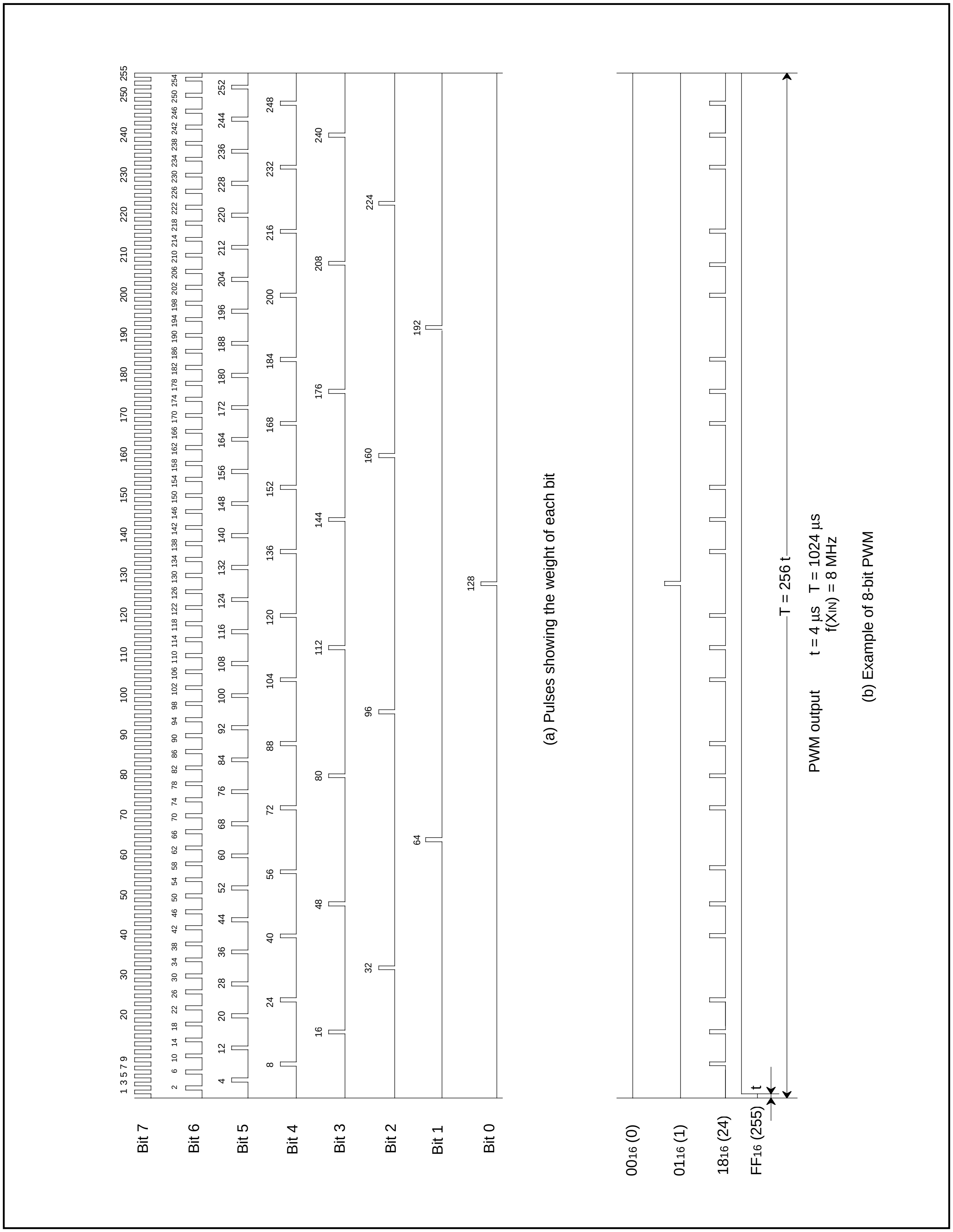

Fig. 8.7.2 PWM Timing

PWM Mode Register 1

b7 b6 b5 b4 b3 b2 b1 b0

PWM mode register 1 (PN) [Address 020A16]

B	Name	Functions	After reset	R	W
0	PWM counts source selection bit (PN0)	0 : Count source supply 1 : Count source stop	0	R	W
1, 2	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
3	PWM output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	P03/PWM7 output selection bit (PN4)	0 : P03 output 1 : PWM7 output	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out. the values are “0.”		0	R	—

Fig. 8.7.3 PWM Mode Register 1

PWM Mode Register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

PWM mode register 2 (PW) [Address 020B16]

B	Name	Functions	After reset	R	W
0	P04/PWM0 output selection bit (PW0)	0 : P04 output 1 : PWM0 output	0	R	W
1	P05/PWM1 output selection bit (PW1)	0 : P05 output 1 : PWM1 output	0	R	W
2	P06/PWM2 output selection bit (PW2)	0 : P06 output 1 : PWM2 output	0	R	W
3	P07/PWM3 output selection bit (PW3)	0 : P07 output 1 : PWM3 output	0	R	W
4	P00/PWM4 output selection bit (PW4)	0 : P00 output 1 : PWM4 output	0	R	W
5	P01/PWM5 output selection bit (PW5)	0: P01 output 1: PWM5 output	0	R	W
6	P02/PWM6 output selection bit (PW6)	0: P02 output 1: PWM6 output	0	R	W
7	Fix this bit to “0.”		0	R	W

Fig. 8.7.4 PWM Mode Register 2

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8.8 A-D CONVERTER

8.8.1 A-D Conversion Register (AD)

A-D conversion reigister is a read-only register that stores the result of an A-D conversion. This register should not be read during A-D conversion.

8.8.2 A-D Control Register (ADCON)

The A-D control register controls A-D conversion. Bits 2 to 0 of this register select analog input pins. When these pins are not used as analog input pins, they are used as ordinary I/O pins. Bit 3 is the A-D conversion completion bit, A-D conversion is started by writing “0” to this bit. The value of this bit remains at “0” during an A-D conversion, then changes to “1” when the A-D conversion is completed.
Bit 4 controls connection between the resistor ladder and VCC. When not using the A-D converter, the resistor ladder can be cut off from the internal VCC by setting this bit to “0,” accordingly providing low-power dissipation.

8.8.3 Comparison Voltage Generator (Resistor Ladder)

The voltage generator divides the voltage between VSS and VCC by 256, and outputs the divided voltages to the comparator as the reference voltage Vref.

8.8.4 Channel Selector

The channel selector connects an analog input pin, selected by bits 2 to 0 of the A-D control register, to the comparator.

8.8.5 Comparator and Control Circuit

The conversion result of the analog input voltage and the reference voltage “Vref” is stored in the A-D conversion register. The A-D conversion completion bit and A-D conversion interrupt request bit are set to “1” at the completion of A-D conversion.

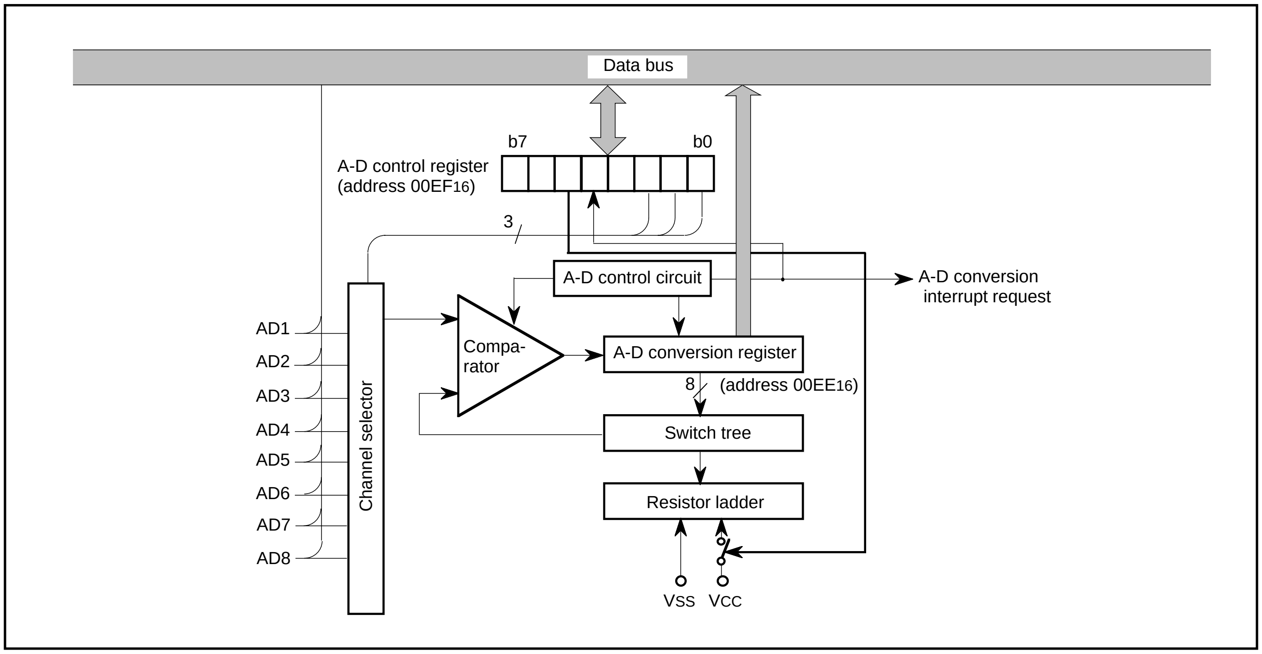

Fig. 8.8.1 A-D Comparator Block Diagram

A-D Control Register

b7	b6	b5	b4	b3	b2	b1	b0
0		0					

A-D control register (ADCON) [Address 00EF16]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADIN0 to ADIN2)	b2 b1 b0 0 0 0 : AD1 0 0 1 : AD2 0 1 0 : AD3 0 1 1 : AD4 1 0 0 : AD5 1 0 1 : AD6 1 1 0 : AD7 1 1 1 : AD8	0	R	W
3	A-D conversion completion bit (ADSTR)	0: Conversion in progress 1: Convertion completed	1	R	W
4	VCC connection selection bit (ADVREF)	0: OFF 1: ON	0	R	W
5	Fix this bit to “0.”		0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—
7	Fix this bit to “0.”		0	R	W

Fig. 8.8.2 A-D Control Register

8.8.6 Conversion Method

① Set bit 7 of the interrupt input polarity register (address 0212_{16}) to "1" to generate an interrupt request at completion of A-D conversion.

② Set the A-D conversion · INT3 interrupt request bit to "0" (even when A-D conversion is started, the A-D conversion · INT3 interrupt reguest bit is not set to "0" automatically).

③ When using A-D conversion interrupt, enable interrupts by setting A-D conversion · INT3 interrupt request bit to "1" and setting the interrupt disable flag to "0."

④ Set the VCC connection selection bit to "1" to connect VCC to the resistor ladder.

⑤ Select analog input pins by the analog input selection bit of the A-D control register.

⑥ Set the A-D conversion completion bit to "0." This write operation starts the A-D conversion. Do not read the A-D conversion register during the A-D conversion.

⑦ Verify the completion of the conversion by the state ("1") of the A-D conversion completion bit, the state ("1") of A-D conversion · INT3 interrupt reguest bit, or the occurrence of an A-D conversion interrupt.

⑧ Read the A-D conversion register to obtain the conversion results.

Note : When the ladder resistor is disconnect from VCC, set the VCC connection selection bit to "0" between steps ⑦ and ⑧.

8.8.7 Internal Operation

When the A-D conversion starts, the following operations are automatically performed.

① The A-D conversion register is set to "00_{16}."

② The most significant bit of the A-D conversion register becomes "1, " and the comparison voltage "Vref" is input to the comparator. At this point, Vref is compared with the analog input voltage "VIN ."

③ Bit 7 is determined by the comparison results as follows.
When Vref < VIN : bit 7 holds "1"
When Vref > VIN : bit 7 becomes "0"

With the above operations, the analog value is converted into a digital value. The A-D conversion terminates in a maximum of 50 machine cycles (12.5 µs at f(XIN) = 8 MHz) after it starts, and the conversion result is stored in the A-D conversion register.

An A-D conversion interrupt request occurs at the same time as A-D conversion completion, the A-D conversion · INT3 interrupt request bit becomes "1." The A-D conversion completion bit also becomes "1."

Table 8.8.1 Expression for Vref and VREF

A-D conversion register contents "n" (decimal notation)	Vref (V)
0	0
1 to 255	$\frac{V_{REF}}{256} \times (n - 0.5)$

Note: VREF indicates the reference voltage (= Vcc).

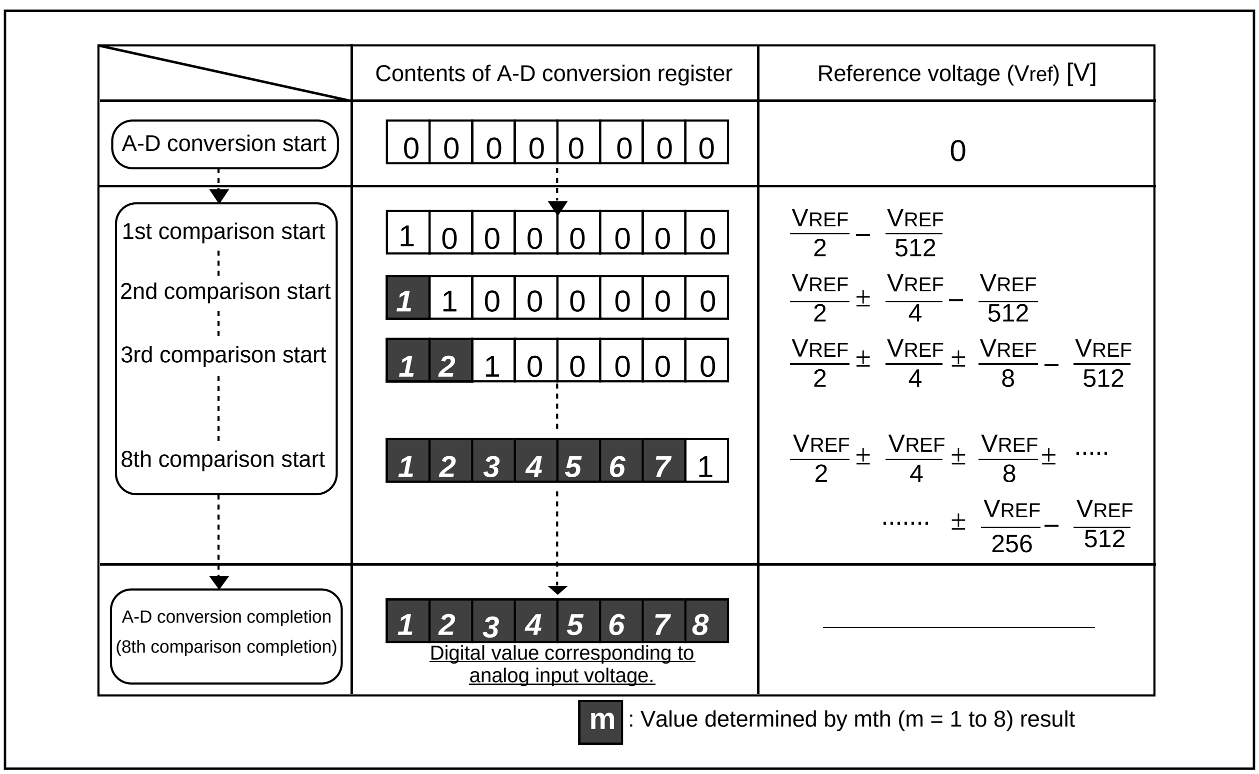

Fig. 8.8.3 Changes in A-D Conversion Register and Comparison Voltage during A-D Conversion

8.8.8 Definition of A-D Conversion Accuracy

The definition of A-D conversion accuracy is described below (refer to Figure 8.8.4).

Accuracy is shown the difference between measurement result output code and output code which is expected for A-D conversion whose specification is ideal by using LSB.

The analog input voltage in accuracy measurement is made to be a middle point of input voltage width (=1 LSB) which outputs the code in which the A-D converter with the ideal characteristics is identical.

For example, 1 LSB's width is 20 mV at V_{REF} = 5.12V.

0 mV, 20 mV, 40 mV and 60 mV are selected for analog input voltage.

A-D conversion accuracy is shown in Fig 8.8.4.

That the output code expected in the ideal A-D converter is "05_{16}" shows that there is actual A-D conversion result with in "03_{16}" to "07_{16}" on the = ±2LSB absolute accuracy, when the analog input voltage is 100 mV.

And, zero error and scale error are contained for the absolute accuracy, and the quantization error is not contained.

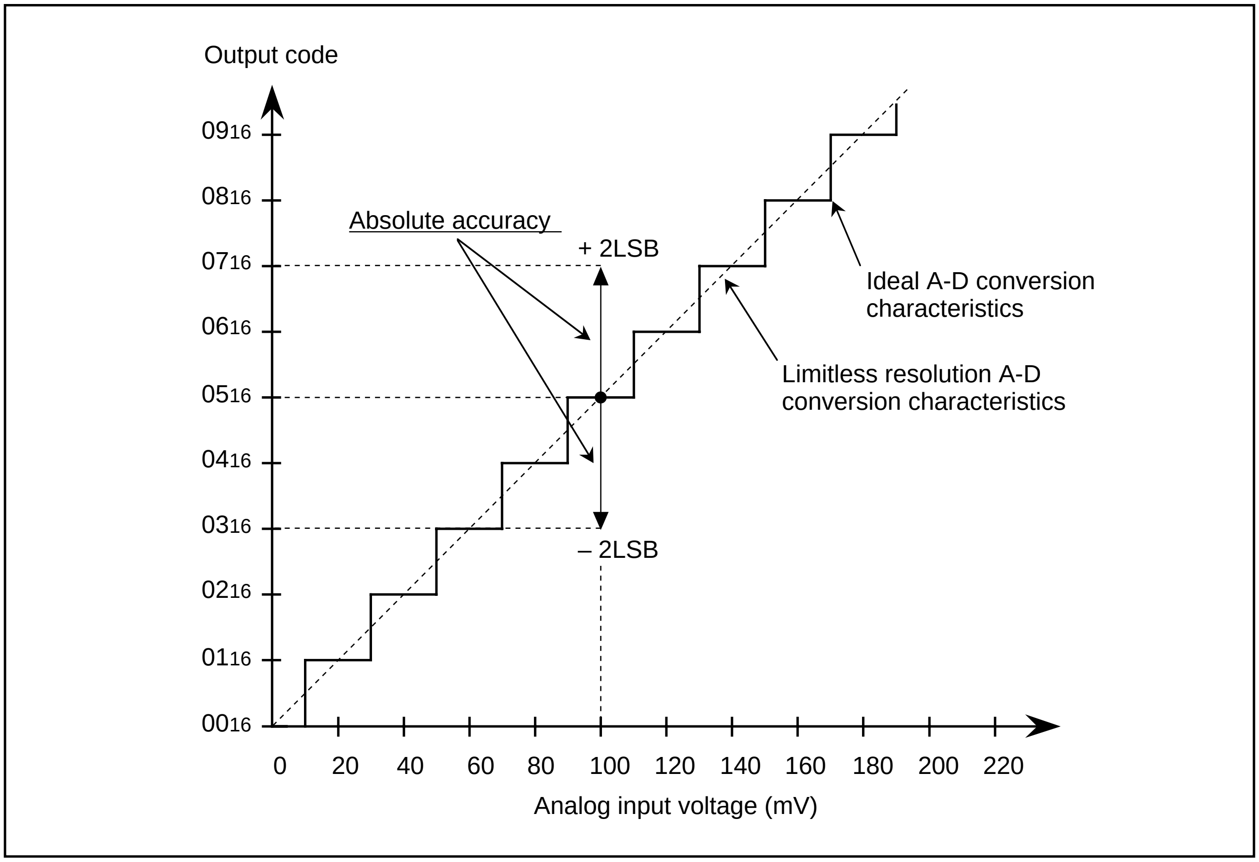

Fig. 8.8.4 Definition of A-D Conversion Accuracy

8.9 ROM CORRECTION FUNCTION

This can correct program data in ROM. Up to 2 addresses can be corrected, a program for correction is stored in the ROM correction vector in RAM as the top address. The ROM correction vectors are 2 vectors.

Vector 1 : address $02C0_{16}$

Vector 2 : address $02E0_{16}$

Set the address of the ROM data to be corrected into the ROM correction address register. When the value of the counter matches the ROM data address in the ROM correction vector as the top address, the main program branches to the correction program stored in the ROM memory for correction. To return from the correction program to the main program, the op code and operand of the JMP instruction (total of 3 bytes) are necessary at the end of the correction program. The ROM correction function is controlled by the ROM correction enable register.

Notes 1: Specify the first address (op code address) of each instruction as the ROM correction address.

2: Use the JMP instruction (total of 3 bytes) to return from the correction program to the main program.

3: Do not set the same ROM correction address to vectors 1 and 2.

4: For the M37281MKH-XXXSP and M37281EKSP, when using the expansion ROM (BK7 = "1"), the ROM correction function do not operate used for addresses 1000_{16} to$1FFF_{16}$. Note that on programming.

ROM correction address 1 (high-order)	$020C_{16}$
ROM correction address 1 (low-order)	$020D_{16}$
ROM correction address 2 (high-order)	$020E_{16}$
ROM correction address 2 (low-order)	$020F_{16}$

Fig. 8.9.1 ROM Correction Address Registers

ROM Correction Enable Register

b7	b6	b5	b4	b3	b2	b1	b0
				0	0		

ROM correction enable register (RCR) [Address 0210_{16}]

B	Name	Functions	After reset	R	W
0	Vector 1 enable bit (RCR0)	0: Disabled 1: Enabled	0	R	W
1	Vector 2 enable bit (RCR1)	0: Disabled 1: Enabled	0	R	W
2, 3	Fix these bits to "0."		0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 8.9.2 ROM Correction Enable Register

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8.10 DATA SLICER

This microcomputer includes the data slicer function for the closed caption decoder (referred to as the CCD). This function takes out the caption data superimposed in the vertical blanking interval of a composite video signal. A composite video signal which makes the sync chip's polarity negative is input to the CV_{IN} pin.

When the data slicer function is not used, the data slicer circuit and the timing signal generating circuit can be cut off by setting bit 0 of the data slicer control register 1 (address $00E0_{16}$) to "0." These settings can realize the low-power dissipation.

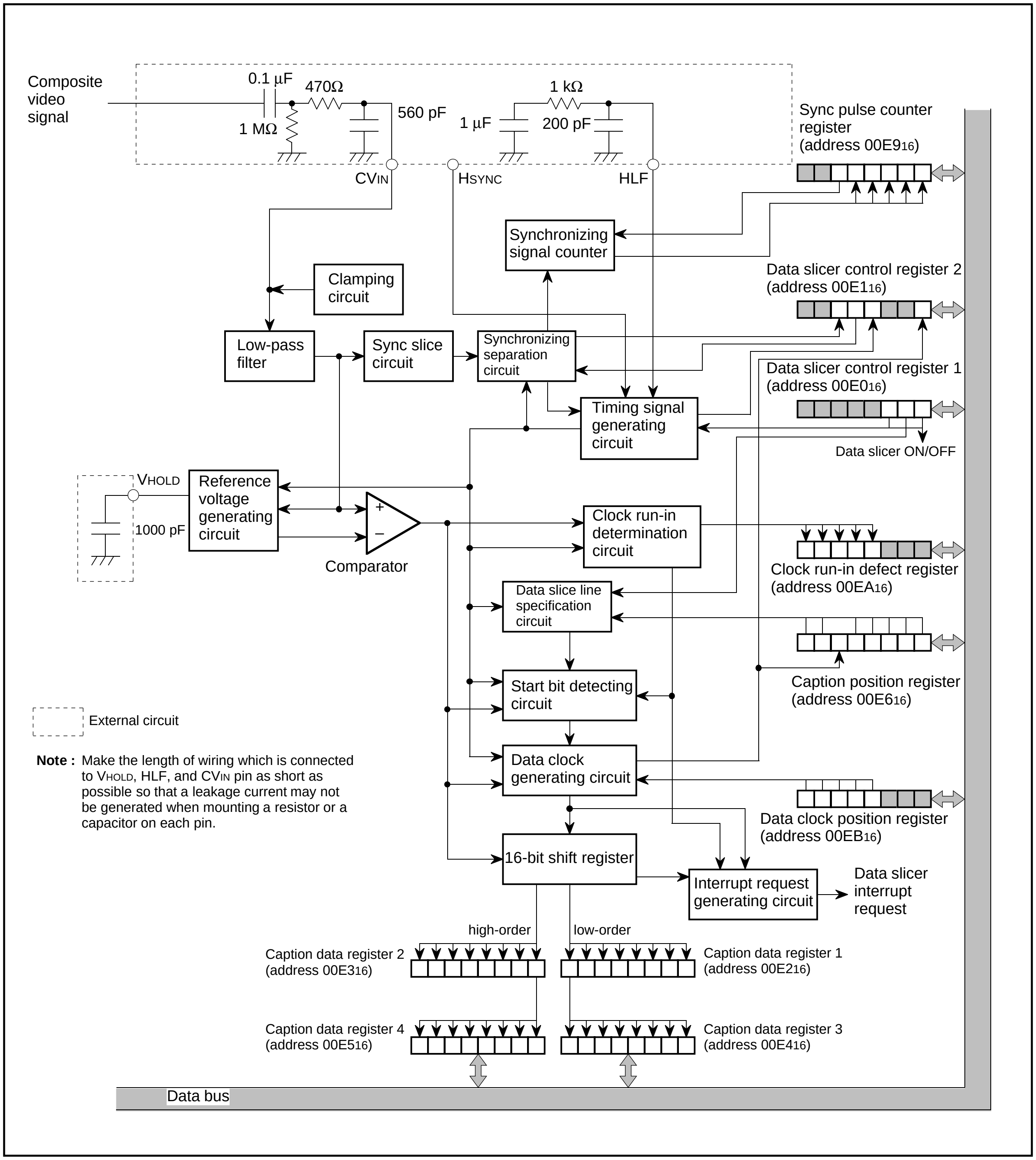


Fig. 8.10.1 Data Slicer Block Diagram

8.10.1 Notes When not Using Data Slicer

When bit 0 of data slicer control register 1 (address $00E0_{16}$) is “0,” terminate the pins as shown in Figure 8.10.2.

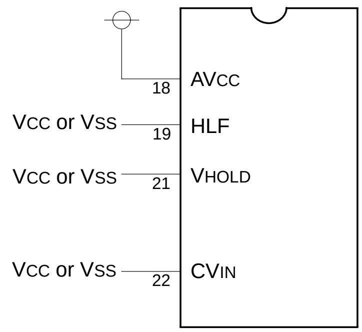
<When data slicer circuit and timing signal generating circuit is in OFF state>

Apply the same voltage as V_{CC} to AV_{CC} pin. (✻)

Apply HLF pin V_{CC} or V_{SS} level.

Apply V_{HOLD} pin V_{CC} or V_{SS} level.

Pull-up CV_{IN} pin to V_{CC} through a resistor of 5 kΩ or more.



(✻) Only M37281EKSP have AVCC pin.
This pin is non-connection pin in M37281MAH-XXXSP, M37281MFH-XXXSP, M37281MKH-XXXSP.
But NC pin of M37281MAH-XXXSP, M37281MFH-XXXSP, M37281MKH-XXXSP is not connect in the IC.
You can apply to Vcc.

Fig. 8.10.2 Termination of Data Slicer Input/Output Pins when Data Slicer Circuit and Timing Generating Circuit Is in OFF State

When both bits 0 and 2 of data slicer control register 1 (address $00E0_{16}$) are “1,” terminate the pins as shown in Figure 8.10.3.

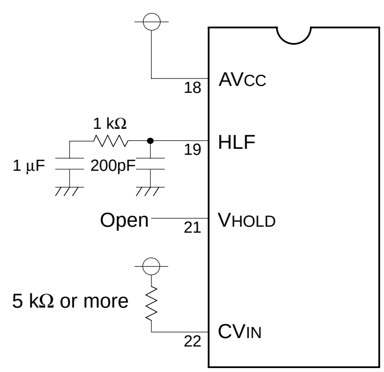
<When using a reference clock generated in timing signal generating circuit as OSD clock>

Apply the same voltage as V_{CC} to AV_{CC} pin. (✻)

Connect the same external circuit as when using data slicer to HLF pin.

Leave V_{HOLD} pin open.

Pull-up CV_{IN} to V_{CC} through a resistor of 5 kΩ or more.



(✻) Only M37281EKSP have AVCC pin.
This pin is non-connection pin in M37281MAH-XXXSP, M37281MFH-XXXSP, M37281MKH-XXXSP.
But NC pin of M37281MAH-XXXSP, M37281MFH-XXXSP, M37281MKH-XXXSP is not connect in the IC.
You can apply to Vcc.

Fig. 8.10.3 Termination of Data Slicer Input/Output Pins when Timing Signal Generating Circuit Is in ON State

Figures 8.10.4 and 8.10.5 the data slicer control registers.

Data Slicer Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0

Data slicer control register 1(DSC1) [Address 00E0$_{16}$]

B	Name	Functions	After reset	R	W
0	Data slicer and timing signal generating circuit control bit (DSC10)	0: Stopped 1: Operating	0	R	W
1	Selection bit of data slice reference voltage generating field (DSC11)	0: F2 1: F1	0	R	W
2	Reference clock source selection bit (DSC12)	0: Video signal 1: HSYNC signal	0	R	W
3 to 7	Fix these bits to “0.”		0	R	W

Definition of fields 1 (F1) and 2 (F2)

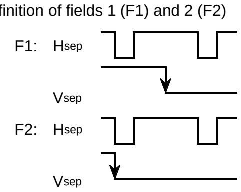


Fig. 8.10.4 Data Slicer Control Register 1

Data Slicer Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0
0 0

Data slicer control register 2 (DSC2) [Address 00E1$_{16}$]

B	Name	Functions	After reset	R	W
0	Caption data latch completion flag 1 (DSC20)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	—
1	Fix this bit to “0.”		0	R	W
2	Test bit	Read-only	Indeterminate	R	—
3	Field determination flag(DSC23)	0: F2 1: F1	Indeterminate	R	—
4	Vertical synchronous signal (V_{sep}) generating method selection bit (DSC24)	0: Method (1) 1: Method (2)	0	R	W
5	V-pulse shape determination flag (DSC25)	0: Match 1: Mismatch	Indeterminate	R	—
6	Fix this bit to “0.”		0	R	W
7	Test bit	Read-only	Indeterminate	R	—

Definition of fields 1 (F1) and 2 (F2)

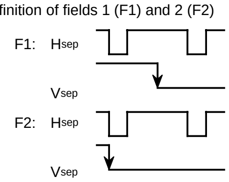


Fig. 8.10.5 Data Slicer Control Register 2

8.10.2 Clamping Circuit and Low-pass Filter

The clamp circuit clamps the sync chip part of the composite video signal input from the CV_{IN} pin. The low-pass filter attenuates the noise of clamped composite video signal. The CV_{IN} pin to which composite video signal is input requires a capacitor (0.1 µF) coupling outside. Pull down the CV_{IN} pin with a resistor of hundreds of kiloohms to 1 MΩ. In addition, we recommend to install externally a simple low-pass filter using a resistor and a capacitor at the CV_{IN} pin (refer to Figure 8.10.1).

8.10.3 Sync Slice Circuit

This circuit takes out a composite sync signal from the output signal of the low-pass filter.

8.10.4 Synchronous Signal Separation Circuit

This circuit separates a horizontal synchronous signal and a vertical synchronous signal from the composite sync signal taken out in the sync slice circuit.

(1)Horizontal Synchronous Signal (H_{sep})

A one-shot horizontal synchronizing signal Hsep is generated at the falling edge of the composite sync signal.

(2)Vertical Synchronous Signal (V_{sep})

As a V_{sep} signal generating method, it is possible to select one of the following 2 methods by using bit 4 of the data slicer control register 2 (address $00E1_{16}$).

- •Method 1 The "L" level width of the composite sync signal is measured. If this width exceeds a certain time, a V_{sep} signal is generated in synchronization with the rising of the timing signal immediately after this "L" level.
- •Method 2 The "L" level width of the composite sync signal is measured. If this width exceeds a certain time, it is detected whether a falling of the composite sync signal exits or not in the "L" level period of the timing signal immediately after this "L" level. If a falling exists, a V_{sep} signal is generated in synchronization with the rising of the timing signal (refer to Figure 8.10.6).

Figure 8.10.6 shows a V_{sep} generating timing. The timing signal shown in the figure is generated from the reference clock which the timing generating circuit outputs.

Reading bit 5 of data slicer control register 2 permits determinating the shape of the V-pulse portion of the composite sync signal. As shown in Figure 8.10.7, when the A level matches the B level, this bit is "0." In the case of a mismatch, the bit is "1."

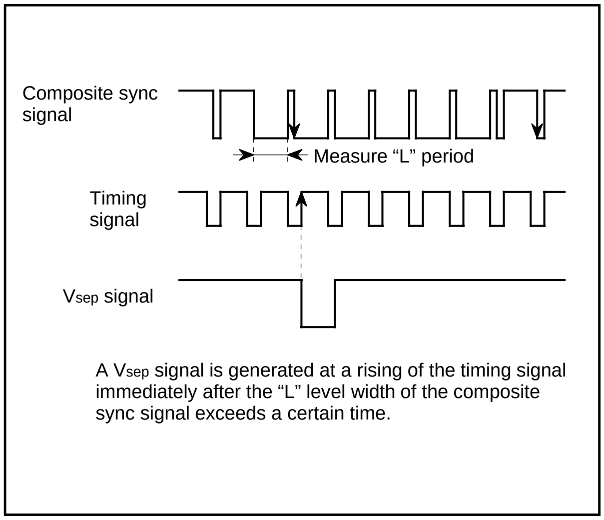


Fig. 8.10.6 Vsep Generating Timing (method 2)

8.10.5 Timing Signal Generating Circuit

This circuit generates a reference clock which is 832 times as large as the horizontal synchronous signal frequency. It also generates various timing signals on the basis of the reference clock, horizontal synchronous signal and vertical synchronizing signal. The circuit operates by setting bit 0 of data slicer control register 1 (address $00E0_{16}$) to "1."

The reference clock can be used as a display clock for OSD function in addition to the data slicer. The HSYNC signal can be used as a count source instead of the composite sync signal. However, when the HSYNC signal is selected, the data slicer cannot be used. A count source of the reference clock can be selected by bit 2 of data slicer control register 1 (address $00E0_{16}$).

For the pins HLF, connect a resistor and a capacitor as shown in Figure 8.10.1. Make the length of wiring which is connected to these pins as short as possible so that a leakage current may not be generated.

Note: It takes a few tens of milliseconds until the reference clock becomes stable after the data slicer and the timing signal generating circuit are started. In this period, various timing signals, H_{sep} signals and V_{sep} signals become unstable. For this reason, take stabilization time into consideration when programming.

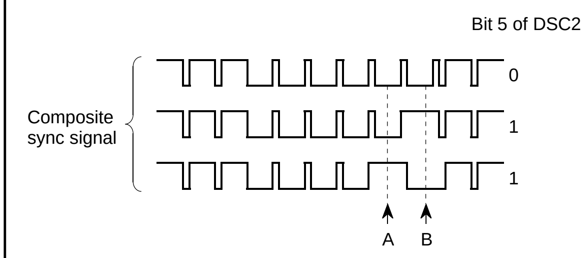


Fig. 8.10.7 Determination of V-pulse Waveform

8.10.6 Data Slice Line Specification Circuit

(1) Specification of Data Slice Line

This circuit decides a line on which caption data is superimposed. The line 21 (fixed), 1 appropriate line for a period of 1 field (total 2 line for a period of 1 field), and both fields (F1 and F2) are sliced their data. The caption position register (address $00E6_{16}$) is used for each setting (refer to Table 8.10.1).

The counter is reset at the falling edge of V_{sep} and is incremented by 1 every H_{sep} pulse. When the counter value matched the value specified by bits 4 to 0 of the caption position register, this H_{sep} is sliced.

The values of "00_{16}" to "$1F_{16}$" can be set in the caption position register (at setting only 1 appropriate line). Figure 8.10.8 shows the signals in the vertical blanking interval. Figure 8.10.9 shows the structure of the caption position register.

(2) Specification of Line to Set Slice Voltage

The reference voltage for slicing (slice voltage) is generated for the clock run-in pulse in the particular line (refer to Table 8.10.1). The field to generate slice voltage is specified by bit 1 of data slicer control register 1. The line to generate slice voltage 1 field is specified by bits 6, 7 of the caption position register (refer to Table 8.10.1).

(3) Field Determination

The field determination flag can be read out by bit 3 of data slicer control register 2. This flag charge at the falling edge of V_{sep}.

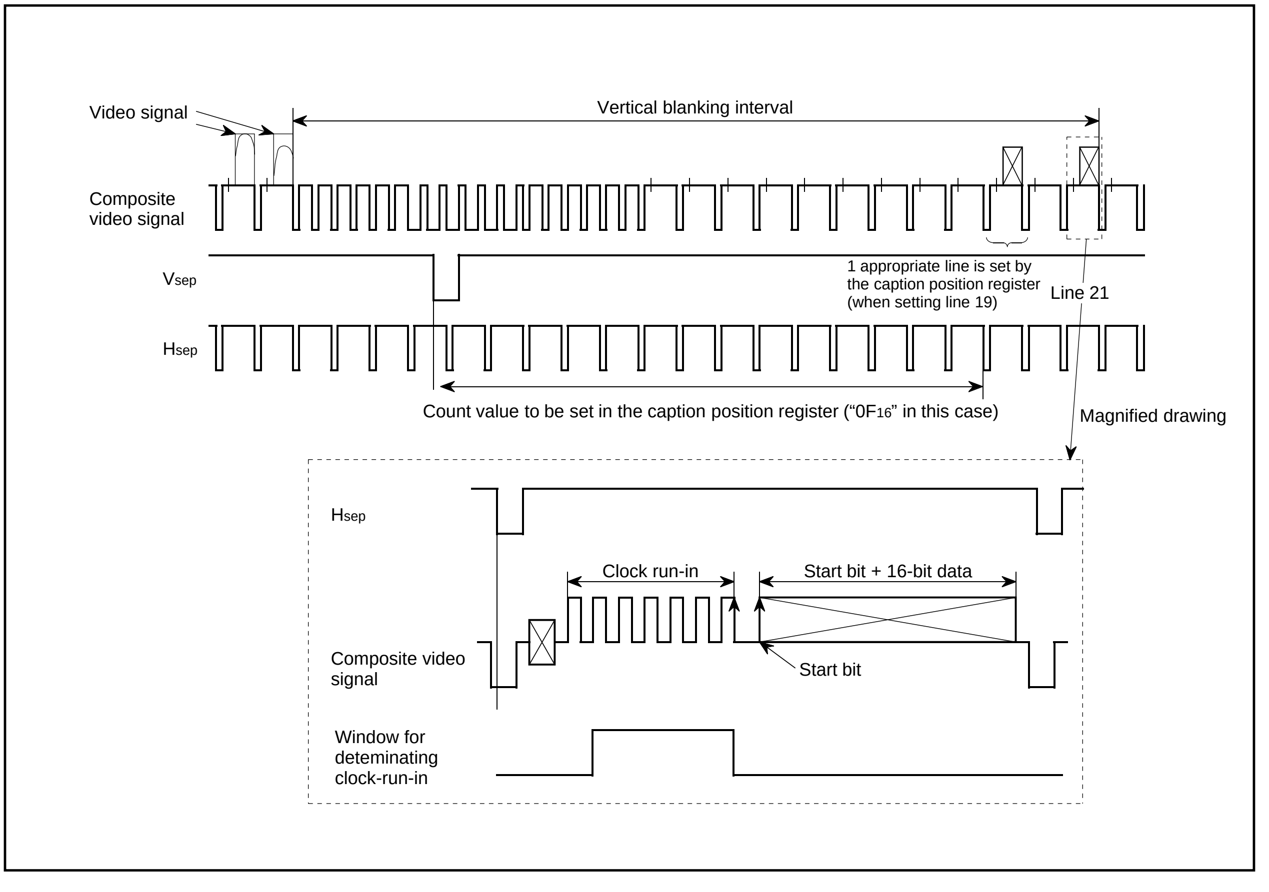
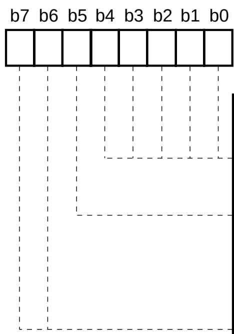


Fig. 8.10.8 Signals in Vertical Blanking Interval

Caption Position Register



Caption Position Register (CPS) [Address $00E6_{16}$]

B	Name	Functions	After reset	R	W
0 to 4	Caption position bits(CPS0 to CPS4)		0	R	W
5	Caption data latch completion flag 2 (CPS5)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	—
6, 7	Slice line mode specification bits (in 1 field) (CPS6, CPS7)	Refer to the corresponding Table (Table 8.10.1).	0	R	W

Fig. 8.10.9 Caption Position Register

Table 8.10.1 Specification of Data Slice Line

CPS		Field and Line to Be Sliced Data	Field and Line to Generate Slice Voltage
b7	b6		
0	0	• Both fields of F1 and F2 • Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2)	• Field specified by bit 1 of DSC1 • Line 21 (total 1 line)
0	1	• Both fields of F1 and F2 • A line specified by bits 4 to 0 of CPS (total 1 line) (See note 3)	• Field specified by bit 1 of DSC1 • A line specified by bits 4 to 0 of CPS (total 1 line) (See note 3)
1	0	• Both fields of F1 and F2 • Line 21 (total 1 line)	• Field specified by bit 1 of DSC1 • Line 21 (total 1 line)
1	1	• Both fields of F1 and F2 • Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2)	• Field specified by bit 1 of DSC1 • Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2)

Notes 1: DSC1 is data slicer control register 1.
CPS is caption position register.
2: Set "00_{16}" to "10_{16}" to bits 4 to 0 of CPS.
3: Set "00_{16}" to "$1F_{16}$" to bits 4 to 0 of CPS.

8.10.7 Reference Voltage Generating Circuit and Comparator

The composite video signal clamped by the clamping circuit is input to the reference voltage generating circuit and the comparator.

(1) Reference Voltage Generating Circuit

This circuit generates a reference voltage (slice voltage) by using the amplitude of the clock run-in pulse in line specified by the data slice line specification circuit. Connect a capacitor between the VHOLD pin and the VSS pin, and make the length of wiring as short as possible so that a leakage current may not be generated.

(2) Comparator

The comparator compares the voltage of the composite video signal with the voltage (reference voltage) generated in the reference voltage generating circuit, and converts the composite video signal into a digital value.

8.10.8 Start Bit Detecting Circuit

This circuit detects a start bit at line decided in the data slice line specification circuit.

The detection of a start bit is described below.

① A sampling clock is generated by dividing the reference clock output by the timing signal.

② A clock run-in pulse is detected by the sampling clock.

③ After detection of the pulse, a start bit pattern is detected from the comparator output.

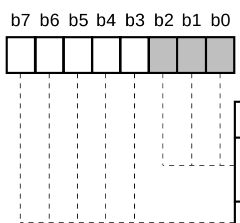
8.10.9 Clock Run-in Determination Circuit

This circuit determinates clock run-in by counting the number of pulses in a window of the composite video signal.

The reference clock count value in one pulse cycle is stored in bits 3 to 7 of the clock run-in detect register (address $00EA_{16}$). Read out these bits after the occurrence of a data slicer interrupt (refer to "8.10.12 Interrupt Request Generating Circuit").

Figure 8.10.10 shows the structure of clock run-in detect register.

Clock Run-in Detect Register



Clock run-in detect register (CRD) [Address $00EA_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Test bits	Read-only	0	R	—
3 to 7	Clock run-in detection bit(CRD3 to CRD7)	Number of reference clocks to be counted in one clock run-in pulse period.	0	R	—

Fig. 8.10.10 Clock Run-in Detect Register

8.10.10 Data Clock Generating Circuit

This circuit generates a data clock synchronized with the start bit detected in the start bit detecting circuit. The data clock stores caption data to the 16-bit shift register. When the 16-bit data has been stored and the clock run-in determination circuit determines clock run-in, the caption data latch completion flag is set. This flag is reset at a falling of the vertical synchronous signal (V_{sep}).

Data Clock Position Register

b7	b6	b5	b4	b3	b2	b1	b0
					0	0	1

Data clock position register (DPS) [Address $00EB_{16}$]

B	Name	Functions	After reset	R W
0	Fix these bits to “1.“		1	R W
1,2	Fix this bit to “0.“		0	R W
3	Data clock position set bits (DPS3 to DPS7)		1	R W
4 to 7			0	

Fig. 8.10.11 Data Clock Position Register

8.10.11 16-bit Shift Register

The caption data converted into a digital value by the comparator is stored into the 16-bit shift register in synchronization with the data clock. The contents of the high-order 8 bits of the stored caption data can be obtained by reading out data register 2 (address $00E3_{16}$) and data register 4 (address $00E5_{16}$). The contents of the low-order 8 bits can be obtained by reading out data register 1 (address $00E2_{16}$) and data register 3 (address $00E4_{16}$), respectively. These registers are reset to “0” at a falling of V_{sep}. Read out data registers 1 and 2 after the occurrence of a data slicer interrupt (refer to “8.10.12 Interrupt Request Generating Circuit”).

8.10.12 Interrupt Request Generating Circuit

The interrupt requests as shown in Table 8.10.3 are generated by combination of the following bits; bits 6 and 7 of the caption position register (address $00E6_{16}$). Read out the contents of data registers 1 to 4 and the contents of bits 3 to 7 of the clock run-in detect register after the occurrence of a data slicer interrupt request.

Table 8.10.2 Contents of Caption Data Latch Completion Flag and 16-bit Shift Register

Slice Line Specification Mode		Contents of Caption Data Latch Completion Flag		Contents of 16-bit Shift Register	
CPS		Completion Flag 1 (bit 0 of DSC2)	Completion Flag 2 (bit 5 of CPS)	Caption Data Registers 1, 2	Caption Data Registers 3, 4
bit 7	bit 6				
0	0	Line 21	A line specified by bits 4 to 0 of CPS	16-bit data of line 21	16-bit data of a line specified by bits 4 to 0 of CPS
0	1	A line specified by bits 4 to 0 of CPS	Invalid	16-bit data of a line specified by bits 4 to 0 of CPS	Invalid
1	0	Line 21	Invalid	16-bit data of line 21	Invalid
1	1	Line 21	A line specified by bits 4 to 0 of CPS	16-bit data of line 21	16-bit data of a line specified by bits 4 to 0 of CPS

CPS: Caption position register
DSC2: Data slicer control register 2

Table 8.10.3 Occurence Sources of Interrupt Request

Caption position register		Occurence Souces of Interrupt Request at End of Data Slice Line
b7	b6	
0	0	After slicing line 21
	1	After a line specified by bits 4 to 0 of CPS
1	0	After slicing line 21
	1	After slicing line 21

8.10.13 Synchronous Signal Counter

The synchronous signal counter counts the composite sync signal taken out from a video signal in the data slicer circuit or the vertical synchronous signal V_{sep} as a count source.

The count value in a certain time (T time) generated by $f(X_{IN})/2^{13}$ or $f(X_{IN})/2^{13}$ is stored into the 5-bit latch. Accordingly, the latch value changes in the cycle of T time. When the count value exceeds "$1F_{16}$," "$1F_{16}$" is stored into the latch.

The latch value can be obtained by reading out the sync pulse counter register (address $00E9_{16}$). A count source is selected by bit 5 of the sync pulse counter register.

The synchronous signal counter is used when bit 0 of PWM mode register 1 (address 0208_{16}).

Figure 8.10.12 shows the structure of the sync pulse counter and Figure 8.10.13 shows the synchronous signal counter block diagram.

Sync Pulse Counter Register

b7 b6 b5 b4 b3 b2 b1 b0

Sync pulse counter register (HC) [Address $00E9_{16}$]

B	Name	Functions	After reset	R	W
0 to 4	Count value (HC0 to HC4)		Indeterminate	R	—
5	Count source (HC5)	0: HSYNC signal 1: Composite sync signal	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 8.10.12 Sync Pulse Counter Register

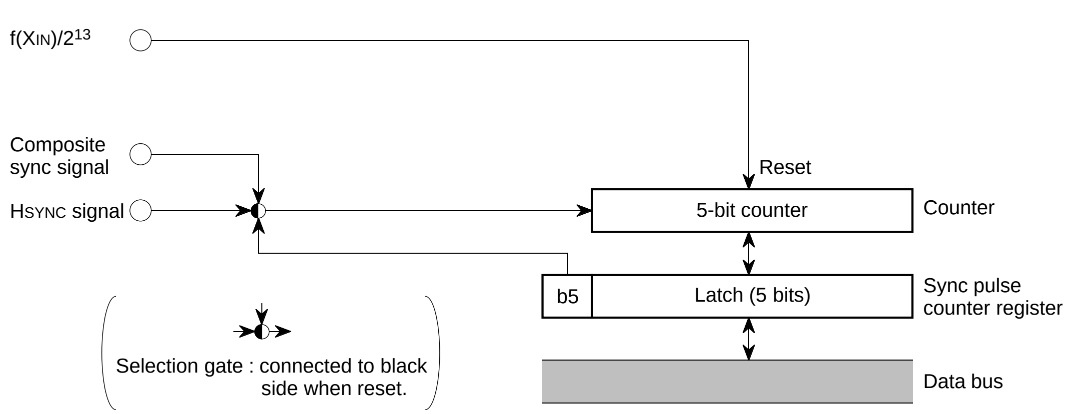


Fig. 8.10.13 Synchronous Signal Counter Block Diagram

8.11 OSD FUNCTIONS

Table 8.11.1 outlines the OSD functions.

This OSD function can display the following: the block display (32 characters × 16 lines), the SPRITE display. And besides, the function can display the both display at the same time. There are 3 display modes and they are selected by a block unit. The display modes are selected by block control register i (i = 1 to 16).

The features of each mode are described below.

Table.8.11.1 Features of Each Display Style

Parameter \ Display style		Block display: CC mode (Closed caption mode)	Block display: OSD mode (On-screem display mode)	Block display: CDOSD mode (Color dot on-screen display mode)	SPRITE display
Number of display characters		32 characters × 16 lines			1 character
Dot structure		16 × 20 dots (Character display area: 16 × 26 dots)	16 × 20 dots	16 × 26 dots	16 × 20 dots
Kinds of characters		510 kinds		62 kinds	1 kind
Font memory		ROM			RAM
Kinds of character sizes		4 kinds	14 kinds		8 kinds
	Pre-divide ratio (Note 1)	× 1, × 2	× 1, × 2, × 3		× 1, × 2
	Dot size	1Tc × 1/2H, 1Tc × 1H	1Tc × 1/2H, 1Tc × 1H, 1.5Tc × 1/2H, 1.5Tc × 1H, 2Tc × 2H, 3Tc × 3H		1Tc × 1/2H, 1Tc × 1H, 2Tc × 1H, 2Tc × 2H
Attribute		Smooth italic, under line, flash (Blinking)	Border	—	—
Character font coloring		1 screen: 8 kinds (per character unit) Max. 64 kinds	1 screen: 16 kinds (per character unit) Max. 64 kinds	1 screen: 8 kinds (per dot unit) (only specified dots are colored per character unit) Max. 64 kinds	1 screen: 8 kinds (per dot unit) Max. 64 kinds
Character background coloring		Possible (a character unit, 1 screen: 4 kinds, Max. 64 kinds)	Possible (a character unit,1 screen: 16 kinds, Max. 64 kinds)	—	—
Display layer		Layer 1	Layer 1 and layer 2		Layer 3 (with highest priority)
OSD output (Note 2)		Analog R, G, B output (each 4 adjustment levels : 64 colors), Digital OUT1, OUT2 output			
Raster coloring		Possible (a screen unit)			
Other function (Note 3)		Auto solid space function Triple layer OSD function, window function, blank funtion	Triple layer OSD function, window function, blank funtion		
Display position		Horizontal: 256 levels, Vertical: 1024 levels			Horizontal: 2048 levels Vertical: 1024 levels
Display expansion (multiline display)		Possible			

Notes1: The character size is specified with dot size and pre-divide ratio (refer to "8.11.3 Dot Size").
2: SPRITE display do not output OUT2.
3: SPRITE display is not referred as windowed function.

The OSD circuit has an extended display mode. This mode allows multiple lines (16 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 8.11.1 shows the configuration of OSD character display area. Figure 8.11.2 shows the block diagram of the OSD circuit. Figure 8.11.3 shows the OSD control register 1. Figure 8.11.4 shows the block control register i.

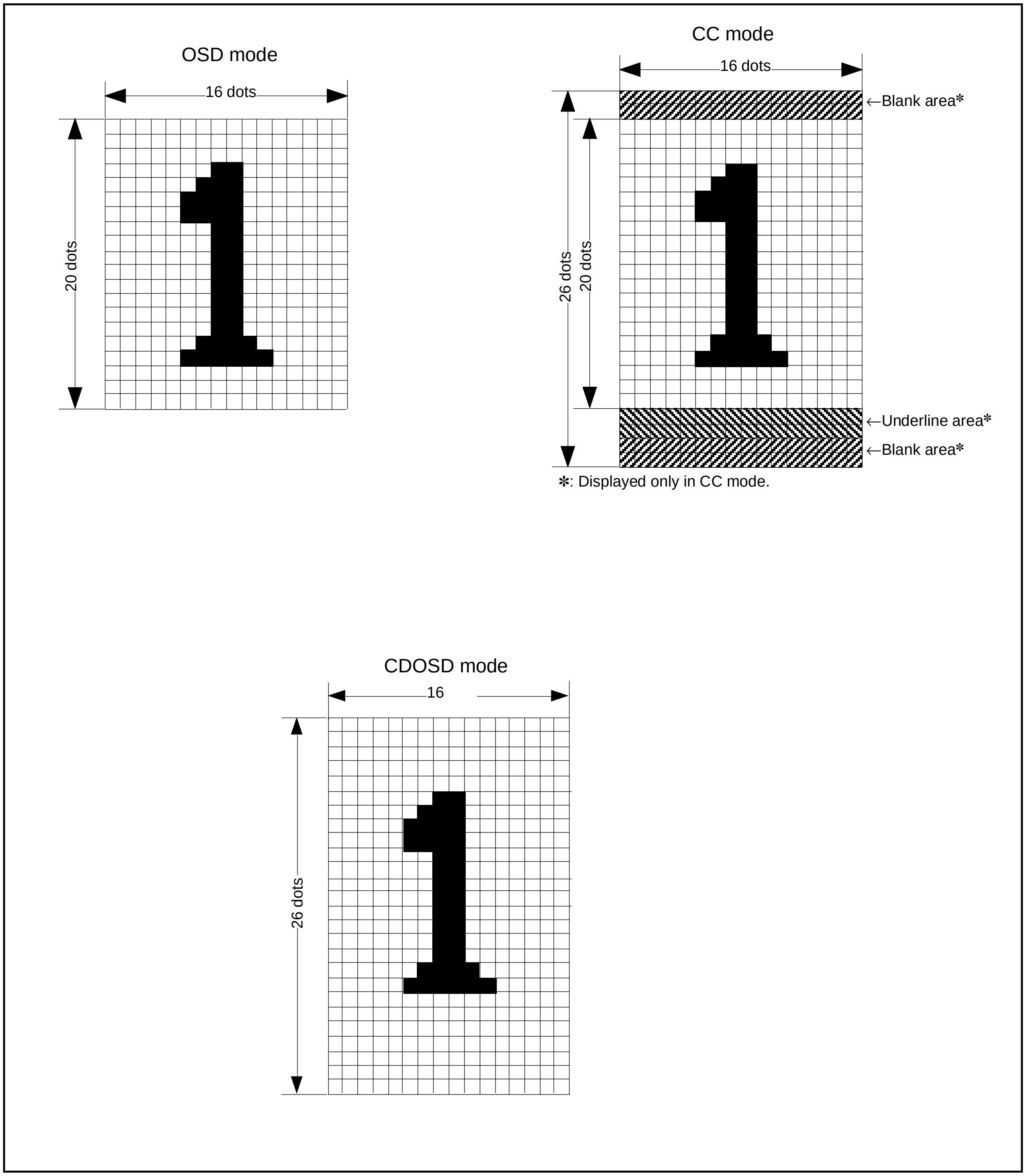


Fig. 8.11.1 Configuration of OSD Character Display Area

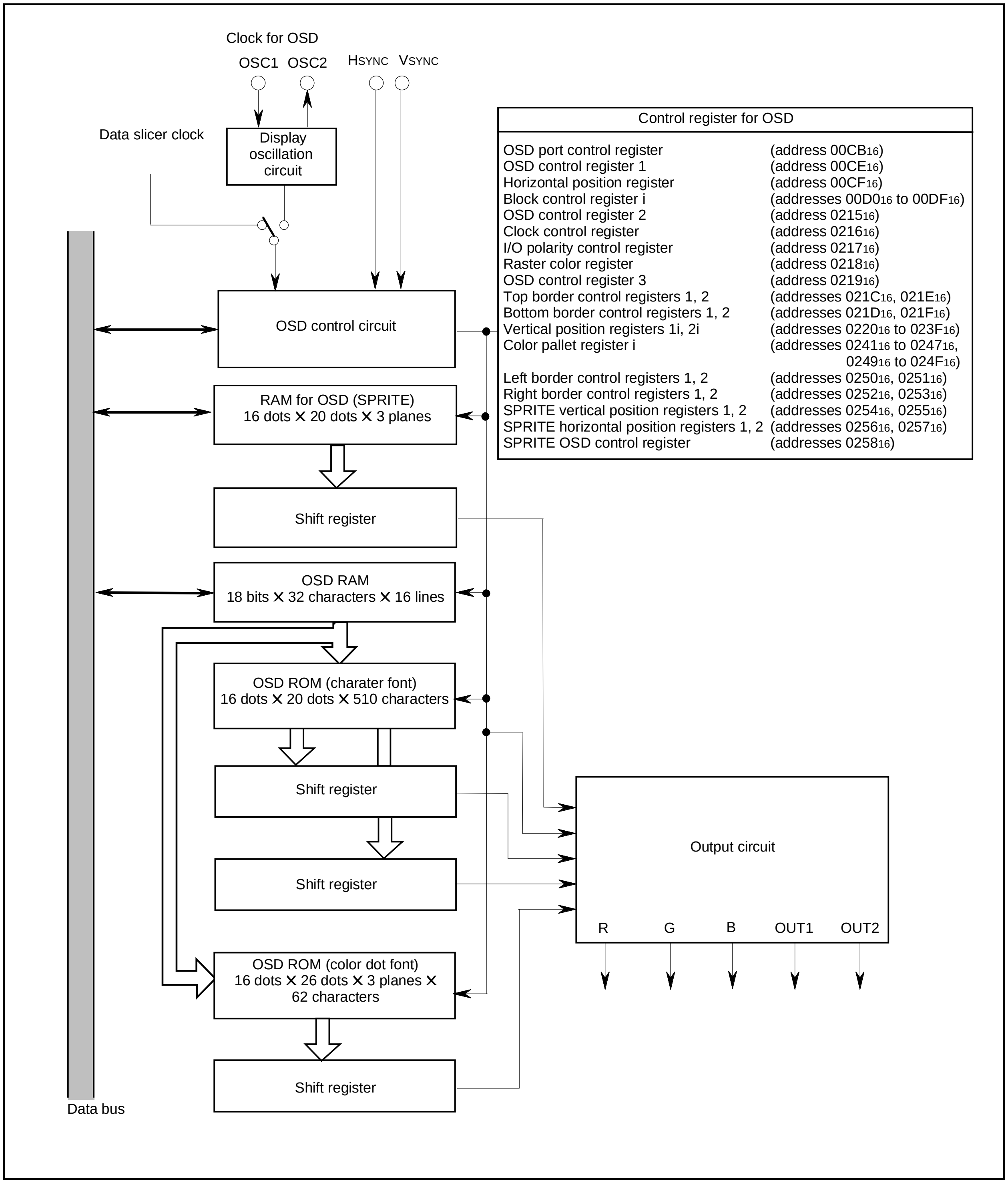


Fig. 8.11.2 Block Diagram of OSD Circuit

OSD Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

OSD control register 1 (OC1) [Address 00CE16]

B	Name	Functions	After reset	R W
0	OSD control bit (OC10) (See note 1)	0 : All-blocks display off 1 : All-blocks display on	0	R W
1	Scan mode selection bit (OC11)	0 : Normal scan mode 1 : Bi-scan mode	0	R W
2	Border type selection bit (OC12)	0 : All bordered 1 : Shadow bordered (See note 2)	0	R W
3	Flash mode selection bit (OC13)	0 : Color signal of character background part does not flash 1 : Color signal of character background part flashes	0	R W
4	Automatic solid space control bit (OC14)	0 : OFF 1 : ON	0	R W
5	Vertical window/blank control bit (OC15)	0 : OFF 1 : ON	0	R W
6, 7	Layer mixing control bits (OC16, OC17) (See note 3)	b7 b6 0 0: Logic sum (OR) of layer 1's color and layer 2's color 0 1: Layer 1's color has priority 1 0: Layer 2's color has priority 1 1: Do not set.	0	R W

Notes 1 : Even this bit is switched during display, the display screen remains unchanged until a rising (falling) of the next VSYNC.
2 : Shadow border is output at right and bottom side of the font.
3 : OUT2 is always ORed, regardless of values of these bits.

Fig. 8.11.3 OSD Control Register 1

Block Control Register i

b7 b6 b5 b4 b3 b2 b1 b0

Block control register i (BCi) (i=1 to 16) [Addresses 00D0₁₆ to 00DF₁₆]

<table>
<tr><th>B</th><th>Name</th><th colspan="6">Functions</th><th>After reset</th><th>R</th><th>W</th></tr>
<tr><td>0, 1</td><td>Display mode selection bits (BCi0, BCi1)</td><td colspan="6">b1 b0
0 0: Display OFF
0 1: OSD mode
1 0: CC mode
1 1: CDOSD mode</td><td>Indeterminate</td><td>R</td><td>W</td></tr>
<tr><td>2</td><td>Border control bit (BCi2)</td><td colspan="6">0 : Border OFF
1 : Border ON</td><td>Indeterminate</td><td>R</td><td>W</td></tr>
<tr><td rowspan="3">3, 4</td><td rowspan="3">Dot size selection bits (BCi3, BCi4)</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>Pre-divide ratio</td><td>Dot size</td><td rowspan="3">Indeterminate</td><td rowspan="3">R</td><td rowspan="3">W</td></tr>
<tr><td>0</td><td>0</td><td>0
0
1
1</td><td>0
1
0
1</td><td>×1</td><td>1Tc × 1/2H
1Tc × 1H
2Tc × 2H
3Tc × 3H</td></tr>
<tr><td>0</td><td>1</td><td>0
0
1
1</td><td>0
1
0
1</td><td rowspan="2">×2</td><td>1Tc × 1/2H
1Tc × 1H
2Tc × 2H
3Tc × 3H</td></tr>
<tr><td rowspan="2">5, 6</td><td rowspan="2">Pre-divide ratio selection bit (BCi5, BCi6)</td><td>1</td><td>1</td><td>0
0</td><td>0
1</td><td>1.5Tc × 1/2H (See note 3)
1.5Tc × 1H (See note 3)</td><td rowspan="2">Indeterminate</td><td rowspan="2">R</td><td rowspan="2">W</td></tr>
<tr><td>1</td><td>1</td><td>0
0
1
1</td><td>0
1
0
1</td><td>×3</td><td>1Tc × 1/2H
1Tc × 1H
2Tc × 2H
3Tc × 3H</td></tr>
<tr><td>7</td><td colspan="7">Nothing is assigned. This bit is a write disable bit.
When this bit is read out, the value is indeterminate.</td><td>Indeterminate</td><td>R</td><td>—</td></tr>
</table>

Notes 1: Tc is OSD clock cycle divided in pre-divide circuit.
2: H is HSYNC.
3: This character size is available only in Layer 2. At this time, set layer 1's pre-divide ratio = × 2, layer 1's horizontal dot size = 1Tc.

Fig. 8.11.4 Block Control Register i (i = 1 to 16)

8.11.1 Triple Layer OSD

Three built-in layers of display screens accommodate triple display of channels, volume, etc., closed caption, and SPRITE displays within layers 1 to 3.

The layer to be displayed in each block is selected by bit 0 or 1 of the OSD control register 2 for each display mode (refer to Figure 8.11.7). Layer 3 always displays the SPRITE display.

When the layer 1 block and the layer 2 block overlay, the screen is composed (refer to Figure 8.11.5) with layer mixing by bit 6 or 7 of the OSD control register 1, as shown in Figure 8.11.3. Layer 3 always takes display priority of layers 1 and 2.

Notes 1: When mixing layer 1 and layer 2, note Table 8.11.2.
2: OUT2 is always ORed, regardless of values of bits 6, 7 of the OSD control register 1. And besides, even when OUT2 (layer 1 or layer 2) overlaps with SPRITE display (layer 3), OUT2 is output.

Table 8.11.2 Mixing Layer 1 and Layer 2

<table>
<tr><th>Block / Parameter</th><th>Block in Layer 1</th><th colspan="2">Block in Layer 2</th></tr>
<tr><td>Display mode</td><td>CC, OSD, CDOSD mode</td><td colspan="2">OSD, CDOSD mode</td></tr>
<tr><td rowspan="4">Pre-divide ratio
Dot size</td><td>× 1, × 2 (CC mode)
× 1 to × 3 (OSD, CDOSD mode)</td><td colspan="2">Same as layer 1</td></tr>
<tr><td rowspan="2">1Tc × 1/2H, 1Tc × 1H
(CC mode)</td><td>Pre-divide ratio = × 1</td><td>Pre-divide ratio = × 2</td></tr>
<tr><td>1Tc × 1/2H
1Tc × 1H</td><td>1Tc × 1/2H, 1.5Tc × 1/2H
1Tc × 1H, 1.5Tc × 1H</td></tr>
<tr><td>1Tc × 1H, 1Tc × 1/2H,
2Tc × 2H, 3Tc × 3H
(OSD, CDOSD mode)</td><td colspan="2">• Same size as layer 1
• 1.5Tc can be selected only when: layer 1’s pre-divide ratio = × 2 AND layer 1’s horizontal dot size = 1Tc.
As this time, vertical dot size is the same as layer 1.</td></tr>
<tr><td>Horizontal display start position</td><td>Arbitrary</td><td colspan="2">Same position as layer 1</td></tr>
<tr><td>Vertical display start position</td><td colspan="3">Arbitrary
However, when dot size is 2Tc × 2H or 2Tc × 3H, set difference between vertical display position of layer 1 and that of layer 2 as follows.
•2Tc × 2H: 2H Units
•3Tc × 3H: 3H Units</td></tr>
</table>

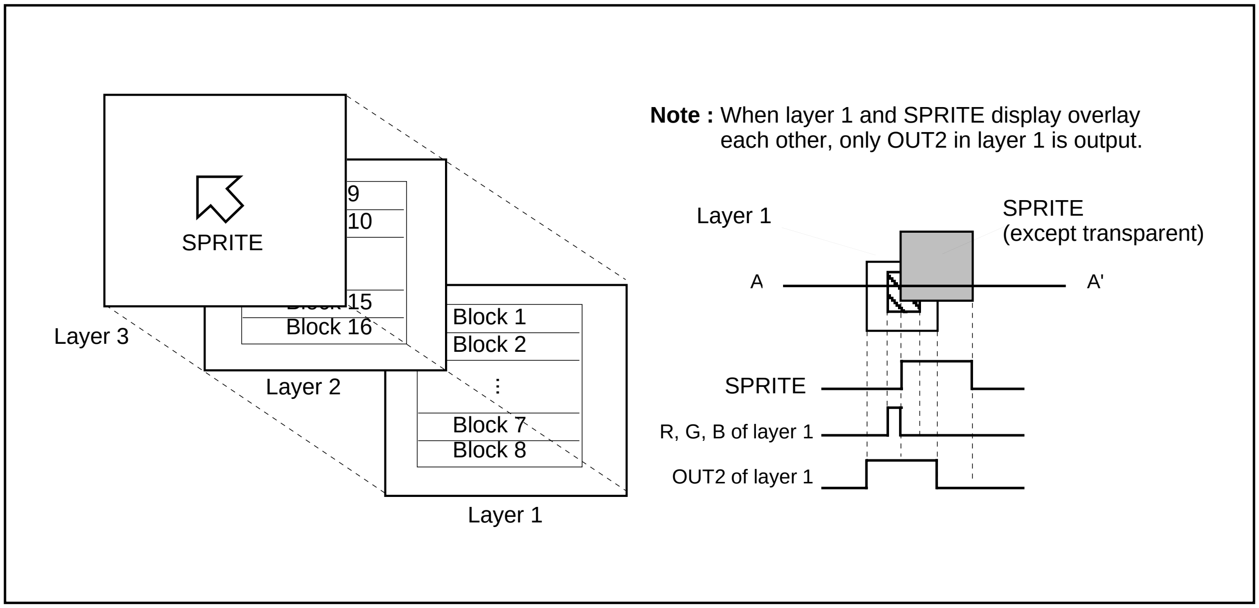
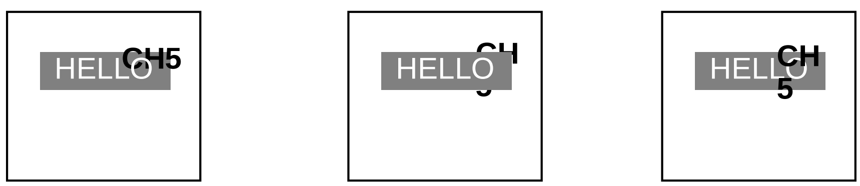


Fig. 8.11.5 Triple Layer OSD

Display example of layer 1 = “HELLO,” layer 2 = “CH5”



Logical sum (OR) of layer 1’s color and layer 2’s color (See note)
Bit 7 = “0,” bit 6 = “0”

Layer 1’s color has priority
Bit 7 = “0,” bit 6 = “1”

Layer 2’s color has priority
Bit 7 = “1,” bit 6 = “0”

Note: Layer mixing is not logical sum (OR) of colors, but that of each bit of color pallet register.
Example) When logical sum (OR) is performed on color pallet 1 (0001_2) and color pallet 2 (0010_2), the color set to color pallet 3 (0011_2) is output, regardless of color pallets 1 and 2 contents.

Fig. 8.11.6 Display Example of Triple Layer OSD

OSD Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

OSD control register 2 (OC2) [Address 0215_{16}]

B	Name	Functions	After reset	R	W
0, 1	Display layer selection bits (OC20, OC21)	b1 b0: Layer 1 / Layer 2 0 0: CC, OSD, CDOSD / — 0 1: CC, OSD / CDOSD 1 0: CC, CDOSD / OSD 1 1: CC / CDOSD OSD	0	R	W
2	R, G, B signal output selection bit(OC22)	0: Digital output (See note) 1: Analog output (4 gradations)	0	R	W
3	Solid space output bit (OC23)	0: OUT1 output 1: OUT2 output	0	R	W
4	Horizotal window/blank coutrol bit (OC24)	0: OFF 1: ON	0	R	W
5	Window/blank selection bit 1 (horizontal) (OC25)	0: Horizontal blank function 1: Horizontal window function	0	R	W
6	Window/blank selection bit 2 (vertical) (OC26)	0: Vertical blank function 1: Vertical window function	0	R	W
7	OSD interrupt request selection bit (OC27)	0: At completion of layer 1 block display 1: At completion of layer 2 block display	0	R	W

Note: When setting bit 1 of the OSD port control register to "1," the value which is converted from the 4-adjustment-level analog to the 2-bit digital is output regardless of this bit value as follows : the high-order bit (R1, G1 and B1) is output from pins $P5_2$, $P5_3$ and $P5_4$, and the low-order bit is (R0, G0 and B0) output from pins $P1_7$, $P1_5$ and $P1_6$. And besides, when not using OSD function, the low-power dissipation can realize by setting this bit to "0."

Fig. 8.11.7 OSD Control Register 2

8.11.2 Display Position

The display start positions of characters are specified by a block. There are 16 blocks, blocks 1 to 16. Up to 32 characters can be displayed in each block (refer to "8.11.6 Memory for OSD").

The display position of each block can be set in both horizontal and vertical directions by software.

The display start position in the horizontal direction can be selected for all blocks in common from 256-step display positions in units of 4 TOSC (TOSC = OSD oscillation cycle).

The display start position in the vertical direction for each block can be selected from 1024-step display positions in units of 1 TH (TH = HSYNC cycle).

Blocks are displayed in conformance with the following rules:

- When the display start position is overlapped with another block (Figure 8.11.8 (b)), a lower block number (1 to 16) is displayed on the front.
- When another block display position appears while one block is displayed (Figure 8.11.8 (c)), the block with a larger set value as the vertical display start position is displayed. However, do not display block with the dot size of 2TC × 2H or 3TC × 3H during display period (✻) of another block.

✻ In the case of OSD mode block: 20 dots in vertical from the vertical display start position.

✻ In the case of CC or CDOSD mode block: 26 dots in vertical from the vertical display start position.

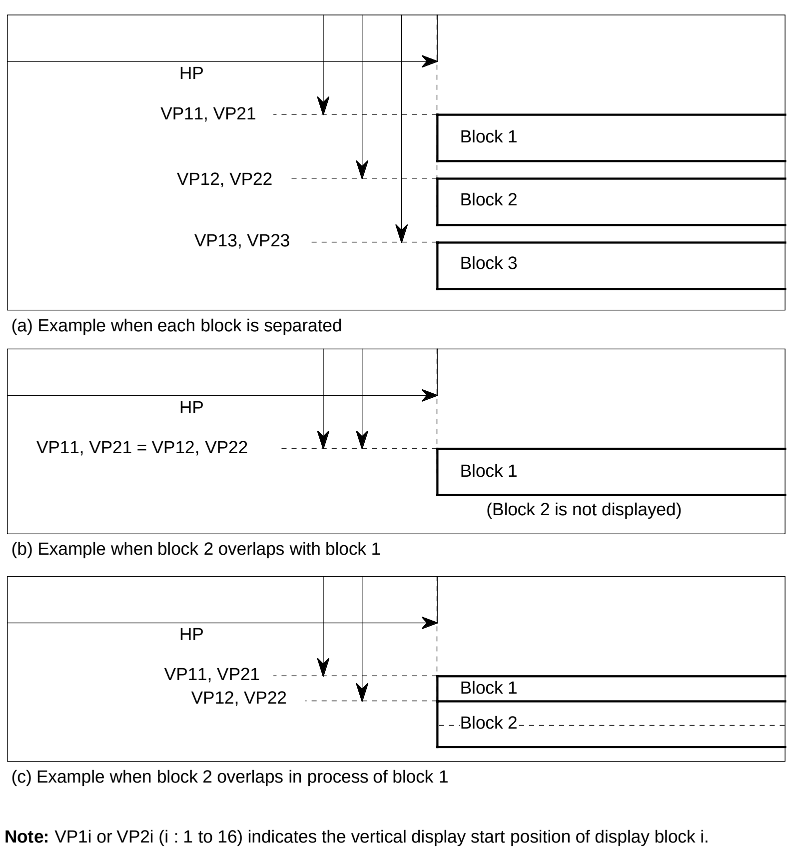
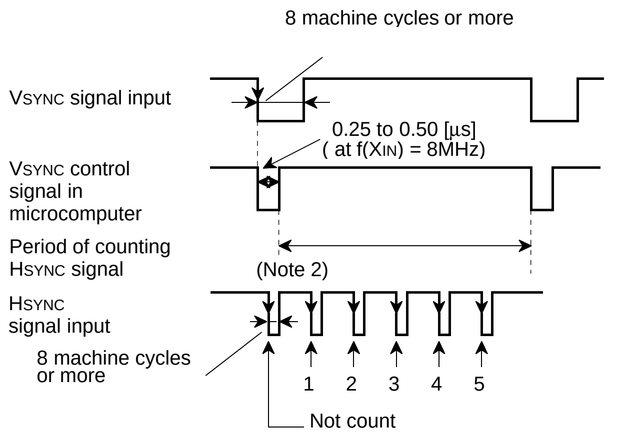


Fig. 8.11.8 Display Position

The display start position in the vertical direction is determined by counting the horizontal sync signal (HSYNC). At this time, when VSYNC and HSYNC are positive polarity (negative polarity), it starts to count the rising edge (falling edge) of HSYNC signal from after fixed cycle of rising edge (falling edge) of VSYNC signal. So interval from rising edge (falling edge) of VSYNC signal to rising edge (falling edge) of HSYNC signal needs enough time (2 machine cycles or more) for avoiding jitter. The polarity of HSYNC and VSYNC signals can select with the I/O polarity control register (address 0217_{16}).



When bits 0 and 1 of the I/O polarity control register (address 0217_{16}) are set to “1” (negative polarity)

Notes 1 : The vertical position is determined by counting falling edge of HSYNC signal after rising edge of VSYNC control signal in the microcomputer.

2 : Do not generate falling edge of HSYNC signal near rising edge of VSYNC control signal in microcomputer to avoid jitter.

3 : The pulse width of VSYNC and HSYNC needs 8 machine cycles or more.

Fig. 8.11.9 Supplement Explanation for Display Position

The vertical start position for each block can be set in 1024 steps (where each step is 1TH (TH: HSYNC cycle)) as values "00_{16}" to "FF_{16}" in vertical position register 1i (i = 1 to 16) (addresses 0220_{16} to $022F_{16}$) and values "00_{16}" to "03_{16}" in vertical position register 2i (i = 1 to 16) (addresses 0230_{16} to $023F_{16}$). The vertical position registers are shown in Figures 8.11.10 and 8.11.11.

Vertical Position Register 1i

b7 b6 b5 b4 b3 b2 b1 b0

Vertical position register 1i (VP1i) (i = 1 to 16) [Addresses 0220_{16} to $022F_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of vertical display start positions (VP1i0 to VP1i7) (See note 1)	Vertical display start positions (low-order 8 bits) TH × (setting value of low-order 2 bits of VP2i × 16^2 + setting value of low-order 4 bits of VP1i × 16^1 + setting value of low-order 4 bits of VP1i × 16^0)	Indeterminate	R	W

Notes 1: Do not "00_{16}" and "01_{16}" to VP1i at VP2i = "00_{16}."

2: TH is cycle of HSYNC.

3: VP2i is vertical position register 2i.

Fig. 8.11.10 Vertical Position Register 1i (i = 1 to 16)

Vertical Position Register 2i

b7 b6 b5 b4 b3 b2 b1 b0

Vertical position register 2i (VP2i) (i = 1 to 16) [Addresses 0230_{16} to $023F_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Control bits of vertical display start positions (VP2i0, VP2i1) (See note 1)	Vertical display start positions (high-order 2 bits) TH × (setting value of low-order 2 bits of VP2i × 16^2 + setting value of low-order 4 bits of VP1i × 16^1 + setting value of low-order 4 bits of VP1i × 16^0)	Indeterminate	R	W
2 to 7	Nothing ic assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R	—

Notes 1: Do not set "00_{16}" and "01_{16}" to VP1i at VP2i = "00_{16}."

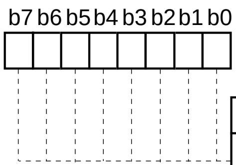
2: TH is cycle of HSYNC.

3: VP1i is vertical position register 1i.

Fig. 8.11.11 Vertical Position Register 2i (i = 1 to 16)

The horizontal display position is common to all blocks, and can be set in 256 steps (where 1 step is 4TOSC, TOSC being the oscillating cycle for display) as values "00_{16}" to "FF_{16}" in bits 0 to 7 of the horizontal position register (address $00CF_{16}$). The horizontal position register is shown in Figure 8.11.12.

Horizontal Position Register



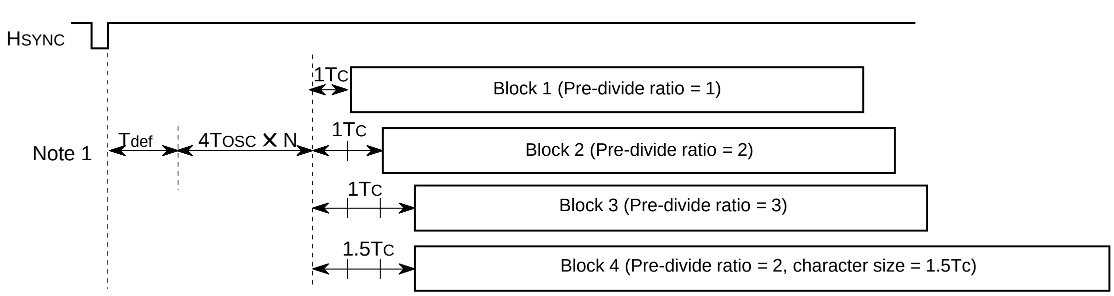
Horizontal position register (HP) [Address $00CF_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of horizontal display start positions (HP0 to HP7)	Horizontal display start positions 4TOSC × (setting value of high-order 4 bits × 16^1 +setting value of low-order 4 bits × 16^0)	0	R	W

Notes 1. The setting value synchronizes with the VSYNC.
2. TOSC = OSD oscillation period.

Fig. 8.11.11 Horizontal Position Register

Note : 1TC (TC : OSD clock cycle divided in pre-divide circuit) gap occurs between the horizontal display start position set by the horizontal position register and the most left dot of the 1st block. Accordingly, when 2 blocks have different pre-divide ratios, their horizontal display start position will not match.
Ordinaly, this gap is 1TC regardless of character sizes, however, the gap is 1.5TC only when the character size is 1.5TC.



N : Value of horizontal position register (decimal notation)
Tc : OSD clock cycle divided in pre-divide circuit
Tosc : OSD oscillation cycle
Tdef : 50 Tosc

Fig. 8.11.12 Notes on Horizontal Display Start Position

8.11.3 Dot Size

The dot size can be selected by a block unit. The dot size in vertical direction is determined by dividing HSYNC in the vertical dot size control circuit. The dot size in horizontal is determined by dividing the following clock in the horizontal dot size control circuit : the clock gained by dividing the OSD clock source (data slicer clock, OSC1, main clock) in the pre-divide circuit. The clock cycle divided in the pre-divide circuit is defined as 1TC.

The dot size is specified by bits 6 to 3 of the block control register.

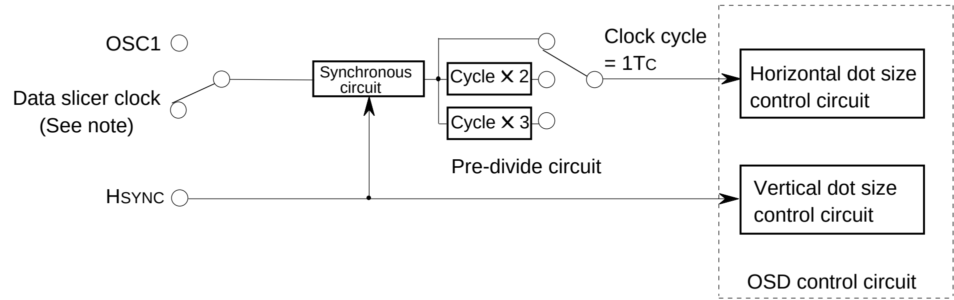
Refer to Figure 8.11.4 (the block control register i), refer to Figure 8.11.6 (the clock control register).

The block diagram of dot size control circuit is shown in Figure 8.11.14.

Notes 1: The pre-divide ratio = 3 cannot be used in the CC mode.

2: The pre-divide ratio of the layer 2 must be same as that of the layer 1 by the block control register i.

3: In the bi-scan mode, the dot size in the vertical direction is 2 times as ompared with the normal mode. Refer to "8.11.13 Scan Mode" about the scan mode.



Note: To use data slicer clock, set bit 0 of data slicer control register 1 to "1."

Fig. 8.11.14 Block Diagram of Dot Size Control Circuit

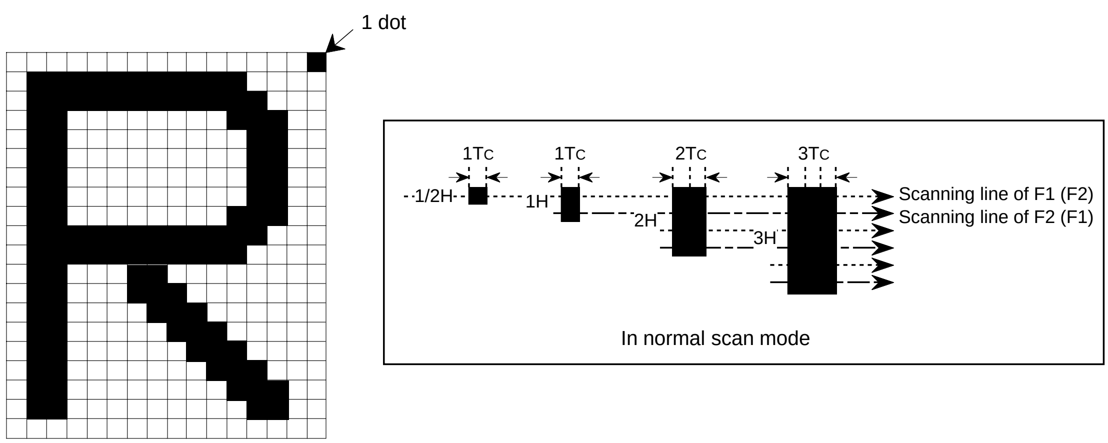


Fig. 8.11.15 Definition of Dot Sizes

8.11.4 Clock for OSD

As a clock for display to be used for OSD, it is possible to select one of the following 3 types.

- Data slicer clock output from the data slicer (approximately 26 MHz)
- Clock from the LC oscillator supplied from the pins OSC1 and OSC2
- Clock from the ceramic resonator or the quartz-crystal oscillator from the pins OSC1 and OSC2

The clock for display to be used for OSD can be selected by bit 7 of port P3 direction register, bit 2 and bit 1 of clock source control register (address 0216_{16}). If the pins OSC1 and OSC2 are not used as OSD clock input/output, these pins can be used as the sub-clock input/output, or port P6.

Table 8.11.3 Setting of $P6_3$/OSC1/X_{CIN}, $P6_4$/OSC2/X_{COUT}

Registers \ Function		Clock input/output pins for OSD		Sub-clock input/output pins	Input port
Bit 7 of Port P3 Direction Register		0		0	1
Clock Control Register	Bit 2	1	1	0	0
	Bit 1	0	1	0	1

Clock Control Register

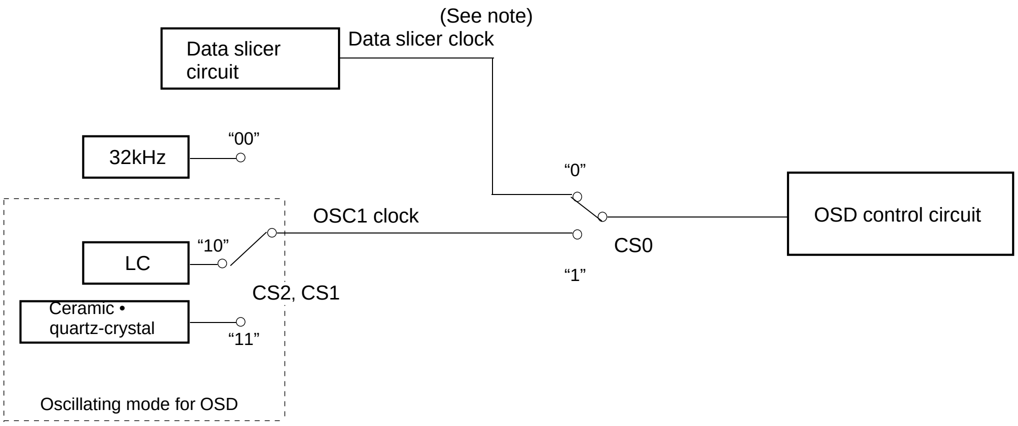
b7 b6 b5 b4 b3 b2 b1 b0: [ ] 0 0 0 0 [ ] [ ] [ ] — Clock control register (CS) [Address 0216_{16}]

B	Name	Functions	After reset	R W
0	Clock selection bit (CS0)	0: Data slicer clock 1: OSC1 clock	0	R W
1, 2	OSC1 oscillating mode selection bits (CS1, CS2)	b2 b1 0 0: 32kHz oscillating mode. 0 1: Used as input port of $P6_3$ and $P6_4$ (See note 1). 1 0: LC oscillating mode 1 1: Ceramic • quartz-crystal oscillating mode	0	R W
3 to 6	Fix these bits to “0.”		0	R W
7	Test bit (See note 2)		0	R W

Note 1: Set bit 7 of address $00C7_{16}$ to “1”, when OSC1 and OSC2 are used as $P6_3$ and $P6_4$.

2: Be sure to set bit 7 to “0” for program of the mask and the EPROM versions. For the emulator MCU version (M37280ERSS), be sure to set bit 7 to “1” when using the data slicer clock for software debugging.

Fig. 8.11.16 Clock Control Register



Note : To use data slicer clock, set bit 0 of data slicer control register 1 to "1."

Fig. 8.11.17 Block Diagram of OSD Selection Circuit

8.11.5 Field Determination Display

To display the block with vertical dot size of 1/2H, whether an even field or an odd field is determined through differences in a synchronizing signal waveform of interlacing system. The dot line 0 or 1 (refer to Figure 8.11.19) corresponding to the field is displayed alternately.

In the following, the field determination standard for the case where both the horizontal sync signal and the vertical sync signal are negative-polarity inputs will be explained. A field determination is determined by detecting the time from a falling edge of the horizontal sync signal until a falling edge of the VSYNC control signal (refer to Figure 8.11.9) in the microcomputer and then comparing this time with the time of the previous field. When the time is longer than the comparing time, it is regarded as even field. When the time is shorter, it is regarded as odd field.

The field determination flag changes at a rising edge of VSYNC control signal in the microcomputer.

The contents of this field can be read out by the field determination flag (bit 7 of the I/O polarity control register at address 0217_{16}). A dot line is specified by bit 6 of the I/O polarity control register (refer to Figure 8.11.19).

However, the field determination flag read out from the CPU is fixed to "0" at even field or "1" at odd field, regardless of bit 6.

I/O Polarity Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I/O polarity control register (PC) [Address 0217_{16}]

B	Name	Functions	After reset	R	W
0	HSYNC input polarity switch bit (PC0)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
1	VSYNC input polarity switch bit (PC1)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
2	R, G, B output polarity switch bit (PC2)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
3	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0".		0	R	—
4	OUT1 output polarity switch bit (PC4)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
5	OUT2 output polarity switch bit (PC5)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
6	Display dot line selection bit (PC6) (See note)	0 : "□" at even field "▨" at odd field 1 : "▨" at even field "□" at odd field	0	R	W
7	Field determination flag(PC7)	0 : Even field 1 : Odd field	1	R	—

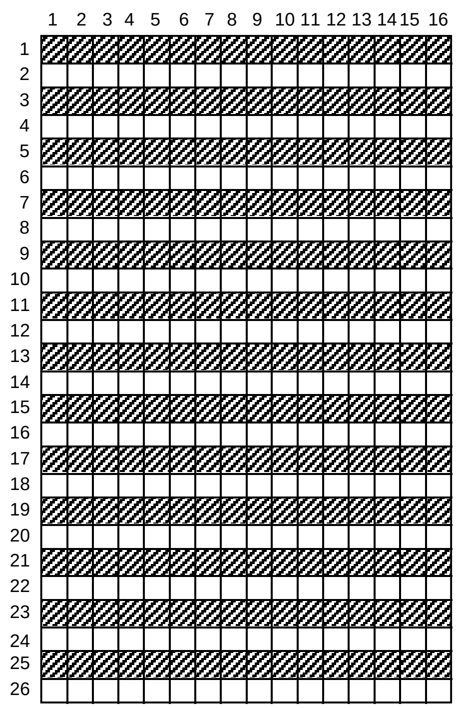
Note: Refer to Fig. 8.11.19.

Fig. 8.11.18 I/O Polarity Control Register

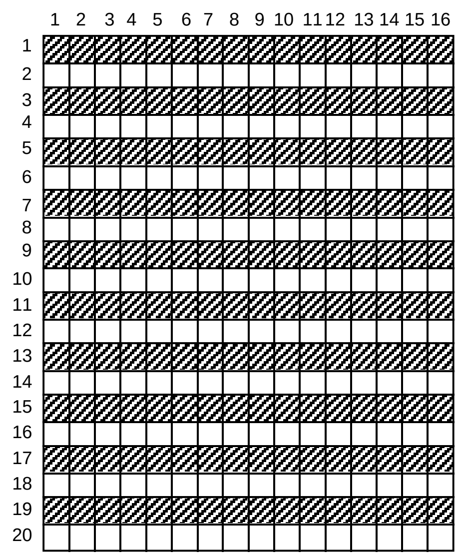
Both HSYNC signal and VSYNC signal are negative-polarity input

HSYNC		Field	Field determination flag(Note)	Display dot line selection bit	Display dot line
VSYNC and VSYNC control signal in microcomputer Upper : VSYNC signal Lower : VSYNC control signal in microcomputer	(n–1) field (Odd-numbered) T1 0.25 to 0.50[µs] at f(XIN) =8 MHz	Odd			
	(n) field (Even-numbered) T2	Even	0 (T2 > T1)	0	Dot line 1 □
				1	Dot line 0 ▨
	(n+1) field (Odd-numbered) T3	Odd	1 (T3 < T2)	0	Dot line 0 ▨
				1	Dot line 1 □

When using the field determination flag, be sure to set bit 0 of the PWM mode register 1 (address $020A_{16}$) to "0."



CC mode · CDOSD mode



OSDS mode

When the display dot line selection bit is "0," the "□" font is displayed at even field, the "▨" font is displayed at odd field. Bit 7 of the I/O polarity control register can be read as the field determination flag : "1" is read at odd field, "0" is read at even field.

OSD ROM font configuration diagram

Note : The field determination flag changes at a rising edge of the VSYNC control signal (negative-polarity input) in the microcomputer.

Fig. 8.11.19 Relation Between Field Determination Flag and Display Font

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8.11.6 Memory for OSD

There are 2 types of memory for OSD : OSD ROM (addresses 10800_{16} to $157FF_{16}$ and 18000_{16} to $1ACFF_{16}$) used to specify character dot data and OSD RAM (addresses 0700_{16} to $07A7_{16}$ and 0800_{16} to $0FDF_{16}$) used to specify the kinds of display characters, display colors, and SPRITE display. The following describes each type of memory.

(1) OSD ROM (addresses 10800_{16} to $157FF_{16}$, 18000_{16} to $1ACFF_{16}$)

The dot pattern data for OSD characters is stored in the character font area in the OSD ROM and the CD font data for OSD characters is stored in the color dot font area in the OSD ROM. To specify the kinds of the character font and the CD font, it is necessary to write the character code into the OSD RAM.

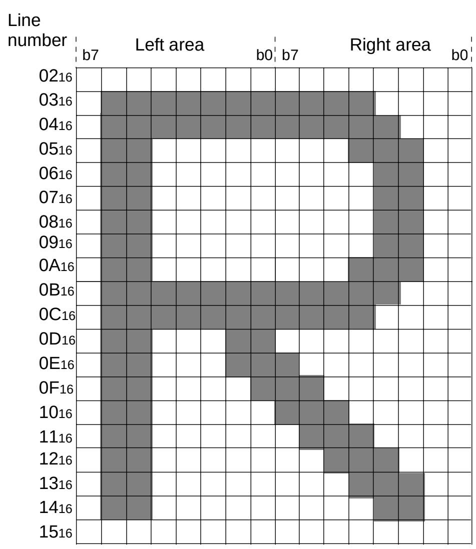
The modes are selected by bit 3 of the OSD control register 3 for each screen.

The character font data storing address is shown in Figure 8.11.20. The CD font data storing address is shown in Figure 8.11.21. The 510 kinds of character font and 62 kinds of CD font can be stored.

OSD ROM address of character font data

OSD ROM address bit	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Line number / Character code / Area bit	1	0	Line number					Character code									Area bit

Line number = “02_{16}” to “15_{16}”
Character code = “00_{16}” to “$1FF_{16}$” (“$0FF_{16}$” and “100_{16}” can not be used. Write “FF_{16}” to corresponding addresses.)
Area bit = 0: Left area
1: Right area



Character font

Fig. 8.11.20 Character Font Data Storing Address

OSD ROM address of CD font data

OSD ROM address bit	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Line number/CD code/ Area bit	1	1	Plain selection bit		Line number (MSB to LSB)					CD code (C5 to C0)						1	Area bit

Line number = "00_{16}" to "19_{16}"
CD code = "00_{16}" to "$3F_{16}$" ("$1F_{16}$" and "20_{16}" cannot be used. Write "FF_{16}" to the corresponding address.)
Area bit = 0 : Area 0   1 : Area 1

Plane 2
(Color palette selection bit 2)

1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Plane 1
(Color palette selection bit 1)

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Plane 0
(Color palette selection bit 0)

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
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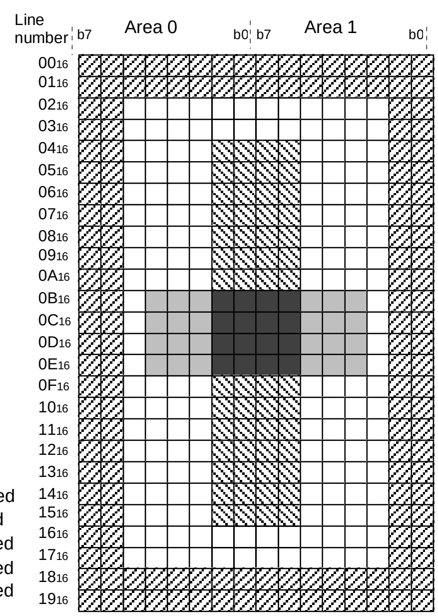
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Line number	b7	Area 0						b0	b7	Area 1						b0
00_{16}	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
01_{16}	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
02_{16}	4	4	0	0	0	0	0	0	0	0	0	0	0	0	4	4
03_{16}	4	4	0	0	0	0	0	0	0	0	0	0	0	0	4	4
04_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
05_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
06_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
07_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
08_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
09_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
$0A_{16}$	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
$0B_{16}$	4	4	0	1	1	1	3	3	3	3	1	1	1	0	4	4
$0C_{16}$	4	4	0	1	1	1	3	3	3	3	1	1	1	0	4	4
$0D_{16}$	4	4	0	1	1	1	3	3	3	3	1	1	1	0	4	4
$0E_{16}$	4	4	0	1	1	1	3	3	3	3	1	1	1	0	4	4
$0F_{16}$	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
10_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
11_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
12_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
13_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
14_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
15_{16}	4	4	0	0	0	0	2	2	2	2	0	0	0	0	4	4
16_{16}	4	4	0	0	0	0	0	0	0	0	0	0	0	0	4	4
17_{16}	4	4	0	0	0	0	0	0	0	0	0	0	0	0	4	4
18_{16}	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
19_{16}	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4

When bit 3 of OSD control register 3 is "0 (1)"

- 0 Color palette set by RC13 to RC16 of OSD RAM is selected
- 1 Color palette 1 (9) is selected
- 2 Color palette 2 (10) is selected
- 3 Color palette 3 (11) is selected
- 4 Color palette 4 (12) is selected



Display example

Fig. 8.11.21 Color Dot Font Data Storing Address

(2) OSD RAM (addresses 0700_{16} to $07A7_{16}$, 0800_{16} to $0FFF_{16}$)

The OSD RAM for SPRITE consisting of 3 planes, is assigned to addresses 0700_{16} to $07A7_{16}$. Each plane corresponds to each color pallet selection bit and the color pallet of each dot is determined from among 8 kinds.

The OSD RAM for character is allocated at addresses 0800_{16} to $0FFF_{16}$, and is divided into a display character code specification part, color code 1 specification part, and color code 2 specification part for each block. Tables 8.11.5 and 8.11.6 show the contents of the OSD RAM.

For example, to display 1 character position (the left edge) in block 1, write the character code in address 0800_{16}, write color code 1 at 0820_{16}, and write color code 2 at 0840_{16}. The structure of the OSD RAM is shown in Figure 8.11.23.

Note : For the layer 2 's OSD mode block with dot size of $1.5T_C \times 1/2H$ and $1.5T_C \times 1H$, the 3nth (n = 1 to 10) character is skipped as compared with ordinary block (blocks with dot size of $1T_C \times 1/2H$, or blocks on the layer 1). Accordingly, maximum 22 characters are only displayed in 1 block. Blocks with dot size of $1T_C \times 1/2H$ and $1T_C \times 1H$, or blocks on the layer 1

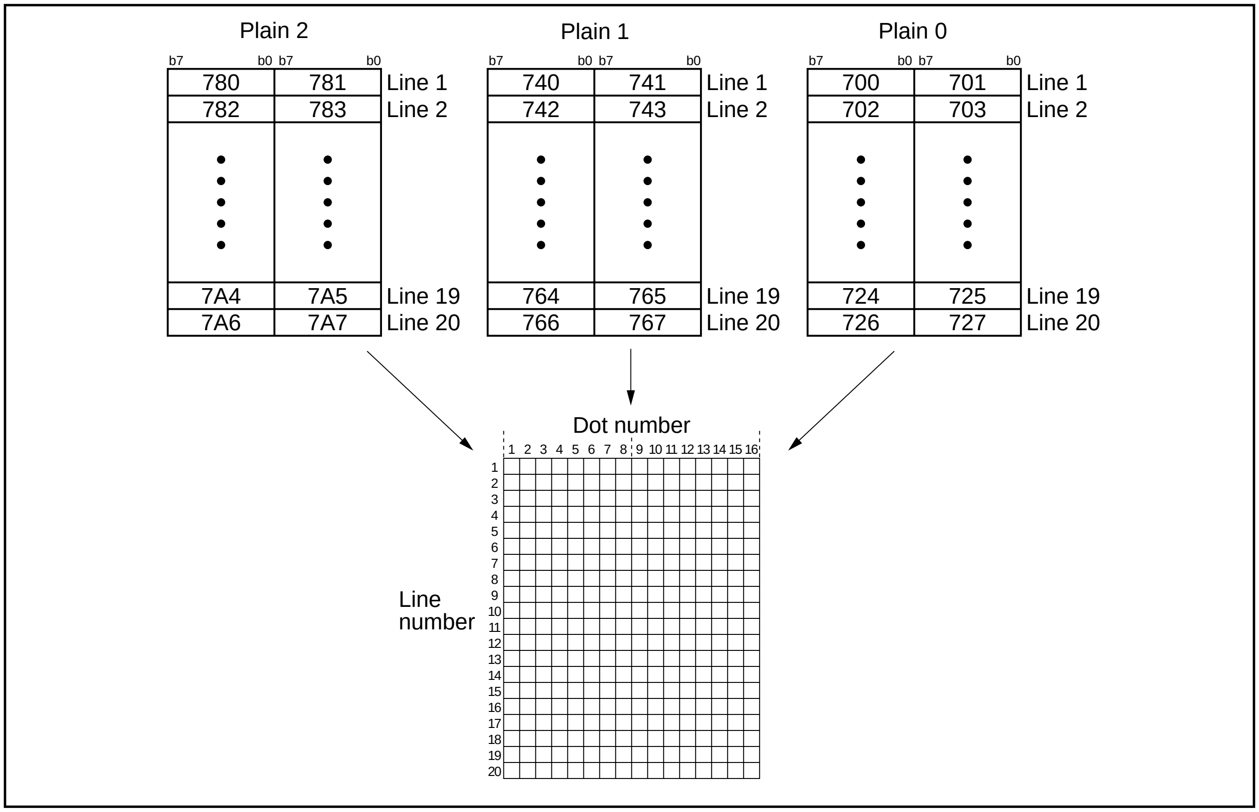
However, note the following:

- In OSD mode
  The character is not displayed, and only the left 1/3 part of the 22nd character back ground is displayed in the 22nd's character area. When not displaying this background, set transparent for background.
- In CDOSD mode
  The character is not displayed, and color pallet color specified by bit 3 to 6 of color code 1 can be output in the 22nd's character area (left 1/3 part).

The RAM data for the 3nth character does not effect the display.
Any character data can be stored here (refer to Figure 8.11.22).

Table 8.11.4 Contents of OSD RAM (SPRITE)

Line (from top)	Dot (from left)	Plain 0 (Color pallet selection bit 0)	Plain 1 (Color pallet selection bit 1)	Plain 2 (Color pallet selection bit 2)
Line 1	Dots 1 to 8 Dots 9 to 16	0700_{16} 0701_{16}	0740_{16} 0741_{16}	0780_{16} 0781_{16}
Line 2	Dots 1 to 8 Dots 9 to 16	0702_{16} 0703_{16}	0742_{16} 0743_{16}	0782_{16} 0783_{16}
:	:	:	:	:
Line 19	Dots 1 to 8 Dots 9 to 16	0724_{16} 0725_{16}	0764_{16} 0765_{16}	$07A4_{16}$ $07A5_{16}$
Line 20	Dots 1 to 8 Dots 9 to 16	0726_{16} 0727_{16}	0766_{16} 0767_{16}	$07A6_{16}$ $07A7_{16}$



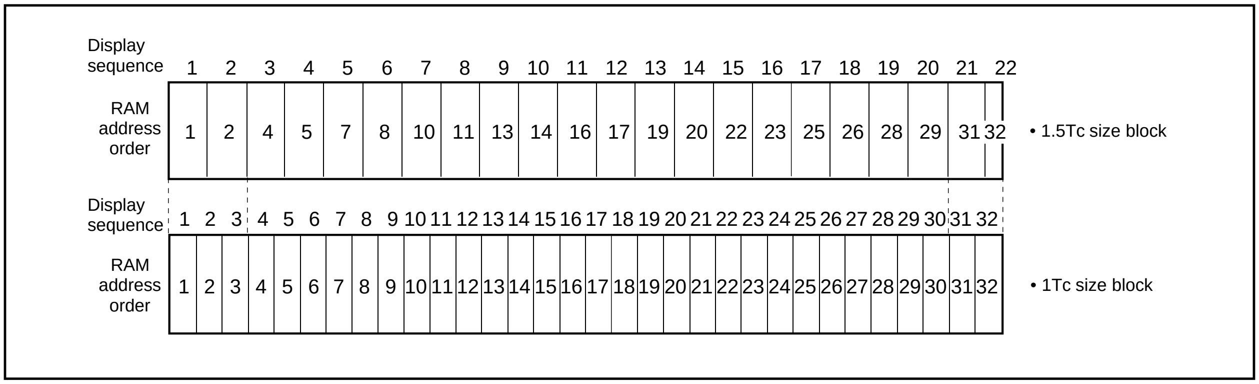


Fig. 8.11.22 RAM Data for 3nth Character

Table 8.11.5 Contents of OSD RAM (Character)

Block	Display Position (from left)	Character Code Specification	Color Code 1 Specification	Color Code 2 Specification
Block 1	1st character	0800_{16}	0820_{16}	0840_{16}
	2nd character : 31st character	0801_{16} : $081E_{16}$	0821_{16} : $083E_{16}$	0841_{16} : $085E_{16}$
	32nd character	$081F_{16}$	$083F_{16}$	$085F_{16}$
Block 2	1st character	0880_{16}	$08A0_{16}$	$08C0_{16}$
	2nd character : 31st character	0881_{16} : $089E_{16}$	$08A1_{16}$: $08BE_{16}$	$08C1_{16}$: $08DE_{16}$
	32nd character	$089F_{16}$	$08BF_{16}$	$08DF_{16}$
Block 3	1st character	0900_{16}	0920_{16}	0940_{16}
	2nd character : 31st character	0901_{16} : $091E_{16}$	0921_{16} : $093E_{16}$	0941_{16} : $095E_{16}$
	32nd character	$091F_{16}$	$093F_{16}$	$095F_{16}$
Block 4	1st character	0980_{16}	$09A0_{16}$	$09C0_{16}$
	2nd character : 31st character	0981_{16} : $099E_{16}$	$09A1_{16}$: $09BE_{16}$	$09C1_{16}$: $09DE_{16}$
	32nd character	$099F_{16}$	$09BF_{16}$	$09DF_{16}$
Block 5	1st character	$0A00_{16}$	$0A20_{16}$	$0A40_{16}$
	2nd character : 31st character	$0A01_{16}$: $0A1E_{16}$	$0A21_{16}$: $0A3E_{16}$	$0A41_{16}$: $0A5E_{16}$
	32nd character	$0A1F_{16}$	$0A3F_{16}$	$0A5F_{16}$
Block 6	1st character	$0A80_{16}$	$0AA0_{16}$	$0AC0_{16}$
	2nd character : 31st character	$0A81_{16}$: $0A9E_{16}$	$0AA1_{16}$: $0ABE_{16}$	$0AC1_{16}$: $0ADE_{16}$
	32nd character	$0A9F_{16}$	$0ABF_{16}$	$0ADF_{16}$
Block 7	1st character	$0B00_{16}$	$0B20_{16}$	$0B40_{16}$
	2nd character : 31st character	$0B01_{16}$: $0B1E_{16}$	$0B21_{16}$: $0B3E_{16}$	$0B41_{16}$: $0B5E_{16}$
	32nd character	$0B1F_{16}$	$0B3F_{16}$	$0B5F_{16}$
Block 8	1st character	$0B80_{16}$	$0BA0_{16}$	$0BC0_{16}$
	2nd character : 31st character	$0B81_{16}$: $0B9E_{16}$	$0BA1_{16}$: $0BBE_{16}$	$0BC1_{16}$: $0BDE_{16}$
	32nd character	$0B9F_{16}$	$0BBF_{16}$	$0BDF_{16}$
Block 9	1st character	$0C00_{16}$	$0C20_{16}$	$0C40_{16}$
	2nd character : 31st character	$0C01_{16}$: $0C1E_{16}$	$0C21_{16}$: $0C3E_{16}$	$0C41_{16}$: $0C5E_{16}$
	32nd character	$0C1F_{16}$	$0C3F_{16}$	$0C5F_{16}$
Block 10	1st character	$0C80_{16}$	$0CA0_{16}$	$0CC0_{16}$
	2nd character : 31st character	$0C81_{16}$: $0C9E_{16}$	$0CA1_{16}$: $0CBE_{16}$	$0CC1_{16}$: $0CDE_{16}$
	32nd character	$0C9F_{16}$	$0CBF_{16}$	$0CDF_{16}$

Table 8.11.6 Contents of OSD RAM (continued)

Block	Display Position (from left)	Character Code Specification	Color Code 1 Specification	Color Code 2 Specification
Block 11	1st character	$0D00_{16}$	$0D20_{16}$	$0D40_{16}$
	2nd character : 31st character	$0D01_{16}$: $0D1E_{16}$	$0D21_{16}$: $0D3E_{16}$	$0D41_{16}$: $0D5E_{16}$
	32nd character	$0D1F_{16}$	$0D3F_{16}$	$0D5F_{16}$
Block 12	1st character	$0D80_{16}$	$0DA0_{16}$	$0DC0_{16}$
	2nd character : 31st character	$0D81_{16}$: $0D9E_{16}$	$0DA1_{16}$: $0DBE_{16}$	$0DC1_{16}$: $0DDE_{16}$
	32nd character	$0D9F_{16}$	$0DBF_{16}$	$0DDF_{16}$
Block 13	1st character	$0E00_{16}$	$0E20_{16}$	$0E40_{16}$
	2nd character : 31st character	$0E01_{16}$: $0E1E_{16}$	$0E21_{16}$: $0E3E_{16}$	$0E41_{16}$: $0E5E_{16}$
	32nd character	$0E1F_{16}$	$0E3F_{16}$	$0E5F_{16}$
Block 14	1st character	$0E80_{16}$	$0EA0_{16}$	$0EC0_{16}$
	2nd character : 31st character	$0E81_{16}$: $0E9E_{16}$	$0EA1_{16}$: $0EBE_{16}$	$0EC1_{16}$: $0EDE_{16}$
	32nd character	$0E9F_{16}$	$0EBF_{16}$	$0EDF_{16}$
Block 15	1st character	$0F00_{16}$	$0F20_{16}$	$0F40_{16}$
	2nd character : 31st character	$0F01_{16}$: $0F1E_{16}$	$0F21_{16}$: $0F3E_{16}$	$0F41_{16}$: $0F5E_{16}$
	32nd character	$0F1F_{16}$	$0F3F_{16}$	$0F5F_{16}$
Block 16	1st character	$0F80_{16}$	$0FA0_{16}$	$0FC0_{16}$
	2nd character : 31st character	$0F81_{16}$: $0F9E_{16}$	$0FA1_{16}$: $0FBE_{16}$	$0FC1_{16}$: $0FDE_{16}$
	32nd character	$0F9F_{16}$	$0FBF_{16}$	$0FDF_{16}$

Note: Do not read from/write to the addresses in Table 8.11.7.

Table 8.11.7 List of Access Disable Addresses

0860_{16} to $087F_{16}$	$0C60_{16}$ to $0C7F_{16}$
$08E0_{10}$ to $08FF_{16}$	$0CE0_{16}$ to $0CFF_{16}$
0960_{16} to $097F_{16}$	$0D60_{16}$ to $0D7F_{16}$
$09E0_{16}$ to $09FF_{16}$	$0DE0_{16}$ to $0DFF_{16}$
$0A60_{16}$ to $0A7F_{16}$	$0E60_{16}$ to $0E7F_{16}$
$0AE0_{16}$ to $0AFF_{16}$	$0EE0_{16}$ to $0EFF_{16}$
$0B60_{16}$ to $0B7F_{16}$	$0F60_{16}$ to $0F7F_{16}$
$0BE0_{16}$ to $0BFF_{16}$	$0FE0_{16}$ to $0FFF_{16}$

Blocks 1 to 16

b7							b0	b7							b0	b1	b0
RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	RC17	RC16	RC15	RC14	RC13	RC12	RC11	RC10	RC21	RC20
Character code								Color code 1								Color code 2	

Bit	CC mode		OSD mode		CDOSD mode	
	Bit name	Function	Bit name	Function	Bit name	Function
RF0	Character code (Low-order 8 bits)	Specify character code in OSD ROM (See note 3)	Character code (Low-order 8 bits)	Specify character code in OSD ROM (See note 3)	CD code (6 bits)	Specify character code in OSD ROM (color dot) (See note 4)
RF1						
RF2						
RF3						
RF4						
RF5						
RF6					Not used	————
RF7						
RC10	Character code (High-order 1 bits)		Character code (High-order 1 bits)			
RC11	Character: Color pallet selection bit 0	Specify color pallet for character (See note 5)	Character: Color pallet selection bit	Specify color pallet for character (See note 5)		
RC12	Character: Color pallet selection bit 1		Character: Color pallet selection bit			
RC13	Character: Color pallet selection bit 2		Character: Color pallet selection bit		Dot color: Color pallet selection bit 0	Specify a dot which selects color pallet 0 or 8 by OSD ROM (See note 6)
RC14	Italic control	0: Italic OFF 1: Italic ON	Character: Color pallet selection bit 3		Dot color: Color pallet selection bit 1	
RC15	Flash control	0: Flash OFF 1: Flash ON	Character background: Color pallet selection bit 0	Specify color pallet for background (See note 5)	Dot color: Color pallet selection bit 2	
RC16	Underline control	0: Underline OFF 1: Underline ON	Character background: Color pallet selection bit 1		Dot color: Color pallet selection bit 3	
RC17	OUT2 output control	0: OUT2 output OFF 1: OUT2 output ON	OUT2 output control	0: OUT2 output OFF 1: OUT2 output ON	OUT2 output control	0: OUT2 output OFF 1: OUT2 output ON
RC20	Character background: Color pallet selection bit 0	Specify color pallet for background (See note 5)	Character background: Color pallet selection bit 2	Specify color pallet for background (See note 5)	Not used	————
RC21	Character background: Color pallet selection bit 1		Character background: Color pallet selection bit 3			

Notes 1: Read value of bits 2 to 7 of the color code 2 is undefined.
2: For "not used" bits, the write value is read.
3: Do not use character code "0FF16," "10016."
4: Do not use character code "1F16," "2016."
5: Refer to Figure 8.11.24.
6: Only CDOSD mode, a dot which selects color pallet 0 or 8 is colored to the color pallet set by RC13 to RC16 of OSD RAM in character units.

Fig. 8.11.23 Structure of OSD RAM

8.11.7 Character Color

As shown in Figure 2.11.24, there are 16 built-in color pallets. Color pallet 0 is fixed at transparent, and color pallet 8 is fixed at black. The remaining 14 colors can be set to any of the 64 colors available. The setting procedure for character colors is as follows:

- CC mode .... 8 kinds
  Color pallet selection range (color pallets 0 to 7 or 8 to 15) can be selected by bit 0 of the OSD control register 3 (address 0219_{16}). Color pallets are set by bits RC11 to RC13 of the OSD RAM from among the selection range.
- OSD mode .... 15 kinds
  Color pallets are set by bits RC11 to RC14 of the OSD RAM.
- CDOSD mode .... 8 kinds
  Color pallet selection range (color pallets 0 to 7 or 8 to 15) can be selected by bit 3 of the OSD control register 3 (address 0219_{16}). Color pallets are set in dot units according to the CD font data (the OSD RAM<color dot font> contents)from among the selection range.
  Only in CDOSD mode, a dot which selects color pallet 0 or 8 is colored to the color pallet set by RC13 to RC16 of OSD RAM in character units (refer to Figure 8.11.26).
- SPRITE display .... 8 kinds
  Color pallet selection range (color pallets 0 to 7 or 8 to 15) can be selected by bit 4 of the OSD control register 3 (address 0219_{16}). Color pallets are set in dot units according to the CD font data (the OSD RAM<color dot font> contents) from among the selection range.

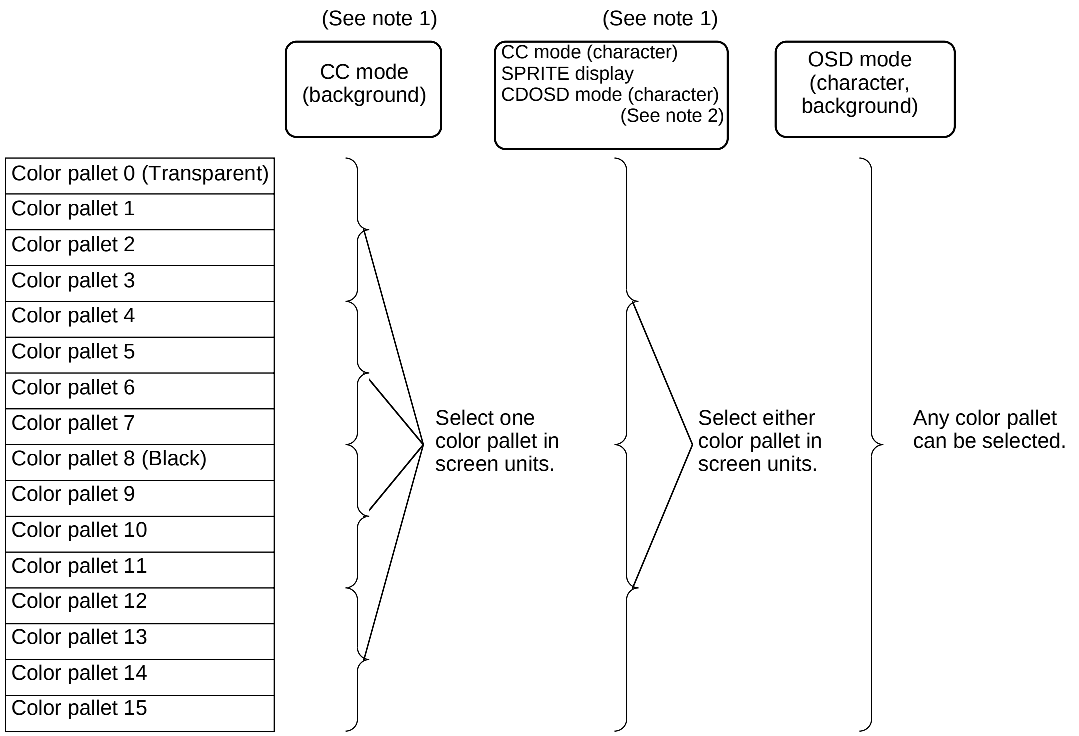
Notes 1: Color pallet 8 is always selected for bordering and solid space output (OUT 1 output) regardless of the set value in the register.
2: Color pallet 0 (transparent) and the transparent setting of other color pallets will differ. When there are multiple layers overlapping (on top of each other, piled up), and the priority layer is color pallet 0 (transparent), the bottom layer is displayed, but if the priority layer is the transparent setting of any other color pallet, the background is displayed without displaying the bottom layer (refer to Figure 8.11.26).

8.11.8 Character Background Color

The display area around the characters can be colored in with a character background color. Character background colors are set in character units.

- CC mode .... 4 kinds
  Color pallet selection range (color pallets 0 to 3, 4 to 7, 8 to 11, or 12 to 15) can be selected by bits 1 and 2 of the OSD control register 3 (address 0219_{16}). Color pallets are set by bits RC20 and RC21 of the OSD RAM from among the selection range.
- OSD mode .... 15 kinds
  Color pallets are set by bits RC15, RC16, RC20, and RC21 of the OSD RAM.

Note : The character background is displayed in the following part:
(character display area) – (character font) – (border).
Accordingly, the character background color and the color signal for these two sections cannot be mixed.



Notes 1: Color pallets are selected by OSD control register 3 (address 0219_{16}).
2: Only in CDOSD mode, a dot which selects color pallet 0 or 8 is colored to of OSD RAM in character units.

Fig. 8.11.24 Color Code Selection

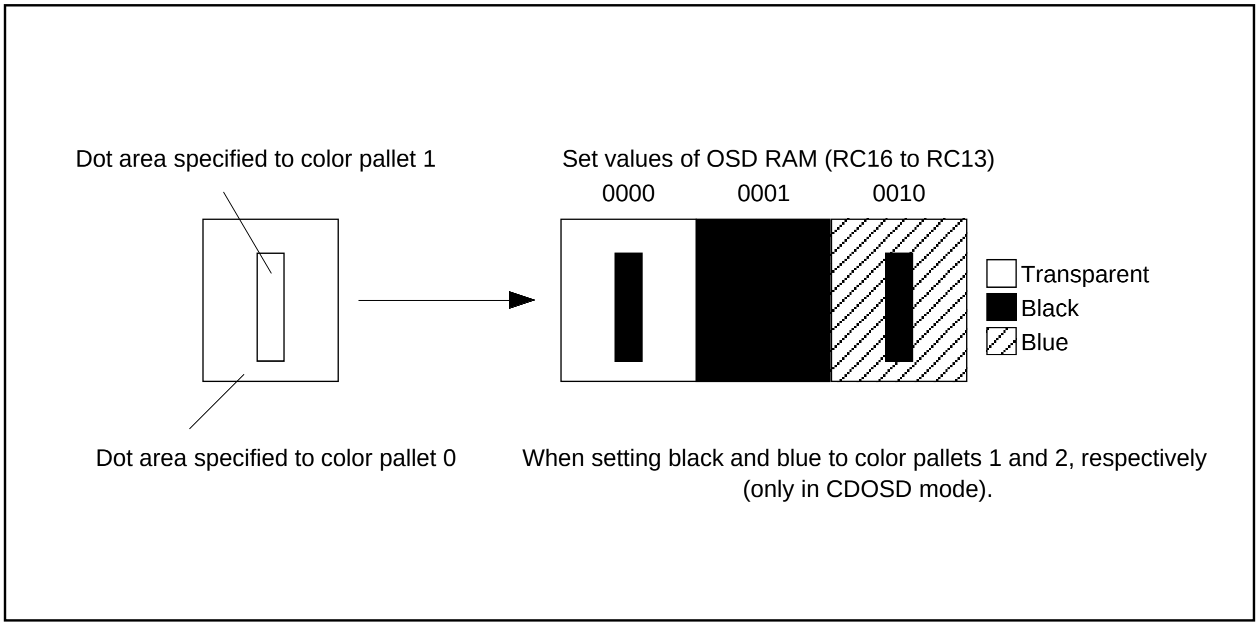


Fig. 8.11.25 Set of Color Pallet 0 or 8 in CDROM Mode

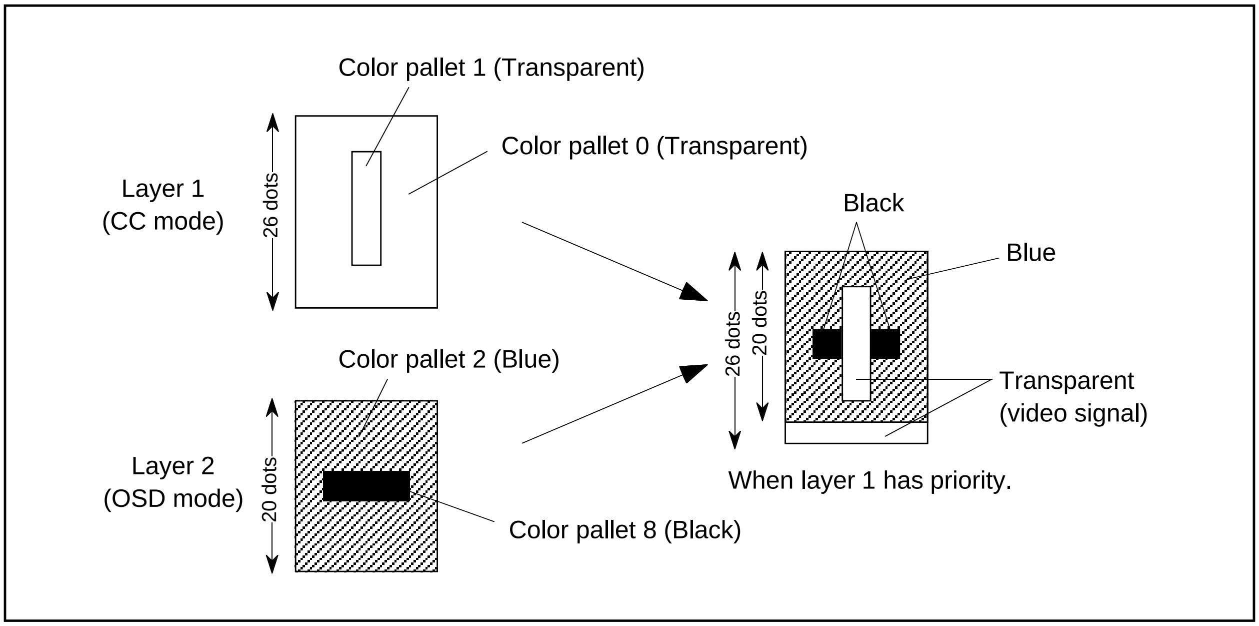


Fig. 8.11.26 Difference Between Color Code 0 (Transparent) and Transparent Setting of Other Color Codes

OSD Control Register 3

b7 b6 b5 b4 b3 b2 b1 b0

OSD control register 3 (OC3) [Address 0219₁₆]

B	Name	Functions	After reset	R	W
0	CC mode character color selection bit (OC30)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
1, 2	CC mode character background color selection bits (OC31, OC32) (See note)	b1 b1 0 0: Color code 0 to 3 0 1: Color code 4 to 7 1 0: Color code 8 to 11 1 1: Color code 12 to 15	0	R	W
3	CDOSD mode character color selection bit (OC33)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
4	SPRITE color selection bit (OC34)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
5	OSD mode window control bit (OC35)	0: Window OFF 1: Window ON	0	R	W
6	CC mode window control bit (OC36)	0: Window OFF 1: Window ON	0	R	W
7	CDOSD mode window control bit (OC37)	0: Window OFF 1: Window ON	0	R	W

Note: Color pallet 8 is always selected for solid space (when OUT1 output is selected), regardress of value of this register.

Fig. 8.11.27 OSD Control Register 3

Color Pallet Register i

b7 b6 b5 b4 b3 b2 b1 b0

Color pallet register i (CRi) (i = 1 to 7, 9to15) [Addresses 0241₁₆to 0247₁₆,0249₁₆to 024F₁₆]

B	Name	Functions	After reset	R	W
0, 1	R signal output control bits (CRi0, CRi1)	b0 b1 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R	W
2, 3	G signal output control bits (CRi2, CRi3)	b3 b2 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R	W
4, 5	B signal output control bits (CRi4, CRi5)	b5 b4 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R	W
6	OUT1 signal output control bit (CRi6)	0: No output 1: Output	Indeterminate	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—

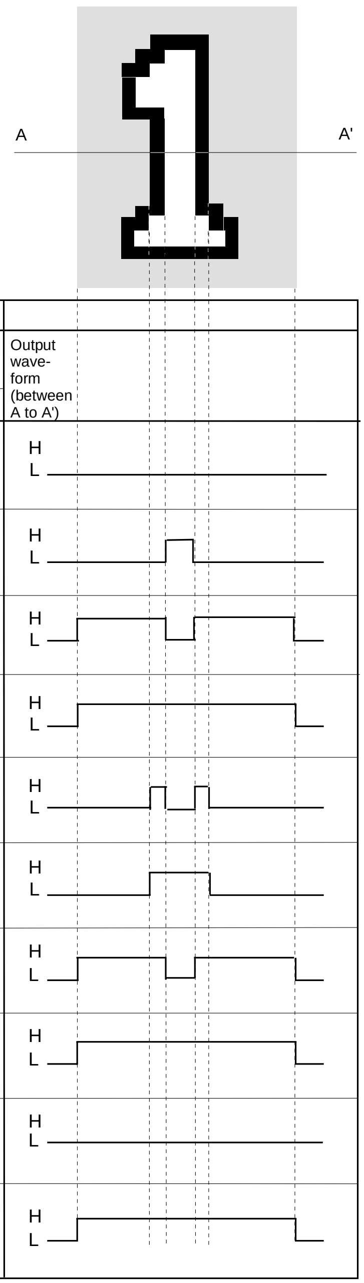
Note: When selecting digital output, the output is Vcc at all values other than "00."

Fig. 8.11.28 Color Pallet Register i (i = 1 to 7, 9 to 15)

8.11.9 OUT1, OUT2 Signals

The OUT1, OUT2 signals are used to control the luminance of the video signal. The output waveform of the OUT1, OUT2 signals is controlled by bit 6 of the color code register i (refer to Figure 8.11.28), bit 2 of the block control register i (refer to Figure 8.11.14) and RC17 of OSD RAM. The setting values for controlling OUT1, OUT2 and the corresponding output waveform is shown in Figure 12.11.29.

Note: When OUT2 signal is output, set bit 6 of OSD port control register (refer to Figure 8.11.56) to "1."



	Conditions: OUT2 output control (RC17 of OSD RAM)	Conditions: Border output control bit (See note 1) (Bit 2 of block control register i)	Conditions: OUT1 control bit (See note 2) (b6 of color pallet register i) Background	Conditions: OUT1 control bit (See note 2) (b6 of color pallet register i) Character	Output wave-form (between A to A')
OUT1 signal	×	0	0	0	
				1	
			1	0	
				1	
		1	0	0	
				1	
			1	0	
				1	
OUT2 signal	0	×	×	×	
	1	×	×	×	

Notes 1: This control is only valid in the OSD mode. It is invalid in CC/CDOSD mode .
2: In the CDOSD mode, coloring is performed for each dot. Accordingly, OUT1 outputs to dots which bit 6 (CRi6) of the color pallet register i is set to "0."
3: OUT2 cannot be output in sprite OSD.
4: × is an arbitrary value.

Fig. 8.11.29 Setting Value for Controlling OUT1, OUT2 and Corresponding Output Waveform

8.11.10 Attribute

The attributes (flash, underline, italic) are controlled to the character font. The attributes to be controlled are different depending on each mode.

CC mode .... Flash, underline, italic for each character
OSD mode .... Border (all bordered, shadow bordered can be selected) for each block

(1) Under line

The underline is output at the 23rd and 24th lines in vertical direction only in the CC mode. The underline is controlled by RC16 of OSD RAM. The color of underline is the same color as that of the character font.

(2) Flash

The parts of the character font, the underline, and the character background are flashed only in the CC mode. The flash is controlled by RC15 of OSD RAM. The ON/OFF for flash is controlled by bit 3 of the OSD control register 1 (refer to Figure 8.11.3). When this bit is “0”, only character font and underline flash. When “1”, for a character without solid space output, R, G, B and OUT1 (all display area) flash, for a character with solid space output, only R, G and B (all display area) flash. The flash cycle bases on the VSYNC count.

<NTSC method>

· VSYNC cycle ✕ 48 ≈ 800 ms (at flash ON)

· VSYNC cycle ✕ 16 ≈ 267 ms (at flash OFF)

(3) Italic

The italic is made by slanting the font stored in OSD ROM to the right only in the CC mode. The italic is controlled by RC14 of OSD RAM.

The display example of attribute is shown in Figure 8.11.30. In this case, “R” is displayed.

Notes 1: When setting both the italic and the flash, the italic character flashes.

2: When a flash character (with flash character background) adjoin on the right side of a non-flash italic character, parts out of the non-flash italic character is also flashed.

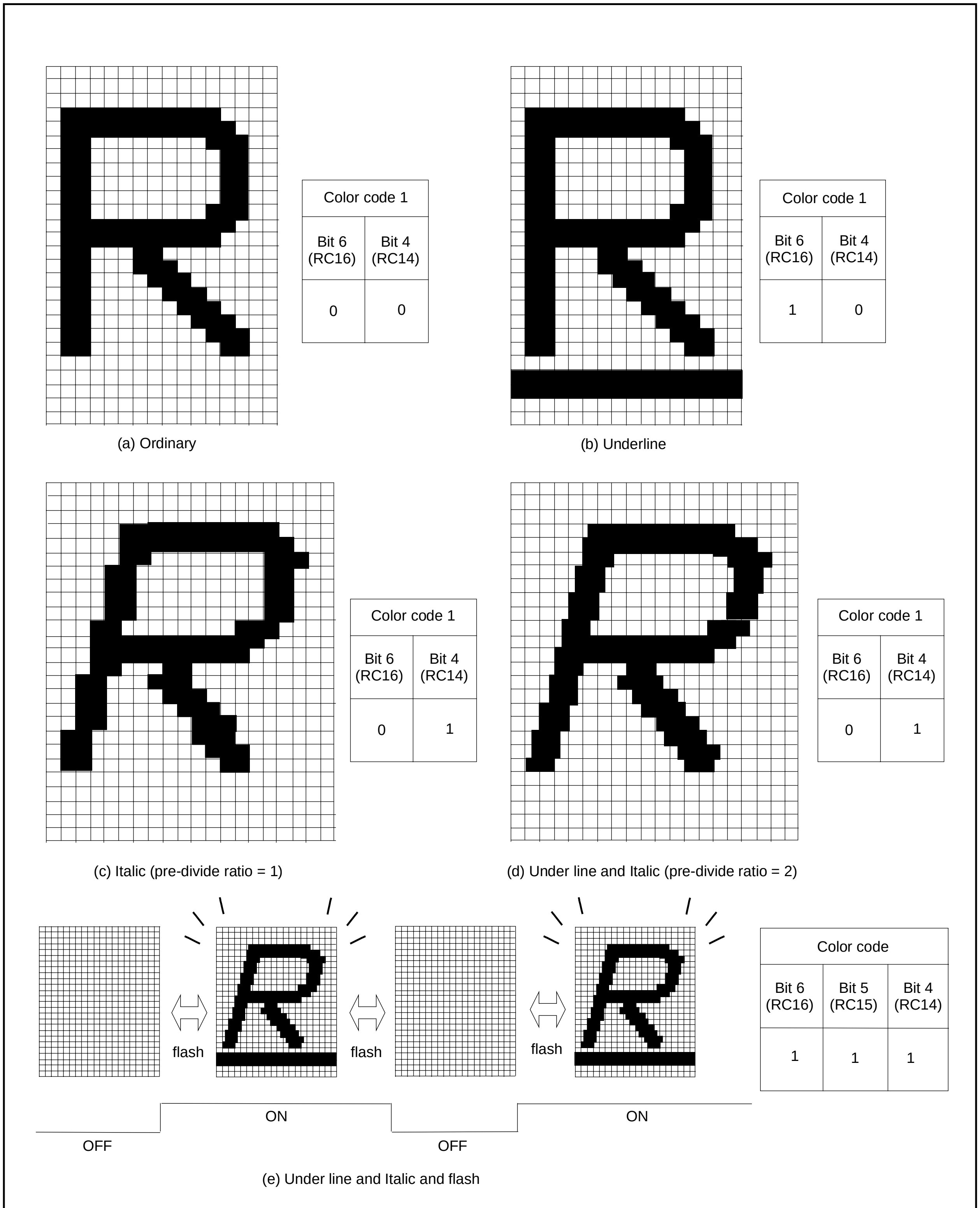
3: OUT2 is not flashed.

4: When the pre-divide ratio = 1, the italic character with slant of 1 dot ✕ 5 steps is displayed ; when thepre-divide ratio = 2, the italic character with slant of 1/2 dot ✕ 10 steps is displayed (refer to Figure 8.11.30 (c), (d)). However, when displaying the italic character with the pre-divide ratio = 1, set the OSD clock frequency to 11 MHz to 14 MHz.

5: The boundary of character color is displayed in italic. However, the boundary of character background color is not affected by the italic (refer to Figure 8.11.31).

6: The adjacent character (one side or both side) to an italic character is displayed in italic even when the character is not specified to display in italic (refer to Figure 8.11.31).

7: When displaying the 32nd character in the italic and when solid space is off (OC14 = “0”), parts out of character area is not displayed (refer to Figure 8.11.30).



(a) Ordinary

Color code 1	
Bit 6 (RC16)	Bit 4 (RC14)
0	0

(b) Underline

Color code 1	
Bit 6 (RC16)	Bit 4 (RC14)
1	0

(c) Italic (pre-divide ratio = 1)

Color code 1	
Bit 6 (RC16)	Bit 4 (RC14)
0	1

(d) Under line and Italic (pre-divide ratio = 2)

Color code 1	
Bit 6 (RC16)	Bit 4 (RC14)
0	1

(e) Under line and Italic and flash

Color code		
Bit 6 (RC16)	Bit 5 (RC15)	Bit 4 (RC14)
1	1	1

Fig. 8.11.30 Example of Attribute Display (in CC Mode)

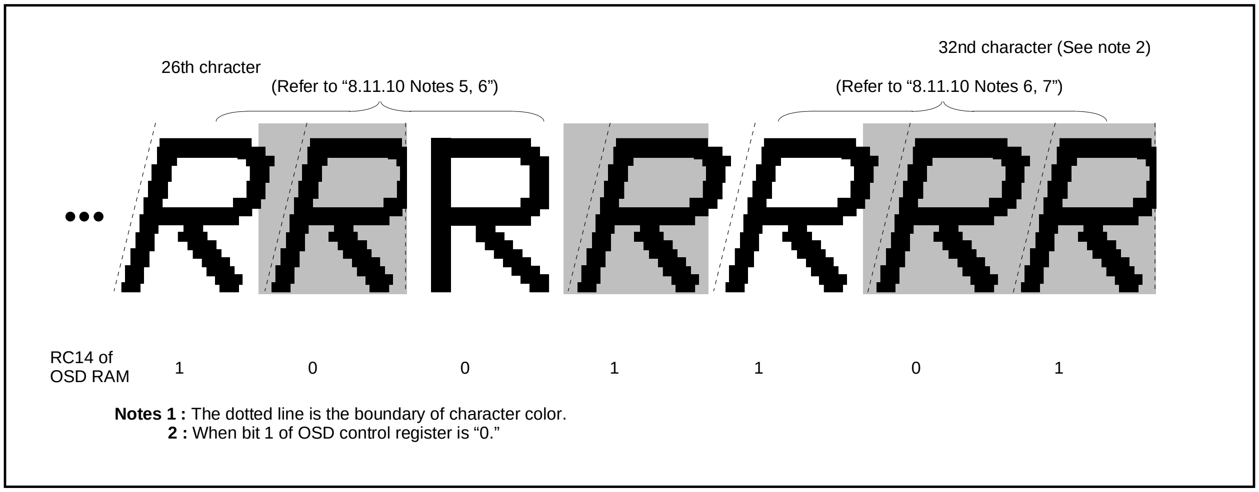


Fig. 8.11.31 Example of Italic Display

(4) Border

The border is output only in the OSD mode. The all bordered (bordering around of character font) and the shadow bordered (bordering right and bottom sides of character font) are selected (refer to Figure 8.11.32) by bit 2 of the OSD control register 1 (refer to Figure 8.11.3). The ON/OFF switch for borders can be controlled in block units by bit 2 of the block control register i (refer to Figure 8.11.4).

The OUT1 signal is used for border output. The border color is fixed at color code 8 (block). The border color for each screen is specified by the border color register i.

The horizontal size (x) of border is 1Tc (OSD clock cycle divided in the pre-divide circuit) regardless of the character font dot size. However, only when the pre-divide ratio = 2 and character size = 1.5Tc, the horizontal size is 1.5Tc. The vertical size (y) different depending on the screen scan mode and the vertical dot size of character font.

Notes 1: The border dot area is the shaded area as shown in Figure 8.11.34.

2: When the border dot overlaps on the next character font, the character font has priority (refer to Figure 8.11.35 A). When the border dot overlaps on the next character back ground, the border has priority (refer to Figure 8.11.35 B).

3: The border in vertical out of character area is not displayed (refer to Figure 8.11.35).

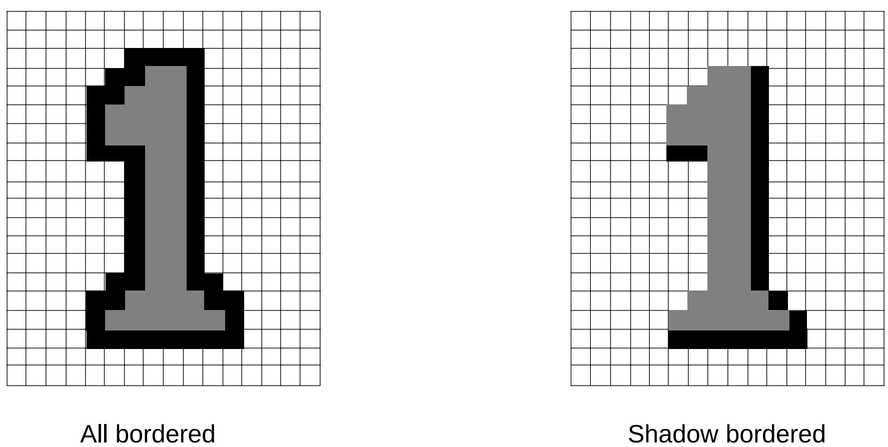
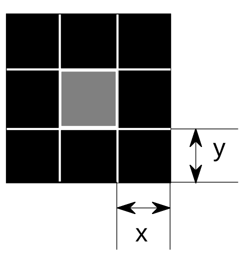


Fig. 8.11.32 Example of Border Display



Scan mode / Border dot size \ Vertical dot size of character font	Normal scan mode		Bi-scan mode
	1/2H	1H, 2H, 3H	1/2H, 1H, 2H, 3H
Horizontal size (x)	1Tc (OSD clock cycle divided in pre-divide circuit) 1.5Tc when selecting 1.5Tc for character size.		
Vertical size (y)	1/2H	1H	1H

Fig. 8.11.33 Horizontal and Vertical Size of Border

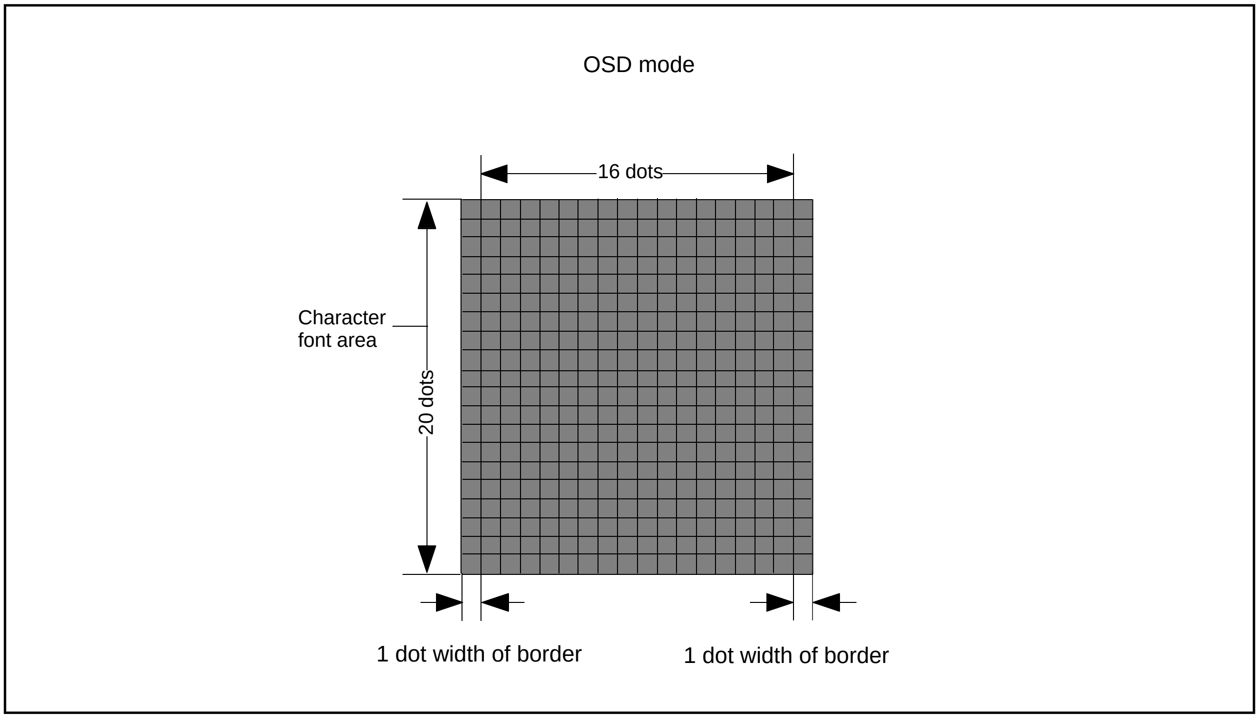


Fig. 8.11.34 Border Area

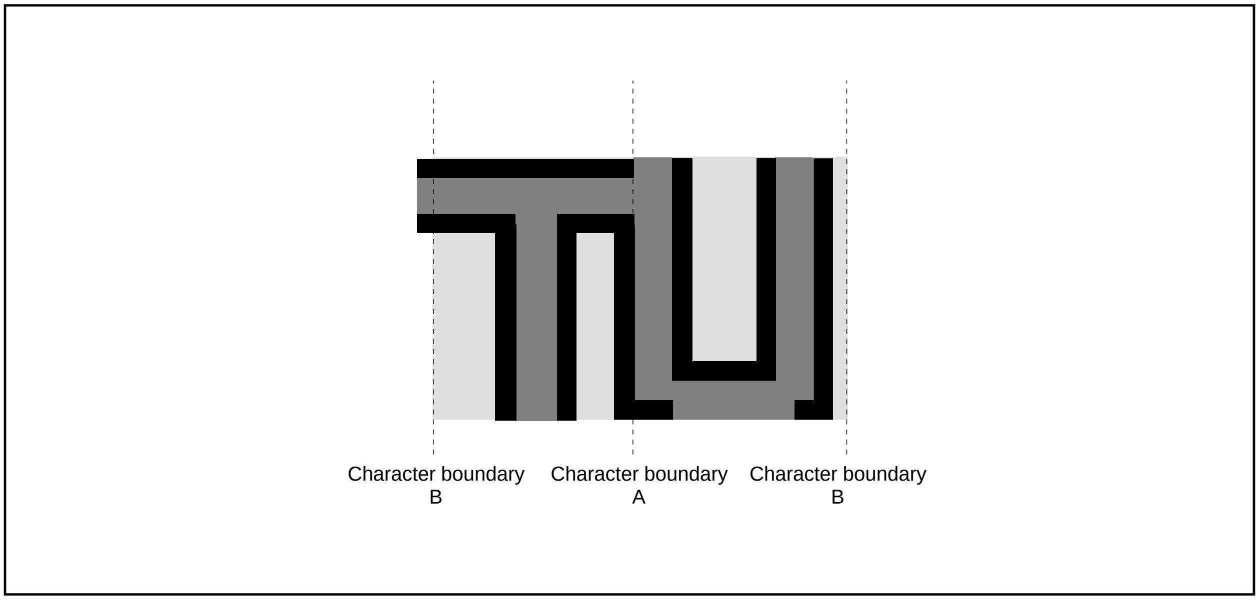


Fig. 8.11.35 Border Priority

8.11.11 Automatic Solid Space Function

This function generates automatically the solid space (OUT1 or OUT2 blank output) of the character area in the CC mode.

The solid space is output in the following area :

- Any character area except character code “009_{16} ”
- Character area on the left and right sides of the above character

This function is turned on and off by bit 4 of the OSD control register 1 (refer to Figure 8.11.3).

And the OUT1 output or OUT2 output can be selected by bit 3 of OSD control register 2.

Note: When selecting OUT1 as solid space output, character background color with solid space output is fixed to color pallet 8 (black) regardless of setting.

Table 8.11.8 Setting for Automatic Solid Space

Bit 4 of OSD Control Register 1	0				1			
Bit 3 of OSD Control Register 2	0		1		0		1	
RC17 of OSD RAM	0	1	0	1	0	1	0	1
OUT1 Output Signal	•Character font area •Character background area		•Character font area •Character background area		•Solid space area		•Character font area •Character background area	
OUT2 Output Signal	OFF	•Character display area	OFF	•Character display area	OFF	•Character display area	OFF	•Solid space •Character display area

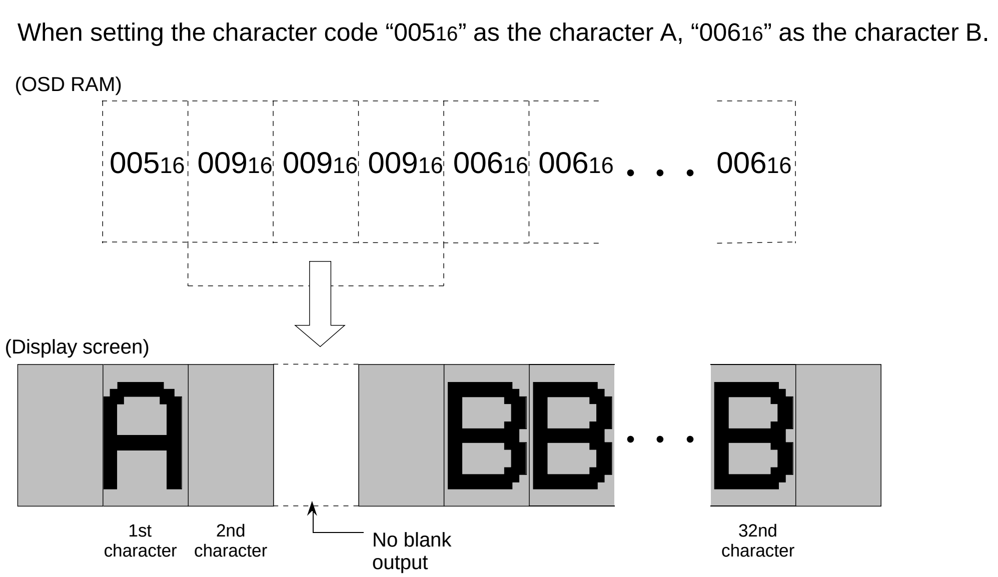


Fig. 8.11.36 Display Screen Example of Automatic Solid Space

8.11.12 Multiline Display

This microcomputer can ordinarily display 16 lines on the CRT screen by displaying 16 blocks at different vertical positions. In addition, it can display up to 16 lines by using OSD interrupts.

An OSD interrupt request occurs at the point at which display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical position registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block. The mode in which an OSD interrupt occurs is different depending on the setting of the OSD control register 2 (refer to Figure 8.11.7).

- When bit 7 of the OSD control register 2 is “0”

  An OSD interrupt request occurs at the completion of layer 1 block display.
- When bit 7 of the OSD control register 2 is “1”

  An OSD interrupt request occurs at the completion of layer 2 block display.

Notes 1: An OSD interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to off display by the display control bit of the block control register i (addresses $00D0_{16}$ to $00DF_{16}$), an OSD interrupt request does not occur (refer to Figure 8.11.37 (A)).

2: When another block display appeares while one block is displayed, an OSD interrupt request occurs only once at the end of the another block display (refer to Figure 8.11.37 (B)).

3: On the screen setting window, an OSD interrupt occurs even at the end of the CC mode block (off display) out of window (refer to Figure 8.11.37 (C)).

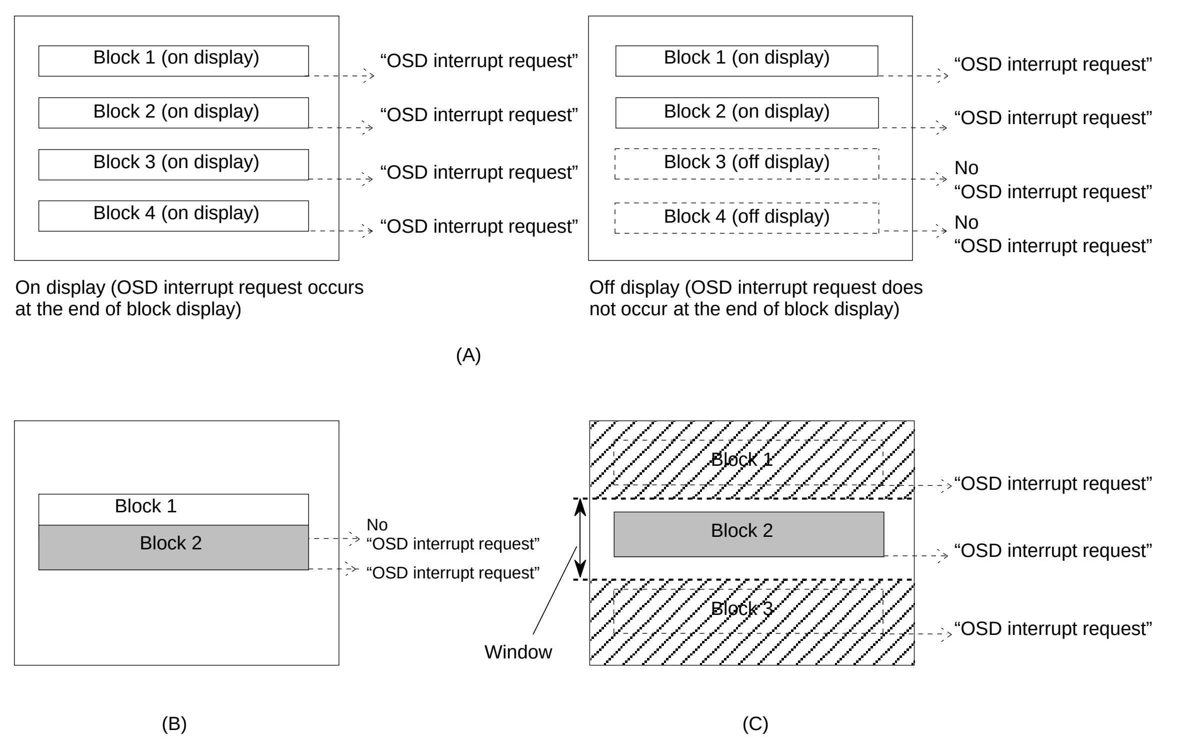


Fig. 8.11.37 Note on Occurence of OSD Interrupt

8.11.13 SPRITE OSD Function

This is especially suitable for cursor and other displays as its function allows for display in any position, regardless of the validity of other OSDs or display positions. The SPRITE font is a RAM font consisting of 16 horizontal dots × 20 vertical dots, three planes, and three bits of data per dot. Each plane has corresponding color pallet selection bits, and 8 kinds of color pallets can be selected by the plane bit combination (three bits) for each dot. In addition, the selection range (color pallets 0 to 7 and 8 to 15) can be set, per screen, by bit 4 of the OSD control register 3. The color pallet is set in dot units according to the selection range and the OSD RAM (SPRITE) contents from among the selection range. It is possible to arbitrarily add font data by software for the RAM font in the SPRITE font.

The SPRITE OSD control register can control SPRITE display, dot size, interrupt position, and interrupt generation factors for the SPRITE OSD. The display position can also be set independently of the block display by the SPRITE horizontal position registers and the SPRITE horizontal vertical position registers. At this time, the horizontal position is set in 2048 steps in 1T_{OSC} units, and the vertical position is set in 1024 steps in 1T_H units. When SPRITE display overlaps with other OSDs, SPRITE display is always given priority. However, the SPRITE display overlaps with the OSD which includes OUT2 output, OUT2 in the OSD is output without masking.

Notes 1: The SPRITE OSD function cannot output OUT2.
2: When using SPRITE OSD, do not set HS1 < "30_{16}" at HS2 = "00_{16}."
3: When using SPRITE OSD, do not set VS = VS = "00_{16}."

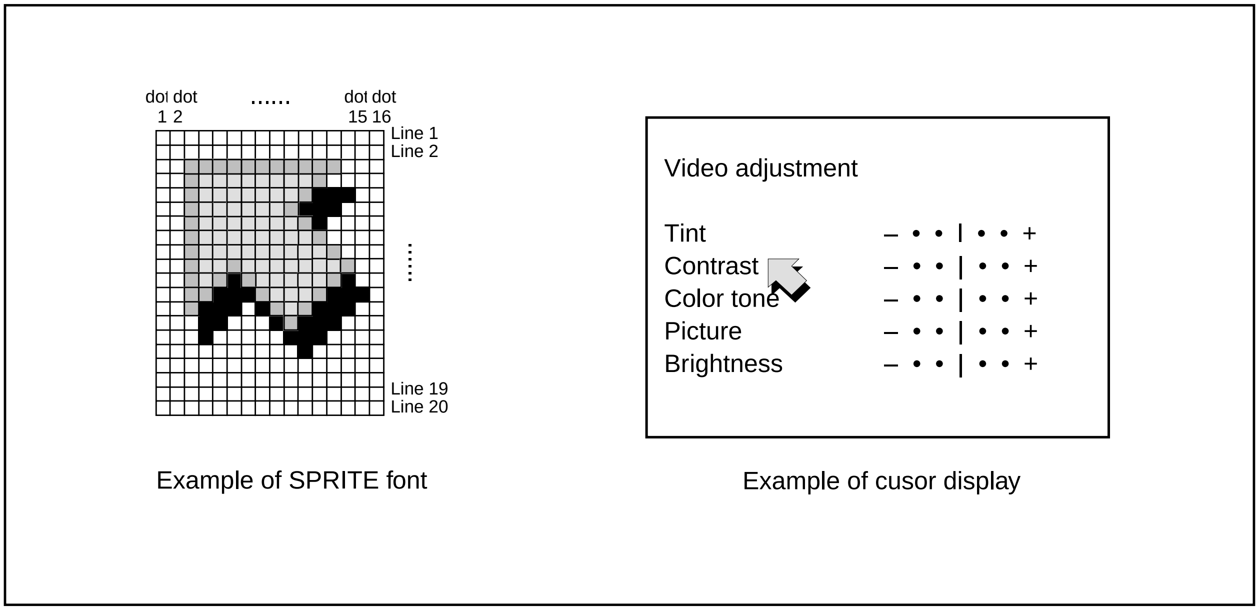


Fig. 8.11.38 SPRITE OSD Display Example

SPRITE OSD Control Register

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE OSD control register (SC) [Address 0258_{16}]

B	Name	Functions	After reset	R	W
0	SPRITE OSD control bit (SC0)	0: Stopped 1: Operating	0	R	W
1	Pre-divide ratio selection bit (SC1)	0: Pre-divide ratio 1 1: Pre-divide ratio 2	0	R	W
2, 3	Dot size selection bits (SC2, SC3)	b3 b2 0 0: 1Tc ✕ 1/2H 0 1: 1Tc ✕ 1H 1 0: 2Tc ✕ 1H 1 1: 2Tc ✕ 2H	0	R	W
4	Interrupt occurrence position selection bit (SC4)	0: After display of horizontal 20 dots 1: After display of horizontal 10 dots or 20 dots	0	R	W
5	X_{IN}/4096 • SPRITE interrupt source switch bit (SC5)	0: X_{IN}/4096 interrupt 1: SPRITE OSD interrupt	0	R	W
6, 7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0”.		0	R	—

Notes 1: Tc : Pre-devided clock period for OSD
2: H : H_{SYNC}

Fig. 8.11.39 SPRITE OSD Control Register

SPRITE Horizontal Position Register 1

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE horizontal position register 1 (HS1) [Address 0256_{16}]

B	Name	Functions	After reset	R	W
0 to 7	Horizontal display start position control bits of SPRITE OSD (HS10 toHS17)	Horizontal display start position (low-order 8 bits) TOSC × (setting value of low-order 3 bits of HS2 ×16^2 + setting value of high-order 4 bits of HS1 ×16^1 + setting value of low-order 4 bits of HS1 ×16^0)	Indeterminate	R	W

Notes 1: Do not set HS1 < “30_{16}” at HS2 = “00_{16}.”
2: TOSC is OSD oscillation period.
3: HS2 is SPRITE horizontal position register 2.

Fig. 8.11.40 SPRITE Horizontal Position Register 1

SPRITE Horizontal Position Register 2

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE horizontal position register 2 (HS2) [Address 0257_{16}]

B	Name	Functions	After reset	R	W
0 to 2	Horizontal display start position control bits of SPRITE OSD (HS20 to HS22)	Horizontal display start position (high-order 3 bits) TOSC × (setting value of low-order 3 bits of HS2 × 16^2 + setting value of high-order 4 bits of HS1 × 16^1 + setting value of low-order 4 bits of HS1 × 16^0)	Indeterminate	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Notes 1: Do not set HS1< “30_{16}” at HS2 = “00_{16}.”
2: TOSC is oscillation period.
3: HS1 is SPRITE horizontal position register 1.

Fig. 8.11.41 SPRITE Horizontal Position Register 2

SPRITE Vertical Position Register 1

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE vertical position register 1 (VS1) [Address 0254$_{16}$]

B	Name	Functions	Afte reset	R	W
0	Vertical display start position control bits of SPRITE OSD (VS10 to VS17)	Vertical display start position (low-order 8 bits) TH × (setting value of low-order 2 bits of VS2 × 16^2 + setting value of high-order 4 bits of VS1 × 16^1 + setting value of low-order 4 bits of VS1 × 16^0)	1	R	W
1 to 7			0		

Notes 1: Do not set "00$_{16}$" to the VS1 at VS2 = "00$_{16}$."
2: T_H is cycle of HSYNC.
3: VS2 is SPRITE vertical position register 2.

Fig. 8.11.42 SPRITE Vertical Position Register 1

SPRITE Vertical Position Register 2

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE vertical position register 2 (VS2) [Address 0255$_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Vertical start position control bits of SPRITE OSD (VS20, VS21)	Vertical display start position (high-order 2 bits) T_H × (setting value of low-order 2 bits of VS2 ×16^2 + setting value of high-order 4 bits of VS1 ×16^1 + setting value of low-order 4 bits of VS1 ×16^0)	0	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0".		0	R	—

Notes 1: Do not set "00$_{16}$" to the VS1 at VS2 = "00$_{16}$."
2: T_H is cycle of HSYNC.
3: VS1 is SPRITE vertical position register 1.

Fig. 8.11.43 SPRITE Vertical Position Register 2

RENESAS

8.11.14 Window Function

The window function can be set windows on-screen, and output OSD within only the area where the window is set.
The ON/OFF for vertical window function is performed by bit 5 of OSD control register 1 and is used to select vertical window function or vertical blank function by bit 6 of OSD control register 2. Accordingly, the vertical window function cannot be used simultaneously with the vertical blank function. The display mode to validate the window function is selected by bits 5 to 7 of OSD control register 3. The top boundary is set by top border control registers 1, 2 (TB1, TB2) and the bottom boundary is set by bottom border control registers 1, 2 (BB1, BB2).
The ON/OFF for horizontal window function is performed by bit 4 of OSD control register 2 and is used interchangeably for the horizontal blank function with bit 5 of OSD control register 2. Accordingly, the horizontal blank function cannot be used simultaneously with the horizontal window function. The display mode to validate the window function is selected by bits 5 to 7 of OSD control register 3. The left boundary is set by left border control registers 1, 2 (LB1, LB2), and the right boundary is set by right border control registers 1, 2 (RB1, RB2).

Notes 1: Horizontal blank and horizontal window, as well as vertical blank and vertical window can not be used simultaneously.
2: When the window function is ON by OSD control registers 1 and 2, the window function of OUT2 is valid in all display mode regardless of setting value of OSD control register 3 (bits 5 to 7). For example, even when make the window function valid in only CC mode, the function of OUT2 is valid in OSD and CDOSD modes.
3: The SPRITE display is not effected by the window function.

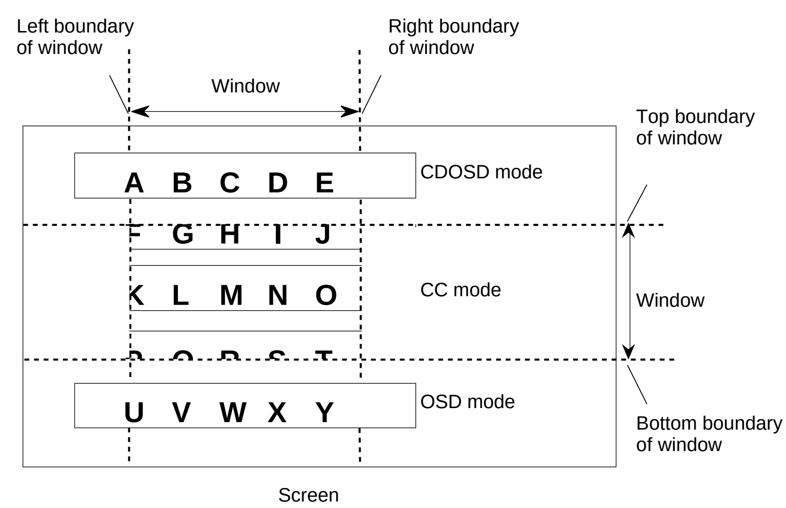


Fig. 8.11.44 Example of window function (When CC Mode Is Valid)

8.11.15 Blank Function

The blank function can output blank (OUT1) area on all sides (vertical and horizontal) of the screen.

The ON/OFF for vertical blank function is performed by bit 5 of the OSD control register 1 and is used to select vertical window function or vertical blank function by bit 6 of the OSD control register 2. Accordingly, the vertical blank function cannot be used simultaneously with the vertical window function. The top border is set by the top border control registers 1, 2 (TB1, TB2) and the bottom border is set by the bottom border control registers 1, 2 (BB1, BB2), in 1H units.

The ON/OFF for horizontal blank function is performed by bit 4 of the OSD control register 2 and is used interchangeably for the horizontal window function with bit 5 of the OSD control register 2 . Accordingly, the horizontal blank function cannot be used simultaneously with the horizontal window function. The left border is set by the left border control registers 1, 2 (LB1, LB2) and the right border is set by the right border control registers 1, 2 (RB1, RB2), in 1TOSC units.

The OSD output (except raster) in area with blank output is not deleted.

These blank signals are not output in the horizontal/vertical blanking interval.

Notes 1: Horizontal blank and horizontal window, as well as vertical blank and vertical window cannot be used simultaneously.

2: When all-blocks display is OFF (bit 0 of OSD control register 1 = “0”), do not use vertical blank.

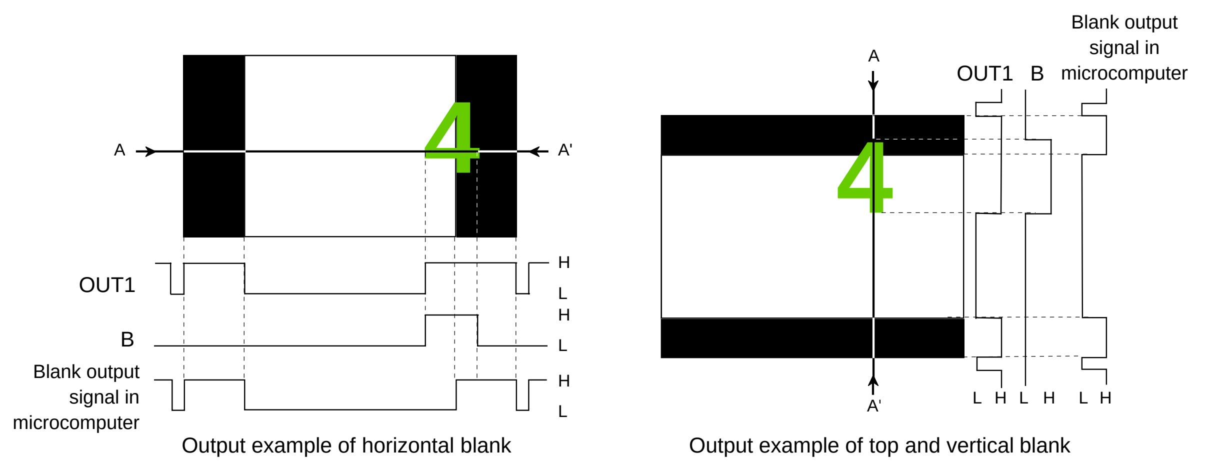


Fig. 8.11.45 Blank Output Example (When OSD Output is B + OUT1)

Top Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Top border control register 1 (TB1) [Address 021C16]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of top border (TB10 to TB17)	Top border position (low-order 8 bits) TH × (setting value of low-order 2 bits of TB2 × 16^2 + setting value of high-order 4 bits of TB1 ×16^1 + setting value of low-order 4 bits of TB1 ×16^0)	Indeterminate	R	W

Notes 1: Do not set “0016” or “0116” to the TB1 at TB2 = “00 16.”
2: TH is cycle of HSYNC.
3: TB2 is top border control register 2.

Fig. 8.11.46 Top Border Control Register 1

Top Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Top border control register 2 (TB2) [Address 021E16]

B	Name	Functions	After reset	R	W
0, 1	Control bits of top border (TB20 ,TB21)	Top border position (high-order 2 bits) TH × (setting value of low-order 2 bits of TB2 ×16^2 + setting value of high-order 4 bits of TB1 ×16^1 + setting value of low-order 4 bits of TB1 ×16^0)	Indeterminate	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R	—

Notes 1: Do not set “0016” or “0116” to the TB1 at TB2 = “00 16.”
2: TH is cycle of HSYNC.
3: TB1 is top border control register 1.

Fig. 8.11.47 Top Border Control Register 2

Bottom Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Bottom border control register 1 (BB1) [Address $021D_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of bottom border (BB10 to BB17)	Bottom border position (low-order 8 bits) $T_H \times$ (setting value of low-order 2 bits of BB2 $\times 16^2$ + setting value of high-order 4 bits of BB1 $\times 16^1$ + setting value of low-order 4 bits of BB1 $\times 16^0$)	Indeterminate	R	W

Notes 1: Set values fit for the following condition:
$(TB1 + TB2 \times 16^2) < (BB1 + BB2 \times 16^2)$.
2: T_H is cycle of HSYNC.
3: BB2 is bottom border control reigster 2.

Fig. 8.11.48 Bottom Border Control Register 1

Bottom Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Bottom border control register 2 (BB2) [Address $021F_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Control bits of bottom border (BB20, BB21)	Bottom border position (high-order 2 bits) $T_H \times$ (setting value of low-order 2 bits of BB2 $\times 16^2$ + setting value of high-order 4 bits of BB1 $\times 16^1$ + setting value of low-order 4 bits of BB1 $\times 16^0$)	Indeterminate	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R	—

Notes 1: Set values fit for the following condition:
$(TB1 + TB2 \times 16^2) < (BB1 + BB2 \times 16^2)$.
2: T_H is cycle of HSYNC.
3: BB1 is bottom border control reigster 1.

Fig. 8.11.49 Bottom Border Control Register 2

Left Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Left border control register 1 (LB1) [Address 0250_{16}]

B	Name	Functions	After reset	R	W
0	Control bits of left border (LB10 to LB17)	Left border position (low-order 8 bits) Tosc × (setting value of low-order 3 bits of LB2 ×16^2 + setting value of high-order 4 bits of LB1 ×16^1 + setting value of low-order 4 bits of LB1 ×16^0)	1	R	W
1 to 7			0		

Notes 1: Do not set LB1 = LB2 = "00_{16}."
2: Set values fit for the following condition:
(LB1 + LB2 × 16^2) < (RB1 + RB2 × 16^2).
3: Tosc is OSD oscillation period.
4: LB2 is left border control register 2.

Fig. 8.11.50 Left BorderControl Register 1

Left Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Left border controlregister 2 (LB2) [Address 0251_{16}]

B	Name	Functions	After reset	R	W
0 to 2	Control bits of left border (LB20 to LB22)	Left borderposition (high-order 3 bits) Tosc × (setting value of low-order 3 bits of LB2 ×16^2 + setting value of high-order 4 bits of LB1 ×16^1 + setting value of low-order 4 bits of LB1 ×16^0)	0	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		0	R	W

Notes 1: Do not set LB1 = LB2 = "00_{16}."
2: Set values fit for the following condition:
(LB1 + LB2 × 16^2) < (RB1 + RB2 × 16^2).
3: Tosc is OSD oscillation period.
4: LB1 is left border control register 1.

Fig. 8.11.51 Left BorderControl Register 2

Right Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Right border control register 1 (RB1) [Address 0252_{16}]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of right border (RB10 to RB17)	Right border position (low-order 8 bits) Tosc × (setting value of low-order 3 bits of RB2 × 16^2 + setting value of high-order 4 bits of RB1 × 16^1 + setting value of low-order 4 bits of RB1 × 16^0)	1	R	W

Notes 1: Set values fit for the following condition:
(LB1 + LB2 × 16^2) < (RB1 + RB2 × 16^2).
2: Tosc is OSD oscillation period.
3: RB2 is right border control register 2.

Fig. 8.11.52 Right Border Control Register 1

Right Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Right border control register 2 (RB2) [Address 0253_{16}]

B	Name	Functions	After reset	R	W
0 to 2	Control bits of right border (RB20 to RB22)	Right border position (high-order 3 bits) Tosc× (setting value of low-order 3 bits of RB2 × 16^2 + setting value of high-order 4 bits of RB1 × 16^1 + setting value of low-order 4 bits of RB1 × 16^0)	1	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0”.		0	R	W

Notes 1: Set values fit for the following condition:
(LB1 + LB2 × 16^2) < (RB1 + RB2 × 16^2).
2: Tosc is OSD oscillation period.
3: RB1 is right border control register 1.

Fig. 8.11.53 Right Border Control Register 2

8.11.16 Raster Coloring Function

An entire screen (raster) can be colored by setting the bits 6 to 0 of the raster color register. Since each of the R, G, B, OUT1, and OUT2 pins can be switched to raster coloring output, 64 raster colors can be obtained.

When the character color/the character background color overlaps with the raster color, the color (R, G, B, OUT1, OUT2),specified for the character color/the character background color, takes priority of the raster color. This ensures that the character color/the character background color is not mixed with the raster color.

The raster color register is shown in Figure 8.11.54, the example of raster coloring is shown in Figure 8.11.55.

Note : Raster is not output to the area which includes blank output.

Raster Color Register

b7 b6 b5 b4 b3 b2 b1 b0

Raster color register (RC) [Address 0218₁₆]

B	Name	Functions	At reset	R	W
0, 1	Raster color R control bits (RC0, RC1)	b0 b1 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
2, 3	Raster color G control bits (RC2, RC3)	b3 b2 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
4, 5	Raster color B control bits (RC4, RC5)	b5 b4 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
6	Raster color OUT1 control bits (RC6)	0: No output 1: Output	0	R	W
7	Raster color OUT2 0 control bits (RC7)	0: No output 1: Output	0	R	W

Note: When selecting digital output, Vcc is output at any other values except "00."

Fig. 8.11.54 Raster Color Register

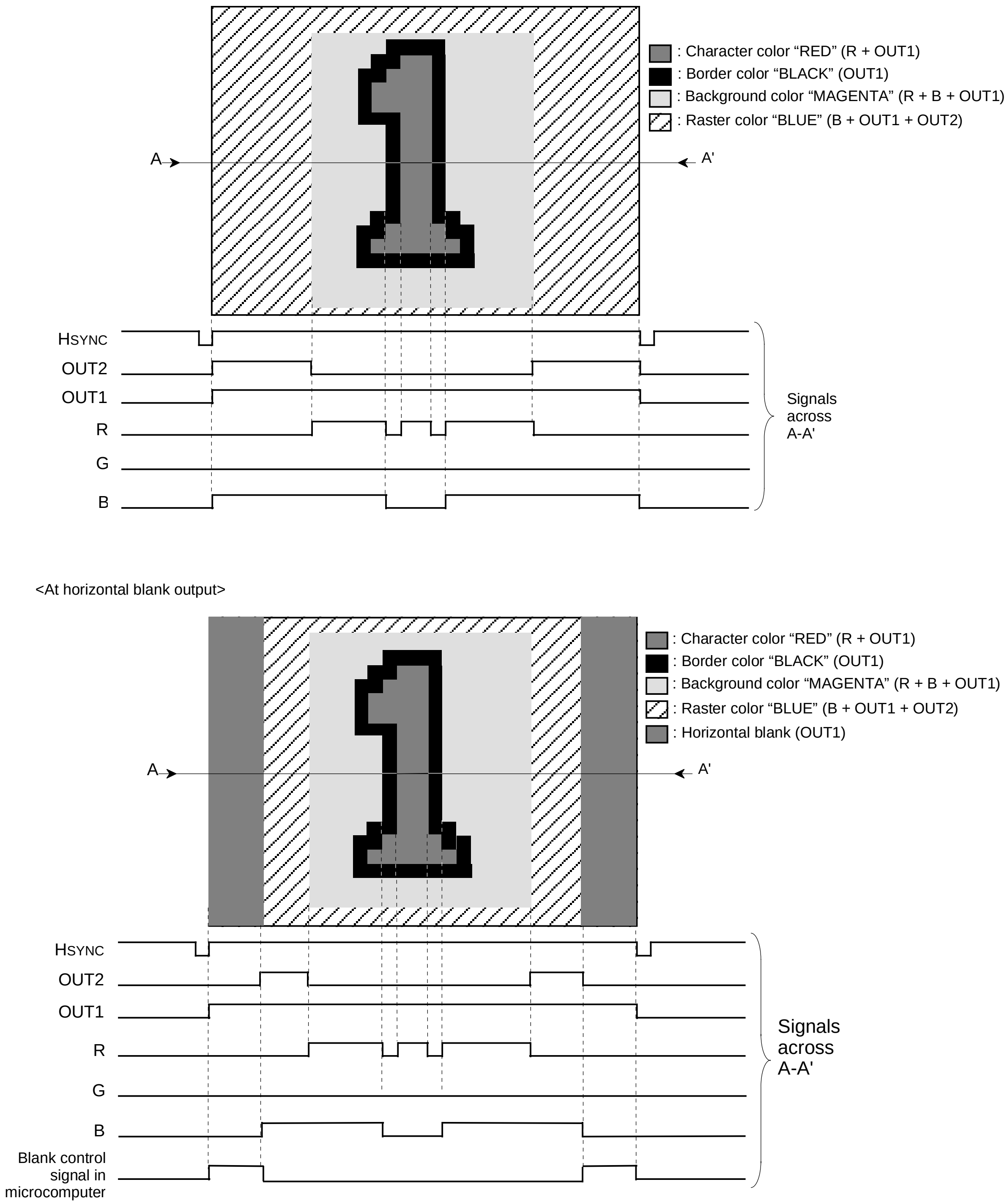


Fig. 8.11.55 Example of Raster Coloring

8.11.17 Scan Mode

This microcomputer has the bi-scan mode for corresponding to HSYNC of double speed frequency. In the bi-scan mode, the vertical start display position and the vertical size is two times as compared with the normal scan mode. The scan mode is selected by bit 1 of the OSD control register 1 (refer to Figure 8.11.3).

Table 8.11.9 Setting for Scan Mode

Parameter \ Scan Mode	Normal Scan	Bi-Scan
Bit 1 of OSD Control Register 1	0	1
Vertical Display Start Position	Value of vertical position register × 1H	Value of vertical position register × 2H
Vertical Dot Size	1TC × 1/2H 1TC × 1H 2TC × 2H 3TC × 3H	1TC × 1H 1TC × 2H 2TC × 4H 3TC × 6H

8.11.18 OSD Output Pin Control

The OSD output pins R(R1), G(G1), B(B1) and OUT1 can also function as ports $P5_2$ to $P5_5$. Set the corresponding bit of the OSD port control register (address $00CB_{16}$) to “0” to specify these pins as OSD output pins, or set it to “1” to specify it as a general-purpose port P5 pin.
Pins R0, G0 and B0 can also function as ports $P1_7$, $P1_5$ and $P1_6$, respectively. Set bit 1 of the OSD port control register to “0” to specify these pins as a general-purpose output port P1 pin, or set it to “1” to specify it as OSD output pins. When “0,” 4-adjustment-level analog output is output from pins R, G and B. When “1,” the value which is converted from the analog to the 2-bit digital is output as follows: the high-order bit is output pins R1, G1 and B1 and the low-order bit is output from pins R0, G0 and B0.
The OUT2 can also function as Port $P1_0$. Set bit 0 of the port P1 direction register (address $00C3_{16}$) to “1” (output mode). After that, set bit 6 of the OSD port control register to “1” to specify the pin as OSD output pin, or set it to “0” to specify as port $P1_0$ pin.
The input polarity of the HSYNC, VSYNC and output polarity of signals R, G, B, OUT1 and OUT2 can be specified with the I/O polarity control register (address 0217_{16}). Set a bit to “0” to specify positive polarity; set it to “1” to specify negative polarity (refer to Figure 8.11.18).
The OSD port control register is shown in Figure 8.11.56.

Note: When using ports $P5_2$ to $P5_4$ as general-purpose pins, set bit 2 of OSD control register 2 (address 0215_{16}) to “0.”

OSD Port Control Register

b7 b6 b5 b4 b3 b2 b1 b0: 0 _ _ _ _ _ _ 0

OSD port control register (PF) [Address $00CB_{16}$]

b	Name	Functions	After reset	R W
0	Fix this bit to “0”		0	R W
1	R, G, B output method selection bit (RGB2BIT)	0 : 4-adjustment-level analog is output from pins R, G, B. 1 : Value which is converted from 4-adjustment-level analog to 2-bit digital is output as below: High-order: from R1, G1, B1 Low-order: from R0, G0, B0	0	R W
2	Port $P5_2$ output signal selection bit (R)	0 : R signal output 1 : Port $P5_2$ output	0	R W
3	Port $P5_3$ output signal selection bit (G)	0 : G signal output 1 : Port $P5_3$ output	0	R W
4	Port $P5_4$ output signal selection bit (B)	0 : B signal output 1 : Port $P5_4$ output	0	R W
5	Port $P5_5$ output signal selection bit (OUT1)	0 : OUT1 signal output 1 : Port $P5_5$ output	0	R W
6	Port $P1_0$ output signal selection bit (OUT2)	0 : Port $P1_0$ signal output 1 : OUT2 output	0	R W
7	Fix this bit to “0”		0	R W

Fig. 8.11.56 OSD Port Control Register

8.12. SOFTWARE RUNAWAY DETECT FUNCTION

This microcomputer has a function to decode undefined instructions to detect a software runaway.

When an undefined op-code is input to the CPU as an instruction code during operation, the following processing is done.

① The CPU generates an undefined instruction decoding signal.

② The device is internally reset because of occurrence of the undefined instruction decoding signal.

③ As a result of internal reset, the same reset processing as in the case of ordinary reset operation is done, and the program restarts from the reset vector.

Note, however, that the software runaway detecting function cannot be invalid.

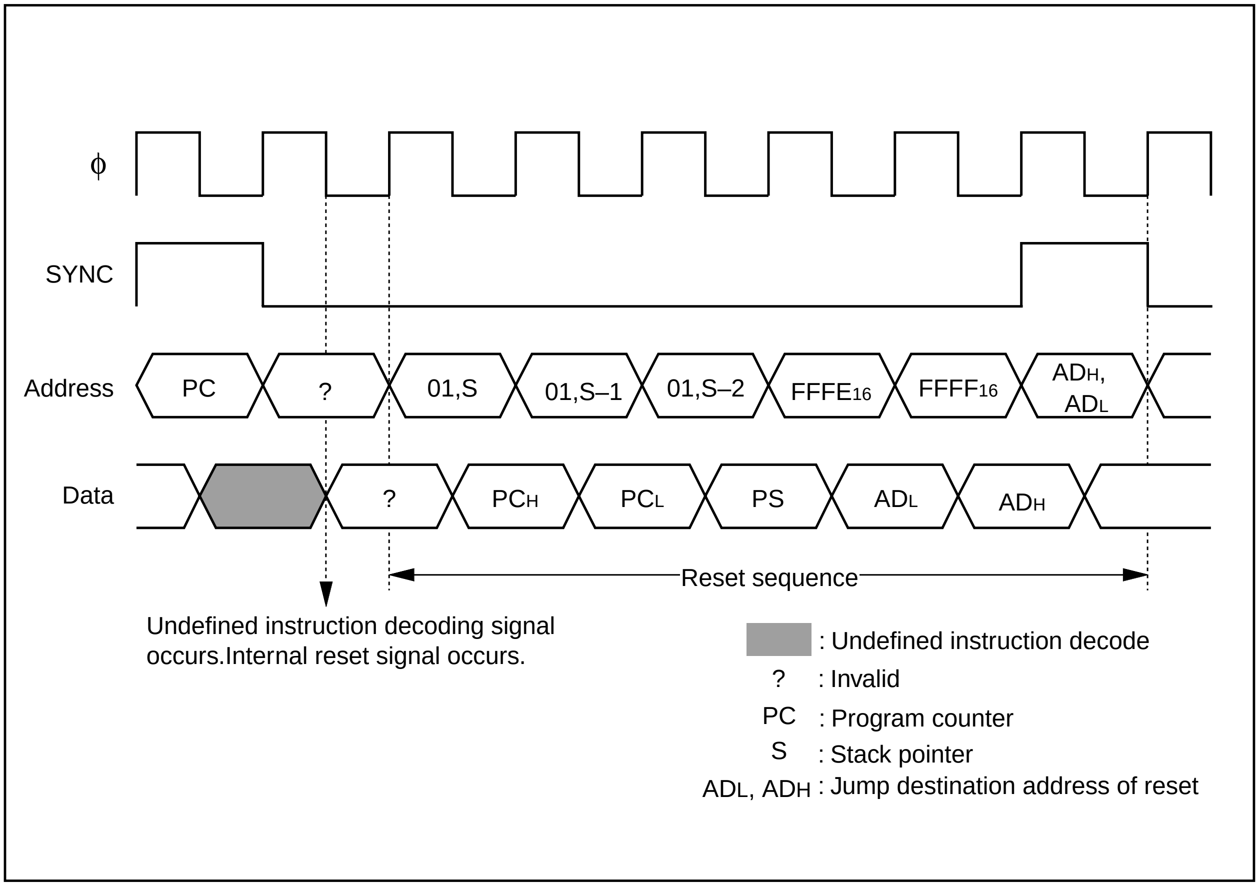


Fig.8.12.1 Sequence at Detecting Software Runaway Detection

8.13. RESET CIRCUIT

When the oscillation of a quartz-crystal oscillator or a ceramic resonator is stable and the power source voltage is 5 V ± 10 %, hold the $\overline{\text{RESET}}$ pin at LOW for 2 µs or more, then return is to HIGH. Then, as shown in Figure 8.13.2, reset is released and the program starts form the address formed by using the content of address $FFFF_{16}$ as the high-order address and the content of the address $FFFE_{16}$ as the low-order address. The internal state of microcomputer at reset are shown in Figures 8.2.4 to 8.2.9.

An example of the reset circuit is shown in Figure 8.13.1.

The reset input voltage must be kept 0.9 V or less until the power source voltage surpasses 4.5 V.

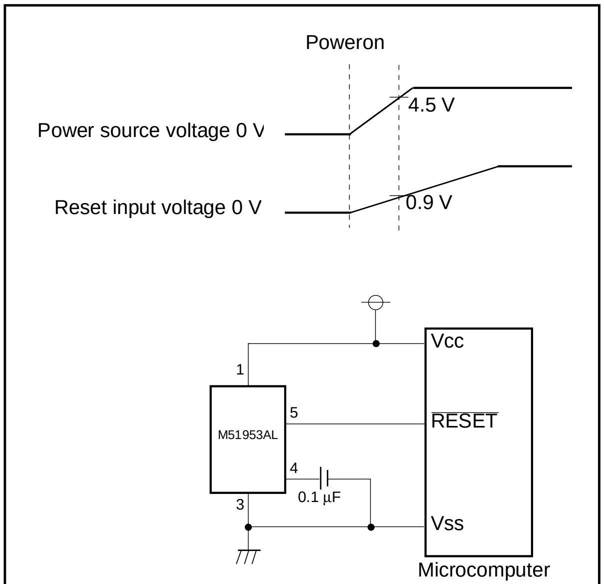
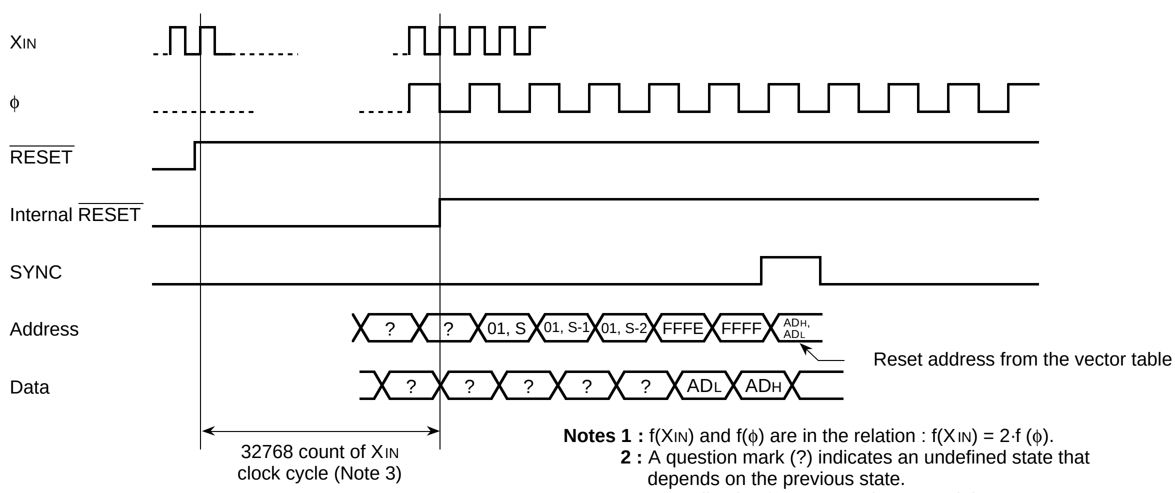


Fig.8.13.1 Example of Reset Circuit



Notes 1 : f(XIN) and f(φ) are in the relation : f(XIN) = 2·f (φ).

2 : A question mark (?) indicates an undefined state that depends on the previous state.

3 : Immediately after a reset, timer 3 and timer 4 are connected by hardware. At this time, "FF_{16}" is set in timer 3 and "07_{16}" is set to timer 4. Timer 3 counts down with f(XIN)/16, and reset state is released by the timer 4 overflow signal.

Fig.8.13.2 Reset Sequence

8.14 CLOCK GENERATING CIRCUIT

This microcomputer has 2 built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT. When using XCIN-XCOUT as sub-clock, clear bits 5 and 4 of the clock source control register to "0." To supply a clock signal externally, input it to the XIN (XCIN) pin and make the XOUT (XCOUT) pin open. When not using XCIN clock, connect the XCIN to VSS and make the XCOUT pin open.
After reset has completed, the internal clock ϕ is half the frequency of XIN. Immediately after poweron, both the XIN and XCIN clock start oscillating. To set the internal clock ϕ to low-speed operation mode, set bit 7 of the CPU mode register (address $00FB_{16}$) to "1."

8.14.1 OSCILLATION CONTROL

(1) Stop Mode

When the STP instruction is executed, the internal clock ϕ stops at HIGH. At the same time, timers 3 and 4 are connected by hardware and "FF_{16}" is set in timer 3 and "07_{16}" is set in timer 4. Select f(XIN)/16 or f(XCIN)/16 as the timer 3 count source (set both bit 0 of the timer mode register 2 and bit 6 at address $00C7_{16}$ to "0" before the execution of the STP instruction). Moreover, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction. The oscillator restarts when external interrupt is accepted. However, the internal clock ϕ keeps its HIGH level until timer 4 overflows, allowing time for oscillation stabilization when a ceramic resonator or a quartz-crystal oscillator is used.

(2) Wait Mode

When the WIT instruction is executed, the internal clock ϕ stops in the HIGH level but the oscillator continues running. This wait state is released at reset or when an interrupt is accepted (Note). Since the oscillator does not stop, the next instruction can be executed at once.

Note: In the wait mode, the following interrupts are invalid.
- VSYNC interrupt
- OSD interrupt
- All timers interrupts using external clock from port pin input as count source
- All timer interrupts using f(XIN)/2 or f(XCIN)/2 as count source
- All timer interrupts using f(XIN)/4096 or f(XCIN)/4096 as count source
- f(XIN)/4096 interrupt
- Multi-master I^2C-BUS interface interrupt
- Data slicer interrupt
- A-D conversion interrupt
- SPRITE OSD interrupt

(3) Low-speed Mode

If the internal clock is generated from the sub-clock (XCIN), a low power consumption operation can be realized by stopping only the main clock XIN. To stop the main clock, set bit 6 (CM6) of the CPU mode register ($00FB_{16}$) to "1." When the main clock XIN is restarted, the program must allow enough time to for oscillation to stabilize.
Note that in low-power-consumption mode the XCIN-XCOUT drivability can be reduced, allowing even lower power consumption. To reduce the XCIN-XCOUT drivability, clear bit 5 (CM5) of the CPU mode register ($00FB_{16}$) to "0." At reset, this bit is set to "1" and strong drivability is selected to help the oscillation to start. When an STP instruction is executed, set this bit to "1" by software before executing.

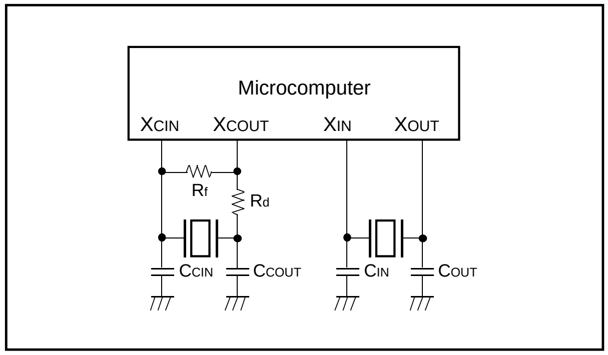


Fig.8.14.1 Ceramic Resonator Circuit Example

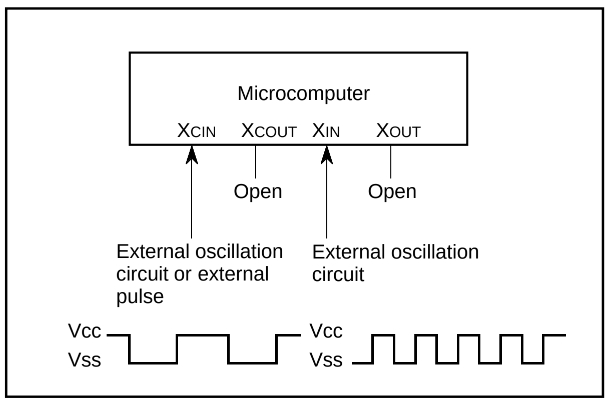
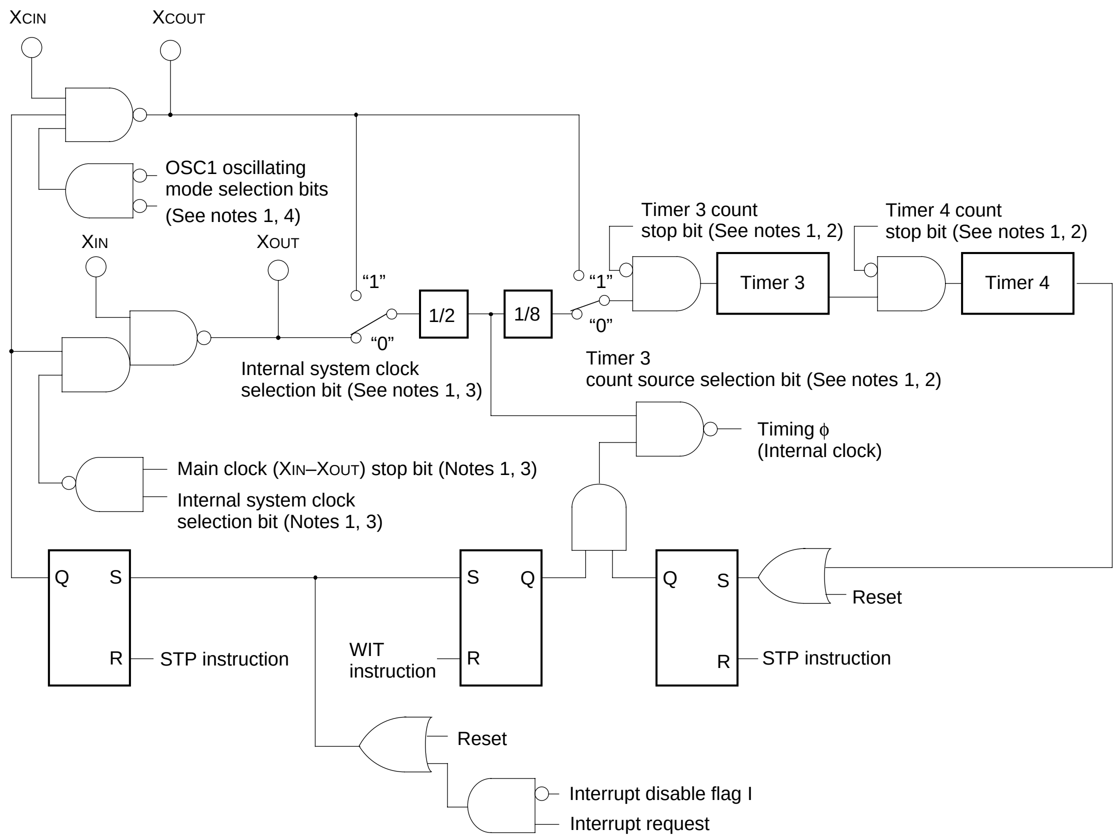


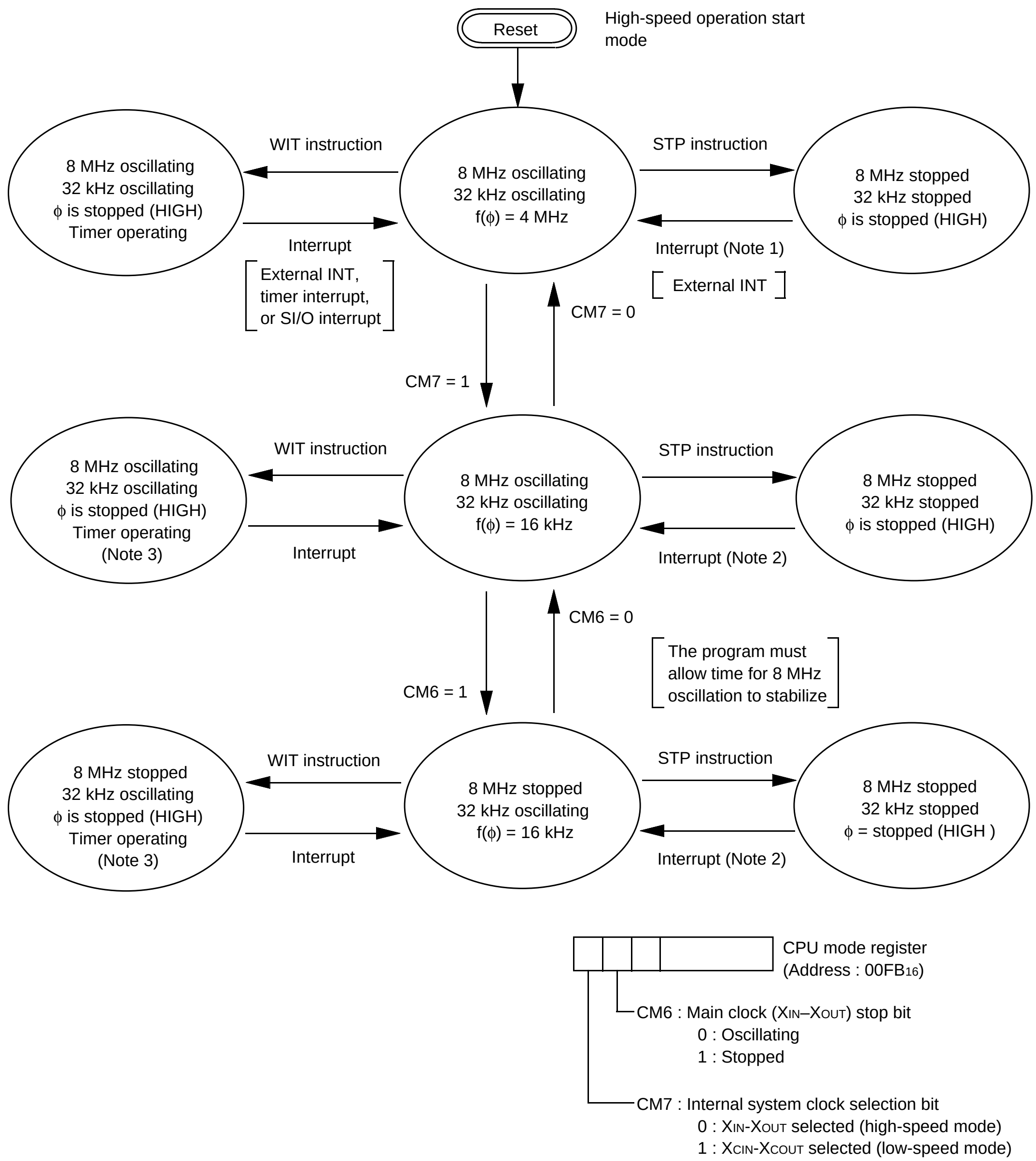
Fig.8.14.2 External Clock Input Circuit Example

RENESAS



Notes 1 : The value at reset is "0."
2 : Refer to timer mode register 2.
3 : Refer to CPU mode register (next page).
4 : Refer to clock source control register.

Fig.8.14.3 Clock Generating Circuit Block Diagram



The example assumes that 8 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. The φ indicates the internal clock.

Notes 1: When the STP state is ended, a delay of approximately 4 ms is automatically generated by timer 3 and timer 4.

2: The delay after the STP state ends is approximately 1 s.

3: When the internal clock φ divided by 8 is used as the timer count source, the frequency of the count source is 2 kHz.

Fig.8.14.4 State Transitions of System Clock

8.15. DISPLAY OSCILLATION CIRCUIT

The OSD oscillation circuit has a built-in clock oscillation circuits, so that a clock for OSD can be obtained simply by connecting an LC, a ceramic resonator, or a quartz-crystal oscillator across the pins OSC1 and OSC2. Which of the sub-clock or the OSD oscillation circuit is selected by setting bits 5 and 4 of the clock control register (address 0216_{16}).

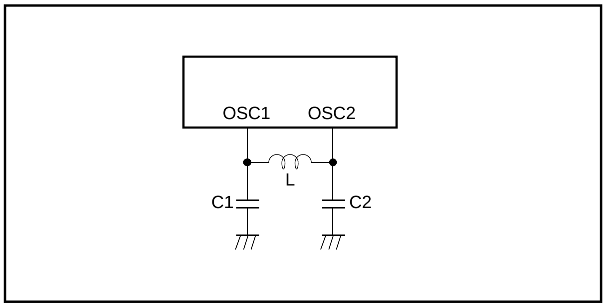


Fig.8.15.1 Display Oscillation Circuit

8.16. AUTO-CLEAR CIRCUIT

When a power source is supplied, the auto-clear function will operate by connecting the following circuit to the $\overline{\text{RESET}}$ pin.

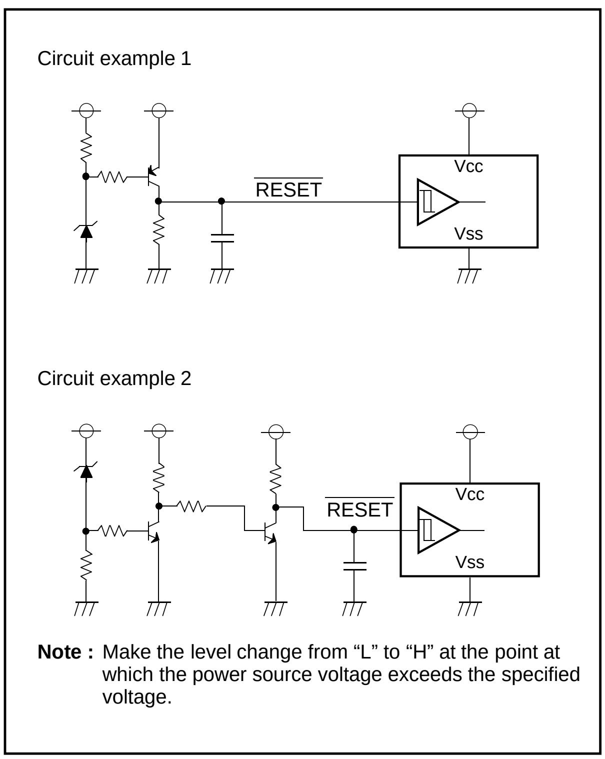


Fig.8.16.1 Auto-clear Circuit Example

8.17. ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to SERIES 740 <Software> User's Manual for details.

8.18. MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to SERIES 740 <Software> User's Manual for details.

9. PROGRAMMING NOTES

- The divide ratio of the timer is 1/(n+1).
- Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- After the ADC and SBC instructions are executed (in the decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.
- An NOP instruction is needed immediately after the execution of a PLP instruction.
- In order to avoid noise and latch-up, connect a bypass capacitor (≈ 0.1µF) directly between the V_{CC} pin–V_{SS} pin, AV_{CC} pin–V_{SS} pin, and the V_{CC} pin–CNV_{SS} pin, using a thick wire.

10. ABSOLUTE MAXIMUM RATINGS

Symbol	Parametear		Conditions	Ratings	Unit
V_{CC}, (AV_{CC})	Power source voltage	V_{CC}, (See note 1)	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6	V
V_I	Input voltage	CNVSS		–0.3 to 6	V
V_I	Input voltage	P00–P07, P10–P17, P20–P27, P30, P31, P40–P46, P64, P63, P70–P72, XIN, HSYNC, VSYNC, RESET		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	P00–P07, P10–P17, P20–P27, P30, P31, P52–P55, SOUT, SCLK, XOUT, OSC2		–0.3 to V_{CC} + 0.3	V
I_{OH}	Circuit current	P52–P55, P10, P03, P15–P17, P20–P27, P30, P31		0 to 1 (See note 2)	mA
I_{OL1}	Circuit current	P52–P57, P10, P03, P15–P17, P20–P27, P65–P67, SOUT, SCLK		0 to 2 (See note 3)	mA
I_{OL2}	Circuit current	P11–P14		0 to 6 (See note 3)	mA
I_{OL3}	Circuit current	P00–P02, P04–P07		0 to 1 (See note 3)	mA
I_{OL4}	Circuit current	P30, P31		0 to 10 (See note 4)	mA
P_d	Power dissipation		T_a = 25 °C	550	mW
T_{opr}	Operating temperature			–10 to 70	℃
T_{stg}	Storage temperature			–40 to 125	℃

11. RECOMMENDED OPERATING CONDITIONS (Ta = –10 °C to 70 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter			Limits Min.	Typ.	Max.	Unit
V_{CC}, (AV_{CC})	Power source voltage (See note 1, 5), During CPU, OSD, data slicer operation			4.5	5.0	5.5	V
V_{CC}, (AV_{CC})	RAM hold voltage (when clock is stopped)			2.0		5.5	V
V_{SS}	Power source voltage			0	0	0	V
V_{IH1}	HIGH input voltage	P00–P07, P10–P17, P20–P27, P30, P31, P40–P46, P63, P64, P70–P72, HSYNC, VSYNC, RESET, XIN		0.8V_{CC}		V_{CC}	V
V_{IH2}	HIGH input voltage	SCL1, SCL2, SDA1, SDA2		0.7V_{CC}		V_{CC}	V
V_{IL1}	LOW input voltage	P00–P07, P10–P17, P20–P27, P30, P31, P40–P46, P63, P64, P70–P72		0		0.4 V_{CC}	V
V_{IL2}	LOW input voltage	SCL1, SCL2, SDA1, SDA2		0		0.3 V_{CC}	V
V_{IL3}	LOW input voltage (See note 7)	RESET, XIN, OSC1, HSYNC, VSYNC, INT1–INT3, TIM2, TIM3, SCLK, SIN		0		0.2 V_{CC}	V
I_{OH}	HIGH average output current (See note 2)	P52–P55, P10, P03, P15–P17, P20–P27, P30, P31				1	mA
I_{OL1}	LOW average output current (See note 3)	P51–P55, P10, P03, P15–P17, P20–P27, SOUT, SCLK				2	mA
I_{OL2}	LOW average output current (See note 3)	P11–P14				6	mA
I_{OL3}	LOW average output current (See note 3)	P00–P02, P04–P07				1	mA
I_{OL4}	LOW average output current (See note 4)	P30, P31				10	mA
f(XIN)	Oscillation frequency (for CPU operation) (See note 6)	XIN		7.9	8.0	8.1	MHz
f(XCIN)	Oscillation frequency (for sub-clock operation)	XCIN		29	32	35	kHz
fosc	Oscillation frequency (for OSD)	OSC1	LC oscillating mode	11.0		27.0	MHz
			Ceramic oscillating mode	25.5	26.5	27.5	MHz
R_L	Load resistance	During R,G,B analog output		20.0			
f_{hs1}	Input frequency	TIM2, TIM3, INT1–INT3				100	kHz
f_{hs2}	Input frequency	SCLK				1	MHz
f_{hs3}	Input frequency	SCL1, SCL2				400	kHz
f_{hs4}	Input frequency	Horizontal sync. signal of video signal		15.262	15.734	16.206	kHz
V_I	Input amplitude video signal	CVIN		1.5	2.0	2.5	V

12. ELECTRIC CHARACTERISTICS (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, Ta = –10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Typ.	Max.	Unit	Test circuit
I_{CC}	Power source current	System operation	V_{CC} = 5.5 V, f(X_{IN}) = 8 MHz	CRT OFF Data slicer OFF		15	30	mA	1
				CRT ON (digital output) Data slicer ON		30	50		
				CRT ON (analog output) Data slicer ON		50	70		
			V_{CC} = 5.5 V, f(X_{IN}) = 0, f(X_{CIN}) = 32 kHz, OSD OFF, Data slicer OFF, Low-power dissipation mode set (CM5 = “0”, CM6 = “1”)			60	200	µA	
		Wait mode	V_{CC} = 5.5 V, f(X_{IN}) = 8 MHz			2	4	mA	
			V_{CC} = 5.5 V, f(X_{IN}) = 0, f(X_{CIN}) = 32kHz, Low-power dissipation mode set (CM5 = “0”, CM6 = “1”)			25	100	µA	
		Stop mode	V_{CC} = 5.5 V, f(X_{IN}) = 0 f(X_{CIN}) = 0			1	10	V	
V_{OH}	HIGH output voltage	$P5_2$–$P5_5$, $P1_0$, $P0_3$, $P1_5$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$	V_{CC} = 4.5 V I_{OH} = –0.5 mA		2.4			V	2
V_{OL}	LOW output voltage	S_{OUT}, S_{CLK}, $P0_0$–$P0_7$, $P1_0$, $P1_5$–$P1_7$, $P2_0$–$P2_7$, $P3_2$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$–$P6_7$	V_{CC} = 4.5 V I_{OL} = 0.5 mA				0.4	V	2
	LOW output voltage	$P3_0$, $P3_1$	V_{CC} = 4.5 V I_{OL} = 10.0 mA				3.0		
	LOW output voltage	$P1_1$–$P1_4$	V_{CC} = 4.5 V	I_{OL} = 3 mA			0.4		
				I_{OL} = 6 mA			0.6		
V_{T+} – V_{T-}	Hysteresis (See note 6)	$\overline{RESET}$, H_{SYNC}, V_{SYNC}, INT1, INT2, INT3, TIM2, TIM3, S_{IN}, S_{CLK}, SCL1, SCL2, SDA1, SDA2	V_{CC} = 5.0 V			0.5	1.3	V	3
I_{IZH}	HIGH input leak current	$\overline{RESET}$, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P4_0$–$P4_6$, $P6_3$, $P6_4$, $P7_0$–$P7_2$, H_{SYNC}, V_{SYNC}	V_{CC} = 5.5 V V_I = 5.5 V				5	µA	4
I_{IZL}	LOW input leak current	$\overline{RESET}$, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P4_0$–$P4_6$, $P6_3$, $P6_4$, $P7_0$–$P7_2$, H_{SYNC}, V_{SYNC}	V_{CC} = 5.5 V V_I = 0 V				5	mA	
R_{BS}	I^2C-BUS·BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		V_{CC} = 4.5 V				130	Ω	5

Notes 1: The total current that flows out of the IC must be 20 or less.
2: The total input current to IC (I_{OL1} + I_{OL2} + I_{OL3}) must be 20 mA or less.
3: The total average input current for ports $P3_0$, $P3_1$ to IC must be 10 mA or less.
4: Connect 0.1 µF or more capacitor externally between the power source pins V_{CC}–V_{SS} (and AV_{CC}–V_{SS}) so as to reduce power source noise.
Also connect 0.1 µF or more capacitor externally between the pins V_{CC}–CNV_{SS}. ( ) ···M37280EKSP
5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8 MHz.
6: $P1_6$, $P4_1$–$P4_4$ have the hysteresis when these pins are used as interrupt input pins or timer input pins. $P1_1$–$P1_4$ have the hysteresis when these pins are used as multi-master I^2C-BUS interface ports. $P1_7$, $P4_6$ and $P7_2$ have the hysteresis when these pins are used as serial I/O pins.
7: When using the sub-clock, set f_{CLK} < f_{CPU}/3.
8: Pin names in each parameter is described as below.
(1) Dedicated pins: dedicated pin names.
(2) Duble-/triple-function ports
• When the same limits: I/O port name.
• When the limits of functins except ports are different from I/O port limits: function pin name.

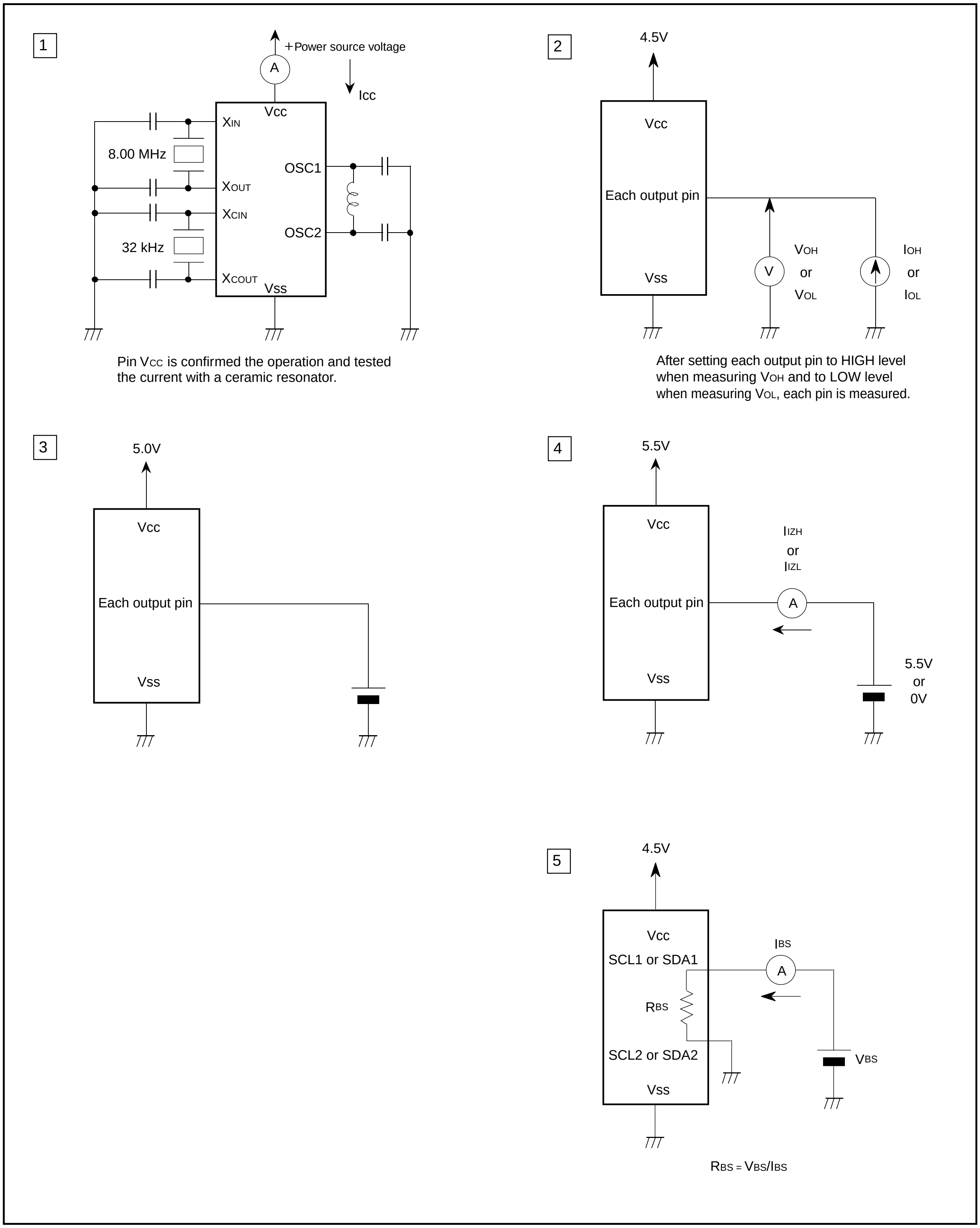


Fig.12.1 Test circuit

13. ANALOG R, G, B OUTPUT CHARACTERISTICS

(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = –10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
R_O	Output resistance	V_{CC} = 4.5 V			2	kΩ
V_{OE}	Output deviation	V_{CC} = 5.5 V			±0.5	V
T_{ST}	Settling time	V_{CC} = 4.5 V, load capacity of 10 pF, load resistor of 20 kΩ, 70 % DC level			50	ns

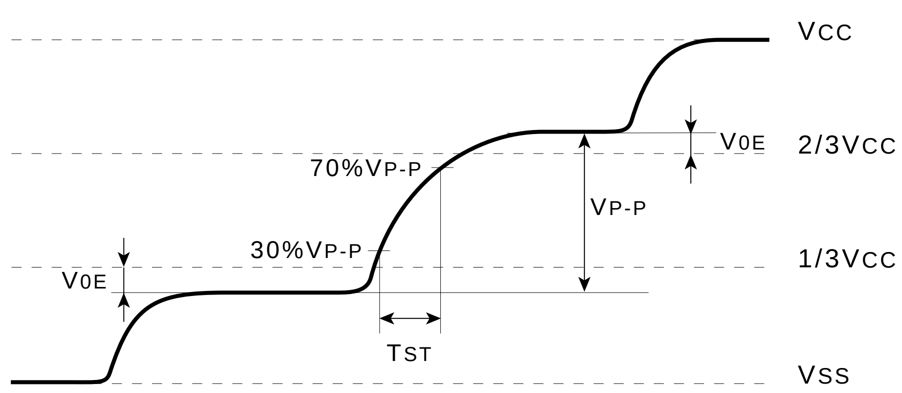


Fig.13.1 Analog R, G, B, Output Characteristics

14. A-D CONVERTER CHARACTERISTICS

(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = –10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Absolute accuracy (excludig guantization error)	Vcc = 5 V			±2.5	LSB
T_{CONV}	Conversion time		12.25		12.5	µs
R_{LADDER}	Ladder resistor			25		kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

15. MULTI-MASTER I²C-BUS BUS LINE CHARACTERISTICS

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time for START condition	4.0		0.6		µs
t_{LOW}	LOW period of SCL clock	4.7		1.3		µs
t_R	Rising time of both SCL and SDA signals		1000	20+0.1C_b	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	HIGH period of SCL clock	4.0		0.6		µs
t_F	Falling time of both SCL and SDA signals		300	20+0.1C_b	300	ns
$t_{SU;DAT}$	Data set-up time	250		100		ns
$t_{SU;STA}$	Set-up time for repeated START condition	4.7		0.6		µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0		0.6		µs

Note: C_b = total capacitance of 1 bus line

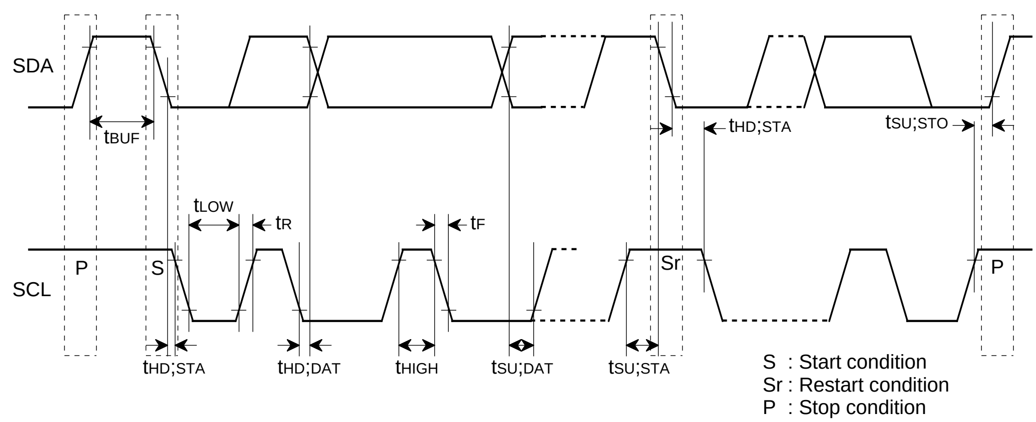


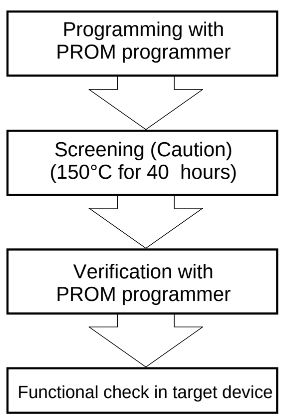
Fig.15.1 Definition Diagram of Timing on Multi-master I²C-BUS

16. PROM PROGRAMMING METHOD

The built-in PROM of the One Time PROM version (blank) and the built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37281EKSP	PCA7400

The PROM of the One Time PROM version (blank) is not tested or screened in the assembly process nor any following processes. To ensure proper operation after programming, the procedure shown in Figure 16.1 is recommended to verify programming.



Caution : The screening temperature is far higher than the storage temperature. Never expose to 150°C exceeding 100 hours.

Fig. 16.1 Programming and Testing of One Time PROM Version

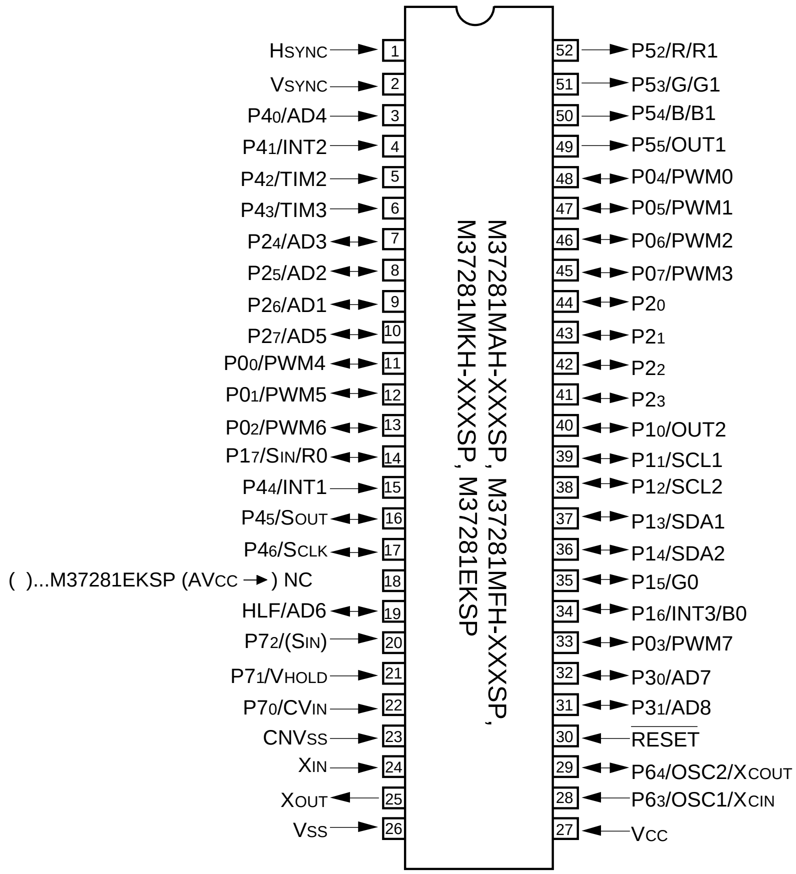
17. DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- Mask ROM Order Confirmation Form
- Mark Specification Form
- Data to be written to ROM, in EPROM form (52-pin DIP Type 27C101, three identical copies) or FDK

18. APPENDIX

Pin Configuration (TOP VIEW)

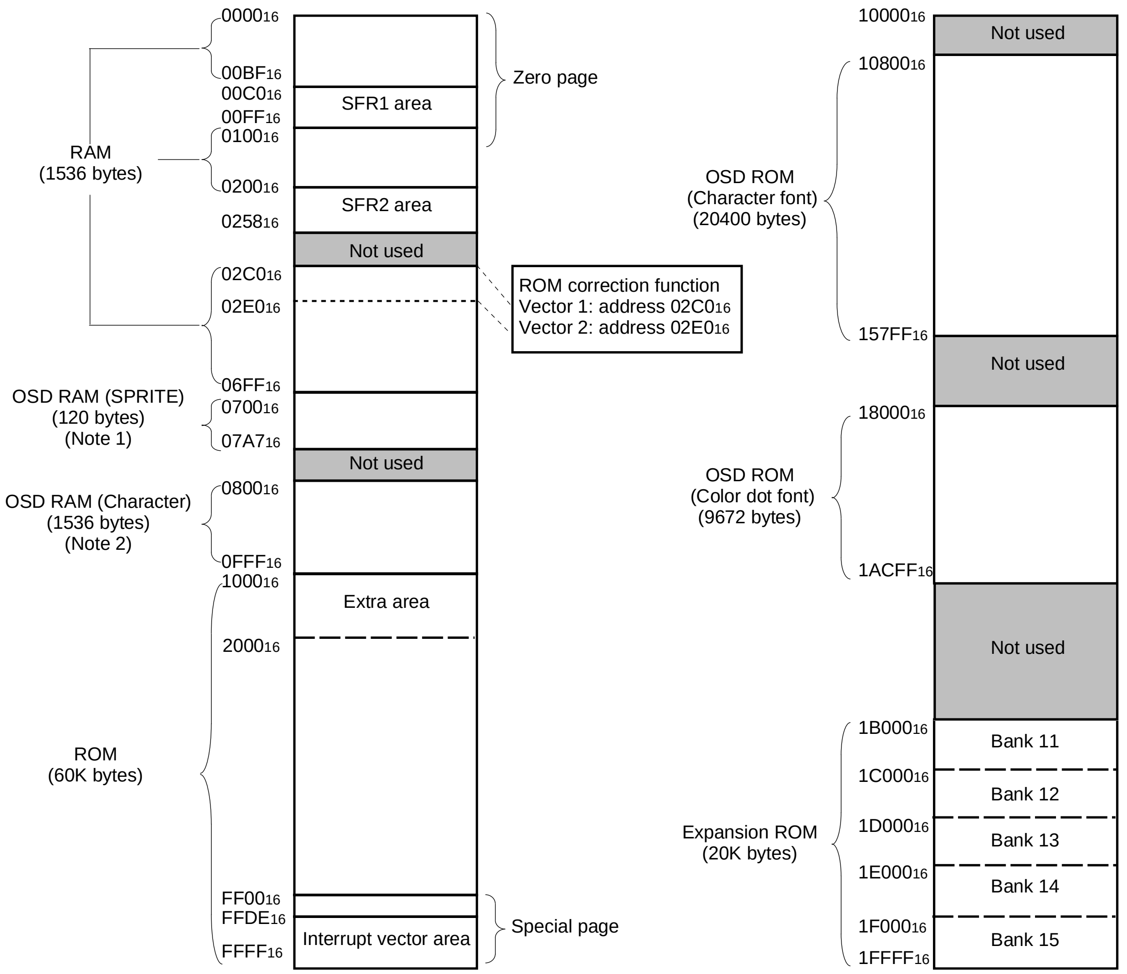


Outline 52P4B

Note: Only 18th pin is NC pin of M37281MAH/MFH/MKH-XXXSP. This pin is AVcc pin of M37281EKSP. But NC pin of M37281MAH/MFH/MKH-XXXSP is not connect in the IC. You can apply to Vcc.

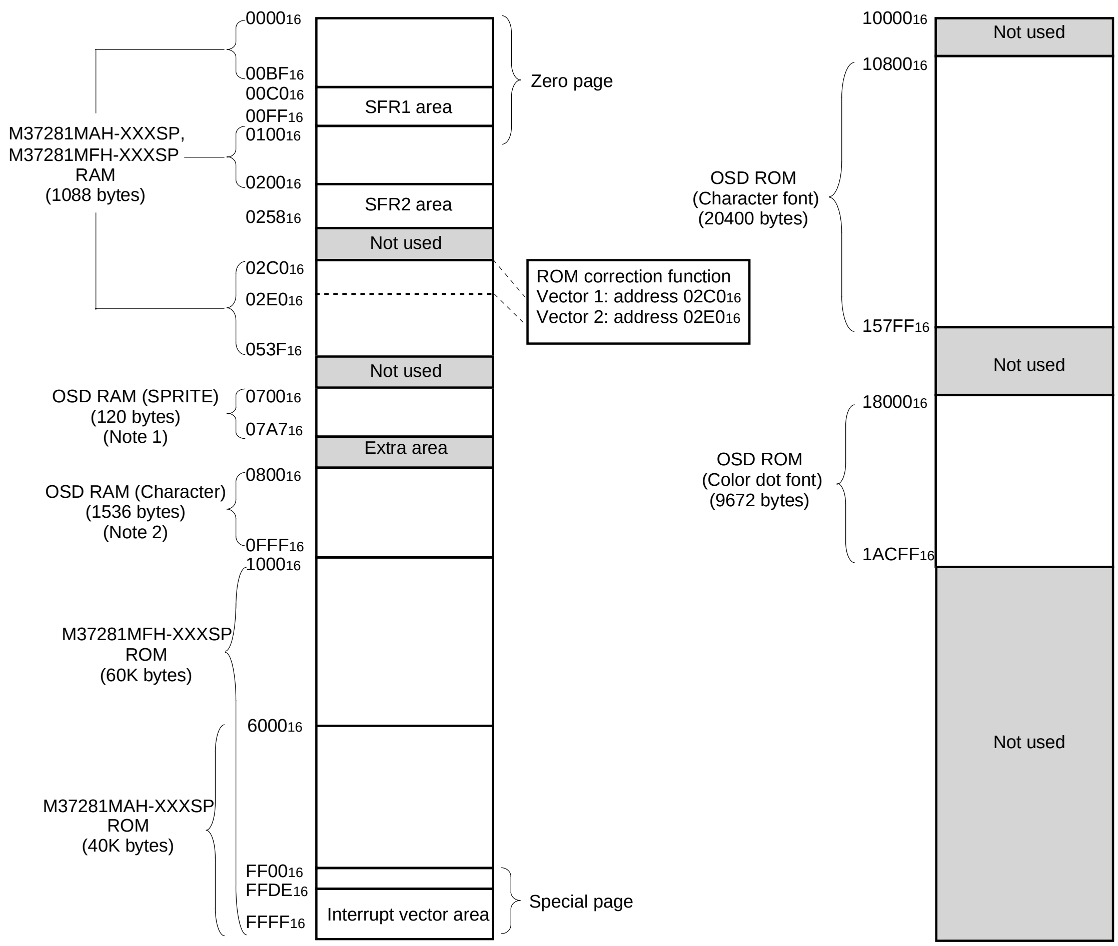
Memory Map

■ M37281MKH-XXXSP, M37281EKSP



Notes 1: Refer to Table 8.11.6 OSD RAM (SPRITE).
2: Tables 8.11.4 and 8.11.5 OSD RAM (Character).

■ M37281MAH-XXXSP, M37281MFH-XXXSP



Notes 1: Refer to Table 8.11.6 OSD RAM (SPRITE).
2 : Tables 8.11.4 and 8.11.5 OSD RAM (Character).

Memory Map of Special Function Register (SFR)

■ SFR1 area (addresses $C0_{16}$ to DF_{16})

<Bit allocation>

[ ] : } Function bit
[Name] :

[grey] : No function bit

[0] : Fix to this bit to “0” (do not write to “1”)

[1] : Fix to this bit to “1” (do not write to “0”)

<State immediately after reset>

[0] : “0” immediately after reset

[1] : “1” immediately after reset

[?] : Indeterminate immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset (b7 … b0)
$C0_{16}$	Port P0 (P0)									?
$C1_{16}$	Port P0 direction register (D0)									00_{16}
$C2_{16}$	Port P1 (P1)									?
$C3_{16}$	Port P1 direction register (D1)									00_{16}
$C4_{16}$	Port P2 (P2)									?
$C5_{16}$	Port P2 direction register (D2)									00_{16}
$C6_{16}$	Port P3 (P3)									?
$C7_{16}$	Port P3 direction register (D3)	P6IM	T3CS							00_{16}
$C8_{16}$	Port P4 (P4)									?
$C9_{16}$	Port P4 direction register (D4)								0	00_{16}
CA_{16}	Port P5 (P5)									?
CB_{16}	OSD port control register (PF)	0	OUT2	OUT1	B	G	R	RGB 2BIT	0	00_{16}
CC_{16}	Port P6 (P6)									?
CD_{16}	Port P7 (P7)									0 0 0 0 0 ? ? ?
CE_{16}	OSD control register 1 (OC 1)	OC17	OC16	OC15	OC14	OC13	OC12	OC11	OC10	00_{16}
CF_{16}	Horizontal position register (HP)	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	00_{16}
$D0_{16}$	Block control register 1 (BC_1)		$BC_{1}6$	$BC_{1}5$	$BC_{1}4$	$BC_{1}3$	$BC_{1}2$	$BC_{1}1$	$BC_{1}0$	?
$D1_{16}$	Block control register 2 (BC_2)		$BC_{2}6$	$BC_{2}5$	$BC_{2}4$	$BC_{2}3$	$BC_{2}2$	$BC_{2}1$	$BC_{2}0$	?
$D2_{16}$	Block control register 3 (BC_3)		$BC_{3}6$	$BC_{3}5$	$BC_{3}4$	$BC_{3}3$	$BC_{3}2$	$BC_{3}1$	$BC_{3}0$	?
$D3_{16}$	Block control register 4 (BC_4)		$BC_{4}6$	$BC_{4}5$	$BC_{4}4$	$BC_{4}3$	$BC_{4}2$	$BC_{4}1$	$BC_{4}0$	?
$D4_{16}$	Block control register 5 (BC_5)		$BC_{5}6$	$BC_{5}5$	$BC_{5}4$	$BC_{5}3$	$BC_{5}2$	$BC_{5}1$	$BC_{5}0$	?
$D5_{16}$	Block control register 6 (BC_6)		$BC_{6}6$	$BC_{6}5$	$BC_{6}4$	$BC_{6}3$	$BC_{6}2$	$BC_{6}1$	$BC_{6}0$	?
$D6_{16}$	Block control register 7 (BC_7)		$BC_{7}6$	$BC_{7}5$	$BC_{7}4$	$BC_{7}3$	$BC_{7}2$	$BC_{7}1$	$BC_{7}0$	?
$D7_{16}$	Block control register 8 (BC_8)		$BC_{8}6$	$BC_{8}5$	$BC_{8}4$	$BC_{8}3$	$BC_{8}2$	$BC_{8}1$	$BC_{8}0$	?
$D8_{16}$	Block control register 9 (BC_9)		$BC_{9}6$	$BC_{9}5$	$BC_{9}4$	$BC_{9}3$	$BC_{9}2$	$BC_{9}1$	$BC_{9}0$	?
$D9_{16}$	Block control register 10 (BC_{10})		$BC_{10}6$	$BC_{10}5$	$BC_{10}4$	$BC_{10}3$	$BC_{10}2$	$BC_{10}1$	$BC_{10}0$	?
DA_{16}	Block control register 11 (BC_{11})		$BC_{11}6$	$BC_{11}5$	$BC_{11}4$	$BC_{11}3$	$BC_{11}2$	$BC_{11}1$	$BC_{11}0$	?
DB_{16}	Block control register 12 (BC_{12})		$BC_{12}6$	$BC_{12}5$	$BC_{12}4$	$BC_{12}3$	$BC_{12}2$	$BC_{12}1$	$BC_{12}0$	?
DC_{16}	Block control register 13 (BC_{13})		$BC_{13}6$	$BC_{13}5$	BC_{13}	$BC_{13}3$	$BC_{13}2$	$BC_{13}1$	$BC_{13}0$	?
DD_{16}	Block control register 14 (BC_{14})		$BC_{14}6$	$BC_{14}5$	$BC_{14}4$	$BC_{14}3$	$BC_{14}2$	$BC_{14}1$	$BC_{14}0$	?
DE_{16}	Block control register 15 (BC_{15})		$BC_{15}6$	$BC_{15}5$	$BC_{15}4$	$BC_{15}3$	$BC_{15}2$	$BC_{15}1$	$BC_{15}0$	?
DF_{16}	Block control register 16 (BC_{16})		$BC_{16}6$	$BC_{16}5$	$BC_{16}4$	$BC_{16}3$	$BC_{16}2$	$BC_{16}1$	$BC_{16}0$	?

■ SFR1 area (addresses $E0_{16}$ to FF_{16})

<Bit allocation>

- [ ] : } Function bit
- [Name] : } Function bit
- (shaded box) : No function bit
- (shaded) 0 : Fix to this bit to “0” (do not write to “1”)
- (shaded) 1 : Fix to this bit to “1” (do not write to “0”)

<State immediately after reset>

- 0 : “0” immediately after reset
- 1 : “1” immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	b7							b0	State immediately after reset (b7–b0)
$E0_{16}$	Data slicer control register 1 (DSC1)	0	0	0	0	0	DSC12	DSC11	DSC10	00_{16}
$E1_{16}$	Data slicer control register 2 (DSC2)		0	DSC25	DSC24	DSC23		0	DSC20	? 0 ? 0 ? ? 0 ?
$E2_{16}$	Caption data register 1 (CD1)	CDL17	CDL16	CDL15	CDL14	CDL13	CDL12	CDL11	CDL10	00_{16}
$E3_{16}$	Caption data register 2 (CD2)	CDH17	CDH16	CDH15	CDH14	CDH13	CDH12	CDH11	CDH10	00_{16}
$E4_{16}$	Caption data register 3 (CD3)	CDL27	CDL26	CDL25	CDL24	CDL23	CDL22	CDL21	CDL20	00_{16}
$E5_{16}$	Caption data register 4 (CD4)	CDH27	CDH26	CDH25	CDH24	CDH23	CDH22	CDH21	CDH20	00_{16}
$E6_{16}$	Caption Position register (CPS)	CPS7	CPS6	CPS5	CPS4	CPS3	CPS2	CPS1	CPS0	0 0 ? 0 0 0 0 0
$E7_{16}$	Data slicer test register 2	00_{16}								00_{16}
$E8_{16}$	Data slicer test register 1	00_{16}								00_{16}
$E9_{16}$	Sync signal counter register (HC)			HC5	HC4	HC3	HC2	HC1	HC0	0 0 ? ? ? ? ? ?
EA_{16}	Clock run-in detect register (CRD)	CRD7	CRD6	CRD5	CRD4	CRD3				00_{16}
EB_{16}	Data clock position register (DPS)	DPS7	DPS6	DPS5	DPS4	DPS3	0	0	1	09_{16}
EC_{16}										?
ED_{16}	Bank control register (BK)	BK7	BK6	0	0	BK3	BK2	BK1	BK0	00_{16}
EE_{16}	A-D conversion register (AD)									?
EF_{16}	A-D control register (ADCON)	0		0	ADVREF	ADSTR	ADIN2	ADIN1	ADIN0	0 ? 0 0 1 0 0 0
$F0_{16}$	Timer 1 (T1)									FF_{16}
$F1_{16}$	Timer 2 (T2)									07_{16}
$F2_{16}$	Timer 3 (T3)									FF_{16}
$F3_{16}$	Timer 4 (T4)									07_{16}
$F4_{16}$	Timer mode register 1 (TM1)	TM17	TM16	TM15	TM14	TM13	TM12	TM11	TM10	00_{16}
$F5_{16}$	Timer mode register 2 (TM2)	TM27	TM26	TM25	TM24	TM23	TM22	TM21	TM20	00_{16}
$F6_{16}$	I^2C data shift register (S0)	D7	D6	D5	D4	D3	D2	D1	D0	?
$F7_{16}$	I^2C address register (S0D)	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW	00_{16}
$F8_{16}$	I^2C status register (S1)	MST	TRX	BB	PIN	AL	AAS	AD0	LRB	0 0 0 1 0 0 0 ?
$F9_{16}$	I^2C control register (S1D)	BSEL1	BSEL0	10BIT SAD	ALS	ESO	BC2	BC1	BC0	00_{16}
FA_{16}	I^2C clock control register (S2)	ACK	ACK BIT	FAST MODE	CCR4	CCR3	CCR2	CCR1	CCR0	00_{16}
FB_{16}	CPU mode register (CM)	CM7	CM6	CM5	1	1	CM2	0	0	$3C_{16}$
FC_{16}	Interrupt request register 1 (IREQ1)		ADR	VSCR	OSDR	TM4R	TM3R	TM2R	TM1R	00_{16}
FD_{16}	Interrupt request register 2 (IREQ2)	0	TM56R	IICR	IN2R	CKR	SIOR	DSR	IN1R	00_{16}
FE_{16}	Interrupt control register 1 (ICON1)		ADE	VSCE	OSDE	TM4E	TM3E	TM2E	TM1E	00_{16}
FF_{16}	Interrupt control register 2 (ICON2)	TM56S	TM56E	IICE	IN2E	CKE	SIOE	DSE	IN1E	00_{16}

■ SFR2 area (addresses 200_{16} to $21F_{16}$)

<Bit allocation>

- ☐ : / Name : } Function bit
- ▒ : No function bit
- 0 : Fix to this bit to “0” (do not write to “1”)
- 1 : Fix to this bit to “1” (do not write to “0”)

<State immediately after reset>

- 0 : “0” immediately after reset
- 1 : “1” immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	b7							b0	State immediately after reset (b7–b0)
200_{16}	PWM0 register (PWM0)									?
201_{16}	PWM1 register (PWM1)									?
202_{16}	PWM2 register (PWM2)									?
203_{16}	PWM3 register (PWM3)									?
204_{16}	PWM4 register (PWM4)									?
205_{16}	PWM5 register (PWM5)									?
205_{16}	PWM6 register (PWM6)									?
207_{16}	PWM7 register (PWM7)									?
208_{16}		—	—	—	—	—	—	—	—	?
209_{16}		—	—	—	—	—	—	—	—	?
$20A_{16}$	PWM mode register 1 (PN)	—	—	—	PN4	PN3	—	—	PN0	00_{16}
$20B_{16}$	PWM mode register 2 (PW)	0	PW6	PW5	PW4	PW3	PW2	PW1	PW0	00_{16}
$20C_{16}$	ROM correction address 1 (high-order)									00_{16}
$20D_{16}$	ROM correction address 1 (low-order)									00_{16}
$20E_{16}$	ROM correction address 2 (high-order)									00_{16}
$20F_{16}$	ROM correction address 2 (low-order)									00_{16}
210_{16}	ROM correction enable register (RCR)	—	—	—	—	0	0	RCR1	RCR0	00_{16}
211_{16}	Test register	00_{16}								00_{16}
212_{16}	Interrupt input polarity register (IP)	AD/INT3 SEL	POL3	—	POL2	POL1	—	—	—	00_{16}
213_{16}	Serial I/O mode register (SM)	—	SM6	SM5	SM4	SM3	SM2	SM1	SM0	00_{16}
214_{16}	Serial I/O register (SIO)									?
215_{16}	OSD control register 2(OC2)	OC27	OC26	OC25	OC24	OC23	OC12	OC21	OC20	00_{16}
216_{16}	Clock control register (CS)	—	0	0	0	0	CS2	CS1	CS0	00_{16}
217_{16}	I/O polarity control register (PC)	PC7	PC6	PC5	PC4	—	PC2	PC1	PC0	80_{16}
218_{16}	Raster color register (RC)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	00_{16}
219_{16}	OSD control register 3(OC3)	OC37	OC36	OC35	OC34	OC33	OC32	OC31	OC30	00_{16}
$21A_{16}$	Timer 5 (TM5)									FF_{16}
$21B_{16}$	Timer 6 (TM6)									07_{16}
$21C_{16}$	Top border control register 1 (TB1)	TB17	TB16	TB15	TB14	TB13	TB12	TB11	TB10	?
$21D_{16}$	Bottom border control register 1 (BB1)	BB17	BB16	BB15	BB14	BB13	BB12	BB11	BB10	?
$21E_{16}$	Top border control register 2 (TB2)	—	—	—	—	—	—	TB21	TB20	?
$21F_{16}$	Bottom border control register 2 (BB2)	—	—	—	—	—	—	BB21	BB20	?

■ SFR2 area (addresses 220$_{16}$ to 23F$_{16}$)

<Bit allocation>

- ☐ : } Function bit
- Name : } Function bit
- (shaded) : No function bit
- 0 : Fix to this bit to "0" (do not write to "1")
- 1 : Fix to this bit to "1" (do not write to "0")

<State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset b7 … b0
220$_{16}$	Vertical position register 1_1 ($VP1_1$)	$VP1_17$	$VP1_16$	$VP1_15$	$VP1_14$	$VP1_13$	$VP1_12$	$VP1_11$	$VP1_10$	?
221$_{16}$	Vertical position register 1_2 ($VP1_2$)	$VP1_27$	$VP1_26$	$VP1_25$	$VP1_24$	$VP1_23$	$VP1_22$	$VP1_21$	$VP1_20$	?
222$_{16}$	Vertical position register 1_3 ($VP1_3$)	$VP1_37$	$VP1_36$	$VP1_35$	$VP1_34$	$VP1_33$	$VP1_32$	$VP1_31$	$VP1_30$	?
223$_{16}$	Vertical position register 1_4 ($VP1_4$)	$VP1_47$	$VP1_46$	$VP1_45$	$VP1_44$	$VP1_43$	$VP1_42$	$VP1_41$	$VP1_40$	?
224$_{16}$	Vertical position register 1_5 ($VP1_5$)	$VP1_57$	$VP1_56$	$VP1_55$	$VP1_54$	$VP1_53$	$VP1_52$	$VP1_51$	$VP1_50$	?
225$_{16}$	Vertical position register 1_6 ($VP1_6$)	$VP1_67$	$VP1_66$	$VP1_65$	$VP1_64$	$VP1_63$	$VP1_62$	$VP1_61$	$VP1_60$	?
226$_{16}$	Vertical position register 1_7 ($VP1_7$)	$VP1_77$	$VP1_76$	$VP1_75$	$VP1_74$	$VP1_73$	$VP1_72$	$VP1_71$	$VP1_70$	?
227$_{16}$	Vertical position register 1_8 ($VP1_8$)	$VP1_87$	$VP1_86$	$VP1_85$	$VP1_84$	$VP1_83$	$VP1_82$	$VP1_81$	$VP1_80$	?
228$_{16}$	Vertical position register 1_9 ($VP1_9$)	$VP1_97$	$VP1_96$	$VP1_95$	$VP1_94$	$VP1_93$	$VP1_92$	$VP1_91$	$VP1_90$	?
229$_{16}$	Vertical position register 1_{10} ($VP1_{10}$)	$VP1_{10}7$	$VP1_{10}6$	$VP1_{10}5$	$VP1_{10}4$	$VP1_{10}3$	$VP1_{10}2$	$VP1_{10}1$	$VP1_{10}0$	?
22A$_{16}$	Vertical position register 1_{11} ($VP1_{11}$)	$VP1_{11}7$	$VP1_{11}6$	$VP1_{11}5$	$VP1_{11}4$	$VP1_{11}3$	$VP1_{11}2$	$VP1_{11}1$	$VP1_{11}0$	?
22B$_{16}$	Vertical position register 1_{12} ($VP1_{12}$)	$VP1_{12}7$	$VP1_{12}6$	$VP1_{12}5$	$VP1_{12}4$	$VP1_{12}3$	$VP1_{12}2$	$VP1_{12}1$	$VP1_{12}0$	?
22C$_{16}$	Vertical position register 1_{13} ($VP1_{13}$)	$VP1_{13}7$	$VP1_{13}6$	$VP1_{13}5$	$VP1_{13}4$	$VP1_{13}3$	$VP1_{13}2$	$VP1_{13}1$	$VP1_{13}0$	?
22D$_{16}$	Vertical position register 1_{14} ($VP1_{14}$)	$VP1_{14}7$	$VP1_{14}6$	$VP1_{14}5$	$VP1_{14}4$	$VP1_{14}3$	$VP1_{14}2$	$VP1_{14}1$	$VP1_{14}0$	?
22E$_{16}$	Vertical position register 1_{15} ($VP1_{15}$)	$VP1_{15}7$	$VP1_{15}6$	$VP1_{15}5$	$VP1_{15}4$	$VP1_{15}3$	$VP1_{15}2$	$VP1_{15}1$	$VP1_{15}0$	?
22F$_{16}$	Vertical position register 1_{16} ($VP1_{16}$)	$VP1_{16}7$	$VP1_{16}6$	$VP1_{16}5$	$VP1_{16}4$	$VP1_{16}3$	$VP1_{16}2$	$VP1_{16}1$	$VP1_{16}0$	?
230$_{16}$	Vertical position register 2_1 ($VP2_1$)							$VP2_11$	$VP2_10$	?
231$_{16}$	Vertical position register 2_2 ($VP2_2$)							$VP2_21$	$VP2_20$	?
232$_{16}$	Vertical position register 2_3 ($VP2_3$)							$VP2_31$	$VP2_30$	?
233$_{16}$	Vertical position register 2_4 ($VP2_4$)							$VP2_41$	$VP2_40$	?
234$_{16}$	Vertical position register 2_5 ($VP2_5$)							$VP2_51$	$VP2_50$	?
235$_{16}$	Vertical position register 2_6 ($VP2_6$)							$VP2_61$	$VP2_60$	?
236$_{16}$	Vertical position register 2_7 ($VP2_7$)							$VP2_71$	$VP2_70$	?
237$_{16}$	Vertical position register 2_8 ($VP2_8$)							$VP2_81$	$VP2_80$	?
238$_{16}$	Vertical position register 2_9 ($VP2_9$)							$VP2_91$	$VP2_90$	?
239$_{16}$	Vertical position register 2_{10} ($VP2_{10}$)							$VP2_{10}1$	$VP2_{10}0$	?
23A$_{16}$	Vertical position register 2_{11} ($VP2_{11}$)							$VP2_{11}1$	$VP2_{11}0$	?
23B$_{16}$	Vertical position register 2_{12} ($VP2_{12}$)							$VP2_{12}1$	$VP2_{12}0$	?
23C$_{16}$	Vertical position register 2_{13} ($VP2_{13}$)							$VP2_{13}1$	$VP2_{13}0$	?
23D$_{16}$	Vertical position register 2_{14} ($VP2_{14}$)							$VP2_{14}1$	$VP2_{14}0$	?
23E$_{16}$	Vertical position register 2_{15} ($VP2_{15}$)							$VP2_{15}1$	$VP2_{15}0$	?
23F$_{16}$	Vertical position register 2_{16} ($VP2_{16}$)							$VP2_{16}1$	$VP2_{16}0$	?

■ SFR2 area (addresses 240_{16} to 258_{16})

<Bit allocation>

- (blank box) : } Function bit
- (Name box) : } Function bit
- (shaded box) : No function bit
- 0 : Fix to this bit to "0" (do not write to "1")
- 1 : Fix to this bit to "1" (do not write to "0")

<State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	b7	b6	b5	b4	b3	b2	b1	b0	State immediately after reset (b7–b0)
240_{16}										?
241_{16}	Color pallet register 1 (CR1)		CR$_1$6	CR$_1$5	CR$_1$4	CR$_1$3	CR$_1$2	CR$_1$1	CR$_1$0	?
242_{16}	Color pallet register 2 (CR2)		CR$_2$6	CR$_2$5	CR$_2$4	CR$_2$3	CR$_2$2	CR$_2$1	CR$_2$0	?
243_{16}	Color pallet register 3 (CR3)		CR$_3$6	CR$_3$5	CR$_3$4	CR$_3$3	CR$_3$2	CR$_3$1	CR$_3$0	?
244_{16}	Color pallet register 4 (CR4)		CR$_4$6	CR$_4$5	CR$_4$4	CR$_4$3	CR$_4$2	CR$_4$1	CR$_4$0	?
245_{16}	Color pallet register 5 (CR5)		CR$_5$6	CR$_5$5	CR$_5$4	CR$_5$3	CR$_5$2	CR$_5$1	CR$_5$0	?
246_{16}	Color pallet register 6 (CR6)		CR$_6$6	CR$_6$5	CR$_6$4	CR$_6$3	CR$_6$2	CR$_6$1	CR$_6$0	?
247_{16}	Color pallet register 7 (CR7)		CR$_7$6	CR$_7$5	CR$_7$4	CR$_7$3	CR$_7$2	CR$_7$1	CR$_7$0	?
248_{16}										?
249_{16}	Color pallet register 9 (CR9)		CR$_9$6	CR$_9$5	CR$_9$4	CR$_9$3	CR$_9$2	CR$_9$1	CR$_9$0	?
$24A_{16}$	Color pallet register10 (CR10)		CR$_{10}$6	CR$_{10}$5	CR$_{10}$4	CR$_{10}$3	CR$_{10}$2	CR$_{10}$1	CR$_{10}$0	?
$24B_{16}$	Color pallet register 11 (CR11)		CR$_{11}$6	CR$_{11}$5	CR$_{11}$4	CR$_{11}$3	CR$_{11}$2	CR$_{11}$1	CR$_{11}$0	?
$24C_{16}$	Color pallet register 12 (CR12)		CR$_{12}$6	CR$_{12}$5	CR$_{12}$4	CR$_{12}$3	CR$_{12}$2	CR$_{12}$1	CR$_{12}$0	?
$24D_{16}$	Color pallet register 13 (CR13)		CR$_{13}$6	CR$_{13}$5	CR$_{13}$4	CR$_{13}$3	CR$_{13}$2	CR$_{13}$1	CR$_{13}$0	?
$24E_{16}$	Color pallet register 14 (CR14)		CR$_{14}$6	CR$_{14}$5	CR$_{14}$4	CR$_{14}$3	CR$_{14}$2	CR$_{14}$1	CR$_{14}$0	?
$24F_{16}$	Color pallet register 15 (CR15)		CR$_{15}$6	CR$_{15}$5	CR$_{15}$4	CR$_{15}$3	CR$_{15}$2	CR$_{15}$1	CR$_{15}$0	?
250_{16}	Left border control register 1 (LB1)	LB17	LB16	LB15	LB14	LB13	LB12	LB11	LB10	01_{16}
251_{16}	Left border control register 2 (LB2)						LB22	LB21	LB20	00_{16}
252_{16}	Right border control register 1 (RB1)	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	FF_{16}
253_{16}	Right border control register 2 (RB2)						RB22	RB21	RB20	07_{16}
254_{16}	SPRITE vertical position register 1 (VS1)	VS17	VS16	VS15	VS14	VS13	VS12	VS11	VS10	?
255_{16}	SPRITE vertical position register 2 (VS2)							VS21	VS20	00_{16}
256_{16}	SPRITE horizontal position register 1 (HS1)	HS17	HS16	HS15	HS14	HS13	HS12	HS11	HS10	?
257_{16}	SPRITE horizontal position register 2 (HS2)						HS22	HS21	HS20	0 0 0 0 0 ? ? ?
258_{16}	SPRITE OSD control register (SC)			SC5	SC4	SC3	SC2	SC1	SC0	00_{16}

Internal State of Processor Status Register and Program Counter at Reset

<Bit allocation>

: } Function bit
Name :

: No function bit

0 : Fix to this bit to “0” (do not write to “1”)

1 : Fix to this bit to “1” (do not write to “0”)

<State immediately after reset>

0 : “0” immediately after reset

1 : “1” immediately after reset

? : Indeterminate immediately after reset

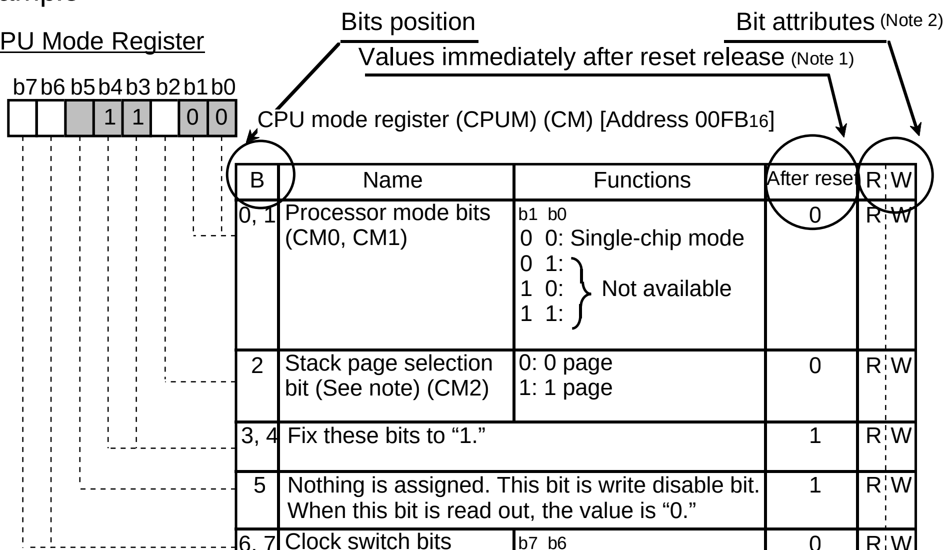
Register	Bit allocation (b7 … b0)								State immediately after reset (b7 … b0)							
Processor status register (PS)	N	V	T	B	D	I	Z	C	?	?	?	?	?	1	?	?
Program counter (PCH)									Contents of address $FFFF_{16}$							
Program counter (PCL)									Contents of address $FFFE_{16}$							

Structure of Register

The figure of each register structure describes its functions, contents at reset, and attributes as follows:

<Example>

CPU Mode Register



CPU mode register (CPUM) (CM) [Address 00FB16]

B	Name	Functions	After reset	R W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: } Not available 1 0: } Not available 1 1: } Not available	0	R W
2	Stack page selection bit (See note) (CM2)	0: 0 page 1: 1 page	0	R W
3, 4	Fix these bits to "1."		1	R W
5	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is "0."		1	R W
6, 7	Clock switch bits (CM6, CM7)	b7 b6 0 0: f(XIN) = 8 MHz 0 1: f(XIN) = 12 MHz 1 0: f(XIN) = 16 MHz 1 1: Do not set	0	R W

: Bit in which nothing is assigned

Notes 1: Values immediately after reset release

0 •••••••••••••••••"0" after reset release

1 •••••••••••••••••"1" after reset release

Indeterminate•••Indeterminate after reset release

2: Bit attributes••••••The attributes of control register bits are classified into 3 types : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

R••••••Read
- R ••••••Read enabled
- – ••••••Read disabled

W••••••Write
- W ••••••Write enabled
- – ••••••Write disabled
- ✻ ••••••"0" can be set by software, but "1" cannot be set.

RENESAS

Addresses $00C1_{16}$, $00C3_{16}$, $00C5_{16}$

Port Pi Direction Register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (Di) (i=0,1,2) [Addresses $00C1_{16}$, $00C3_{16}$, $00C5_{16}$]

B	Name	Functions	After reset	R	W
0	Port Pi direction register	0 : Port Pi_0 input mode 1 : Port Pi_0 output mode	0	R	W
1		0 : Port Pi_1 input mode 1 : Port Pi_1 output mode	0	R	W
2		0 : Port Pi_2 input mode 1 : Port Pi_2 output mode	0	R	W
3		0 : Port Pi_3 input mode 1 : Port Pi_3 output mode	0	R	W
4		0 : Port Pi_4 input mode 1 : Port Pi_4 output mode	0	R	W
5		0 : Port Pi_5 input mode 1 : Port Pi_5 output mode	0	R	W
6		0 : Port Pi_6 input mode 1 : Port Pi_6 output mode	0	R	W
7		0 : Port Pi_7 input mode 1 : Port Pi_7 output mode	0	R	W

Address $00C7_{16}$

Port P3 Direction Register

b7 b6 b5 b4 b3 b2 b1 b0

Port P3 direction register (D3) [Address $00C7_{16}$]

B	Name	Functions	After reset	R	W
0	Port P3 direction register	0 : Port $P3_0$ input mode 1 : Port $P3_0$ output mode	0	R	W
1		0 : Port $P3_1$ input mode 1 : Port $P3_1$ output mode	0	R	W
2 to 5	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
6	Timer 3 count source selection bit (T3CS)	Refer to Timer section.	0	R	W
7	Ports $P6_3$, $P6_4$ selection bits (P6IM)	Refer to clock control register (address 0216_{16}).	0	R	W

RENESAS

Address 00C9$_{16}$

Port P4 Direction Register

b7 b6 b5 b4 b3 b2 b1 b0

Port P3 direction register (D4) [Address 00C9$_{16}$]

B	Name	Functions	After reset	R	W
0	Fix this bit to "0"		0	R	W
1 to 4	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
5	Port P4 direction register	0 : Port P4$_5$ input mode 1 : SOUT output ✻	0	R	W
6		0 : Port P4$_6$ input mode 1 : SOUT output ✻	0	R	W
7	Nothing is assigned. This bit is write disable bit. When this bit is read out, the values is "0."		0	R	—

✻ When serial I/O is used

Address 00CB$_{16}$

OSD Port Control Register

b7 b6 b5 b4 b3 b2 b1 b0

OSD port control register (PF) [Address 00CB$_{16}$]

b	Name	Functions	After reset	R	W
0	Fix this bit to "0"		0	R	W
1	R, G, B output method selection bit (RGB2BIT)	0 : 4-adjustment-level analog is output from pins R, G, B. 1 : Value which is converted from 4-adjustment-level analog to 2-bit digital is output as below: High-order: from R1, G1, B1 Low-order: from R0, G0, B0	0	R	W
2	Port P5$_2$ output signal selection bit (R)	0 : R signal output 1 : Port P5$_2$ output	0	R	W
3	Port P5$_3$ output signal selection bit (G)	0 : G signal output 1 : Port P5$_3$ output	0	R	W
4	Port P5$_4$ output signal selection bit (B)	0 : B signal output 1 : Port P5$_4$ output	0	R	W
5	Port P5$_5$ output signal selection bit (OUT1)	0 : OUT1 signal output 1 : Port P5$_5$ output	0	R	W
6	Port P1$_0$ output signal selection bit (OUT2)	0 : Port P1$_0$ signal output 1 : OUT2 output	0	R	W
7	Fix this bit to "0"		0	R	W

Address 00CE16

OSD Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

OSD control register 1 (OC1) [Address 00CE16]

B	Name	Functions	After reset	R	W
0	OSD control bit (OC10) (See note 1)	0 : All-blocks display off 1 : All-blocks display on	0	R	W
1	Scan mode selection bit (OC11)	0 : Normal scan mode 1 : Bi-scan mode	0	R	W
2	Border type selection bit (OC12)	0 : All bordered 1 : Shadow bordered (See note 2)	0	R	W
3	Flash mode selection bit (OC13)	0 : Color signal of character background part does not flash 1 : Color signal of character background part flashes	0	R	W
4	Automatic solid space control bit (OC14)	0 : OFF 1 : ON	0	R	W
5	Vertical window/blank control bit (OC15)	0 : OFF 1 : ON	0	R	W
6, 7	Layer mixing control bits (OC16, OC17) (See note 3)	b7 b6 0 0: Logic sum (OR) of layer 1's color and layer 2's color 0 1: Layer 1's color has priority 1 0: Layer 2's color has priority 1 1: Do not set.	0	R	W

Notes 1 : Even this bit is switched during display, the display screen remains unchanged until a rising (falling) of the next VSYNC.
2 : Shadow border is output at right and bottom side of the font.
3 : OUT2 is always ORed, regardless of values of these bits.

Address 00CF16

Horizontal Position Register

b7 b6 b5 b4 b3 b2 b1 b0

Horizontal position register (HP) [Address 00CF16]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of horizontal display start positions (HP0 to HP7)	Horizontal display start positions 4TOSC × (setting value of high-order 4 bits × 16^1 +setting value of low-order 4 bits × 16^0)	0	R	W

Notes 1. The setting value synchronizes with the VSYNC.
2. TOSC = OSD oscillation period.

Addresses 00D0₁₆ to 00DF₁₆

Block Control Register i

b7 b6 b5 b4 b3 b2 b1 b0

Block control register i (BCi) (i=1 to 16) [Addresses $00D0_{16}$ to $00DF_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Display mode selection bits (BCi0, BCi1)	b1 b0 0 0: Display OFF 0 1: OSD mode 1 0: CC mode 1 1: CDOSD mode	Indeterminate	R	W
2	Border control bit (BCi2)	0 : Border OFF 1 : Border ON	Indeterminate	R	W
3, 4	Dot size selection bits (BCi3, BCi4)	(see dot size table below)	Indeterminate	R	W
5, 6	Pre-divide ratio selection bit (BCi5, BCi6)	(see dot size table below)	Indeterminate	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—

b6	b5	b4	b3	Pre-divide ratio	Dot size
0	0	0	0	× 1	1Tc × 1/2H
		0	1		1Tc × 1H
		1	0		2Tc × 2H
		1	1		3Tc × 3H
0	1	0	0	× 2	1Tc × 1/2H
		0	1		1Tc × 1H
		1	0		2Tc × 2H
		1	1		3Tc × 3H
1	1	0	0		1.5Tc × 1/2H (See note 3)
		0	1		1.5Tc × 1H (See note 3)
1	1	0	0	× 3	1Tc × 1/2H
		0	1		1Tc × 1H
		1	0		2Tc × 2H
		1	1		3Tc × 3H

Notes 1: Tc is OSD clock cycle divided in pre-divide circuit.
2: H is HSYNC.
3: This character size is available only in Layer 2. At this time, set layer 1's pre-divide ratio = × 2, layer 1's horizontal dot size = 1Tc.

Address 00E0₁₆

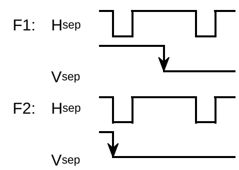
Data Slicer Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0			

Data slicer control register 1(DSC1) [Address 00E0₁₆]

B	Name	Functions	After reset	R	W
0	Data slicer and timing signal generating circuit control bit (DSC10)	0: Stopped 1: Operating	0	R	W
1	Selection bit of data slice reference voltage generating field (DSC11)	0: F2 1: F1	0	R	W
2	Reference clock source selection bit (DSC12)	0: Video signal 1: HSYNC signal	0	R	W
3 to 7	Fix these bits to “0.”		0	R	W

Definition of fields 1 (F1) and 2 (F2)



Address 00E1₁₆

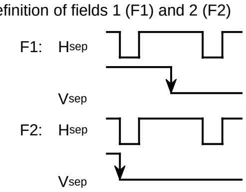
Data Slicer Control Register 2

b7	b6	b5	b4	b3	b2	b1	b0
	0					0	

Data slicer control register 2 (DSC2) [Address 00E1₁₆]

B	Name	Functions	After reset	R	W
0	Caption data latch completion flag 1 (DSC20)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	—
1	Fix this bit to “0.”		0	R	W
2	Test bit	Read-only	Indeterminate	R	—
3	Field determination flag(DSC23)	0: F2 1: F1	Indeterminate	R	—
4	Vertical synchronous signal (V_{sep}) generating method selection bit (DSC24)	0: Method (1) 1: Method (2)	0	R	W
5	V-pulse shape determination flag (DSC25)	0: Match 1: Mismatch	Indeterminate	R	—
6	Fix this bit to “0.”		0	R	W
7	Test bit	Read-only	Indeterminate	R	—

Definition of fields 1 (F1) and 2 (F2)



Address 00E6₁₆

Caption Position Register

b7 b6 b5 b4 b3 b2 b1 b0

Caption Position Register (CPS) [Address 00E6₁₆]

B	Name	Functions	After reset	R	W
0 to 4	Caption position bits(CPS0 to CPS4)		0	R	W
5	Caption data latch completion flag 2 (CPS5)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	—
6, 7	Slice line mode specification bits (in 1 field) (CPS6, CPS7)	Refer to the corresponding Table (Table 8.10.1).	0	R	W

Address 00E9₁₆

Sync Pulse Counter Register

b7 b6 b5 b4 b3 b2 b1 b0

Sync pulse counter register (HC) [Address 00E9₁₆]

B	Name	Functions	After reset	R	W
0 to 4	Count value (HC0 to HC4)		Indeterminate	R	—
5	Count source (HC5)	0: HSYNC signal 1: Composite sync signal	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Address 00EA₁₆

Clock Run-in Detect Register

b7 b6 b5 b4 b3 b2 b1 b0

Clock run-in detect register (CRD) [Address 00EA₁₆]

B	Name	Functions	After reset	R	W
0 to 2	Test bits	Read-only	0	R	—
3 to 7	Clock run-in detection bit(CRD3 to CRD7)	Number of reference clocks to be counted in one clock run-in pulse period.	0	R	—

RENESAS

Address 00EB16

Data Clock Position Register

b7 b6 b5 b4 b3 b2 b1 b0: (b2) 0, (b1) 0, (b0) 1

Data clock position register (DPS) [Address 00EB16]

B	Name	Functions	After reset	R	W
0	Fix these bits to “1.“		1	R	W
1,2	Fix this bit to “0.“		0	R	W
3	Data clock position set bits (DPS3 to DPS7)		1	R	W
4 to 7			0		

Address 00ED16

Bank Control Register

b7 b6 b5 b4 b3 b2 b1 b0: (b5) 0, (b4) 0

Bank control register (BK) [Address 00ED16]

B	Name	Functions	After reset	R	W
0 to 3	Bank selection bits (BK0 to BK3)	Bank number is selected (bank 11 to 15)	0	R	W
4, 5	Fix these bits to “0.”		0	R	W
6, 7	Bank control bits (BK6, BK7)	see table below	0	R	W

Bank control bits (BK6, BK7):

b7	b6	Bank ROM	Address 100016 level access
0	×	Not used	Read out from extra area (programmable)
1	0	Used	Read out the data from area specified by the bank selection bits
1	1	Used	Read out from extra area (data-dedicated)

Address 00EF16

A-D Control Register

b7	b6	b5	b4	b3	b2	b1	b0
0		0					

A-D control register (ADCON) [Address 00EF16]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADIN0 to ADIN2)	b2 b1 b0 0 0 0 : AD1 0 0 1 : AD2 0 1 0 : AD3 0 1 1 : AD4 1 0 0 : AD5 1 0 1 : AD6 1 1 0 : AD7 1 1 1 : AD8	0	R	W
3	A-D conversion completion bit (ADSTR)	0: Conversion in progress 1: Convertion completed	1	R	W
4	V_{CC} connection selection bit (ADVREF)	0: OFF 1: ON	0	R	W
5	Fix this bit to “0.”		0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—
7	Fix this bit to “0.”		0	R	W

RENESAS

Address $00F4_{16}$

Timer Mode Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 1 (TM1) [Address $00F4_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (TM10)	0: $f(X_{IN})/16$ or $f(X_{CIN})/16$ (See note) 1: Count source selected by bit 5 of TM1	0	R	W
1	Timer 2 count source selection bit 1 (TM11)	0: Count source selected by bit 4 of TM1 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (TM12)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (TM13)	0: Count start 1: Count stop	0	R	W
4	Timer 2 count source selection bit 2 (TM14)	0: $f(X_{IN})/16$ or $f(X_{CIN})/16$ (See note) 1: Timer 1 overflow	0	R	W
5	Timer 1 count source selection bit 2 (TM15)	0: $f(X_{IN})/4096$ or $f(X_{CIN})/4096$ (See note) 1: External clock from TIM2 pin	0	R	W
6	Timer 5 count source selection bit 2 (TM16)	0: Timer 2 overflow 1: Timer 4 overflow	0	R	W
7	Timer 6 count source selection bit (TM17)	0: $f(X_{IN})/16$ or $f(X_{CIN})/16$ (See note) 1: Timer 5 overflow	0	R	W

Note: Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register.

Address 00F5$_{16}$

Timer Mode Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 2 (TM2) [Address 00F5$_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (TM20)	(b6 at address 00C7$_{16}$) ↓ b0 0 0 : f(XIN)/16 or f(XCIN)/16 (See note) 1 0 : f(XCIN) 0 1 : } External clock from TIM3 pin 1 1 : }	0	R	W
1, 4	Timer 4 count source selection bits (TM21, TM24)	b4 b1 0 0 : Timer 3 overflow signal 0 1 : f(XIN)/16 or f(XCIN)/16 (See note) 1 0 : f(XIN)/2 or f(XCIN)/2 (See note) 1 1 : f(XCIN)	0	R	W
2	Timer 3 count stop bit (TM22)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (TM23)	0: Count start 1: Count stop	0	R	W
5	Timer 5 count stop bit (TM25)	0: Count start 1: Count stop	0	R	W
6	Timer 6 count stop bit (TM26)	0: Count start 1: Count stop	0	R	W
7	Timer 5 count source selection bit 1 (TM27)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Count source selected by bit 6 of TM1	0	R	W

Note: Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

Address 00F6$_{16}$

I^{2}C Data Shift Register

b7 b6 b5 b4 b3 b2 b1 b0

I^{2}C data shift register (S0) [Address 00F6$_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	D0 to D7	This is an 8-bit shift register to store receive data and write transmit data.	Indeterminate	R	W

Note: To write data into the I^{2}C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

Address 00F7$_{16}$

I^{2}C Address Register

b7 b6 b5 b4 b3 b2 b1 b0

I^{2}C address register (S0D) [Address 00F7$_{16}$]

B	Name	Functions	After reset	R	W
0	$\overline{\text{Read}}$/write bit (RBW)	<Only in 10-bit addressing (in slave) mode> The last significant bit of address data is compared. 0: Wait the first byte of slave address after START condition (read state) 1: Wait the first byte of slave address after RESTART condition (write state)	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	<In both modes> The address data is compared.	0	R	W

Address 00F8$_{16}$

I^{2}C Status Register

b7 b6 b5 b4 b3 b2 b1 b0

I^{2}C status register (S1) [Address 00F8$_{16}$]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0" 1 : Last bit = "1" (See note)	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected (See note)	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address mismatch 1 : Address match (See note)	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected (See note)	0	R	—
4	I^{2}C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	1	R	W
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave recieve mode 0 1 : Slave transmit mode 1 0 : Master recieve mode 1 1 : Master transmit mode	0	R	W

Note : These bits and flags can be read out, but cannnot be written.

Address 00F9$_{16}$

I^{2}C Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I^{2}C control register (S1D) [Address 00F9$_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Bit counter (Number of transmit/recieve bits) (BC0 to BC2)	b2 b1 b0 0 0 0: 8 0 0 1: 7 0 1 0: 6 0 1 1: 5 1 0 0: 4 1 0 1: 3 1 1 0: 2 1 1 1: 1	0	R	W
3	I^{2}C-BUS interface use enable bit (ESO)	0: Disabled 1: Enabled	0	R	W
4	Data format selection bit (ALS)	0: Addressing format 1: Free data format	0	R	W
5	Addressing format selection bit (10BIT SAD)	0: 7-bit addressing format 1: 10-bit addressing format	0	R	W
6, 7	Connection control bits between I^{2}C-BUS interface and ports (BSEL0, BSEL1)	b7 b6 Connection port (See note) 0 0: None 0 1: SCL1, SDA1 1 0: SCL2, SDA2 1 1: SCL1, SDA1, SCL2, SDA2	0	R	W

Address 00FA16

I2C Clock Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I2C clock control register (S2) [Address 00FA16]

B	Name	Functions			After reset	R	W
0 to 4	SCL frequency control bits (CCR0 to CCR4)	Register value b4 to b0	Standard clock mode	High speed clock mode	0	R	W
		00 to 02	Setup disabled	Setup disabled			
		03	Setup disabled	333			
		04	Setup disabled	250			
		05	100	400 (See note)			
		06	83.3	166			
		⋮	500/CCR value	1000/CCR value			
		1D	17.2	34.5			
		1E	16.6	33.3			
		1F	16.1	32.3			
		(at f = 4 MHz, unit : kHz)					
5	SCL mode specification bit (FAST MODE)	0: Standard clock mode 1: High-speed clock mode			0	R	W
6	ACK bit (ACK BIT)	0: ACK is returned. 1: ACK is not returned.			0	R	W
7	ACK clock bit (ACK)	0: No ACK clock 1: ACK clock			0	R	W

Note: At 400 kHz in the high-speed clock mode, the duty is as below .
"0" period : "1" period = 3 : 2
In the other cases, the duty is as below.
"0" period : "1" period = 1 : 1

Address 00FB16

CPU Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

b7	b6	b5	b4	b3	b2	b1	b0
			1	1		0	0

CPU mode register (CM) [Address 00FB16]

B	Name	Functions	After reset	R	W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: Not available 1 0: Not available 1 1: Not available	0	R	W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R	W
3, 4	Fix these bits to "1."		1	R	W
5	XCOUT drivability selection bit (CM5)	0: LOW drive 1: HIGH drive	1	R	W
6	Main Clock (XIN–XOUT) stop bit (CM6)	0: Oscillating 1: Stopped	0	R	W
7	Internal system clock selection bit (CM7)	0: XIN–XOUT selected (high-speed mode) 1: XCIN–XCOUT selected (low-speed mode)	0	R	W

Note: This bit is set to "1" after the reset release.

Address 00FC16

Interrupt Request Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
6	A-D conversion • INT3 external interrupt request bit (ADR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

✻ : “0” can be set by software, but “1” cannot be set.

Address 00FD16

Interrupt Request Register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

Interrupt request register 2 (IREQ2) [Address 00FD16]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt request bit (IN1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	Data slicer interrupt request bit (DSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Serial I/O interrupt request bit (SIOR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	f(XIN)/4096 • SPRITE OSD interrupt request bit (CKR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	INT2 external interrupt request bit (IN2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	Multi-master I^2C-BUS interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
6	Timer 5 • 6 interrupt request bit (TM56R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	Fix this bit to “0.”		0	R	W

✻: “0” can be set by software, but “1” cannot be set.

Address $00FE_{16}$

Interrupt Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address $00FE_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	OSD interrupt enable bit (OSDE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	A-D conversion • INT3 external interrupt enable bit (ADE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Address $00FF_{16}$

Interrupt Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 2 (ICON2) [Address $00FF_{16}$]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt enable bit (IN1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Data slicer interrupt enable bit (DSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (SIOE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	$f(X_{IN})/4096$ • SPRITE OSD interrupt enable bit (CKE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	INT2 external interrupt enable bit (IN2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	Multi-master I^2C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Timer 5 • 6 interrupt enable bit (TM56E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Timer 5 • 6 interrupt switch bit (TM56S)	0 : Timer 5 1 : Timer 6	0	R	W

Address $020A_{16}$

PWM Mode Register 1

b7 b6 b5 b4 b3 b2 b1 b0

PWM mode register 1 (PN) [Address $020A_{16}$]

B	Name	Functions	After reset	R	W
0	PWM counts source selection bit (PN0)	0 : Count source supply 1 : Count source stop	0	R	W
1, 2	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
3	PWM output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	$P0_3$/PWM7 output selection bit (PN4)	0 : $P0_3$ output 1 : PWM7 output	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out. the values are “0.”		0	R	—

Address $020B_{16}$

PWM Mode Register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

PWM mode register 2 (PW) [Address $020B_{16}$]

B	Name	Functions	After reset	R	W
0	$P0_4$/PWM0 output selection bit (PW0)	0 : $P0_4$ output 1 : PWM0 output	0	R	W
1	$P0_5$/PWM1 output selection bit (PW1)	0 : $P0_5$ output 1 : PWM1 output	0	R	W
2	$P0_6$/PWM2 output selection bit (PW2)	0 : $P0_6$ output 1 : PWM2 output	0	R	W
3	$P0_7$/PWM3 output selection bit (PW3)	0 : $P0_7$ output 1 : PWM3 output	0	R	W
4	$P0_0$/PWM4 output selection bit (PW4)	0 : $P0_0$ output 1 : PWM4 output	0	R	W
5	$P0_1$/PWM5 output selection bit (PW5)	0: $P0_1$ output 1: PWM5 output	0	R	W
6	$P0_2$/PWM6 output selection bit (PW6)	0: $P0_2$ output 1: PWM6 output	0	R	W
7	Fix this bit to “0.”		0	R	W

RENESAS

Address 0210₁₆

ROM Correction Enable Register

b7 b6 b5 b4 b3 b2 b1 b0: [ ][ ][ ][ ][0][0][ ][ ]

ROM correction enable register (RCR) [Address 0210_{16}]

B	Name	Functions	After reset	R W
0	Vector 1 enable bit (RCR0)	0: Disabled 1: Enabled	0	R W
1	Vector 2 enable bit (RCR1)	0: Disabled 1: Enabled	0	R W
2, 3	Fix these bits to “0.”		0	R W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R —

Address 0212₁₆

Interrupt Input Polarity Register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt input polarity register (IP) [Address 0212_{16}]

B	Name	Functions	After reset	R W
0 to 2	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R —
3	INT1 polarity switch bit (POL1)	0 : Positive polarity 1 : Negative polarity	0	R W
4	INT2 polarity switch bit (POL2)	0 : Positive polarity 1 : Negative polarity	0	R W
5	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is “0.”		0	R —
6	INT3 polarity switch bit (POL3)	0 : Positive polarity 1 : Negative polarity	0	R W
7	A-D conversion • INT3 interrupt source selection bit (AD/INT3SEL)	0 : INT3 interrupt 1 : A-D conversion interrupt	0	R W

Address 0213₁₆

Serial I/O Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O mode register (SM) [Address 0213_{16}]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: f(X_{IN})/8 or f(X_{CIN})/8 0 1: f(X_{IN})/16 or f(X_{CIN})/16 1 0: f(X_{IN})/32 or f(X_{CIN})/32 1 1: f(X_{IN})/64 or f(X_{CIN})/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Port function selection bit (SM3)	0: $P1_1$, $P1_3$ 1: SCL1, SDA1	0	R	W
4	Port function selection bit (SM4)	0: $P1_2$, $P1_4$ 1: SCL2, SDA2	0	R	W
5	Transfer direction selection bit (SM5)	0: Transfer from the last significant bit (LSB) 1: Transfer from the top significant bit (MSB)	0	R	W
6	S_{IN} pin switch bit (SM6)	0: $P1_7$ is S_{IN} pin 1: $P7_2$ is S_{IN} pin	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Address 0215$_{16}$

OSD Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

OSD control register 2 (OC2) [Address 0215$_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Display layer selection bits (OC20, OC21)	b1 b0 / Layer 1 / Layer 2 0 0 / CC, OSD, CDOSD / — 0 1 / CC, OSD / CDOSD 1 0 / CC, CDOSD / OSD 1 1 / CC / CDOSD, OSD	0	R	W
2	R, G, B signal output selection bit(OC22)	0: Digital output (See note) 1: Analog output (4 gradations)	0	R	W
3	Solid space output bit (OC23)	0: OUT1 output 1: OUT2 output	0	R	W
4	Horizotal window/blank coutrol bit (OC24)	0: OFF 1: ON	0	R	W
5	Window/blank selection bit 1 (horizontal) (OC25)	0: Horizontal blank function 1: Horizontal window function	0	R	W
6	Window/blank selection bit 2 (vertical) (OC26)	0: Vertical blank function 1: Vertical window function	0	R	W
7	OSD interrupt request selection bit (OC27)	0: At completion of layer 1 block display 1: At completion of layer 2 block display	0	R	W

Note: When setting bit 1 of the OSD port control register to "1," the value which is converted from the 4-adjustment-level analog to the 2-bit digital is output regardless of this bit value as follows : the high-order bit (R1, G1 and B1) is output from pins $P5_2$, $P5_3$ and $P5_4$, and the low-order bit is (R0, G0 and B0) output from pins $P1_7$, $P1_5$ and $P1_6$. And besides, when not using OSD function, the low-power dissipation can realize by setting this bit to "0."

RENESAS

Address 0216_{16}

Clock Control Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0			

Clock control register (CS) [Address 0216_{16}]

B	Name	Functions	After reset	R	W
0	Clock selection bit (CS0)	0: Data slicer clock 1: OSC1 clock	0	R	W
1, 2	OSC1 oscillating mode selection bits (CS1, CS2)	b2 b1 0 0: 32kHz oscillating mode. 0 1: Used as input port of $P6_3$ and $P6_4$ (See note 1). 1 0: LC oscillating mode 1 1: Ceramic • quartz-crystal oscillating mode	0	R	W
3 to 6	Fix these bits to “0.”		0	R	W
7	Test bit (See note 2)		0	R	W

Note 1: Set bit 7 of address $00C7_{16}$ to “1”, when OSC1 and OSC2 are used as $P6_3$ and $P6_4$.

2: Be sure to set bit 7 to “0” for program of the mask and the EPROM versions. For the emulator MCU version (M37280ERSS), be sure to set bit 7 to “1” when using the data slicer clock for software debugging.

Address 0217_{16}

I/O Polarity Control Register

b7	b6	b5	b4	b3	b2	b1	b0

I/O polarity control register (PC) [Address 0217_{16}]

B	Name	Functions	After reset	R	W
0	HSYNC input polarity switch bit (PC0)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
1	VSYNC input polarity switch bit (PC1)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
2	R, G, B output polarity switch bit (PC2)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
3	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0”.		0	R	—
4	OUT1 output polarity switch bit (PC4)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
5	OUT2 output polarity switch bit (PC5)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
6	Display dot line selection bit (PC6) (See note)	0 : “□” at even field “▨” at odd field 1 : “▨” at even field “□” at odd field	0	R	W
7	Field determination flag(PC7)	0 : Even field 1 : Odd field	1	R	—

Note: Refer to Fig. 8.11.19.

RENESAS

Address 0218₁₆

Raster Color Register

b7 b6 b5 b4 b3 b2 b1 b0

Raster color register (RC) [Address 0218₁₆]

B	Name	Functions	At reset	R	W
0, 1	Raster color R control bits (RC0, RC1)	b0 b1 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
2, 3	Raster color G control bits (RC2, RC3)	b3 b2 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
4, 5	Raster color B control bits (RC4, RC5)	b5 b4 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
6	Raster color OUT1 control bits (RC6)	0: No output 1: Output	0	R	W
7	Raster color OUT2 0 control bits (RC7)	0: No output 1: Output	0	R	W

Note: When selecting digital output, Vcc is output at any other values except “00.”

Address 0219₁₆

OSD Control Register 3

b7 b6 b5 b4 b3 b2 b1 b0

OSD control register 3 (OC3) [Address 0219₁₆]

B	Name	Functions	After reset	R	W
0	CC mode character color selection bit (OC30)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
1, 2	CC mode character background color selection bits (OC31, OC32) (See note)	b1 b1 0 0: Color code 0 to 3 0 1: Color code 4 to 7 1 0: Color code 8 to 11 1 1: Color code 12 to 15	0	R	W
3	CDOSD mode character color selection bit (OC33)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
4	SPRITE color selection bit (OC34)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
5	OSD mode window control bit (OC35)	0: Window OFF 1: Window ON	0	R	W
6	CC mode window control bit (OC36)	0: Window OFF 1: Window ON	0	R	W
7	CDOSD mode window control bit (OC37)	0: Window OFF 1: Window ON	0	R	W

Note: Color pallet 8 is always selected for solid space (when OUT1 output is selected), regardress of value of this register.

Address 021C16

Top Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Top border control register 1 (TB1) [Address 021C16]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of top border (TB10 to TB17)	Top border position (low-order 8 bits) TH ✕ (setting value of low-order 2 bits of TB2 ✕ 16^2 + setting value of high-order 4 bits of TB1 ✕ 16^1 + setting value of low-order 4 bits of TB1 ✕ 16^0)	Indeterminate	R	W

Notes 1: Do not set “0016” or “0116” to the TB1 at TB2 = “0016.”

2: TH is cycle of HSYNC.

3: TB2 is top border control register 2.

Address 021D16

Bottom Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Bottom border control register 1 (BB1) [Address 021D16]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of bottom border (BB10 to BB17)	Bottom border position (low-order 8 bits) TH✕ (setting value of low-order 2 bits of BB2 ✕ 16^2 + setting value of high-order 4 bits of BB1 ✕ 16^1 + setting value of low-order 4 bits of BB1 ✕ 16^0)	Indeterminate	R	W

Notes 1: Set values fit for the following condition:
(TB1 + TB2 ✕ 16^2) < (BB1 + BB2 ✕ 16^2).

2: TH is cycle of HSYNC.

3: BB2 is bottom border control reigster 2.

Address 021E16

Top Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Top border control register 2 (TB2) [Address 021E16]

B	Name	Functions	After reset	R	W
0, 1	Control bits of top border (TB20 ,TB21)	Top border position (high-order 2 bits) TH × (setting value of low-order 2 bits of TB2 × 16^2 + setting value of high-order 4 bits of TB1 × 16^1 + setting value of low-order 4 bits of TB1 × 16^0)	Indeterminate	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R	—

Notes 1: Do not set “0016” or “0116” to the TB1 at TB2 = “0016.”
2: TH is cycle of HSYNC.
3: TB1 is top border control register 1.

Address 021F16

Bottom Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Bottom border control register 2 (BB2) [Address 021F16]

B	Name	Functions	After reset	R	W
0, 1	Control bits of bottom border (BB20, BB21)	Bottom border position (high-order 2 bits) TH × (setting value of low-order 2 bits of BB2 × 16^2 + setting value of high-order 4 bits of BB1 × 16^1 + setting value of low-order 4 bits of BB1 × 16^0)	Indeterminate	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R	—

Notes 1: Set values fit for the following condition:
(TB1 + TB2 × 16^2) < (BB1 + BB2 × 16^2).
2: TH is cycle of HSYNC.
3: BB1 is bottom border control reigster 1.

RENESAS

Addresses 0220_{16} to $022F_{16}$

Vertical Position Register 1i

b7 b6 b5 b4 b3 b2 b1 b0

Vertical position register 1i (VP1i) (i = 1 to 16) [Addresses 0220_{16} to $022F_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of vertical display start positions (VP1i0 to VP1i7) (See note 1)	Vertical display start positions (low-order 8 bits) TH × (setting value of low-order 2 bits of VP2i × 16^2 + setting value of low-order 4 bits of VP1i × 16^1 + setting value of low-order 4 bits of VP1i × 16^0)	Indeterminate	R	W

Notes 1: Do not "00_{16}" and "01_{16}" to VP1i at VP2i = "00_{16}."

2: T_H is cycle of HSYNC.

3: VP2i is vertical position register 2i.

Addresses 0230_{16} to $023F_{16}$

Vertical Position Register 2i

b7 b6 b5 b4 b3 b2 b1 b0

Vertical position register 2i (VP2i) (i = 1 to 16) [Addresses 0230_{16} to $023F_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Control bits of vertical display start positions (VP2i0, VP2i1) (See note 1)	Vertical display start positions (high-order 2 bits) TH × (setting value of low-order 2 bits of VP2i × 16^2 + setting value of low-order 4 bits of VP1i × 16^1 + setting value of low-order 4 bits of VP1i × 16^0)	Indeterminate	R	W
2 to 7	Nothing ic assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R	—

Notes 1: Do not set "00_{16}" and "01_{16}" to VP1i at VP2i = "00_{16}."

2: T_H is cycle of HSYNC.

3: VP1i is vertical position register 1i.

Addresses 0241_{16} to 0247_{16}, 0249_{16} to $024F_{16}$

Color Pallet Register i

b7 b6 b5 b4 b3 b2 b1 b0

Color pallet register i (CRi) (i = 1 to 7, 9to15) [Addresses $0241_{16}$to 0247_{16},$0249_{16}$to $024F_{16}$]

B	Name	Functions	After reset	R	W
0, 1	R signal output control bits (CRi0, CRi1)	b0 b1 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R	W
2, 3	G signal output control bits (CRi2, CRi3)	b3 b2 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R	W
4, 5	B signal output control bits (CRi4, CRi5)	b5 b4 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R	W
6	OUT1 signal output control bit (CRi6)	0: No output 1: Output	Indeterminate	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—

Note: When selecting digital output, the output is Vcc at all values other than “00.”

Address 0250₁₆

Left Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Left border control register 1 (LB1) [Address 0250_{16}]

B	Name	Functions	After reset	R	W
0	Control bits of left border (LB10 to LB17)	Left border position (low-order 8 bits) Tosc × (setting value of low-order 3 bits of LB2 ×16^2 + setting value of high-order 4 bits of LB1 ×16^1 + setting value of low-order 4 bits of LB1 ×16^0)	1	R	W
1 to 7			0		

Notes 1: Do not set LB1 = LB2 = "00_{16}."
2: Set values fit for the following condition:
(LB1 + LB2 × 16^2) < (RB1 + RB2 × 16^2).
3: Tosc is OSD oscillation period.
4: LB2 is left border control register 2.

Address 0251₁₆

Left Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Left border controlregister 2 (LB2) [Address 0251_{16}]

B	Name	Functions	After reset	R	W
0 to 2	Control bits of left border (LB20 to LB22)	Left borderposition (high-order 3 bits) Tosc × (setting value of low-order 3 bits of LB2 ×16^2 + setting value of high-order 4 bits of LB1 ×16^1 + setting value of low-order 4 bits of LB1 ×16^0)	0	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		0	R	W

Notes 1: Do not set LB1 = LB2 = "00_{16}."
2: Set values fit for the following condition:
(LB1 + LB2 × 16^2) < (RB1 + RB2 × 16^2).
3: Tosc is OSD oscillation period.
4: LB1 is left border control register 1.

Address 0252_{16}

Right Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Right border control register 1 (RB1) [Address 0252_{16}]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of right border (RB10 to RB17)	Right border position (low-order 8 bits) Tosc × (setting value of low-order 3 bits of RB2 $\times 16^2$ + setting value of high-order 4 bits of RB1 $\times 16^1$ + setting value of low-order 4 bits of RB1 $\times 16^0$)	1	R	W

Notes 1: Set values fit for the following condition:
$(LB1 + LB2 \times 16^2) < (RB1 + RB2 \times 16^2)$.
2: Tosc is OSD oscillation period.
3: RB2 is right border control register 2.

Address 0253_{16}

Right Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Right border control register 2 (RB2) [Address 0253_{16}]

B	Name	Functions	After reset	R	W
0 to 2	Control bits of right border (RB20 to RB22)	Right border position (high-order 3 bits) Tosc × (setting value of low-order 3 bits of RB2 $\times 16^2$ + setting value of high-order 4 bits of RB1 $\times 16^1$ + setting value of low-order 4 bits of RB1 $\times 16^0$)	1	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0”.		0	R	W

Notes 1: Set values fit for the following condition:
$(LB1 + LB2 \times 16^2) < (RB1 + RB2 \times 16^2)$.
2: Tosc is OSD oscillation period.
3: RB1 is right border control register 1.

Address 0254_{16}

SPRITE Vertical Position Register 1

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE vertical position register 1 (VS1) [Address 0254_{16}]

B	Name	Functions	Afte reset	R	W
0	Vertical display start position control bits of SPRITE OSD (VS10 to VS17)	Vertical display start position (low-order 8 bits) TH × (setting value of low-order 2 bits of VS2 × 16^2 + setting value of high-order 4 bits of VS1 × 16^1 + setting value of low-order 4 bits of VS1 × 16^0)	1	R	W
1 to 7			0		

Notes 1: Do not set "00_{16}" to the VS1 at VS2 = "00_{16}."
2: T_H is cycle of HSYNC.
3: VS2 is SPRITE vertical position register 2.

Address 0255_{16}

SPRITE Vertical Position Register 2

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE vertical position register 2 (VS2) [Address 0255_{16}]

B	Name	Functions	After reset	R	W
0, 1	Vertical start position control bits of SPRITE OSD (VS20, VS21)	Vertical display start position (high-order 2 bits) TH × (setting value of low-order 2 bits of VS2 ×16^2 + setting value of high-order 4 bits of VS1 ×16^1 + setting value of low-order 4 bits of VS1 ×16^0)	0	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0".		0	R	—

Notes 1: Do not set "00_{16}" to the VS1 at VS2 = "00_{16}."
2: T_H is cycle of HSYNC.
3: VS1 is SPRITE vertical position register 1.

Address 0256$_{16}$

SPRITE Horizontal Position Register 1

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE horizontal position register 1 (HS1) [Address 0256$_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Horizontal display start position control bits of SPRITE OSD (HS10 toHS17)	Horizontal display start position (low-order 8 bits) TOSC × (setting value of low-order 3 bits of HS2 ×16^2 + setting value of high-order 4 bits of HS1 ×16^1 + setting value of low-order 4 bits of HS1 ×16^0)	Indeterminate	R	W

Notes 1: Do not set HS1 < "30$_{16}$" at HS2 = "00$_{16}$."

2: TOSC is OSD oscillation period.

3: HS2 is SPRITE horizontal position register 2.

Address 0257$_{16}$

SPRITE Horizontal Position Register 2

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE horizontal position register 2 (HS2) [Address 0257$_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Horizontal display start position control bits of SPRITE OSD (HS20 to HS22)	Horizontal display start position (high-order 3 bits) TOSC × (setting value of low-order 3 bits of HS2 × 16^2 + setting value of high-order 4 bits of HS1 × 16^1 + setting value of low-order 4 bits of HS1 × 16^0)	Indeterminate	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Notes 1: Do not set HS1< "30$_{16}$" at HS2 = "00$_{16}$."

2: TOSC is oscillation period.

3: HS1 is SPRITE horizontal position register 1.

Address 0258₁₆

SPRITE OSD Control Register

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE OSD control register (SC) [Address 0258_{16}]

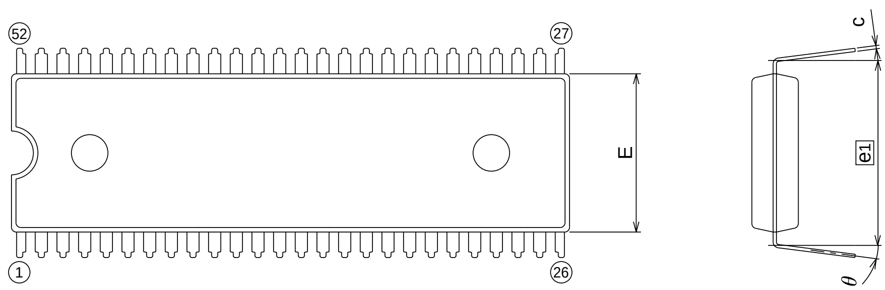
B	Name	Functions	After reset	R	W
0	SPRITE OSD control bit (SC0)	0: Stopped 1: Operating	0	R	W
1	Pre-divide ratio selection bit (SC1)	0: Pre-divide ratio 1 1: Pre-divide ratio 2	0	R	W
2, 3	Dot size selection bits (SC2, SC3)	b3 b2 0 0: 1Tc ✕ 1/2H 0 1: 1Tc ✕ 1H 1 0: 2Tc ✕ 1H 1 1: 2Tc ✕ 2H	0	R	W
4	Interrupt occurrence position selection bit (SC4)	0: After display of horizontal 20 dots 1: After display of horizontal 10 dots or 20 dots	0	R	W
5	X_{IN}/4096 • SPRITE interrupt source switch bit (SC5)	0: X_{IN}/4096 interrupt 1: SPRITE OSD interrupt	0	R	W
6, 7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0”.		0	R	—

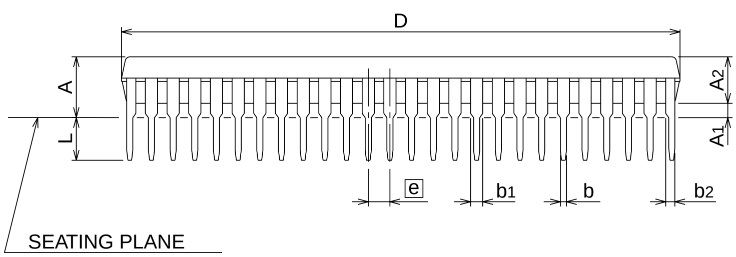
Notes 1: Tc : Pre-devided clock period for OSD
2: H : H_{SYNC}

19. PACKAGE OUTLINE

52P4B (MMP) **Plastic 52pin 600mil SDIP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP52-P-600-1.78	–	5.1	Alloy 42/Cu Alloy





Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.5
A_1	0.51	–	–
A_2	–	3.8	–
b	0.4	0.5	0.59
b_1	0.9	1.0	1.3
b_2	0.65	0.75	1.05
c	0.22	0.27	0.34
D	45.65	45.85	46.05
E	12.85	13.0	13.15
e	–	1.778	–
e_1	–	15.24	–
L	3.0	–	–
θ	0°	–	15°

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REVISION DESCRIPTION LIST	M37281MAH–XXXSP,M37281MFH–XXXSP M37281MKH–XXXSP,M37281EKSP(Rev.1.0) Data Sheet

Rev. No.	Revision Description	Rev. date
1.00	First Edition	0111
1.01	P128 16. PROM PROGRAMMING METHOD Name of Programming Adapter PCA7401 is changed to PCA7400.	0307