TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MP245FK

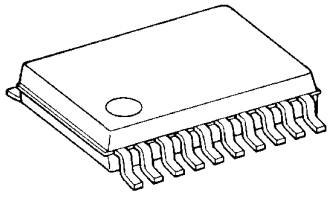
Low-Voltage/Low-Power Octal Bus Transceiver with Bus-hold

The TC7MP245FK is a high-performance CMOS octal bus transceiver. By a low power consumption circuit, power consumption has been reduced when a bus terminal is disable state ($\overline{OE}$=High).

The direction of data transmission is determined by the level of the DIR input. The $\overline{OE}$ input can be used to disable the device so that the busses are effectively isolated.

But, bus of a B bus side at floating state is maintained in an appropriate logic level due to a bus hold circuit to a B bus. Moreover, the bus-hold circuit which is added to a B bus is off when $\overline{OE}$ is low.

All inputs are equipped with protection circuits against static discharge.



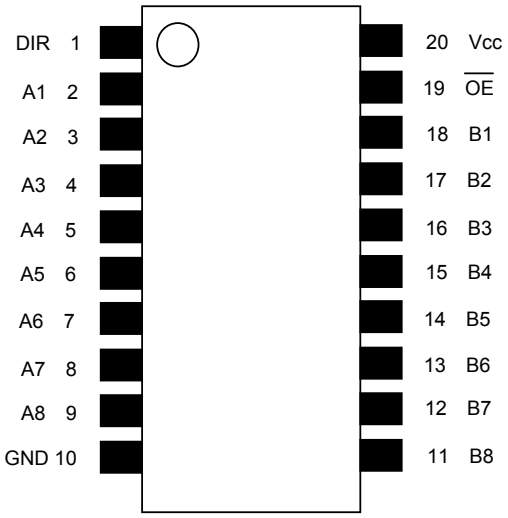
VSSOP20-P-0030-0.50

Weight: 0.03 g (typ.)

Features

- Low-voltage operation : VCC = 1.65 to 3.6 V
- Low power current consumption : By a new input circuit, power consumption in $\overline{OE}$=H is reduced largely. It is most suitable for battery drive products such as personal digital assistant or a cellular phone.
- Quiescent supply current : I_{CC} = 5 μA (max) (Vcc=3.6V)
- High-speed operation : tpd=3.0ns (max) (Vcc=3.3±0.3V)
  tpd=4.6ns (max) (Vcc=2.5±0.2V)
  tpd=10.0ns (max) (Vcc=1.8±0.15V)
- Output current : I_{OHA}/I_{OLA} (A bus) =±12mA (min) (V_{CC}=3.0V)
  : I_{OHB}/I_{OLB} (B bus) =±24mA (min) (V_{CC}=3.0V)
- Latch-up performance : ±300mA
- ESD performance : Machine model ＞±200V
  : Human body model ＞±2000V
- Ultra-small package : VSSOP (US20)
- Bus hold circuit is built in only the B bus side. (Only in $\overline{OE}$=H, a former state is maintained.)
- Floating of A-bus and B-bus are permitted.(When $\overline{OE}$=H)
- Gate IC for control(TC7MP01FK) of DIR and $\overline{OE}$ terminal are prepared.
- 3.6V tolerant function provided on A-bus terminal, DIR and $\overline{OE}$ terminal.
  Note: At the time bus terminal is enable state, please do not give a signal from the outside.

Pin Assighment (top view)



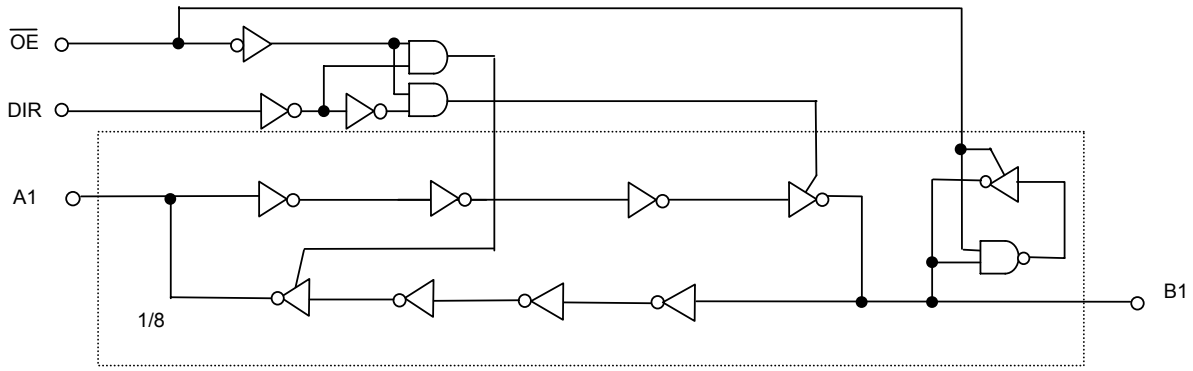
Truth Table

Input		Bus state	Bus hold circuit (B bus)
DIR	$\overline{OE}$		
L	L	B→A(B=A)	OFF
H	L	A→B(A=B)	OFF
X	H	Z	ON*

X: Don't care
Z: High impedance
*: Logic state just before becoming disable is maintained.

Note: When a bus input is in "H" state ,and an output is switched to "enable" to "disable",
Glitch such as "L" state during about 1 to 3ns occurs in an output.
It is not generated when a bus input is in "L" state.

System Diagram



Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	Vcc	−0.5 to 4.6	V
DC input voltage (DIR,$\overline{OE}$)	V_{IN}	−0.5 to 4.6	V
DC input/output voltage(A bus)	VI/OA	−0.5 to 4.6 (Note 1)	V
		−0.5 to Vcc+0.5 (Note 2)	
DC input/output voltage(B bus)	VI/OB	−0.5 to Vcc+0.5	V
Input diode current(DIR,$\overline{OE}$)	I_{IIK}	−50	mA
Input/Output diode current	$I_{I/OK}$	±50	mA
Output current	I_{OUT}	±50	mA
DC VCC/ground current	I_{CC}/I_{GND}	±100	mA
Power dissipation	P_D	180	mW
Storage temperature	Tstg	−65 to 150	°C

Note 1: VCC=0V, or output off state.
Note 2: $\overline{OE}$="L", DIR="L"

Recommended Operating Range

Parameter	Symbol	Rating	Unit
Power supply voltage	Vcc	1.65 to 3.6	V
		1.2 to 3.6(Note 3)	
DC input voltage (DIR,$\overline{OE}$)	V_{IN}	−0.3 to 3.6	V
DC input/output voltage(A bus)	VI/OA	0 to 3.6(Note 4)	V
		0 to Vcc(Note 5)	
DC input/output voltage(B bus)	VI/OB	0 to Vcc	V
Output current (A bus)	I_{OHA}/I_{OLA}	±12(Note 6)	mA
		±9(Note 7)	
		±2(Note 8)	
Output current(B bus)	I_{OHB}/I_{OLB}	±24(Note 6)	mA
		±18(Note 7)	
		±4(Note 8)	
Operating temperature	Topr	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10(Note 9)	ns/V

Note 3: Data retention only

Note 4: V_{CC}=0V, or output off state

Note 5: $\overline{OE}$="L", DIR="L"

Note 6: V_{CC}=3.0 to 3.6V

Note 7: V_{CC}=2.3 to 2.7V

Note 8: V_{CC}=1.65 to 1.95V

Note 9: V_{IN}=0.8 to 2.0V, V_{CC}=3.0V

Electrical Characteristics

DC Characteristics (Ta=-40 to 85℃, 2.7V＜Vcc≦3.6V)

Parameter		Symbol	Test Condition		Vcc(V)	Min	Max	Unit
DC input voltage	H-level	V_{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V_{IL}	—		2.7 to 3.6	—	0.8	
Output voltage (A bus)	H-level	V_{0HA}	V_{IN}= V_{IH}	I_{OHA}=-100uA	2.7 to 3.6	Vcc-0.2	—	V
				I_{OH}=-6mA	2.7	2.2	—	
				I_{OH}=-9mA	3.0	2.4	—	
				I_{OH}=-12mA	3.0	2.2	—	
	L-level	V_{0LA}	V_{IN}= V_{IL}	I_{OLA}=100uA	2.7 to 3.6	—	0.2	
				I_{OL}=6mA	2.7	—	0.4	
				I_{OL}=9mA	3.0	—	0.4	
				I_{OL}=12mA	3.0	—	0.55	
Output voltage (B bus)	H-level	V_{0HB}	V_{IN}= V_{IH}	I_{OHB}=-100uA	2.7 to 3.6	Vcc-0.2	—	V
				I_{OHB}=-12mA	2.7	2.2	—	
				I_{OHB}=-18mA	3.0	2.4	—	
				I_{OHB}=-24mA	3.0	2.2	—	
	L-level	V_{0LB}	V_{IN}= V_{IL}	I_{OLB}=100uA	2.7 to 3.6	—	0.2	
				I_{OLB}=12mA	2.7	—	0.4	
				I_{OLB}=18mA	3.0	—	0.4	
				I_{OLB}=24mA	3.0	—	0.55	
Input leakage current(DIR,/OE)		I_{IN}	V_{IN}=0 to 3.6V		2.7 to 3.6	—	±5.0	μA
Power off leakage current		I_{OFF}	A,DIR,/OE=0 to 3.6V		0	—	5.0	μA
3-state output off-state current		I_{OZA}	V_{INA}=V_{IH} or V_{IL} Vout=0 to 3.6V		2.7 to 3.6	—	±5.0	μA
		I_{OZB}	V_{INB}=V_{IH} or V_{IL} Vout=0 or V_{CC}		2.7 to 3.6	—	±5.0	μA
Quiescent supply current		I_{CC}	V_{IN}=V_{CC} or GND,		2.7 to 3.6	—	5.0	μA
Increase in ICC per input		ΔI_{CC}	V_{IN}=V_{CC}-0.6V (per input)		2.7 to 3.6	—	750	μA
Bushold input minimum drive hold current		I_{IHOLD}	V_{IN}=0.8V		3.0	75	—	μA
			V_{IN}=2.0V			-75	—	
Bushold input over-drive current to change state		I_{IOD}	(Note 10)		3.6	—	550	μA
			(Note 11)			—	-550	

Note 10: An external driver must source at least the specified current to switch from LOW-to-HIGH.
Note 11: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

DC Characteristics (Ta=-40 to 85℃, 2.3V≦Vcc≦2.7V)

Parameter		Symbol	Test Condition		Vcc(V)	Min	Max	Unit
DC input voltage	H-level	V_{IH}	—		2.3 to 2.7	1.6	—	V
	L-level	V_{IL}	—		2.3 to 2.7	—	0.7	
Output voltage (A bus)	H-level	V_{0HA}	V_{IN}= V_{IH}	I_{OHA}=−100uA	2.3 to 2.7	Vcc−0.2	—	V
				I_{OHA}=−3mA	2.3	2.0	—	
				I_{OHA}=−6mA	2.3	1.8	—	
				I_{OHA}=−9mA	2.3	1.7	—	
	L-level	V_{0LA}	V_{IN}= V_{IL}	I_{OLA}=100uA	2.3 to 2.7	—	0.2	
				I_{OLA}=6mA	2.3	—	0.4	
				I_{OLA}=9mA	2.3	—	0.6	
Output voltage (B bus)	H-level	V_{0HB}	V_{IN}= V_{IH}	I_{OHB}=−100uA	2.3 to 2.7	Vcc−0.2	—	V
				I_{OHB}=−6mA	2.3	2.0	—	
				I_{OHB}=−12mA	2.3	1.8	—	
				I_{OHB}=−18mA	2.3	1.7	—	
	L−level	V_{0LB}	V_{IN}= V_{IL}	I_{OLB}=100uA	2.3 to 2.7	—	0.2	
				I_{OLB}=12mA	2.3	—	0.4	
				I_{OLB}=18mA	2.3	—	0.6	
Input leakage current(DIR,/OE)		I_{IN}	V_{IN}=0 to 3.6V		2.3 to 2.7	—	±5.0	μA
Power off leakage current		I_{OFF}	A,DIR,/OE=0 to 3.6V		0	—	5.0	μA
3-state output off-state current		I_{OZA}	V_{INA}=V_{IH} or V_{IL} Vout=0 to 3.6V		2.3 to 2.7	—	±5.0	μA
		I_{OZB}	V_{INB}=V_{IH} or V_{IL} Vout=0 or V_{CC}		2.3 to 2.7	—	±5.0	μA
Quiescent supply current		I_{CC}	V_{IN}=V_{CC} or GND,		2.3 to 2.7	—	5.0	μA
Bushold input minimum drive hold current		I_{IHOLD}	V_{IN}=0.7V		2.3	45	—	μA
			V_{IN}=1.6V			−45	—	
Bushold input over-drive current to change state		I_{IOD}	(Note 12)		2.7	—	400	μA
			(Note 13)			—	−400	

Note 12: An external driver must source at least the specified current to switch from LOW-to-HIGH.
Note 13: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

DC Characteristics (Ta=-40 to 85℃, 1.65V≦Vcc＜2.3V)

Parameter		Symbol	Test Condition		Vcc(V)	Min	Max	Unit
DC input voltage	H-level	V_{IH}	—		1.65 to 2.3	0.7×Vcc	—	V
	L-level	V_{IL}	—		1.65 to 2.3	—	0.2×Vcc	
Output voltage (A bus)	H-level	V_{0HA}	V_{IN}= V_{IH}	I_{OHA}=−100uA	1.65	Vcc−0.2	—	V
				I_{OHA}=−2mA	1.65	1.3	—	
	L-level	V_{0LA}	V_{IN}= V_{IL}	I_{OLA}=2mA	1.65	—	0.2	
Output voltage (B bus)	H-level	V_{0HB}	V_{IN}= V_{IH}	I_{OHB}=−100uA	1.65	Vcc−0.2	—	V
				I_{OHB}=−4mA	1.65	1.3	—	
	L-level	V_{0LB}	V_{IN}= V_{IL}	I_{OLB}=4mA	1.65	—	0.2	
Input leakage current(DIR,/OE)		I_{IN}	V_{IN}=0 to 3.6V		1.65 to 2.3	—	±5.0	μA
Power off leakage current		I_{OFF}	A,DIR,/OE=0 to 3.6V		0	—	5.0	μA
3-state output off-state current		I_{OZA}	V_{INA}=V_{IH} or V_{IL} Vout=0 to 3.6V		1.65 to 2.3	—	±5.0	μA
		I_{OZB}	V_{INB}=V_{IH} or V_{IL} Vout=0 or V_{CC}		1.65 to 2.3	—	±5.0	μA
Quiescent supply current		I_{CC}	V_{IN}=V_{CC} or GND,		1.65 to 2.3	—	5.0	μA
Bushold input minimum drive hold current		$I_{I(HOLD)}$	V_{IN}=0.33V		1.65	20	—	μA
			V_{IN}=1.16V			−20	—	
Bushold input over-drive current to change state		$I_{I(OD)}$	(Note 14)		1.95	—	300	μA
			(Note 15)			—	−300	

Note 14: An external driver must source at least the specified current to switch from LOW-to-HIGH.
Note 15: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

AC Characteristics (Ta=-40 to 85℃,Input: tr=tf=2.0ns,CL=30pF ,RL=500Ω)

Parameter	Symbol	Test Condition	Vcc(V)	Min	Max	Unit
Propagation delay time	tpLH tpHL	Figure 1, Figure 2	1.8±0.15	1.0	10.0	ns
			2.5±0.2	0.8	4.6	
			3.3±0.3	0.6	3.0	
3-state output enable time	tpZL tpZH	Figure 1, Figure 3	1.8±0.15	1.0	15.0	ns
			2.5±0.2	0.8	7.8	
			3.3±0.3	0.6	5.6	
3-state output disable time	tpLZ tpHZ	Figure 1, Figure 3	1.8±0.15	1.0	6.5	ns
			2.5±0.2	0.8	4.3	
			3.3±0.3	0.6	3.9	
Output to output skew	tosLH tosHL	(Note 16)	1.8±0.15	−	0.5	ns
			2.5±0.2	−	0.5	
			3.3±0.3	−	0.5	

For C_L=50pF, add approximately 300ps to the AC maximum specification.

Note 16: Parameter guaranteed by design.

(tosLH = $|t_{pLHm} - t_{pLHn}|$, tosHL = $|t_{pHLm} - t_{pHLn}|$)

Capacitive Characteristics(Ta=25℃)

Characteristics	Symbol	Test Condition	Vcc(V)	Typ.	Unit
Input capacitance	C_{IN}		1.8,2.5,3.3	6	pF
Bus I/O capacitance	CI/O		1.8,2.5,3.3	7	pF
Power dissipation capacitance	CPDA	$\overline{OE}$= "L",finA=100MHz Table 1 (Note 17)	1.8,2.5,3.3	20	pF
		$\overline{OE}$= "H",finA=100MHz Table 1 (Note 17)		0	pF
Power dissipation capacitance	CPDB	$\overline{OE}$= "L",finB=100MHz Table 1 (Note 17)	1.8,2.5,3.3	16	pF
		$\overline{OE}$= "H",finB=100MHz Table 1 (Note 17)		1	pF

Note17: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot V_{IN} + I_{CC}/8$(per bit)

Table1 C_{PD} Test Condition

Function	Pin																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A bus /OE= "L"	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	C	L	V
A bus /OE= "H"	H	P	O	O	O	O	O	O	O	G	O	O	O	O	O	O	O	O	H	V
B bus /OE= "L"	L	C	O	O	O	O	O	O	O	G	X	X	X	X	X	X	X	P	L	V
B bus /OE= "H"	L	O	O	O	O	O	O	O	O	G	O	O	O	O	O	O	O	P	H	V

—Symbol explanation—

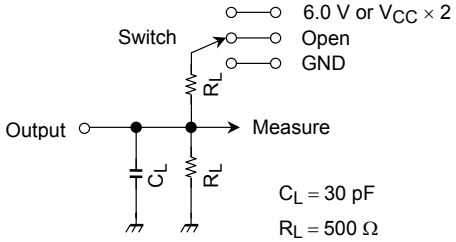
V=V_{CC}(+3.3V) X=Don't care(Fixed to V_{CC} or GND)

G=GND(0V) O=Open

H=Logic1(VCC) C=Connect a condenser(30pF) between output terminal and GND.

L=Logic0(GND) P=Input pulse with 50% duty cycle.

AC Test Circuit



Parameter	Switch	
t_{pLH}, t_{pHL}	Open	
t_{pLZ}, t_{pZL}	6.0 V V_{CC} × 2	@V_{CC} = 3.3 ± 0.3 V @V_{CC} = 2.5 ± 0.2 V @V_{CC} = 1.8 ± 0.15 V
t_{pHZ}, t_{pZH}	GND	

Figure 1

AC Waveform

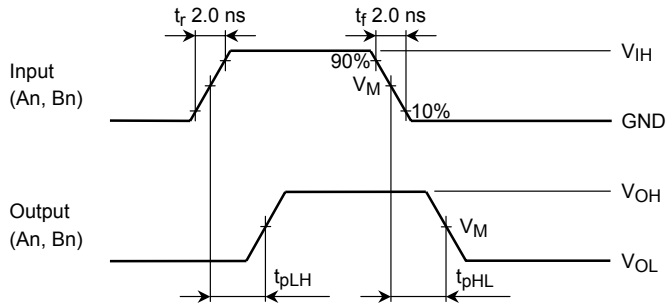


Figure 2 t_{pLH}, t_{pHL}

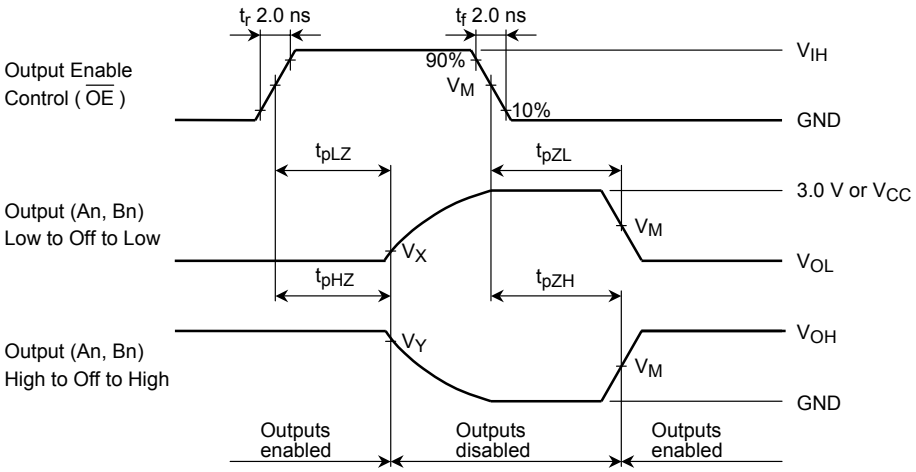
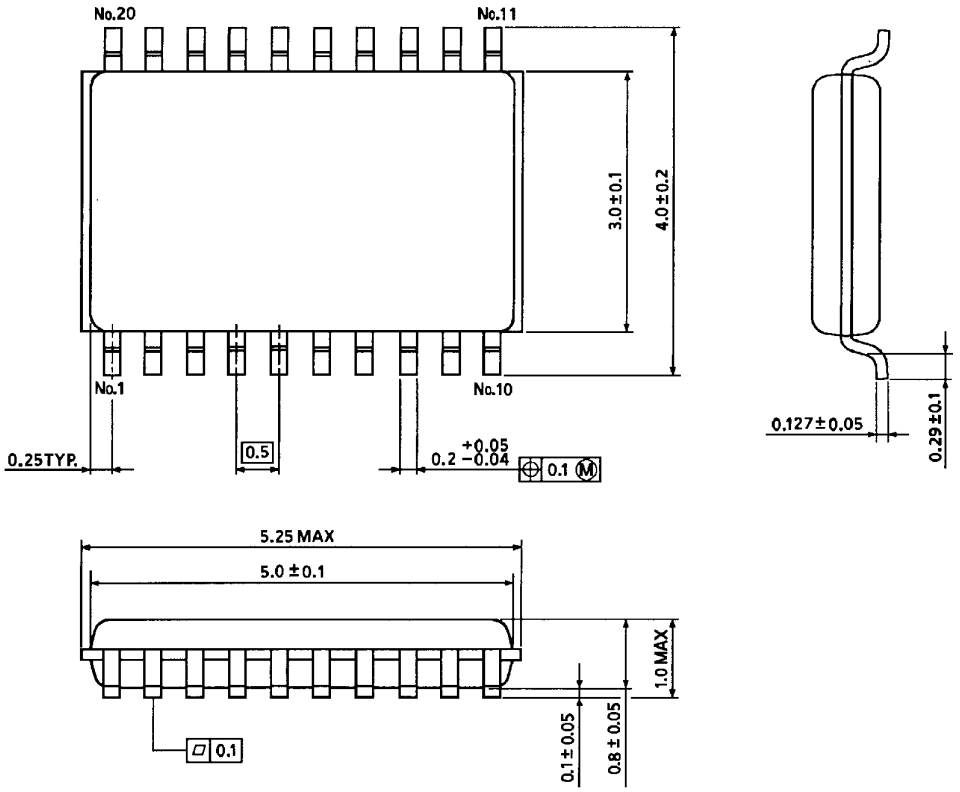


Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Symbol	V_{CC}		
	3.3±0.3 V	2.5±0.2 V	1.8±0.15 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} - 0.3 V	V_{OH} - 0.15 V	V_{OH} - 0.15 V

Package Dimensions

VSSOP20-P-0030-0.50 Unit : mm



Weight: 0.03 g (typ.)

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