M52036SP

SYNC SIGNAL PROCESSOR

REJ03F0086-0100Z
Rev.1.0
Sep.22.2003

Description

The M52036SP is a semiconductor integrated circuit for the automatic selection and rectification of sync waveforms. The IC operates with synchronizing signals in three forms, that is, separate sync(positive or negative polarity, 1 to 5 Vp-p), composite sync (positive or negative polarity, 1 to 5 Vp-p), and synchronous video (negative sync). This IC is optimal for processing sync signals for multi-scan-type displays.

Features

- Indicates the presence or absence of synchronizing-signal input and the polarities of the signals
- Pulse-output circuit is for open-collector output
- Clamp-pulse output and Clamp-pulse trigger is generated at the front edge for separate sync and composite sync input, and at the rear edge for sync on video input.
- 20-pin shrink-DIP

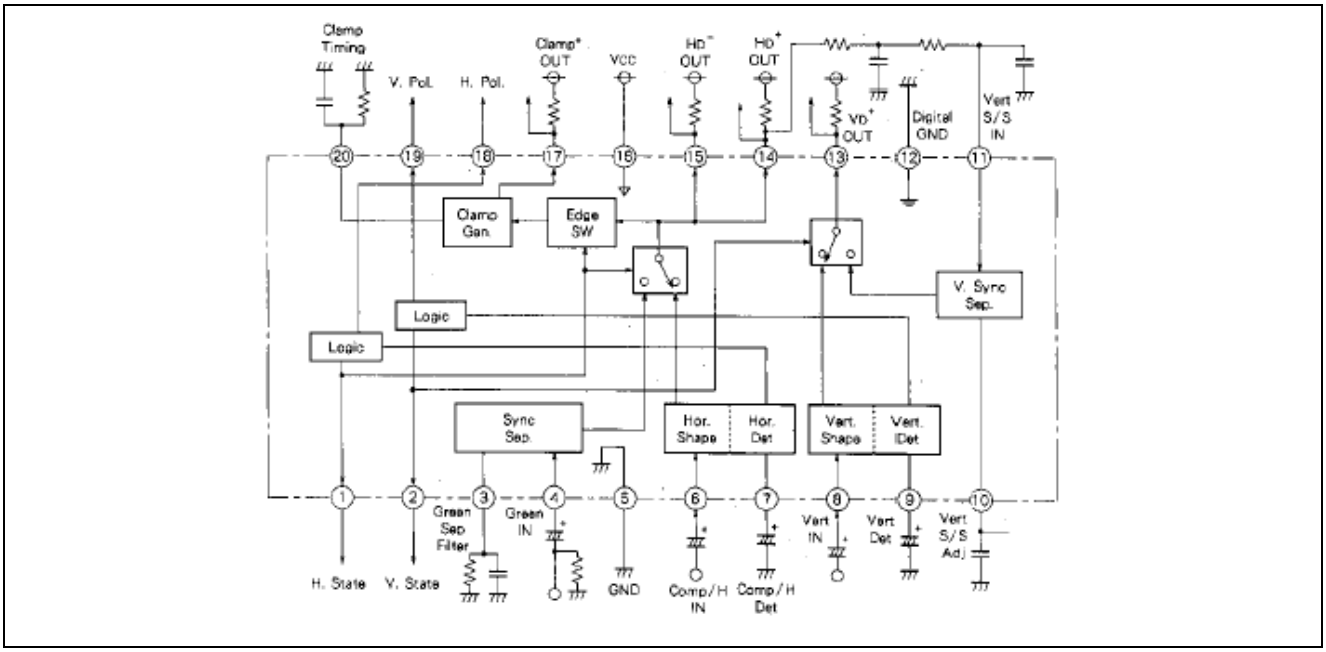
Application

- Display Monitor

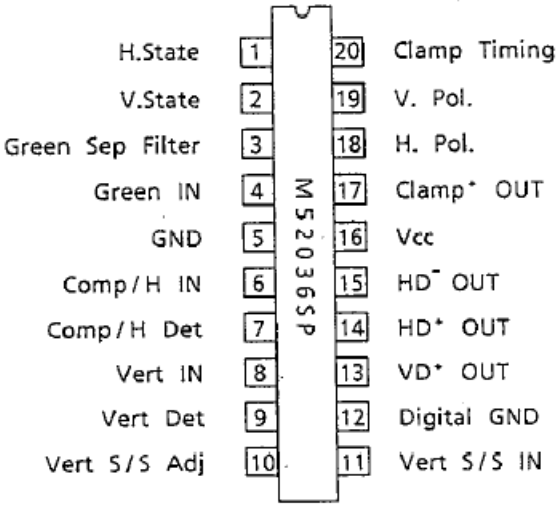
Recommended Operating Condition

- Supply voltage range: 11 to 13 V
- Rated supply voltage: 12 V

Block Diagram

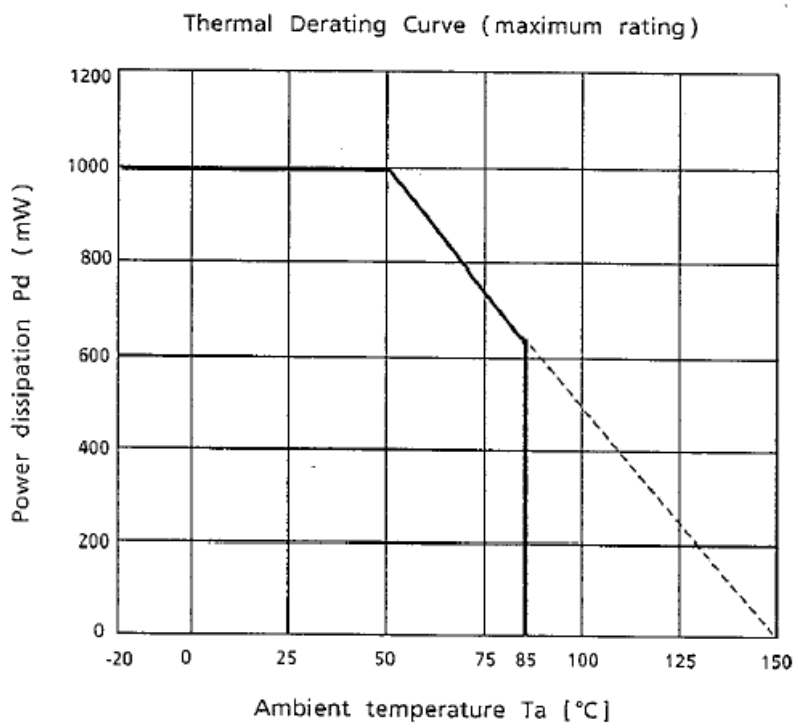


Pin Functions



Absolute Maximum Rating

Item	Symbol	Rated values	Units
Supply voltage	Vcc	14.0	V
Power dissipation	Pd	1000	mW
Operating ambient temperature	Topr	–20 to 85	°C
Storing temperature	Tstg	–40 to 150	°C



Electrical Characteristics

(Ta = 25°C Vcc = 12 V, V_{DD} = Open)

No.	Items	Symbols	Switch conditions 4	6	8	16	Input pins	Input conditions	Output pins	Output waveform	Rated values Min.	Typ.	Max.	Types of Unit	Remarks
			A			16			A		25	35	45	mA	Pins 4, 6, and 8 shall have no input signal. The input pin shall be connected to GND via a capacitor.
1	Circuit current	Icc	2	2	2	2									
2	Pin 1 output Hi level	1OH	2	1	1	1	6	7.5µs 16KHz 1Vp-p	1	DC	4.0	5.0	5.3	V	Refer to Attached Table 2 for truth table.
							8	7.5µs 16KHz 1Vp-p							
3	Pin 1 output Low level	1OL	2	1	1	1	6	7.5µs 16KHz 0.7Vp-p	1	DC	—	—	0.5	V	The input signal 0.7 Vp-p is equivalent to NO SYNC.
							8	7.5µs 16KHz 0.7Vp-p							
4	Pin 2 output Hi leve	2OH	2	1	1	1	6	7.5µs 16KHz 1Vp-p	2	DC	4.0	5.0	5.3	V	Refer to Attached Table 2 for truth table.
							8	7.5µs 16KHz 1Vp-p							
5	Pin 2 output Low level	2OL	2	1	1	1	6	7.5µs 16KHz 0.7Vp-p	2	DC	—	—	0.5	V	The input signal 0.7 Vp-p is equivalent to NO SYNC.
							8	7.5µs 15KHz 0.7Vp-p							
6	Pin 18 output Hi level	18OH	2	1	1	1	6	7.5µs 15KHz 1Vp-p	18	DC	4.0	5.0	5.3	V	Refer to Attached Table 2 for truth table.
							8	7.5µs 16KHz 1Vp-p							
7	Pin 18 output Low level	18OL	2	1	1	1	6	7.5µs 16KHz 1Vp-p	18	DC	—	—	0.5	V	Refer to Attached Table 2 for truth table.
							8	7.5µs 16KHz 1Vp-p							
8	Pin 19 output Hi level	19OH	2	1	1	1	6	7.5µs 16KHz 1Vp-p	19	DC	4.0	5.0	5.3	V	Refer to Attached Table 2 for truth table.
							8	7.5µs 16KHz 1Vp-p							
9	Pin 19 output Low level	19OL	2	1	1	1	6	7.5µs 16KHz 1Vp-p	19	DC	—	—	0.5	V	Refer to Attached Table 2 for truth table.
							8	7.5µs 16KHz 1Vp-p							
10	Threshold voltage	V10	2	2	2	1			10	DC	0.7	1.0	1.4	V	

Electrical Characteristics (cont.)

(Ta = 25°C Vcc = 12 V, V_{DD} = Open)

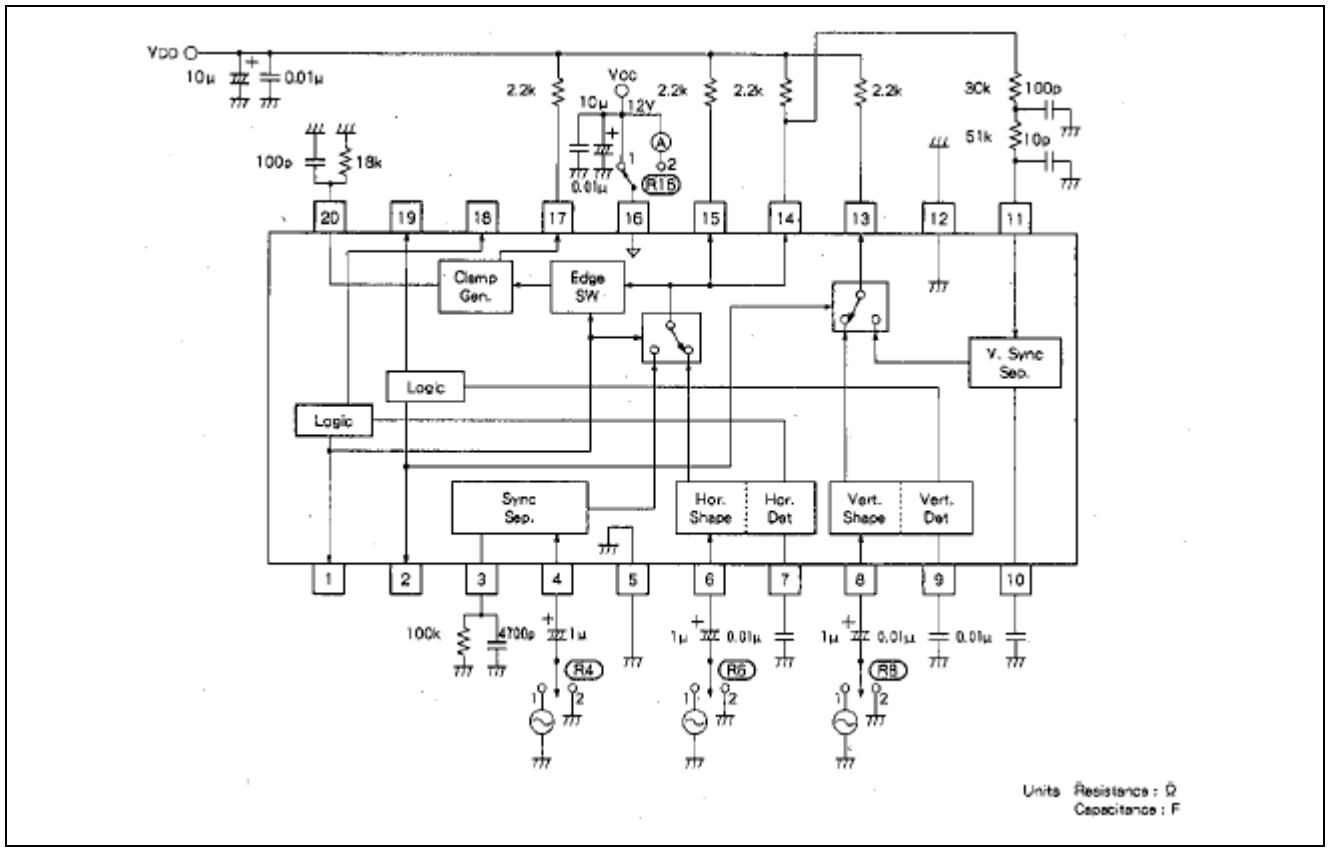
No.	Items	Symbols	Switch conditions 4	6	8	16	Input pins	Input conditions	Output pins	Output waveforms	Rated values Min.	Typ.	Max.	Types of Unit	Remarks
11	Maximum noise amplitude of voltage of input signal	SS-NV	1	2	2	1	4	1.5µs 16KHz 0.1Vp-p	14	No pulse should be output.	--	--	0.1	V	The input signal 0.1Vp-p is a dummy noise signal.
12	Minimum voltage amplitude of input signal	SS-LV	1	2	2	1	4	1.5µs 16KHz 0.2Vp-p	14	16KHz No pulse should be output in this duration.	0.2	--	--	V	If malfunction by noise occurs is checked.
13	15pin HD' Output Low level	15OL	1	1	2	1	4/6	7.5µs 16KHz 1Vp-p	15	..... V Meas	--	--	0.5	V	
14	14pin HD' Output Low level	14OL	1	1	2	1	4/6	7.5µs 16KHz 1Vp-p	14	..... V Meas	--	--	0.5	V	
15	17pin CP' Output Low level	17OL	1	1	2	1	4/6	7.5µs 16KHz 1Vp-p	17	..... V Meas	--	--	0.5	V	
16	13pin VD' Output Low level	13OL	2	2	1	1	8	7.5µs 16KHz 1Vp-p	13	..... V Meas	--	--	0.5	V	

Electrical Characteristics (cont.)

(Ta = 25°C Vcc = 12 V, V_{DD} = Open)

No.	Items	Symbols	Switch conditions 4	6	8	16	Input pins	Input conditions	Output pins	Output waveforms	Rated values Min.	Typ.	Max.	Types of Unit	Remarks
17	HD⁻—delay time (A)	HD⁻—DA	1	1	2	1	4 / 6	7.5µs 16KHz 1Vp-p	15	Input (50%) Output (50%) Time Meas	—	120	350	ns	
18	HD⁻—delay time (B)	HD⁻—DB	1	1	2	1	4 / 6	7.5µs 16KHz 1Vp-p	15	Input 50% Output (50%) Time Meas	—	150	350	ns	
19	HD⁺—delay time (A)	HD⁺—DA	1	1	2	1	4 / 6	7.5µs 16KHz 1Vp-p	14	Input (50%) Output (50%) Time Meas	—	120	350	ns	
20	HD⁺—delay time (B)	HD⁺—DB	1	1	2	1	4 / 6	7.5µs 16KHz 1Vp-p	14	Input (50%) Output (50%) Time Meas	—	100	350	ns	
21	CP⁺ — delay time	CP⁺—DT	1	1	2	1	4 / 6	7.5µs 16KHz 1Vp-p	17	Input (50%) Output (50%) Time Meas	—	120	350	ns	
22	CP⁺—PULSE—WIDTH	CP⁺—PW	1	1	2	1	4 / 6	7.5µs 16KHz 1Vp-p	17	Time Meas	450	700	950	ns	
23	VD⁺—delay time (A)	VD⁺—DA	2	2	1	1	8	7.5µs 16KHz 1Vp-p	13	Input (50%) Output (50%) Time Meas	—	120	350	ns	
24	VD⁺—delay time (B)	VD⁺—DB	2	2	1	1	8	7.5µs 16KHz 1Vp-p	13	Input (50%) Output (50%) Time Meas	—	100	350	ns	

Test Circuit



Logic Table

Table.1 Decoder Logic Output

Input to pin 6 HD.COMP	Input to pin 8 VD	Output pins			
		1	2	18	19
HD. COMP. (POS)	NON	H	L	L	L
HD. COMP. (POS)	VD (POS)	H	H	L	L
HD. COMP. (POS)	VD (NEG)	H	H	L	H
HD. COMP. (NEG)	NON	H	L	H	L
HD. COMP. (NEG)	VD (POS)	H	H	H	L
HD. COMP. (NEG)	VD (NEG)	H	H	H	H
NON	NON	L	L	L	L
NON	VD (POS)	L	H	L	L
NON	VD (NEG)	L	H	L	H

Table.2 Allowable Amplitude of Input Voltage

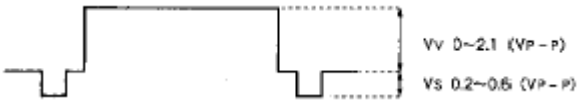
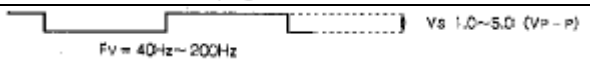
Amplitude of input to pin 4	
Amplitude of input to pin 6	
Amplitude of input to pin 8	

Table.3 Output Priority

Input signals (pin)			Output signals (pin)		
4 pin	6 pin	8 pin	14 pin 15 pin	13 pin	17 pin
O	×	×	4	11	4
O	O	×	6	11	6
O	×	O	4	8	4
O	O	O	6	8	6
×	×	×	×	×	×
×	O	×	6	11	6
×	×	O	×	8	×
×	O	O	6	8	6

Table.4 Pulse Duty Ratio for Allowable Maximum Input Signal

Input Pulse to Pin 6 (HD.COMP.)

F_H = 16 kHz

Maximum voltage amplitude (V_{P-P})		1.0	3.3	4.0	5.0
POS.	%	15.0	13.8	11.2	9.0
	Time (µs)	9.38	8.63	7.00	8.63
NEG.	%	15.0	13.0	10.5	8.8
	Time (µs)	9.38	8.13	6.56	5.50

Input Pulse to Pin 8 (VD)

Fv = 60 Hz

Maximum voltage amplitude (V_{P-P})		1.0	3.3	4.0	5.0
POS.	%	14.1	12.1	9.8	7.7
	Time (ms)	2.35	2.02	1.63	1.28
NEG.	%	14.8	11.3	9.2	7.5
	Time (ms)	2.47	1.88	1.53	1.25

Precautions for Application

1. Input

1) Green (Sync on Video) input (pins [3] and [4])
   The input signals must be in sync negative polarity.
   For sync separation, a method is used in which the sync tip is clamped by a capacitor attached externally to pin [4] and by the C and R attached to pin [3].
   Then sync tip of pin [4] shows approximately 4 V.

2) Comp Sync/H sync, V sync input

Connect the composite sync input to pin [6]. For the separate sync input, connect H and V to pins[6] and [8] respectively. The bias and impedance at pins [6] and [8] are 6 V and 10 kΩ, respectively.

Waveform shaping and polarity detection are performed by a double threshold converter installed inside.

The internal circuit is as shown in Fig.B. The average DC voltage is set to approximately 0.7 V higher and lower than V_2.

Thus, as shown in Fig. A, this processor is energized by an input signal 0.7 Vp-p or over when the duty ratio is small. On the other hand, approximately 1.4 Vp-p is suitable when the duty ratio is large. Fig. C indicates an allowable standard value for the input duty.

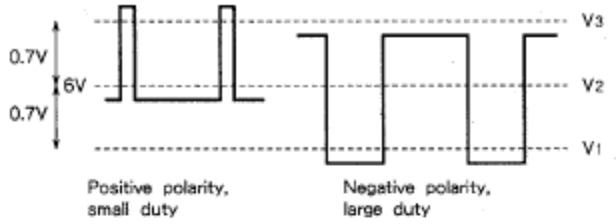


Fig. A

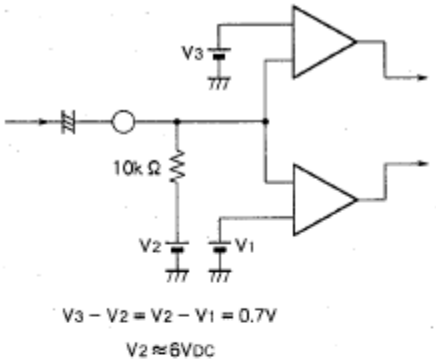


Fig. B

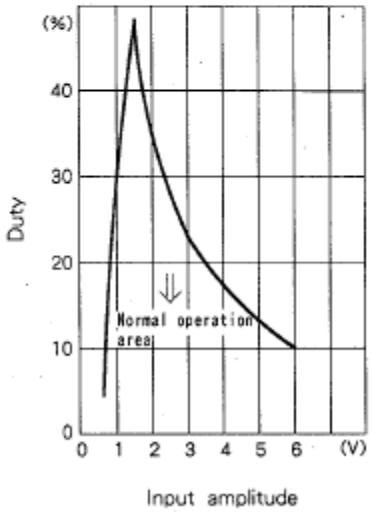


Fig. C

Fig. D shows an example of the measures for improving the allowable duty ratio in a range of 1.4 Vp-p or over of the input signal.

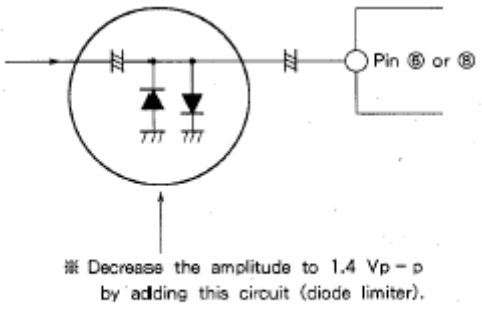


Fig. D

For use in a range outside the specified value, confirm that the waveform complies with Fig. E when measured it after removing the filters in pins [7] and [9].

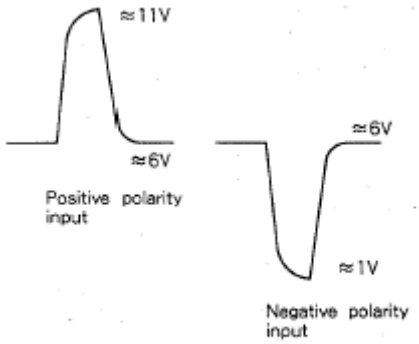


Fig. E

3) Polarity detection and empty input detection (pins [7] and [9])
A capacitor is required to be installed external as a filter for polarity detection and empty input detection. The large the capacitance, the smaller the ripple and reduces malfunction. However, the detecting time is lengthened.
For an input of 15 kHz, a capacitor of 0.05 µF or larger is recommended. For 60 Hz, a 10 µF or larger is sufficient. If it is necessary to use a capacitor of smaller capacitance, measure the waveform at the filter terminal under the condition of the lowest frequency of the input sync signal to be used and the smallest duty ratio. And make sure that the signal shows 7.5 V (actually 6.6 V) or over for positive polarity input or 4.5 V (actually 5.5 V) or lower for a negative polarity input.

4) VERT S/S IN (pins [11])
For V sync separation, signals are generated by externally integrating composite sync signals, and are then input.
The composite sync signals that are input to pin [6] (H + V) ore output to pin [14] HD^+. For V sync separation, pin [14] HD^+ output is externally integrated, and input to pin [11]. Check pin [11] waveform to see if the H element is adequately low.
In the IC, the sync separation threshold level is set to approximately 1 V when no external adjustment is provided.

5) VERT S/S ADJ (pins [10])

The threshold voltage is approximately 1 V when no external adjustment is provided. The threshold voltage is dependent on IC internal resistance. Pin [10] may be open; however, if noise may give adverse effect, ground the pin with capacitor.

When the H element cannot be lowered sufficiently, connect resistance between pin [10] and Vcc to change the threshold level. (Provide resistance such that when V_{DD} (Digital Vcc) is 12 V, the threshold voltage will be 8 V or less; and when V_{DD} 1s 5 V, the threshold voltage will be 4 V or less.)

When there are serration pulses or other pulses during the V period, provide resistance such that the threshold voltage will be half as high as V_{DD}.

2. CP-Width

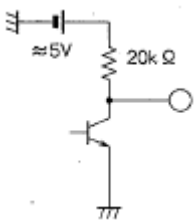
Timing terminal (pins [20])

The time constant depends on the current flowing out through pin [20] and the capacitance of the timing terminal. The current flowing out through pin [20] is usually determined by the terminal voltage and the resistance of externally attached resistor. A pulse width of 0.7 µ sec is obtained by an 18 kΩ (or 200 µA) resistor and a 100 pF capacitor both installed externally.

3. Output stage

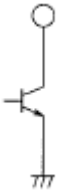
1) Logic output (pins [1], [2], [18] and [19])

This output system is illustrated in the figure shown below. The internal load resistance of this IC is 20 kΩ.



2) Pulse output (pins [13], [14], [15] and [17])

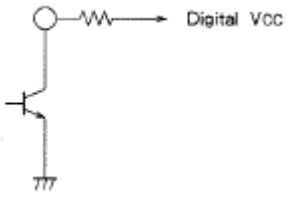
This output system is of open collector type as illustrated in the figure shown below. Approximately 6 mA can be charged in.



3) Power supply

Supply 12 V to pin [16].

For the pulse output power, supply a digital Vcc of 5 to 12 V as illustrated below.



4. Other

Differences between M52036SP and M52346SP

The clamp pulse trigger is different between M52036SP and M52346SP when “S on G” and “H/H + V” are input simultaneously, or when only “H/H + V” is input.

M52036SP: Generated at the first edge of “H/H + V” input.

M52346SP: Generated at the latter edge of “H/H + V” input.

M52346SP clamp pulses are generated at the latter edge of signals that have been given priority.

The M52036SP pin configuration is the same as that of M52346SP.

Package Dimensions

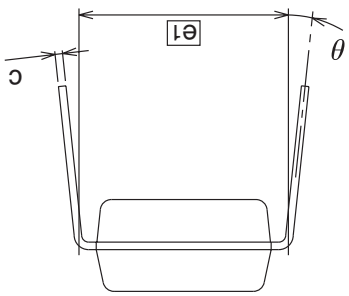
Plastic 20pin 300mil SDIP

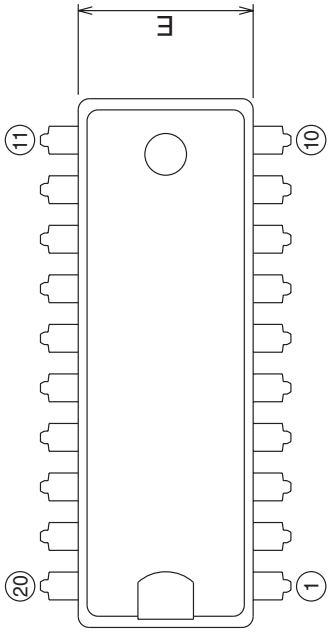
20P4B

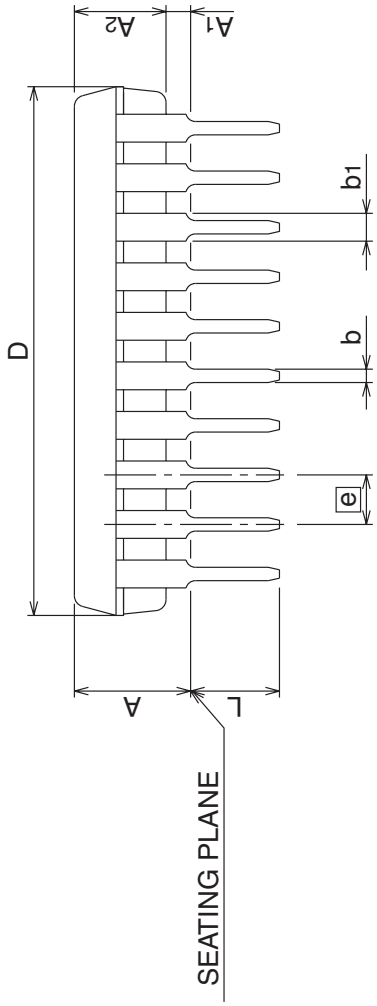
MMP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP20-P-300-1.78	—	1.0	Alloy 42/Cu Alloy

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.38	0.48	0.58
b_1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	—	1.778	—
e1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°







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