2A Bus Termination Regulator

General Description

The RT9173B regulator is designed to convert voltage supplies ranging from 1.7V to 6V into a desired output voltage of which adjusted by two external voltage divider resistors. The regulator is capable of sourcing or sinking up to 2A of current while regulating an output voltage to within 40mV.

The RT9173B, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs. The voltage output of the regulator can be used as a termination voltage for DDR SDRAM.

Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of the output fault conditions.

The RT9173B are available in the popular 5-lead TO-252 and fused SOP-8 (the multiple V_{CNTL} pins on the SOP-8 package are internally connected but lowest thermal resistance) surface mount packages.

Ordering Information

RT9173B □□

- Package Type
  - S : SOP-8
  - L5 : TO-252-5
- Operating Temperature Range
  - P : Pb Free with Commercial Standard
  - G : Green (Halogen Free with Commercial Standard)

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100%matte tin (Sn) plating.

Features

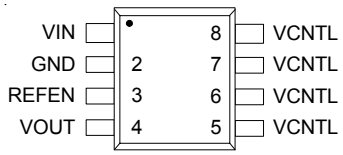
- **Support Both DDR I ($1.25V_{TT}$) and DDR II ($0.9V_{TT}$) Requirements**
- **SOP-8 and TO-252-5 Packages**
- **Capable of Sourcing and Sinking Current**
- **Current-limiting Protection**
- **Thermal Protection**
- **Integrated Power MOSFETs**
- **Generates Termination Voltages for SSTL-2**
- **High Accuracy Output Voltage at Full-Load**
- **Adjustable V_{OUT} by External Resistors**
- **Minimum External Components**
- **Shutdown for Standby or Suspend Mode Operation with High-impedance Output**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

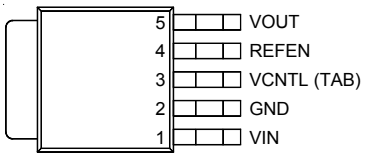
- DDR Memory Termination Supply
- Active Termination Buses
- Desktop PC/AGP Graphics
- Set Top Box/IPC
- Supply Splitter

Pin Configurations

(TOP VIEW)

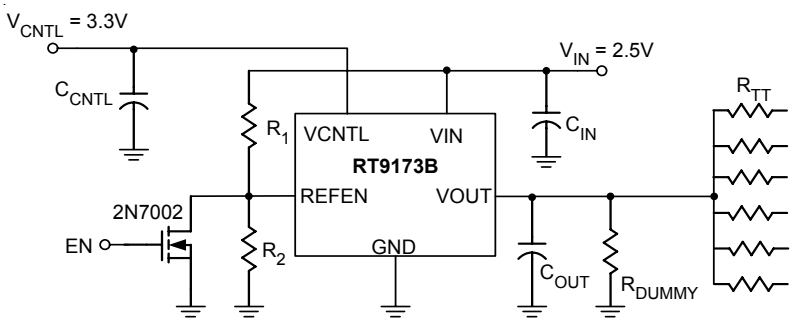


SOP-8



TO-252-5

Typical Application Circuit



$R_1 = R_2 = 100k\Omega$, $R_{TT} = 50\Omega / 33\Omega / 25\Omega$

$C_{OUT(MIN)} = 10\mu F$ (Ceramic) + $1000\mu F$ under the worst case testing condition

$R_{DUMMY} = 1k\Omega$ as for VOUT discharge when VIN is not present but VCNTL is present

$C_{IN} = 470\mu F$ (Low ESR), $C_{CNTL} = 47\mu F$

Test Circuit

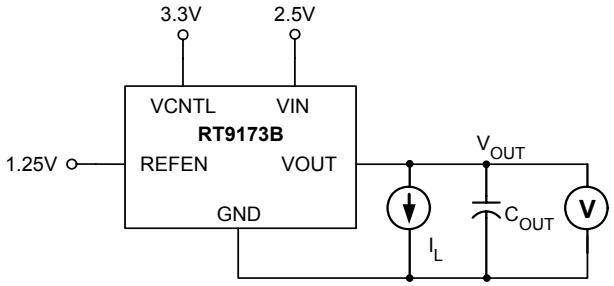


Figure 1. Output Voltage Tolerance, ΔV_{OUT}

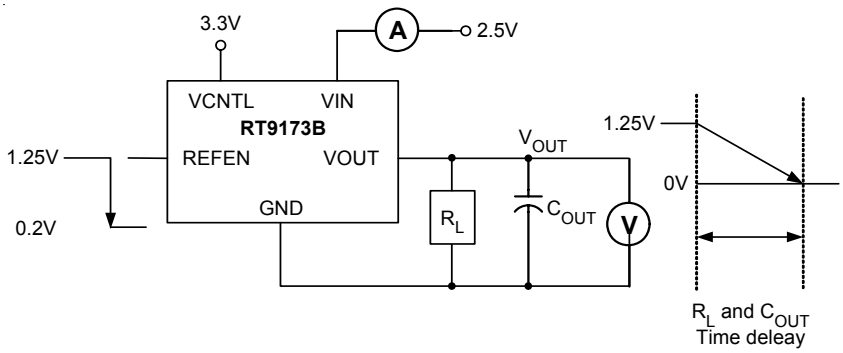


Figure 2. Current in Shutdown Mode, I_{SHDN}

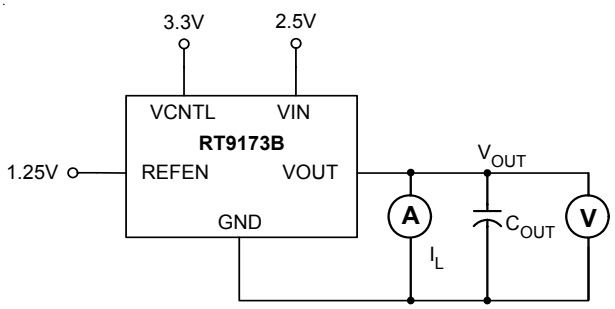


Figure 3. Current Limit for High Side, I_{CLHIGH}

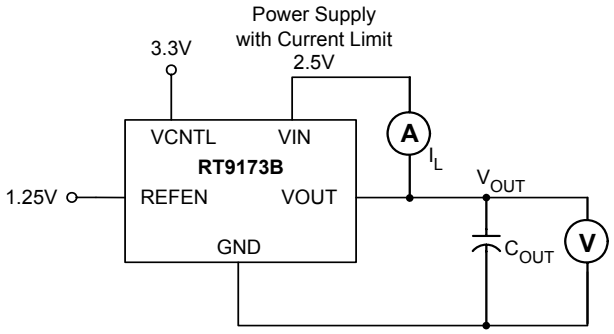


Figure 4. Current Limit for Low Side, I_{CLLOW}

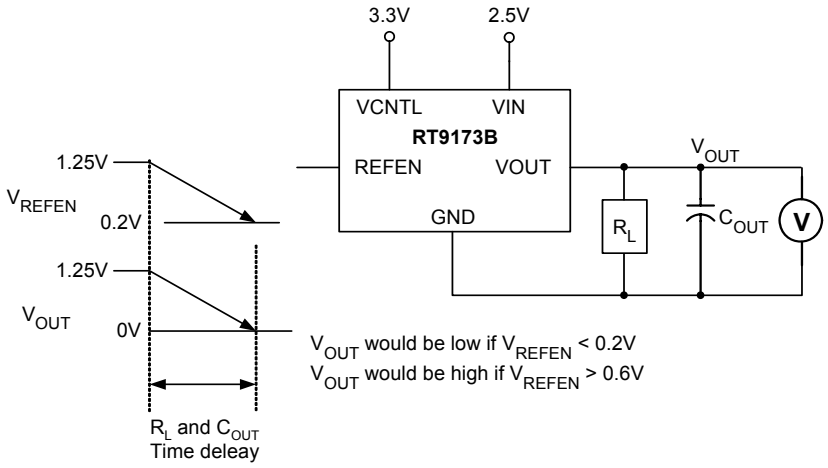
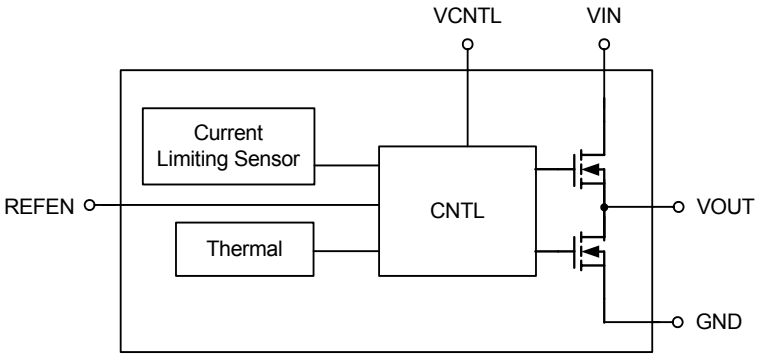


Figure 5. REFEN Pin Shutdown Threshold, $V_{TRIGGER}$

Functional Pin Description

Pin Name	Pin Function
VIN	Power Input
GND	Ground
VCNTL	Gate Drive Voltage
REFEN	Reference Voltage Input and Chip Enable
VOUT	Output Voltage

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Input Voltage ---------- 7V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 ---------- 0.625W
  - TO-252 ---------- 1.471W
- Package Thermal Resistance (Note 5)
  - SOP-8, θ_{JA} ---------- 160°C/W
  - SOP-8, θ_{JC} ---------- 23°C/W
  - TO-252, θ_{JA} ---------- 68°C/W
  - TO-252, θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 2.5V, V_{CNTL} = 3.3V, V_{REFEN} = 1.25V, C_{OUT} = 10µF (Ceramic), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Offset Voltage	V_{OS}	I_{OUT} = 0A, Figure 1 (Note 4)	–20	0	20	mV
Load Regulation	ΔV_{LOAD}	I_L : 0A → 2A, Figure 1	–20	0	20	mV
		I_L : 0A → -2A				
Input Voltage Range (DDR I/II)	V_{IN}	Keep $V_{CNTL} \geq V_{IN}$ on operation power on and power off sequences	1.7	2.5/1.8	--	V
	V_{CNTL}		3	3.3/5	6	
Operating Current of VCNTL	I_{CNTL}	No Load	--	1	2.5	mA
Current In Shutdown Mode	I_{SHDN}	$V_{REFEN} < 0.2V$, R_L = 180Ω, Figure 2	--	50	90	µA
Short Circuit Protection						
Current limit	I_{LIM}	Figure 3,4	2.2	2.6	--	A
Over Temperature Protection						
Thermal Shutdown Temperature	T_{SD}	$3.3V \leq V_{CNTL} \leq 5V$	125	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}	$3.3V \leq V_{CNTL} \leq 5V$	--	35	--	°C
Shutdown Function						
Shutdown Threshold Trigger		Output = High, Figure 5	0.6	--	--	V
		Output = Low, Figure 5	--	--	0.2	

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

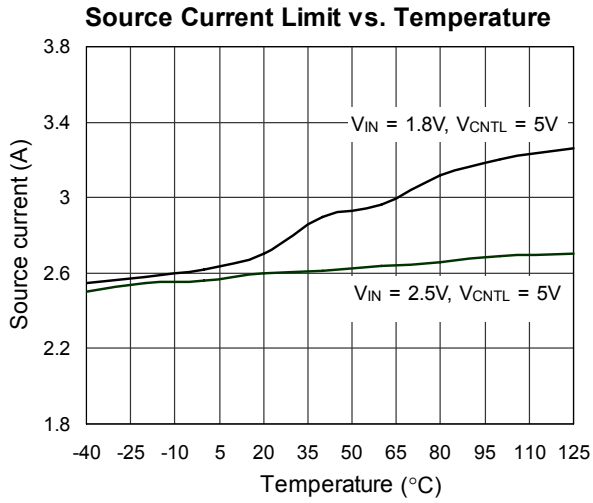
Note 2. Devices are ESD sensitive. Handling precaution recommended. The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

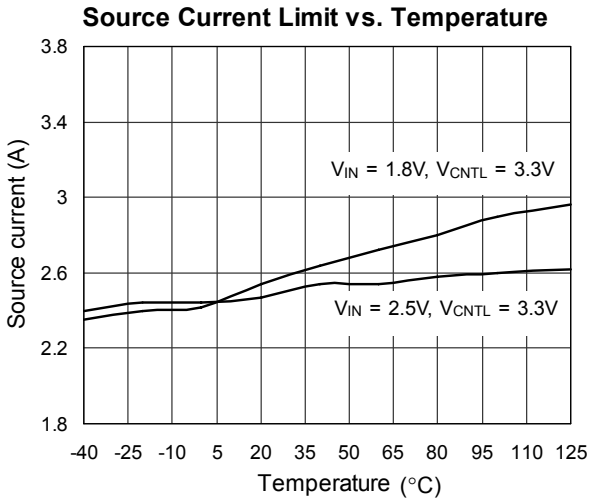
Note 3. The device is not guaranteed to function outside its operating conditions.

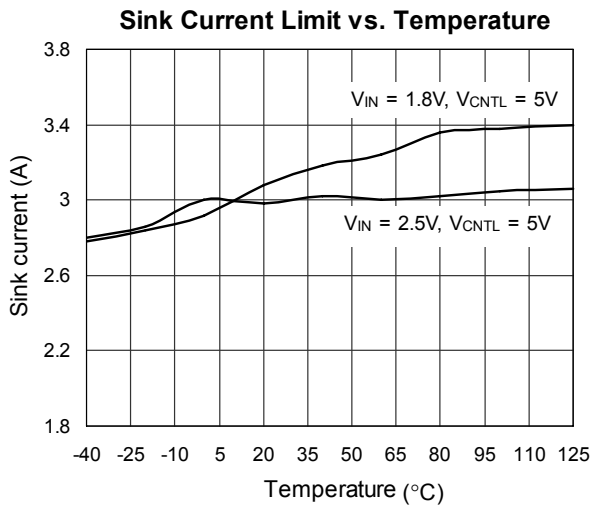
Note 4. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

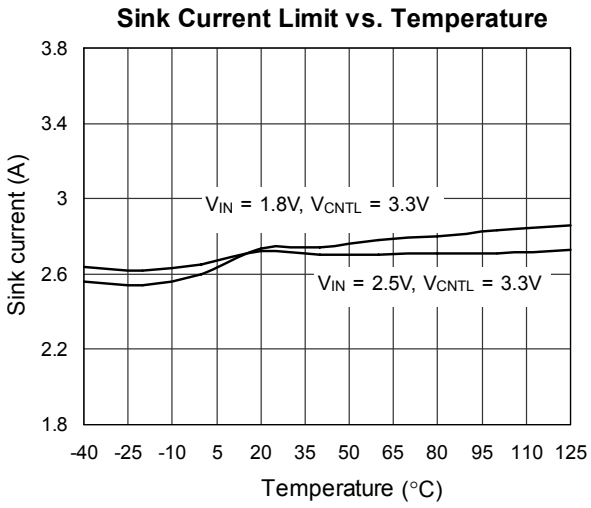
Note 5. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard. The case point of θ_{JC} is on the center of V_{CTRL} pins (Lead 6 & 7) for SOP-8 packages.

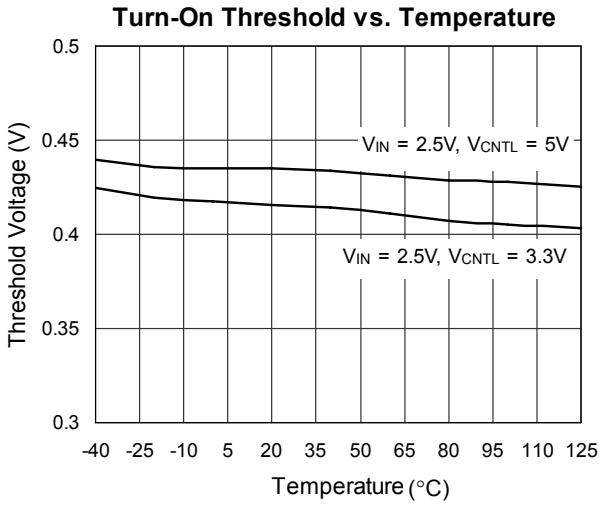
Typical Operating Characteristics

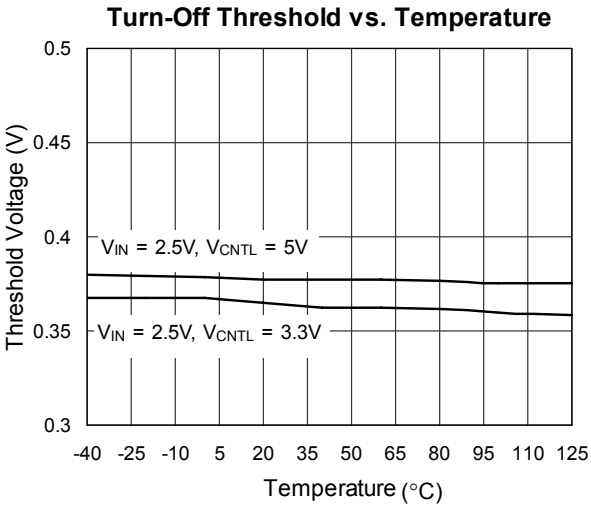


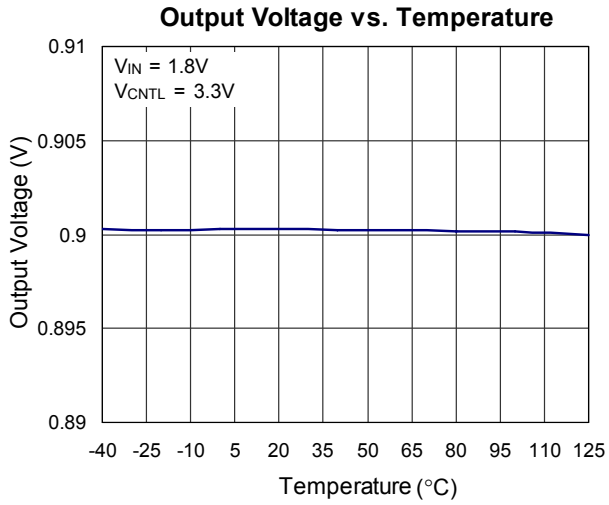


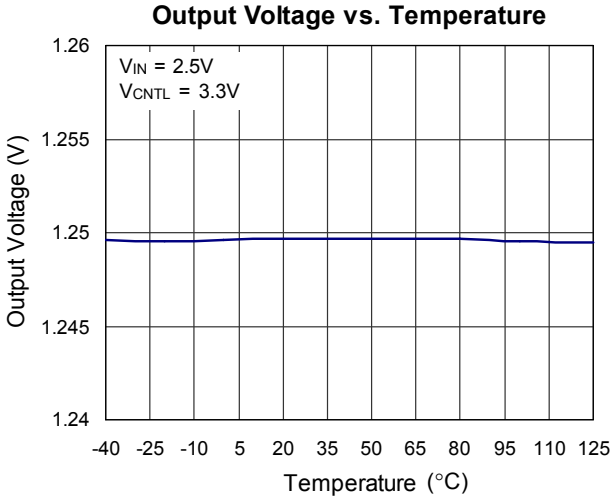


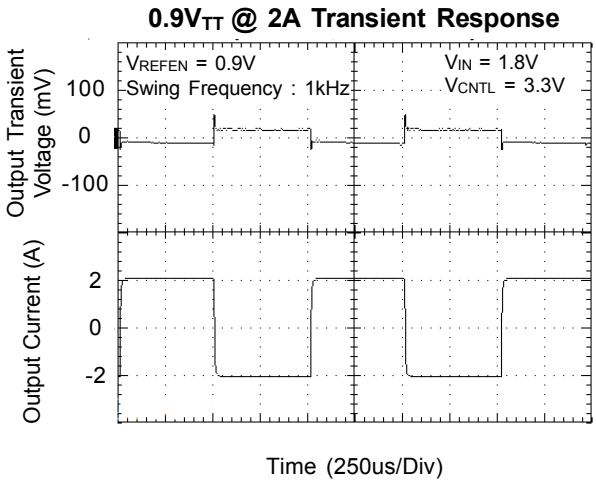


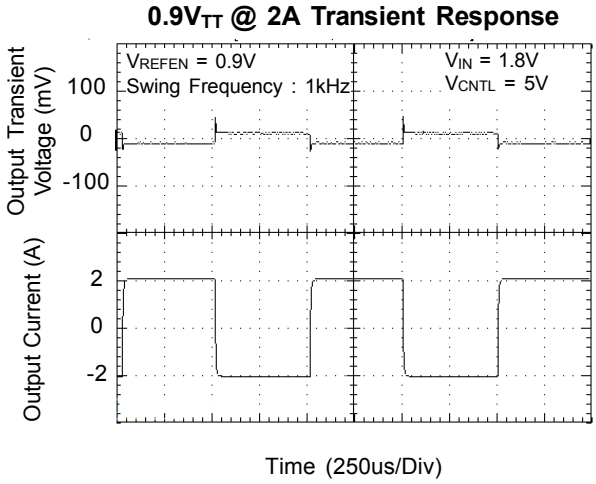


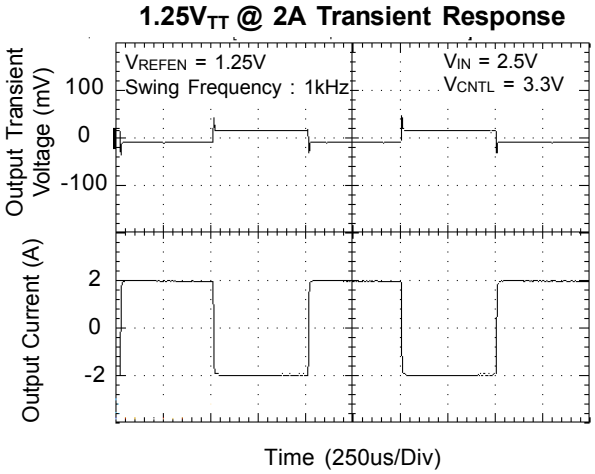


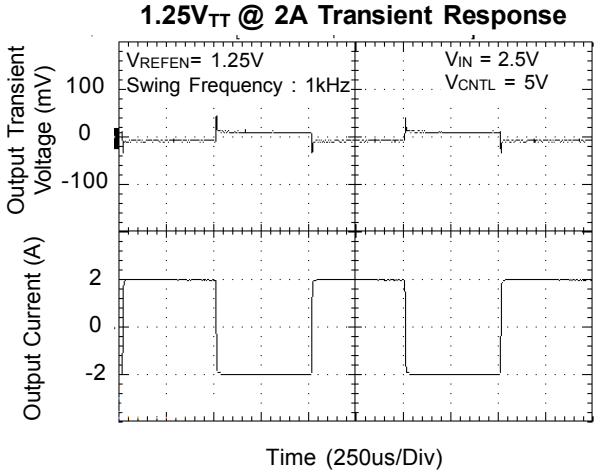




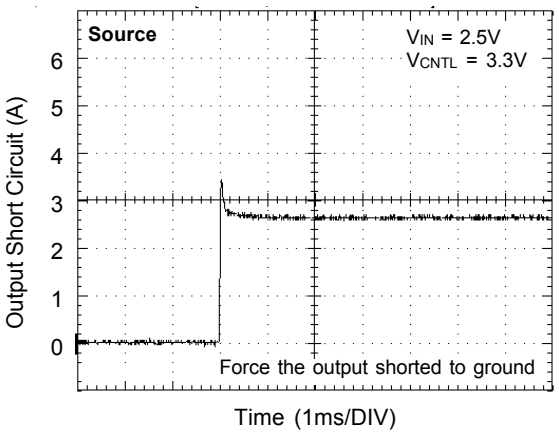




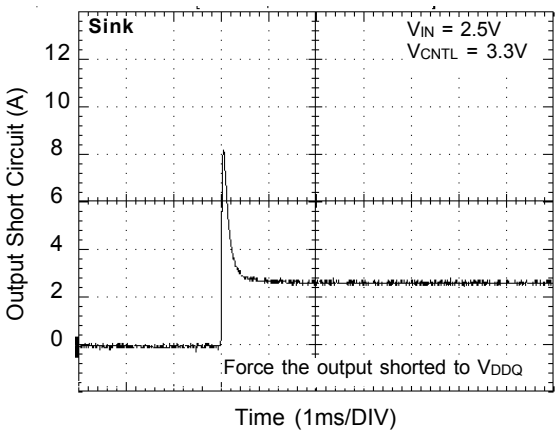




Output Short-Circuit Protection



Output Short-Circuit Protection



Application Information

Internal parasitic diode

Avoid forward-bias internal parasitic diode, V_{OUT} to V_{CNTL}, and V_{OUT} to V_{IN}, the V_{OUT} should not be forced some voltage respect to ground on this pin while the V_{CNTL} or V_{IN} is disappeared.

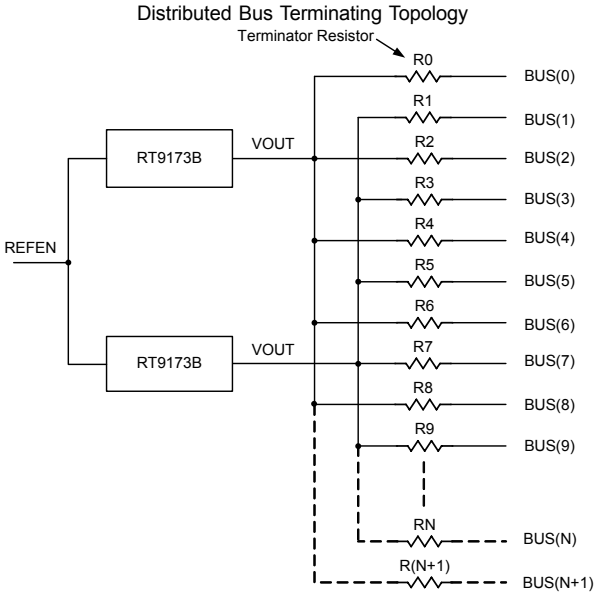
Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V.

In addition, the capacitor and voltage divider form the low-pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.

How to reduce power dissipation on Notebook PC or the dual channel DDR SDRAM application?

In notebook application, using RichTek's Patent "Distributed Bus Terminator Topology" with choosing RichTek's product is encouraged.



General Regulator

The RT9173B could also serves as a general linear regulator. The RT9173B accepts an external reference voltage at REFEN pin and provides output voltage regulated to this reference voltage as shown in Figure 6, where

$V_{OUT} = V_{REF} \times R1/(R1+R2)$

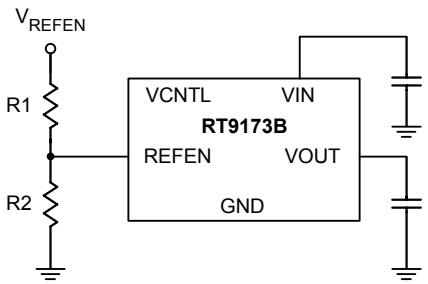
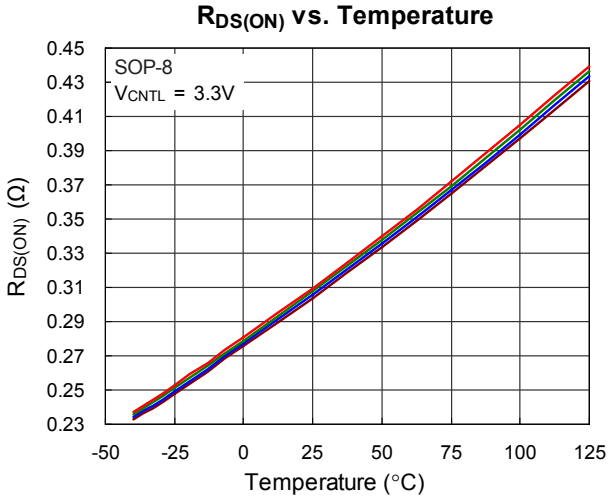
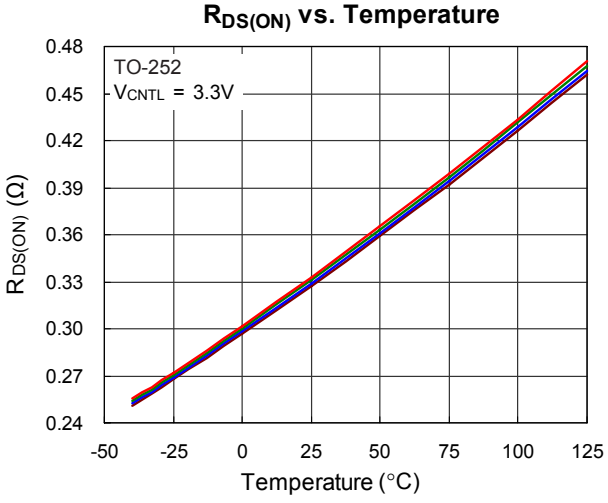


Figure 6

Make sure that V_{CNTL} >= V_{IN} in all conditions including power on and off. As other linear regulator, dropout voltage and thermal issue should be specially considered. Figure 6 and 7 show the $R_{DS(ON)}$ over temperature of RT9173B in SOP-8 and TO-252 packages respectively. The minimum dropout voltage could be obtained by the product of $R_{DS(ON)}$ and output current. For thermal consideration, please refer to the relative sections.





Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the RT9173B. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between RT9173B and the preceding power converter.

Thermal Consideration

An internal thermal limiting circuitry shuts down the RT9173B when junction temperature is over 170°C. This protects the device during overload conditions. It is noted that the thermal limiting circuitry is not intended for normal operation. For maximum reliability, the junction temperature should not exceed absolute maximum operation temperature 125°C during normal operation. The power dissipation should be well considered to keep the junction temperature within the specification.

The power dissipation in RT9173B is calculated as:

$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation can be calculated by following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

The junction to ambient thermal resistance θ_{JA} highly depends on IC package, PCB layout , the rate of surroundings airflow. θ_{JA} for SOP-8 package is 160°C/W and TO-252 package is 68°C/W on standard JEDEC 51-3 (single layer, 1S) thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$P_{D(MAX)} = (125 – 25°C) / 160 = 0.625W$ (SOP-8)

$P_{D(MAX)} = (125 – 25°C) / 68 = 1.471W$ (TO-252)

Since the multiple VCTRL pins of the SOP-8 package are internally shorted and connected to lead frame, it is efficient to dissipate the heat by adding cooper area on VCTRL footprint. Figure 7 shows the relation about thermal resistance θ_{JA} vs. copper area on a standard JEDEC 51-7 (**4 layer**, 2S2P) thermal test board at T_A = 25°C. The corresponding maximum power dissipation is shown in Figure 8. For example, with 10mm x 10mm cooper area, we can obtain the lower thermal resistance about 45°C/W. The power maximum dissipation can be calculated as:

$P_{D(MAX)} = (125 – 25°C) / 45 = 2.22W$ (SOP-8)

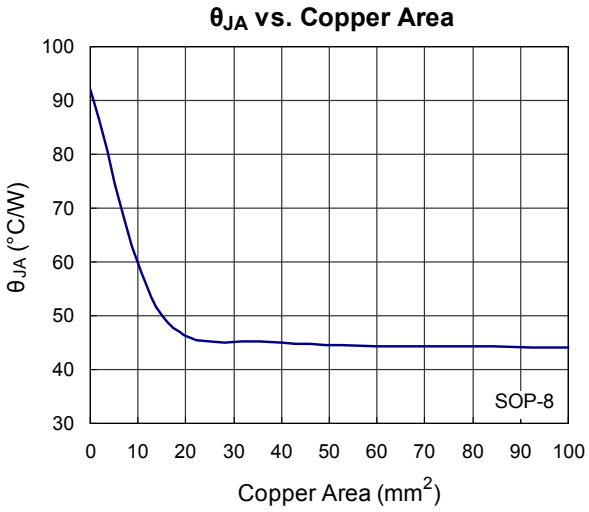


Figure 7

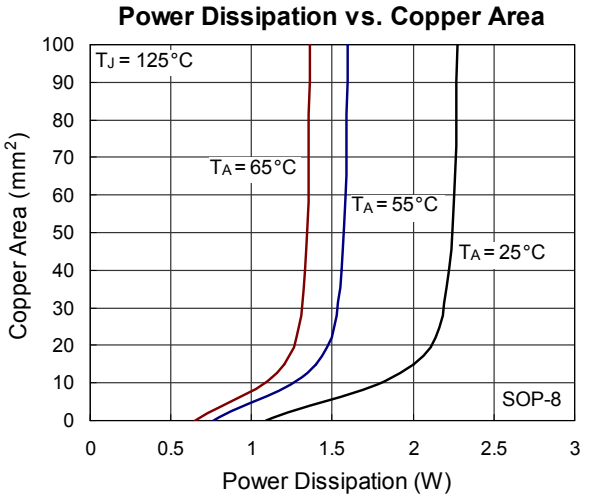
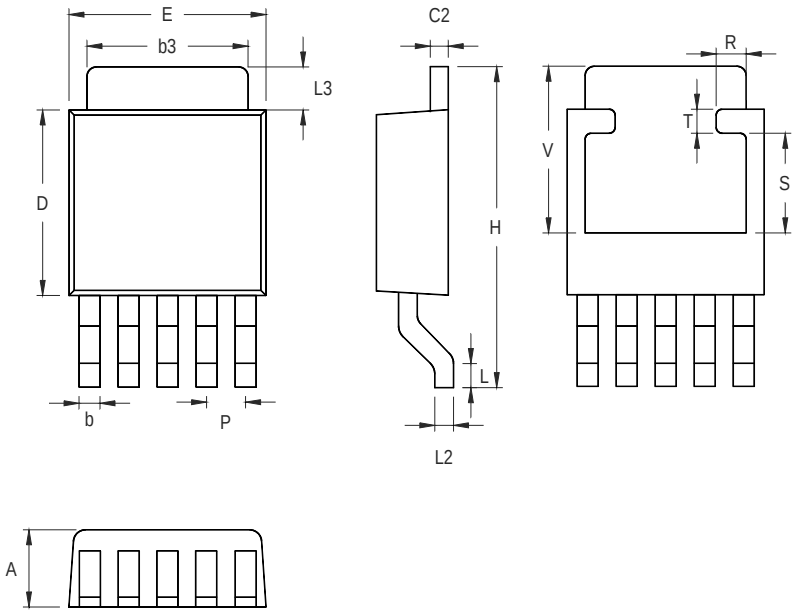


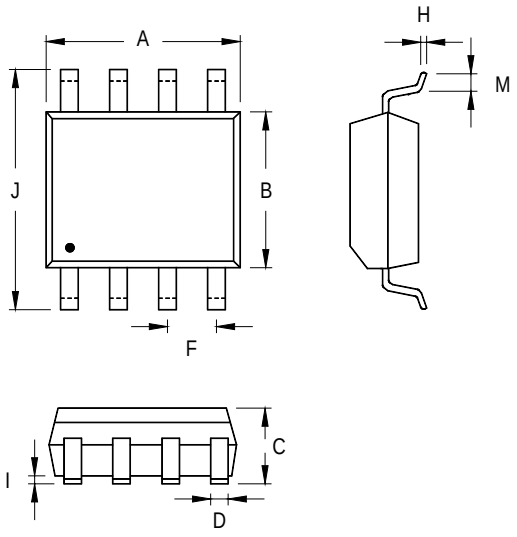
Figure 8

Outline Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.184	2.388	0.086	0.094
b	0.381	0.889	0.015	0.035
b3	4.953	5.461	0.195	0.215
C2	0.457	0.889	0.018	0.035
D	5.334	6.223	0.210	0.245
E	6.350	6.731	0.250	0.265
H	9.000	10.414	0.354	0.410
L	0.508	1.780	0.020	0.070
L2	0.508 Ref.		0.020 Ref.	
L3	0.889	2.032	0.035	0.080
P	1.270 Ref.		0.050 Ref.	
V	5.200 Ref.		0.205 Ref.	
R	0.200	1.500	0.008	0.059
S	2.500	3.400	0.098	0.134
T	0.500	0.850	0.020	0.033

5-Lead TO-252 Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
8F, No. 137, Lane 235, Paochiao Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)89191466 Fax: (8862)89191465
Email: marketing@richtek.com