Target Specification

VSC8115

STS-12/STS-3 Multi Rate
Clock and Data Recovery Unit

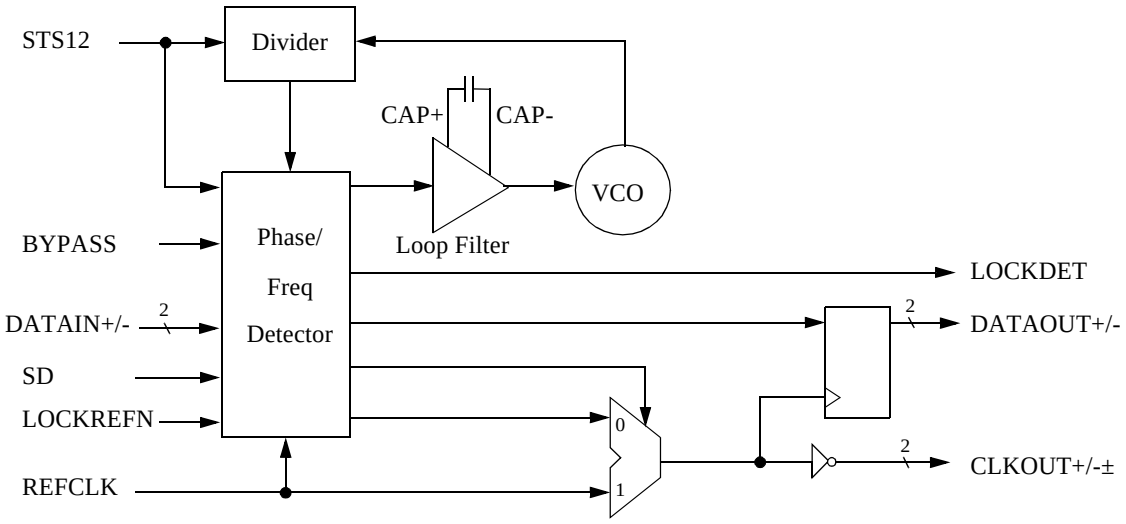
Features

- Performs clock and data recovery for 622.08Mb/s (STS-12/OC-12/STM-4) or 155.52Mb/s (STS-3/OC-3/STM-1) NRZ data
- Meets Bellcore, ITU and ANSI Specifications for Jitter Performance
- 19.44MHz reference frequency LVTTL Input
- Lock Detect output pin monitors data run length and frequency drift from the reference clock
- Data is Retimed at the Output
- Active High Signal Detect LVPECL Input
- Low-jitter high speed outputs can be configured as either LVPECL or low power LVDS
- Low power - 0.188 Watts Typical Power
- +3.3V Power Supply
- 20 Pin TSSOP Package
- Requires One External Capacitor
- PLL bypass operation facilitates the board debug process

General Description

The VSC8115 functions as a clock and data recovery unit for SONET/SDH-based equipment to derive high speed timing signals. The VSC8115 recovers the clock from the scrambled NRZ data operating at 622.08Mb/s (STS-12/OC-12/STM-4) or 155.52Mb/s (STS-3/OC-3/STM-1). After the clock is recovered, the data is retimed using an output flip-flop. Both recovered clock and retimed data outputs can be configured as LVDS or LVPECL signals to facilitate a low-jitter and low power interface.

VSC8115 Block Diagram



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Functional Description

The VSC8115 contains an on-chip PLL consisting of a phase/frequency detector, a loop filter using one external capacitor, a LC-based voltage-controlled oscillator (VCO), and a programmable frequency divider. The phase/frequency detector compares the phase relationship between the VCO output and an external 19.44MHz LVTTL reference clock to make coarse adjustment to the VCO block so that its output is held within ±500ppm of the reference clock. The use of reference clock minimizes the PLL lock time during power up and provides a stable output clock source in the absence of serial input data. The phase/frequency detector also compares the phase relationship between the VCO output and the serial data input to make fine adjustment to the VCO block. The loop filter converts the phase detector output into a smooth DC voltage. This DC voltage is used as the input to the VCO block whose output frequency is a function of the input voltage. A programmable frequency divider down converts the VCO output signal and provides two modes of operation: 622.08Mb/s mode if STS12 is HIGH, or 155.52Mb/s mode if STS12 is LOW.

Lock Detection

The VSC8115 features a lock detection for the PLL. The lock detect (LOCKDET) output goes HIGH to indicate that the PLL is locked to the serial data inputs and that valid data and clock are present at the high speed differential outputs. If LOCKDET output is LOW, then either the PLL is forced to lock to the REFCLK input or the VCO has drifted away from the local reference clock by more than 500 ppm.

Signal Detection

The VSC8115 has a signal detect (SD) input and a lock-to-reference (LOCKREFN) input. The SD pin is a LVPECL input, and the LOCKREFN pin is a LVTTL input. These two control pins are used to indicate a loss of signal condition and they are connected inside the part as shown in Figure 1. If either one of these two inputs goes LOW and BYPASS is LOW, the VSC8115 will enter the loss of signal (LOS) state, and it will hold the DATAOUT+/- output at logic LOW state. During the LOS state, the VSC8115 also will hold the output clock CLKOUT+/- to within ±500ppm of the REFCLK. See Table 1.

Most of the optical module has a signal detect output. This signal detect output indicates that there is sufficient optical power, and it is typically active HIGH. If the signal detect output on the optical module is LVPECL, it should be connected directly to the SD input on the VSC8115, and the LOCKREFN input needs to be tied HIGH. If the signal detect output is LVTTL, it should be connected directly to the LOCKREFN input, and the SD input needs to be tied HIGH.

The SD and LOCKREFN inputs also can be used for other applications when the users need to hold the CLKOUT+/- output to within ±500ppm of the reference clock and to force the DATAOUT+/- output to the logic LOW state.

PLL Bypass Operation

The BYPASS pin is intended for use in production test, and it should be set at logic LOW in the normal operation. If both BYPASS and MODE pins are set at logic HIGH, the VSC8115 will bypass the PLL and will present an inverted version of the REFCLK to the clock output CLKOUT+/-. The REFCLK's rising edge is used to capture data at DATAIN+/- and transmit data at DATAOUT+/-. This bypass operation can be used to facilitate the board debug process.

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Figure 1: Control Diagram for Signal Detection and PLL Bypass Operation

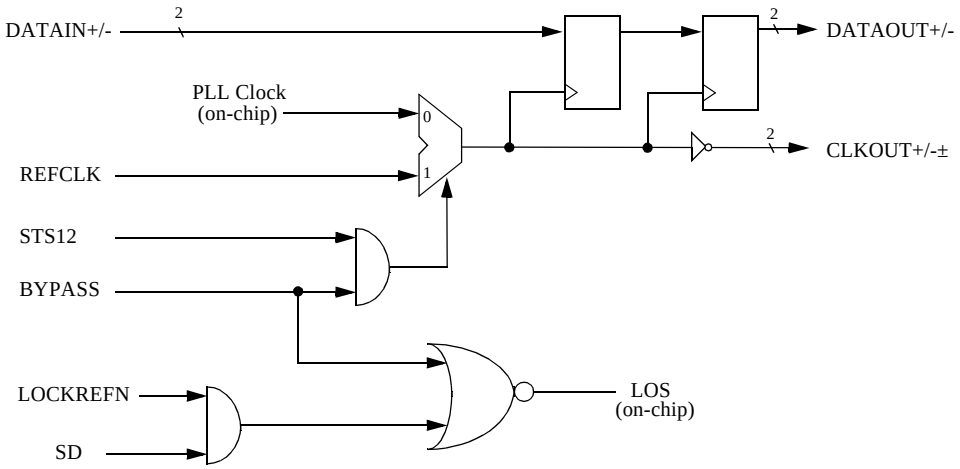

Table 1: Signal Detection and PLL Bypass Operation Control

STS12	*BYPASS*	*LOCKREFN*	*SD*	*LOS*	*DATAOUT*	*CLKOUT*
1	0	1	1	0	DATIN	PLL Clock
1	0	1	0	1	LOW	PLL Clock
1	0	0	1	1	LOW	PLL Clock
1	0	0	0	1	LOW	PLL Clock
1	1	X	X	0	DATIN	$\overline{\text{REFCLK}}$
0	0	1	1	0	DATIN	PLL Clock
0	0	1	0	1	LOW	PLL Clock
0	0	0	1	1	LOW	PLL Clock
0	0	0	0	1	LOW	PLL Clock
0	1	X	X	0	Not Allowed	Not Allowed

AC Characteristics

Table 2: Performance Specifications

Parameters	Min	Typ	Max	Units	Conditions
VCO Center Frequency	—	622.08	—	MHz	
CRU's Reference Clock Frequency Tolerance	-250	—	+250	ppm	
OC-12/STS12 Capture Range	—	±500	—	ppm	With respect to the fixed reference frequency
Clock Output Duty Cycle	45	—	55	% of UI	20% Minimum transition density
Acquisition Lock Time OC-12/STS-12	—	—	16	µs	Valid REFCLK and device already powered up
LVDS Output Rise & Fall Times	—	—	600	ps	10% to 90%, with 100Ω & 5pF capacitive equivalent load
CLKOUT+/- Jitter Generation	—	0.005	0.01	U.I.	No more than 14ps rms jitter on DATAIN+/-
OC-12/STS-12 Jitter Tolerance	0.5	—	—	U.I.	Sinusoidal input jitter of DATAIN+/- from 250KHz to 5MHz

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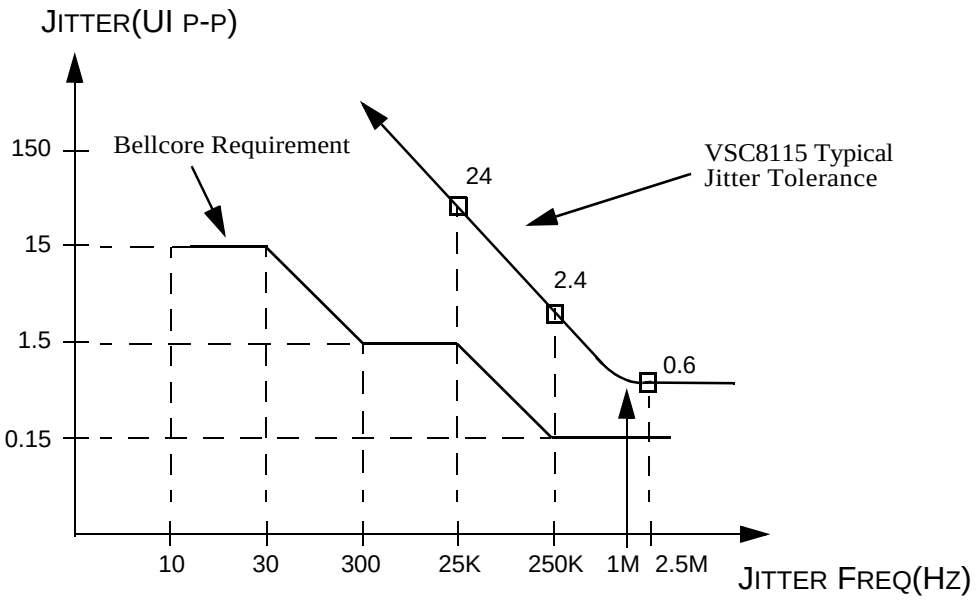
Jitter Tolerance

Jitter Tolerance is the ability of the Clock and Data Recovery Unit to track timing variation in the received data stream. The Bellcore and ITU specifications allow the received optical data to contain jitter. The amount that must be tolerated is a function of the frequency of the jitter. At high frequencies the specifications do not require the VSC8115 to tolerate large amounts, whereas at low frequencies many unit intervals (bit times) of jitter have to be tolerated. Jitter tolerance is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STSN signal versus frequency. The VSC8115 is designed to tolerate this jitter with margin over the specification limits, see Figure 2. The VSC8115 obtains and maintains lock based on the data transition information. When there is no transition on the data stream, the recovered clock frequency will be held to within ±500ppm of the reference clock. The VSC8115 can maintain lock over 1000 bits of no switching on data stream.

Figure 2: Input Jitter Tolerance Specification



Jitter Generation

Jitter generation is defined as the jitter of the serial clock and serial data outputs while rms jitter is presented to the serial data inputs. Maximum jitter generation is 0.01 U.I. when rms jitter of less than 14ps (OC-12) or 56ps (OC-3) is presented to the serial data inputs.

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Retimed Data and Clock Outputs AC Specification

As indicated in figure 3, it is recommended that the retimed data output be captured with the rising edge of the clock output. Data valid time is larger for OC-3/STS-3 mode of operation than that of OC-12/STS-12. Data valid time before the output clock's rising edge is the available setup time (t_{su}) while the data valid time after the clock's rising edge is the available hold time (t_h).

Figure 3: Retimed Data and Clock Outputs Timing Diagram

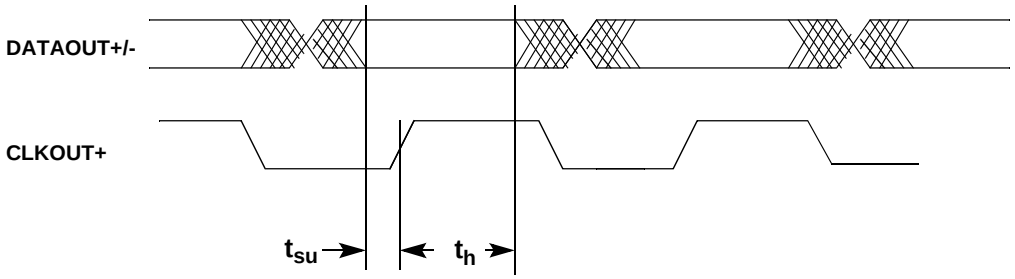

Table 3: Retimed Data and Clock Outputs Timing

Parameters	*Description*	*STS-12 Operation (622.08MHz)*	*STS-3 Operation (155.52MHz)*
t_{su}	Minimum Available Setup Time	450 pS	2.0 nS
t_h	Minimum Available Hold Time	650 pS	3.0 nS

High Speed Outputs

The high speed output buffers, DATAOUT+/- and CLKOUT+/-, can be terminated as either LVDS or LVPECL outputs. If used as LVDS outputs, the transmission lines should be routed with 100-ohm differential impedance, and they need to be terminated at the receive end with a 100-ohm resistor across the differential pair. If used as LVPECL outputs, the transmission line should be 50-ohm terminated with 50-ohm pull down resistors near the receiving end.

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DC Characteristics

Table 4: LVPECL Single-ended Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	V_{DD} - 1.125	—	V_{DD} - 0.5	V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW voltage	V_{DD} - 2.0	—	V_{DD} - 1.5	V	Guaranteed Input LOW Voltage
I_{IH}	Input HIGH current	-0.5	—	10	µA	$V_{IN} = V_{DD}$ - 0.5V
I_{IL}	Input LOW current	-0.5	—	10	µA	$V_{IN} = V_{DD}$ - 2.0V
V_{OL}	Output LOW voltage	V_{DD} - 2.0	—	V_{DD} - 1.8	V	50Ω to (VDD - 2V)
V_{OH}	Output HIGH voltage	V_{DD} - 1.25	—	V_{DD} - 0.67	V	50Ω to (VDD - 2V)

Table 5: LVPECL Differential Inputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	V_{DD} - 1.75	—	V_{DD} - 0.45	V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW voltage	V_{DD} - 2.0	—	V_{DD} - 0.7	V	Guaranteed Input LOW Voltage
ΔV_{IN}	Differential Input Voltage	250	—	—	mV	—
I_{IH}	Input HIGH current	-0.5	—	10	µA	ΔV_{IN} = 0.5V
I_{IL}	Input LOW current	-0.5	—	10	µA	ΔV_{IN} = 0.5V

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Table 6: LVDS Differential Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OCM}	Common Mode voltage	1.0	1.35	1.7	V	100Ω PAD to PADN
ΔV_{OUT}	Differential Output Swing	350	500	750	mV	100Ω PAD to PADN

Table 7: LVPECL Differential Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OCM}	Common Mode voltage	1.12	-	2.0	V	50Ω to (VDD - 2V)
ΔV_{OUT}	Differential Output Swing	400	-	800	mV	50Ω to (VDD - 2V)

Table 8: LVTTL Inputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	2.0	—	VDD	V	—
V_{IL}	Input LOW voltage	0	—	0.8	V	—
I_{IH}	Input HIGH current	-50	---	50	µA	V_{IN} = 2.7V, V_{DD}=MAX
I_{IL}	Input LOW current	-50	---	50	µA	V_{IN} = 0.5V, V_{DD}=MAX

Power Dissipation

Table 9: Power Supply Currents

Parameter	*Description*	*(Typ)*	*(Max)*	*Units*
I_{DD}	Power supply current from V_{DD}	57	80	mA
P_D	Power dissipation	188.1	277	mW

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Absolute Maximum Ratings(1)

Power Supply Voltage (V_{DD}) Potential to GND ..... -0.5V to +4V
DC Input Voltage (LVPECL Inputs) ..... -0.5V to V_{DD} + 0.5V
DC Input Voltage (LVTTL Inputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (LVDS or LVPECL Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^{o} to $+125^{o}$C
Storage Temperature ..... -65^{o}C to $+150^{o}$C
Maximum Input ESD (Human Body Model)
High Speed Outputs (pins 11, 12, 13, & 14) 500V
All Other Pins 1500V

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}) ..... +3.3V ±5 %
Industrial Operating Ambient Temperature Range under Bias ..... -40^{o} to 85^{o}C
Commercial Operating Ambient Temperature Range under Bias ..... 0^{o} to 70^{o}C

Package Pin Descriptions

Figure 4: Pin Diagram

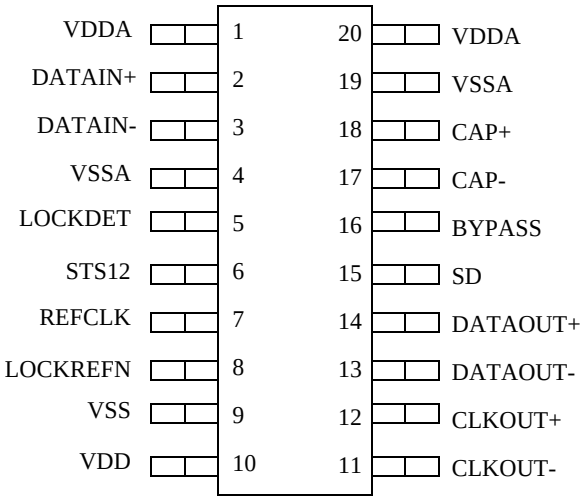

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Table 10: Pin Identification

Signal	*I/O*	*Level*	*Pin Description*
DATAIN+/-	I	LVPECL	Receive data in. The high speed output clock (CLKOUT+/-) is recovered from this high speed differential input data.
DATAOUT+/-	O	LVDS/LVPECL	High speed differential data out. This is the retimed version of the receive data input (DATAIN+/-). Can be configured as either LVDS or LVPECL signal.
CLKOUT+/-	O	LVDS/LVPECL	High speed differential clock out This clock is recovered from the receive data input (DATAIN+/-). Can be configured as either LVDS or LVPECL signal.
STS12	I	LVTTL	STS-12 or STS-3 mode selection. Set HIGH to select the STS-12 operation. Set LOW to select the STS-3 operation.
LOCKREFN	I	LVTTL	Lock to REFCLK input. When set LOW, it holds the CLKOUT+/- output to within ±500ppm of the REFCLK input, and it forces the DATAOUT+/- output to the LOW state.
SD	I	LVPECL	Signal Detect. SD should be connected to the SD output on the optical module. SD is active HIGH. When SD is set HIGH, it means that there is sufficient optical power. When SD is set LOW to indicate loss of signal condition, the CLKOUT+/- output signal will be held to within +500ppm of the REFCLK input; in additions, the DATAOUT+/- will be held in the LOW state.
REFCLK	I	LVTTL	19.44 MHz local reference clock input for the CRU. REFCLK is used for the PLL phase adjustment during power up, and it also serves as a stable clock source in the absence of serial input data.
LOCKDET	O	LVPECL	Active HIGH to indicate that PLL is locked to serial data input, and valid clock and data are present at the serial outputs (DATAOUT+/- and CLKOUT+/-). The LOCKDET will go inactive under the following conditions: (1). If SD is set LOW. (2). If LOCKREFN is set LOW. (3). If the VCO has drifted away from the local reference clock REFCLK by more than 500 ppm.
BYPASS	I	LVTTL	Used for production test. Set to VSS for normal operation.
CAP+/CAP-	I	Analog	External loop filter pins. The loop filter capacitor should be connected to these pins. The capacitor value should be 1.0uF ±10% tolerance.
VDD		+3.3V	+3.3V Power Supply for low speed I/O's and on-chip digital CMOS blocks.
VSS		GND	Ground pin for low speed I/O's and on-chip digital CMOS blocks
VDDA		+3.3V	+3.3V Power Supply for high speed I/O's and on-chip PLL blocks.
VSSA		GND	Ground pins for high speed I/O's and on-chip PLL blocks.

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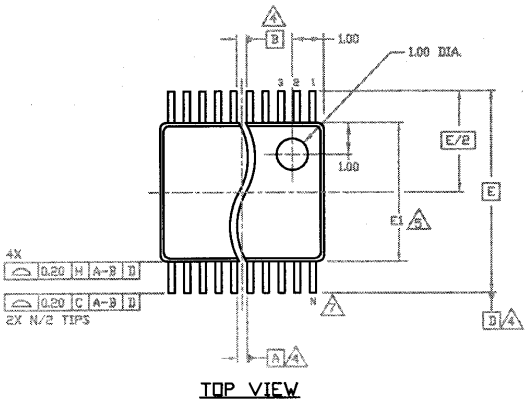
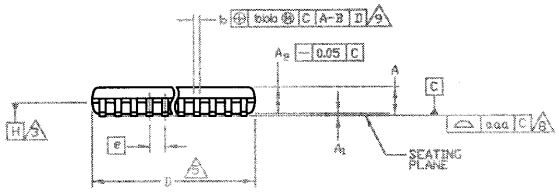
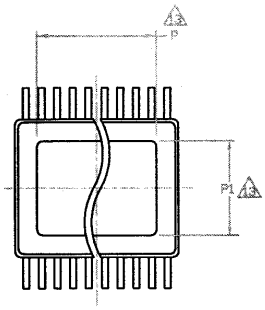
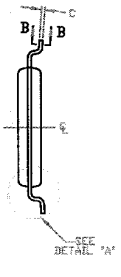
Package Information

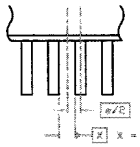
TSSOP Package Drawings

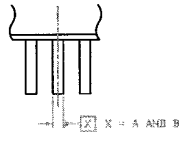


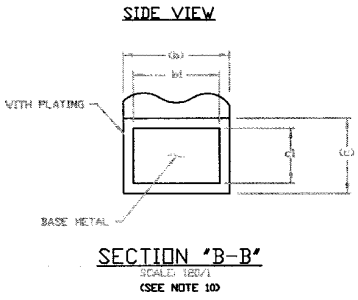


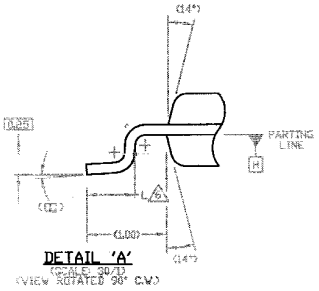












Key	*Min*	*Nom*	*Max*
A	–	–	1.10
A1	0.05	–	0.15
A2	0.85	0.90	0.95
aaa		0.076	
b	0.19	–	0.30
b1	0.19	0.22	0.25
bbb		0.10	
c	0.09	–	0.20
c1	0.09	0.127	0.16
E1	4.30	4.40	4.50
e		0.65 BSC	
E		6.40 BSC	
L	0.50	0.60	0.70
θ	0°	–	8°

Package Thermal Characteristics

The VSC8115 is packaged in a Thin Shrink Small Outline Package (TSSOP). This package conforms to JEDEC package outline standards. It has hi-conductivity copper lead frames and a very low-stress mold compound. The junction to case thermal resistance is 80°C/W for multi-layer PCB applications and 126°C/W for single-layer PCB applications. The air flow versus thermal resistance relationship for multi-layer PCB applications is shown in Table 11.

Table 11: Theta Case to Ambient versus Air Velocity

Air Velocity (LFPM)	*Case to Air Thermal Resistance (°C/W)*	*Ta (Ambient Temperature) Range (°C)*								
		YA			*YA1*			*YA2*		
		(0°C to 75°C) Tcase			*(0°C to 103°C) Tcase*			*(-40°C to 85°C) Tcase*		
0	55.0	15.4	to	59.6	15.4	to	87.6	-55.4	to	69.6
100	52.0	14.6	to	60.4	14.6	to	88.4	-54.6	to	70.4
200	49.0	13.7	to	61.3	13.7	to	89.3	-53.7	to	71.3
400	46.0	12.9	to	62.1	12.9	to	90.1	-52.9	to	72.1

Ordering Information

The order number for this product are:

Part Number	Device Type
VSC8115YA:	STS-12/STS-3 Multi-Rate Clock and Data Recovery Unit in a 20 Pin TSSOP Commercial Temperature, 0°C ambient to 70°C case
VSC8115YA1	STS-12/STS-3 Multi-Rate Clock and Data Recovery Unit in a 20 Pin TSSOP Extended Temperature, 0°C ambient to 110°C case
VSC8115YA2	STS-12/STS-3 Multi-Rate Clock and Data Recovery Unit in a 20 Pin TSSOP Industrial Temperature, -40°C ambient to 85°C case

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