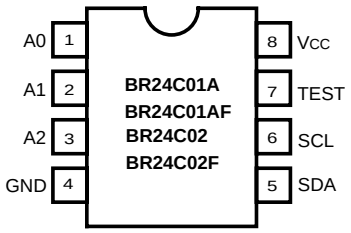
I²C Bus compatible serial EEPROM

BR24C01A / BR24C01AF / BR24C02 / BR24C02F / BR24C04 / BR24C04F

●Features

- Low power CMOS technology.
- 2.7V to 5.5V Operation.
- Two wire serial interface I²C bus™compatible.
- Low power dissipation
  – 0.2mA (typ.) active current: 5V
  – 1.0µA (typ.) standby current: 5V
- Automatic Word Address Incrementing
  – Sequential register read
- Automatic erase-before-write.
- Page write buffer for up to 4 bytes: BR24C01A / AF
  up to 4 bytes: BR24C02 / F
  up to 16 bytes: BR24C04 / F
- DATA security
  –Inhibit to write at low Vcc.
- Noise filters at SCL and SDA pins.
- 8-pin DIP / 8-pin SOP packages.
- 100,000 ERASE / WRITE cycles.
- 10 years Data Retention.

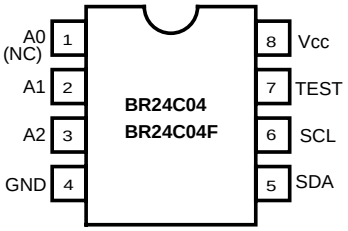
●Pin assignments



●Pin descriptions

Pin name	Function
A0, A1, A2	Slave address setting pin
SCL	Serial data clock
SDA	Serial data input / output
TEST	GND connection
Vcc	Power supply
GND	Ground

●Pin assignments



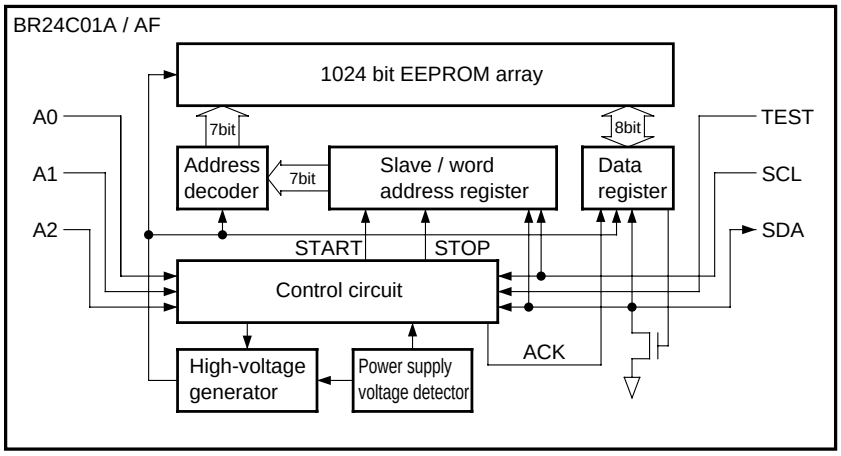
●Pin descriptions

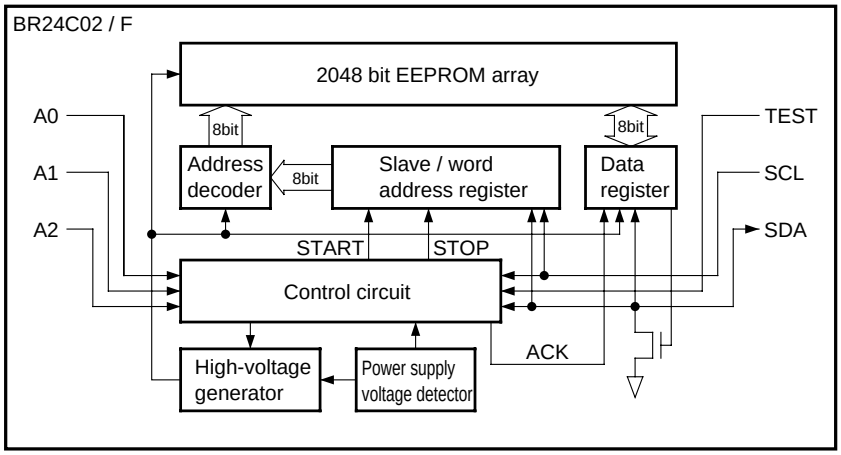
Pin name	Function
A0	N.C.
A1, A2	Slave address setting pin
SCL	Serial data clock
SDA	Serial data input / output
TEST	GND connection
Vcc	Power supply
GND	Ground

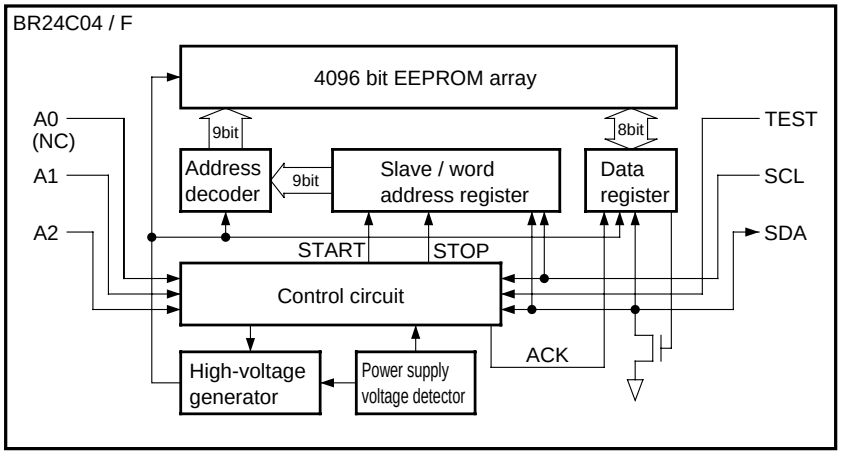
●Over view

The BR24C01A / AF, BR24C02 / F, and BR24C04 / F are 2-wire serial EEPROMs which are electrically programmable.
The configurations are as follows:
BR24C01A / AF: 128 × 8 bit 1K serial EEPROM
BR24C02 / F: 256 × 8 bit 2K serial EEPROM
BR24C04 / F: 512 × 8 bit 4K serial EEPROM

●Block diagram







●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits		Unit
Applied voltage	V_{CC}	– 0.3 ~ + 6.5		V
Power dissipation	Pd	DIP8 pin	500*1	mW
		SOP8 pin	350*2	
Storage temperature	Tstg	– 65 ~ + 125		°C
Operating temperature	Topr	– 40 ~ + 85		°C
Input voltage	—	– 0.3 ~ V_{CC} + 0.3		V

*1 Reduced by 5.0mW for each increase in Ta of 1°C over 25°C.

*2 Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	2.7 ~ 5.5 (WRITE)	V
		2.7 ~ 5.5 (READ)	V
Input voltage	V_{IN}	0 ~ V_{CC}	V

●Electrical characteristics

DC characteristics (unless otherwise noted, Ta = - 40 to + 85°C, V_{CC} = 2.7 to 5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input high level voltage	V_{IH}	0.7V_{CC}	—	—	V	—
Input low level voltage	V_{IL}	—	—	0.3V_{CC}	V	—
Output low level voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3.0mA (SDA)
Input leakage current	I_{LI}	– 10	—	10	µA	V_{IN} = 0V ~ V_{CC}
Output leakage current	I_{LO}	– 10	—	10	µA	V_{OUT} = 0V ~ V_{CC}
Operating current dissipation	I_{CC}	—	—	1.0	mA	V_{CC} = 5.5V, f_{SCL} = 100kHz
Standby current	I_{SB}	—	—	2.0	µA	V_{CC} = 5.5V, SDA · SCL = V_{CC}
SCL frequency	f_{SCL}	—	—	100	kHZ	—

Operating timing characteristics (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 2.7 to 5.5V)

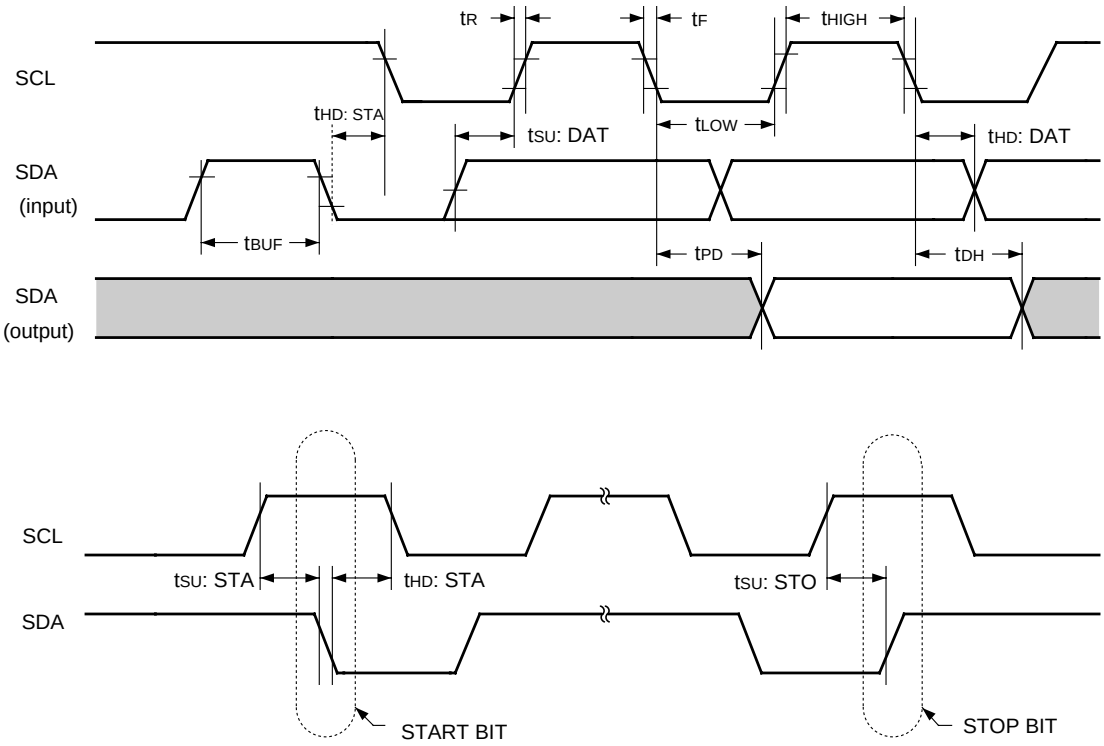
Parameter	Symbol	Min.	Typ.	Max.	Unit
Data clock HIGH time	t_{HIGH}	4.0	—	—	µs
Data clock LOW time	t_{LOW}	4.7	—	—	µs
SDA / SCL rise time	t_R	—	—	1.0	µs
SDA / SCL fall time	t_F	—	—	0.3	µs
Start condition hold time	t_{HD}: STA	4.0	—	—	µs
Start condition setup time	t_{SU}: STA	4.7	—	—	µs
Input data hold time	t_{HD}: DAT	0	—	—	ns
Input data setup time	t_{SU}: DAT	250	—	—	ns
Output data delay time	t_{PD}	0.3	—	3.5	µs
Output data hold time	t_{DH}	0.3	—	—	µs
Stop condition setup time	t_{SU}: STO	4.7	—	—	µs
Bus open time before start of transfer	t_{BUF}	4.7	—	—	µs
Internal write cycle time *1	t_{WR1}	—	—	10	ms
*2	t_{WR2}	—	—	25	ms
Noise erase valid time (SCL / SDA pins)	tI	—	—	0.1	µs

∗1 V_{CC} = 4.5 to 5.5V

∗2 V_{CC} = 2.7 to 4.5V

○ Not designed for radiation resistance.

●Timing charts



- Data is read on the rising edge of SCL.
- Data is output in synchronization with the falling edge of SCL.

Fig.1 Synchronized data input / output timing

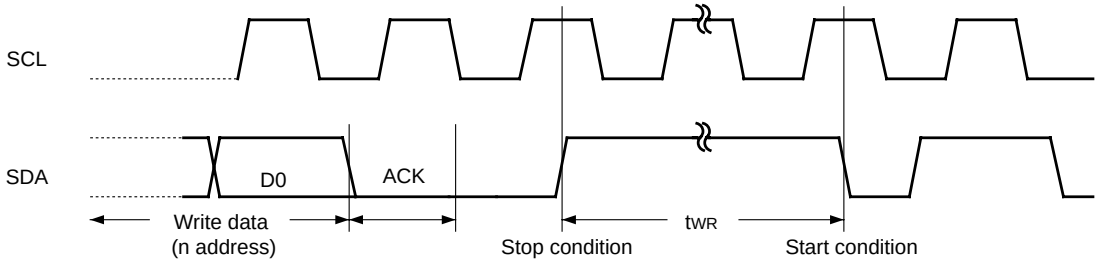


Fig.2 Write cycle timing

●Circuit operation

(1) Start condition (recognition of start bit)

Before executing any command, when SCL is HIGH, a start condition (start bit) is required to cause SDA to fall from HIGH to LOW. This IC is designed to constantly detect whether there is a start condition (start bit) for the SDA and SCL line, and no commands will be executed unless this condition is satisfied.

(See Figure 1 for the synchronized data input / output timing.)

(2) Stop condition (recognition of stop bit)

To stop any command, a stop condition (stop bit) is required. A stop condition is achieved when SDA goes from LOW to HIGH while SCL is HIGH. This enables commands to be completed.

(See Figure 1 for the synchronized data input / output timing.)

(3) Precautions concerning write commands

In the WRITE mode, the transferred data is not written to the memory unless the stop bit is executed.

(4) Device addressing

◇With the BR24C01A / AF and BR24C02 / F

Make sure the slave address is output from the master immediately after the start condition.

The upper four bits of the slave address are used to determine the device type. The device code for this IC is fixed at “1010”.

The next three bits of the slave address (A2, A1, A0 ⋯ device address) are used to select the device. This IC can address up to eight devices on the same bus. The lowermost bit of the slave address (R / $\overline{W}$ ⋯ READ / $\overline{WRITE}$) is used to set the write or read mode as follows.

R / W set to 0 ⋯ Write

(Random read word address setting is also 0)

R / W set to 1 ⋯ Read

1010	A2	A1	A0	R / $\overline{W}$

◇With the BR24C04 / F

Make sure the slave address is output from the master in continuation with the start condition.

The upper four bits of the slave address are used to determine the device type. The device code for this IC is fixed at “1010”.

The next two bits of the slave address (A2, A1 ⋯ device address) are used to select the device. This IC can address up to four devices on the same bus. The next bit of the slave address (PS ⋯ Page Select) is used to select the page. As shown below, it can write to or read from any of the 256 words in the two pages in memory.

PS set to 0 ⋯ Page 1 (000 to 0FF)

PS set to 1 ⋯ Page 2 (100 to 1FF)

The lowermost bit of the slave address (R / $\overline{W}$ ⋯ READ / $\overline{WRITE}$) is used to set the write or read mode as follows.

R / W set to 0 ⋯ Write

(Random read word address setting is also 0)

R / W set to 1 ⋯ Read

1010	A2	A1	PS	R / $\overline{W}$

(5) ACK signal

The acknowledge signal (ACK signal) is determined by software and is used to indicate whether or not a data transfer is proceeding normally. The transmitting device, whether the master or slave, opens the bus after an 8-bit data output (μ-COM when a write or read command of the slave address input; this IC when reading data).

For the receiving device during the ninth clock cycle, SDA is set to LOW and an acknowledge signal (ACK signal) is sent to indicate that it received the 8-bit data (this IC when a write command or a read command of the slave address input, μ-COM when a read command data output).

This IC outputs a LOW acknowledge signal (ACK signal) after recognizing the start condition and slave address (8 bits).

When data is being written to this IC, a LOW acknowledge signal (ACK signal) is output after the receipt of each eight bits of data (word address and write data).

When data is being read from the IC, eight bits of data (read data) are output and the IC waits for a returned LOW acknowledge signal (ACK signal). When an acknowledge signal (ACK signal) is detected and a stop condition is not sent from the master (μ-COM) side, the IC continues to output data. If an acknowledge signal (ACK signal) is not detected, the IC interrupts the data transfer and ceases reading operations after recognizing the stop condition (stop bit). The IC then enters the waiting or standby state.

(See Figure 3 for acknowledge signal (ACK signal) response.)

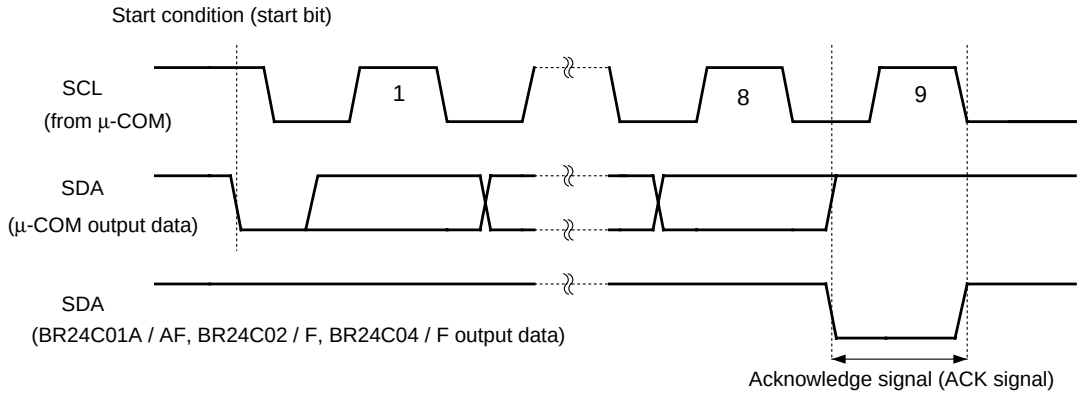


Fig.3 Acknowledge (ACK signal) response
(during write and read slave address input)

(6) Byte write

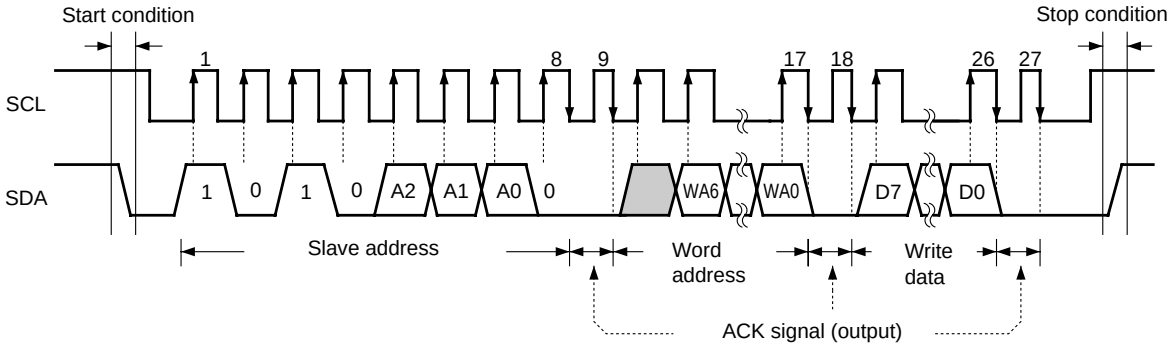


Fig.4 Byte write cycle (BR24C01A / AF)

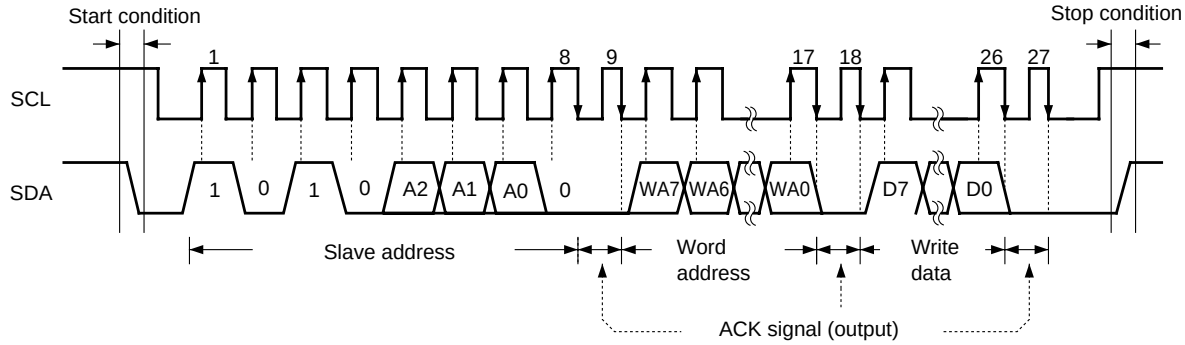


Fig.5 Byte write cycle (BR24C02 / F)

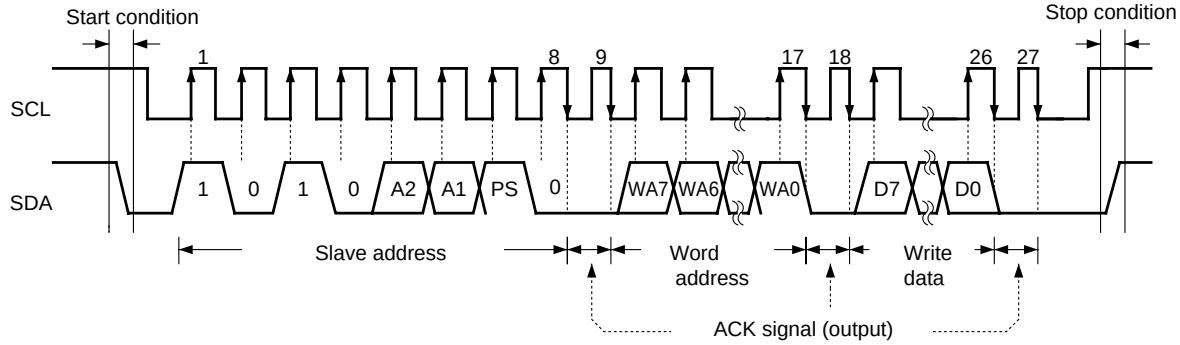


Fig.6 Byte write cycle (BR24C04 / F)

- Data is written to the address designated by the word address (n address).
- After eight bits of data are input, the data is written to the memory cell by issuing the stop bit.

(7) Page write cycle

BR24C01A / AF

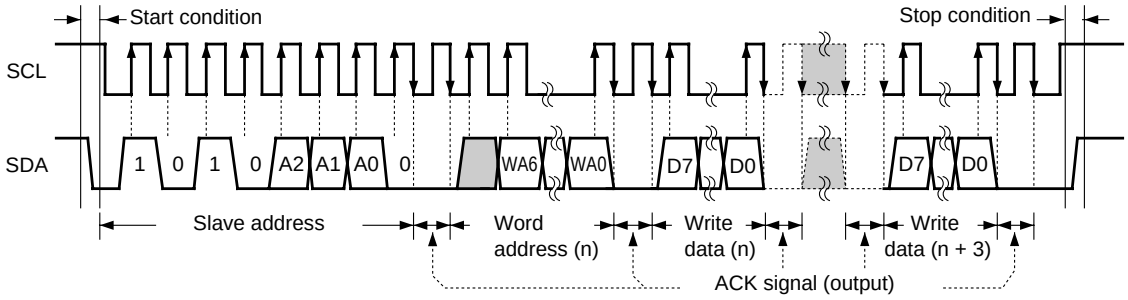


Fig.7

- A 4-byte write is possible using this command.
- The page write command arbitrarily sets the upper five bits (WA6 to WA2) of the word address. The lower two bits (WA1 and WA0) can write up to four bytes of data with the address being incremented internally.

BR24C02 / F

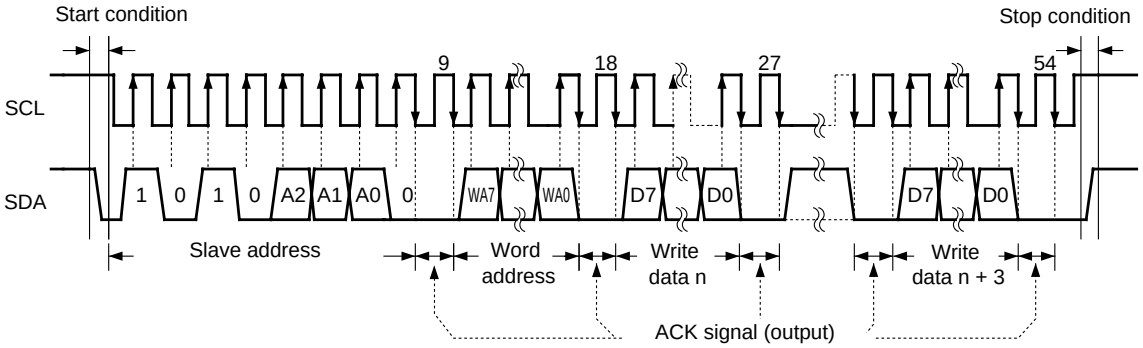


Fig.8

- A 4-byte write is possible using this command.
- The page write command arbitrarily sets the upper six bits (WA7 to WA2) of the word address. The lower two bits (WA1 and WA0) can write up to four bytes of data with the address being incremented internally.

BR24C04 / F

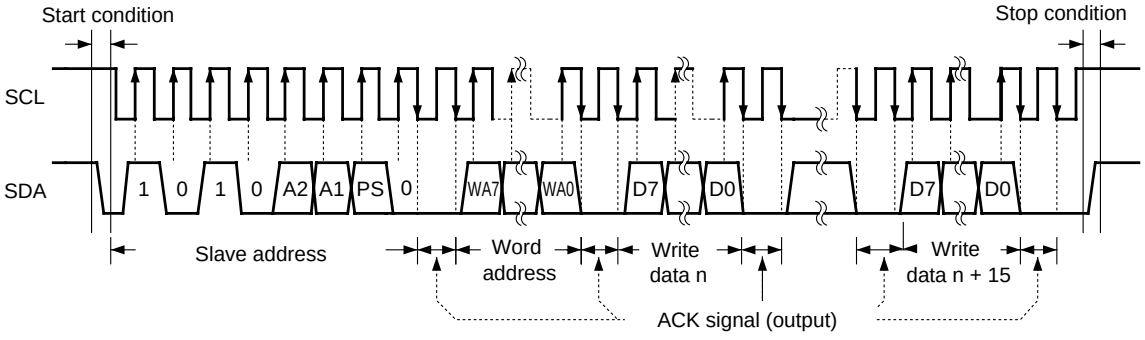


Fig.9

- A 16-byte write is possible using this command.
- The page write command arbitrarily sets the upper four bits (WA7 to WA4) of the word address. The lower four bits (WA3 to WA0) can write up to 16 bytes of data with the address being incremented internally.

(8) Current read

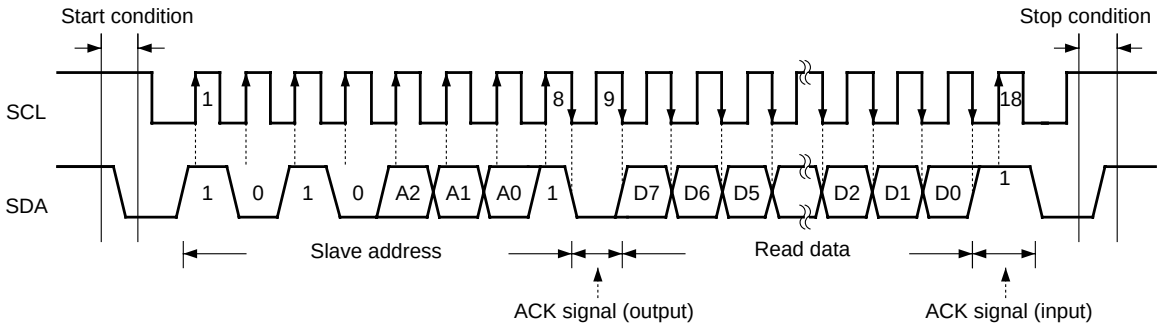


Fig.10 Current read cycle (BR24C01A / AF)

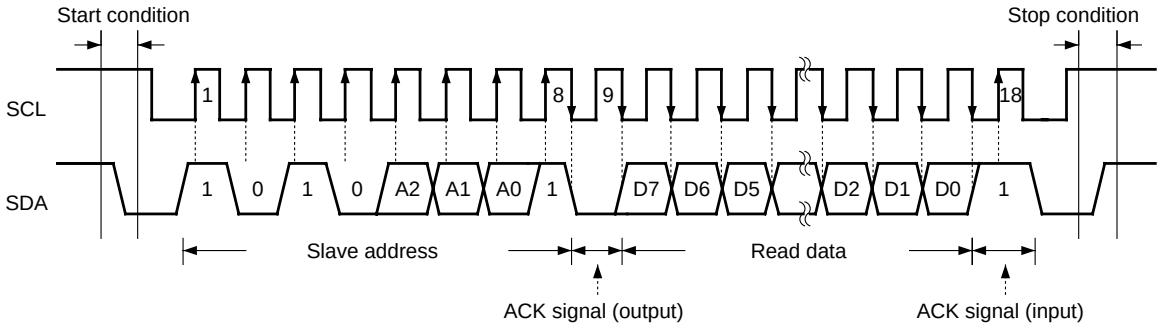


Fig.11 Current read cycle (BR24C02 / F)

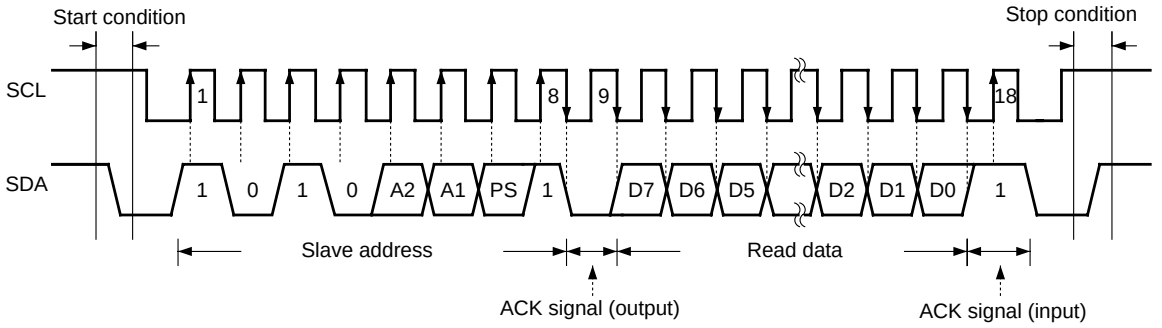


Fig.12 Current read cycle (BR24C04 / F)

- This IC increments the address by one position by using the internal circuit address count. It records the final word address (n address) of the executed write - read command.
- This command reads the data of the next word address (n + 1 address) of the final write word address after the execution of the previous command.
- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. [All words all read enabled]
  (See Figures 16 to 18 for the sequential read cycles.)
- This command is ended by inputting HIGH to the ACK signal after D0 and raising the SDA signal (stop condition) by setting SCL to HIGH.

(9) Random read

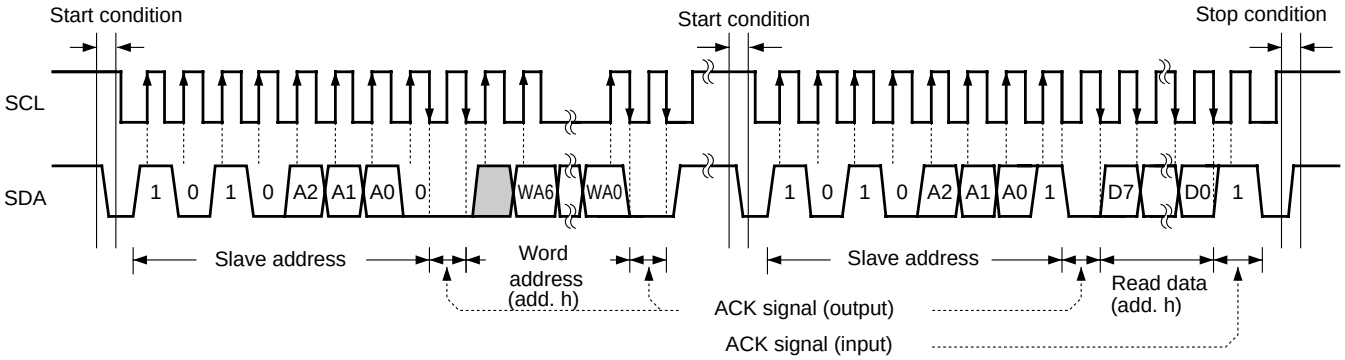


Fig.13 Random read cycle (BR24C01A / AF)

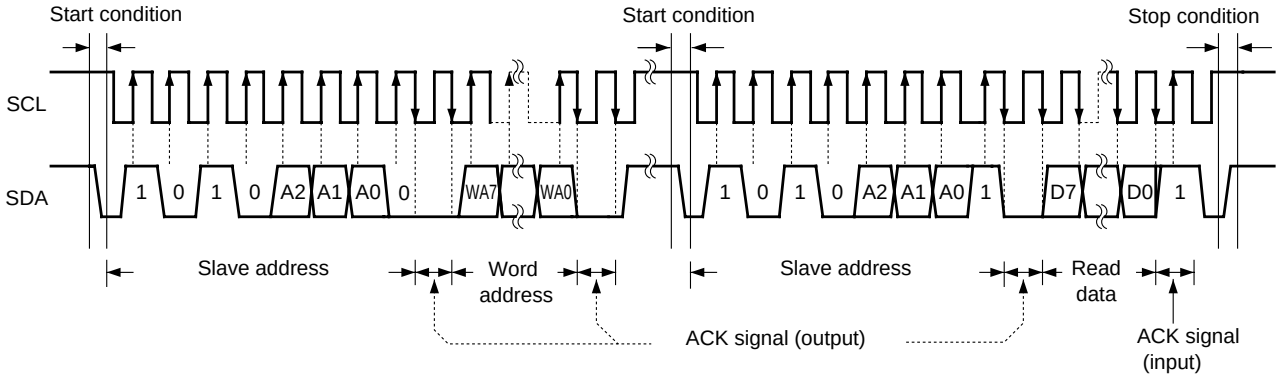


Fig.14 Random read cycle (BR24C02 / F)

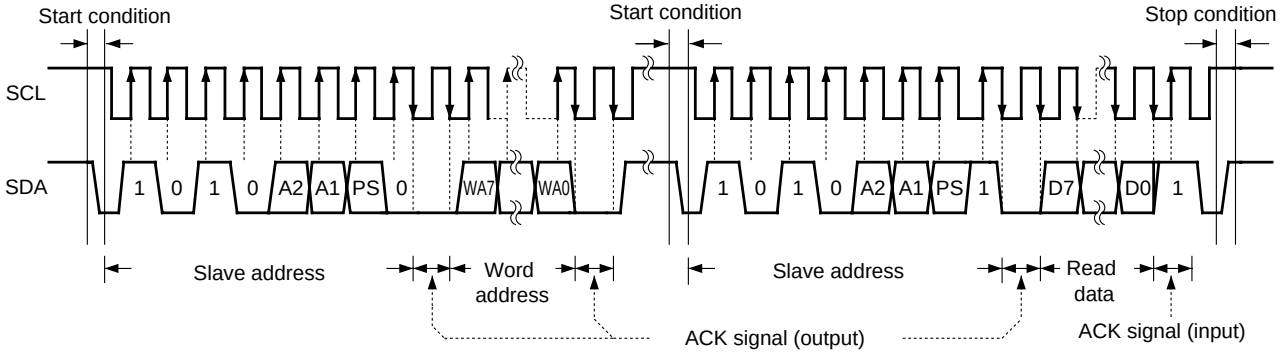


Fig.15 Random read cycle (BR24C04 / F)

- This command can read the designated word address data.
- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. [All words all read enabled]
  (See Figures 16 to 18 for the sequential read cycles.)
- This command is ended by inputting a HIGH signal to the ACK signal after D0 and raising the SDA signal (stop condition) by raising SCL to HIGH.

(10) Sequential read

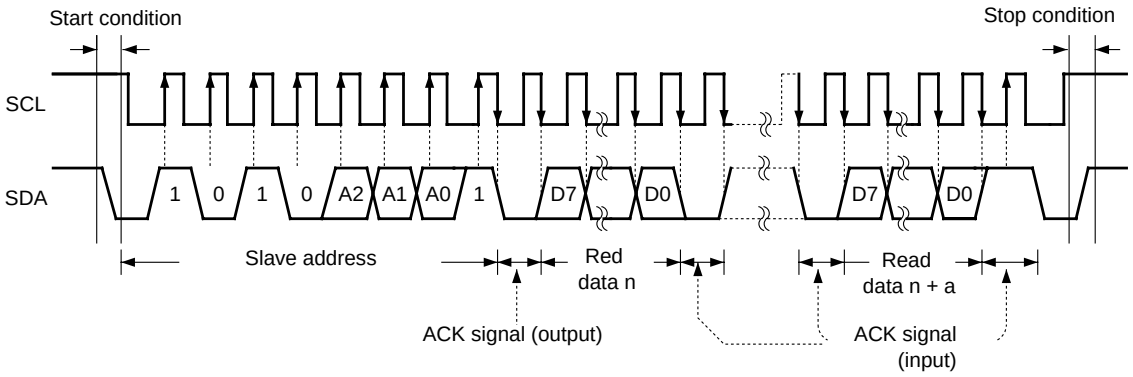


Fig.16 Sequential read cycle (BR24C01A / AF)
(Example: For a current read)

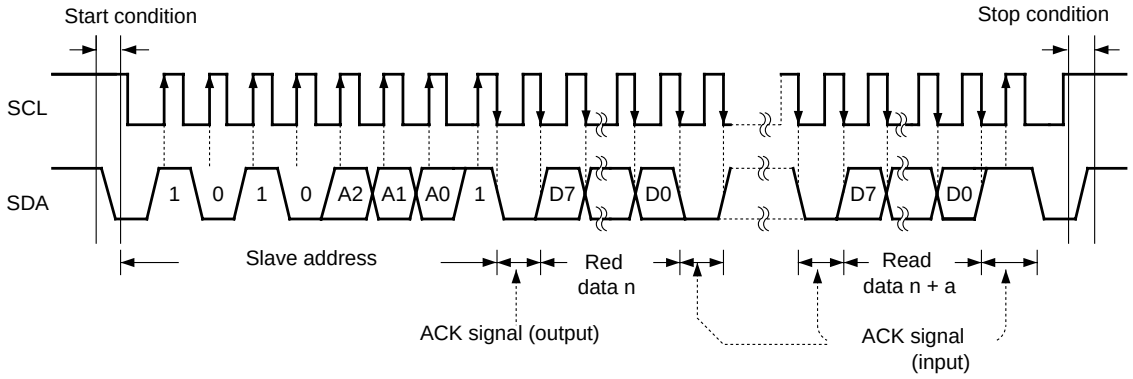


Fig.17 Sequential read cycle (BR24C02 / F)
(Example: For a current read)

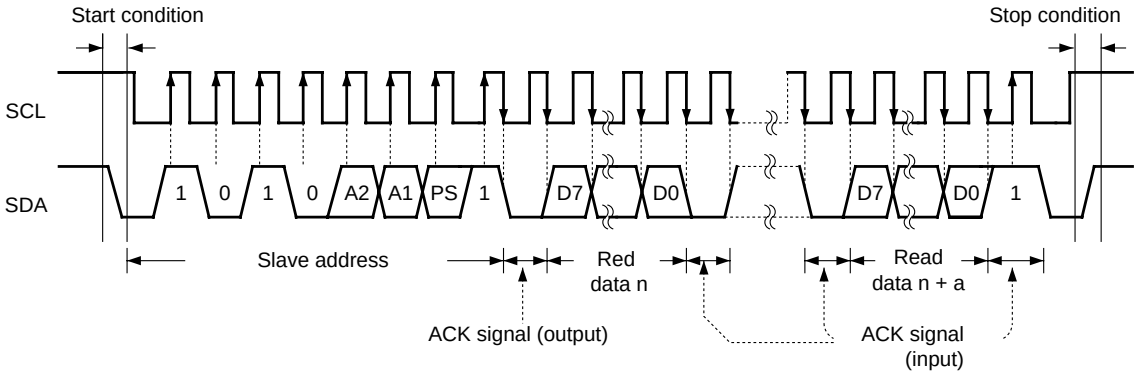


Fig.18 Sequential read cycle (BR24C04 / F)
(Example: For a current read)

- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. [All words can be read]
- This command is ended by inputting a HIGH signal to the ACK signal after D0 and raising the SDA signal (stop condition) using the SCL signal HIGH.
- Sequential reading can also be done with a random read.

●Operation notes

(1) During power rise

During power rise, the V_{CC} may rise passing through the low voltage domain in which the IC internal circuit does not work. For this reason, there is a risk of misoperation when the power rises without full IC internal reset.

To prevent this, pay attention to the following points during a power rise.

1) Set SCL = SDA = “HIGH”

2) Raise the power so as to activate the Power On Reset (P. O. R) circuit.

Follow the steps below as to operate the P. O. R. circuit properly.

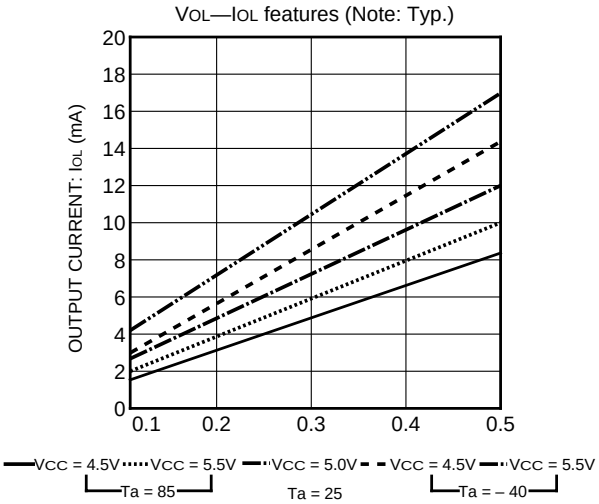
1) Set the power rise time (tR) to within 10ms.

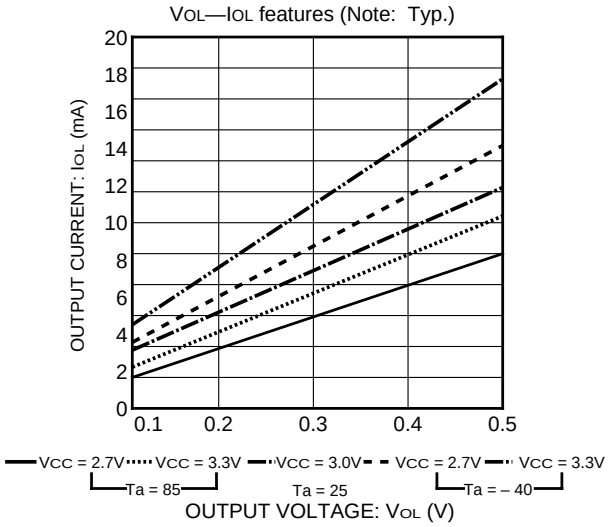
2) Set the OFF domain for once power has been cut to 100ms minimum.

(2) SDA terminal pull-up resistance

The SDA terminal is an open drain output. Consequently, it requires an external pull-up resistance. The appropriate pull-up resistace value is selected from the IC V_{OL}-I_{OL} features, which have been appended as measuring data, as well as V_{IL} and I_{LI} and other personal icons that control the IC in question.

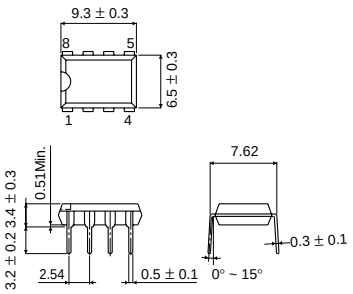
Recommended values 2.0k to 10kΩ



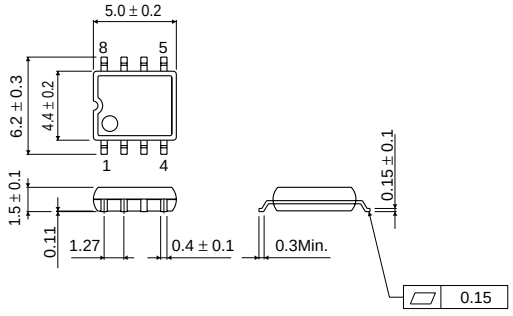


Note: All memory array data are set to “FF” status at time of shipping.

●External dimensions (Units: mm)



DIP8



SOP8