DEC. 1998

Ver. 3.0

8-BIT SINGLE-CHIP MICROCONTROLLERS

GMS90 Series

DATA SHEET

LG Semicon

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Version 3.0

Published by
MCU Application Team

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Device Naming Structure

GMS90X5X - GBXXX XX XX

LG Semicon MCU

Mask ROM version

Frequency

Blank: 12MHz
24: 24MHz
40: 40MHz

Package Type

Blank: 40PDIP
PL: 44PLCC
Q: 44MQFP

ROM Code serial No.

ROM size

1: 4k bytes
2: 8k bytes
4: 16k bytes
6: 24k bytes
8: 32k bytes

Operating Voltage

C: 4.25~5.5V
L: 2.7~3.6V

GMS97X5X X XX

LG Semicon MCU

OTP version

Package Type

Blank: 40PDIP
PL: 44PLCC
Q: 44MQFP

Frequency

Blank: 12/24(5V),12MHz(3V)
H: 33MHz

ROM size

1: 4k bytes
2: 8k bytes
4: 16k bytes
6: 24k bytes
8: 32k bytes

Operating Voltage

C: 4.25~5.5V
L: 2.7~3.6V

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GMS90 Series Selection Guide

Operating Voltage (V)	ROM size (bytes)		RAM size (bytes)	Device Name	Operating Frequency (MHz)
	MASK	OTP			
4.25~5.5	ROM-less		128	GMS90C31	12/24/40
			256	GMS90C32	12/24/40
	4K	-	128	GMS90C51	12/24/40
	8K	-	256	GMS90C52	12/24/40
	16K	-	256	GMS90C54	12/24/40
	24K	-	256	GMS90C56	12/24/40
	32K	-	256	GMS90C58	12/24/40
	-	4K	128	GMS97C51	12/24
	-	4K	128	GMS97C51H	33
	-	8K	256	GMS97C52	12/24
	-	8K	256	GMS97C52H	33
	-	16K	256	GMS97C54	12/24
	-	16K	256	GMS97C54H	33
	-	24K	256	GMS97C56	12/24
	-	24K	256	GMS97C56H	33
	-	32K	256	GMS97C58	12/24
	-	32K	256	GMS97C58H	33
2.7~3.6	ROM-less		128	GMS90L31	12/16
			256	GMS90L32	12/16
	4K	-	128	GMS90L51	12/16
	8K	-	256	GMS90L52	12/16
	16K	-	256	GMS90L54	12/16
	24K	-	256	GMS90L56	12/16
	32K	-	256	GMS90L58	12/16
	-	4K	128	GMS97L51	12
	-	8K	256	GMS97L52	12
	-	16K	256	GMS97L54	12
	-	24K	256	GMS97L56	12
	-	32K	256	GMS97L58	12

Note: The ROM version products in this data book will be applied to new masking version. (From Dec., 1998)
In case that you have old products, please refer to previous data book (prior to this).

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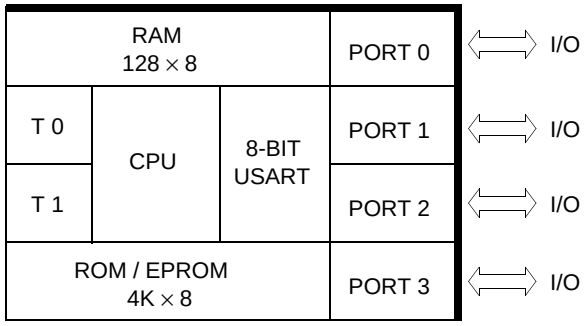
GMS90C31/51, 97C51
GMS90L31/51, 97L51 (Low voltage versions)

- Fully compatible to standard MCS-51 microcontroller
- Wide operating frequency up to 40MHz (for more detail, see “GMS90 Series Selection Guide”)
- 4K × 8 (EP)ROM
- 128 × 8 RAM
- 64K external program memory space
- 64K external data memory space
- Four 8-bit ports
- Two 16-bit Timers / Counters
- USART
- Five interrupt sources, two priority levels
- Power saving Idle and power down mode
- Quick pulse programming algorithm (in the OTP devices)
- 2-level program memory lock (in the OTP devices)
- 2.7Volt low voltage version available
- P-DIP-40, P-LCC-44, P-MQFP-44 package

Block Diagram



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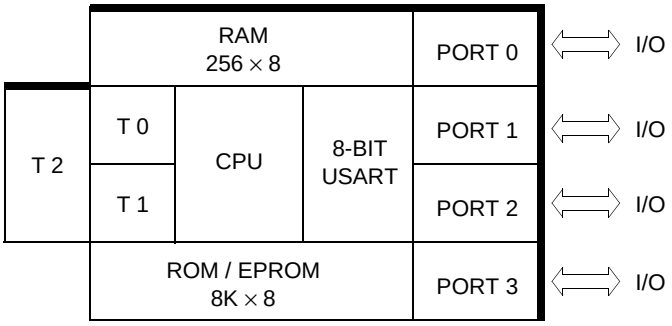
GMS90C32/52, 97C52
GMS90L32/52, 97L52 (Low voltage versions)

- Fully compatible to standard MCS-51 microcontroller
- Wide operating frequency up to 40MHz (for more detail, see “GMS90 Series Selection Guide”)
- 8K × 8 (EP)ROM
- 256 × 8 RAM
- 64K external program memory space
- 64K external data memory space
- Four 8-bit ports
- Three 16-bit Timers / Counters (Timer2 with up/down counter feature)
- USART
- Six interrupt sources, two priority levels
- Power saving Idle and power down mode
- Quick pulse programming algorithm (in the OTP devices)
- 2-level program memory lock (in the OTP devices)
- 2.7Volt low voltage version available
- P-DIP-40, P-LCC-44, P-MQFP-44 package

Block Diagram



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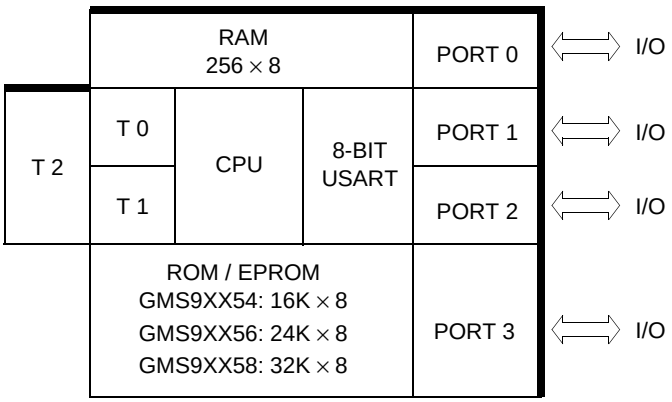
GMS90C54/56/58, 97C54/56/58
GMS90L54/56/58, 97L54/56/58 (Low voltage versions)

- Fully compatible to standard MCS-51 microcontroller
- Wide operating frequency up to 40MHz (for more detail, see “GMS90 Series Selection Guide”)
- 16K/24K/32K bytes (EP)ROM
- 256 × 8 RAM
- 64K external program memory space
- 64K external data memory space
- Four 8-bit ports
- Three 16-bit Timers / Counters (Timer2 with up/down counter feature)
- USART
- One clock output port
- Programmable ALE pin enable / disable
- Six interrupt sources, two priority levels
- Power saving Idle and power down mode
- Quick pulse programming algorithm (in the OTP devices)
- 2-level program memory lock (in the OTP devices)
- 2.7Volt low voltage version available
- P-DIP-40, P-LCC-44, P-MQFP-44 package

Block Diagram



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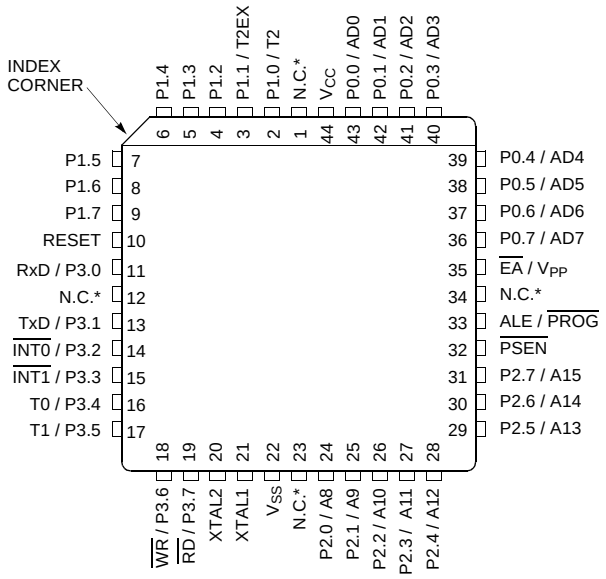
PIN CONFIGURATION

44-PLCC Pin Configuration (top view)



N.C.: Do not connect.

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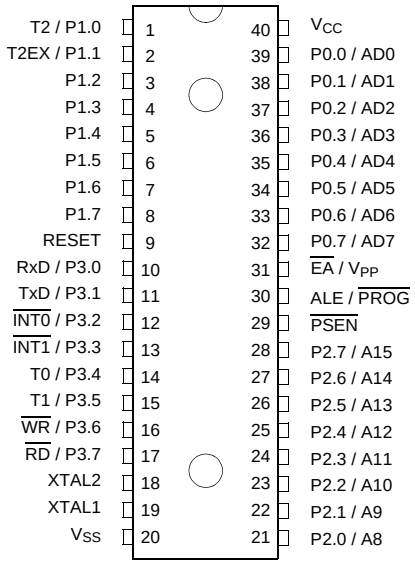
40-PDIP Pin Configuration (top view)



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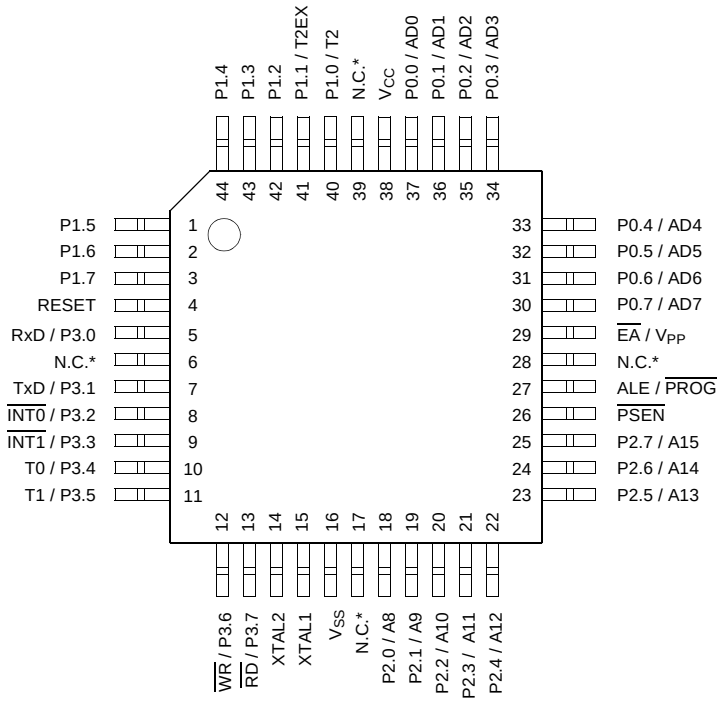
44-MQFP Pin Configuration (top view)



N.C.: Do not connect.

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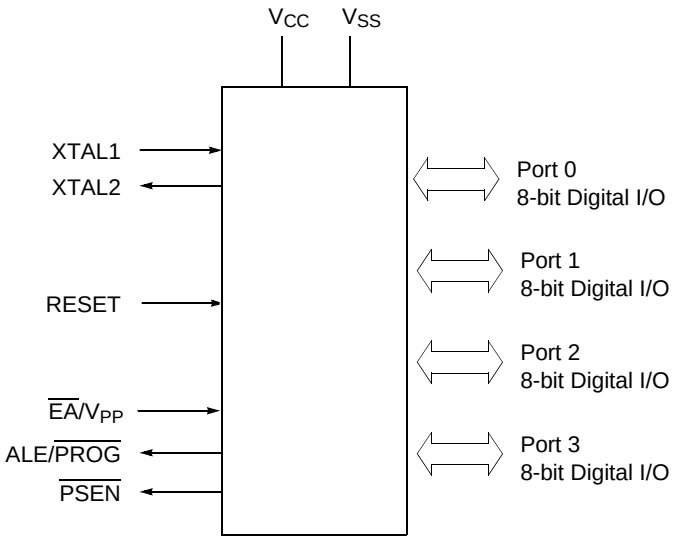
Logic Symbol



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PIN DEFINITIONS AND FUNCTIONS

Symbol	Pin Number			Input/ Output	Function
	PLCC-44	PDIP-40	MQFP-44		
P1.0-P1.7	2-9	1-8	40-44, 1-3	I/O	**Port1** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the pulls-ups (I_{IL}, in the DC characteristics). Pins P1.0 and P1.1 also. Port1 also receives the low-order address byte during program memory verification. Port1 also serves alternate functions of Timer 2.
	2	1	40		P1.0 / T2 : Timer/counter 2 external count input
	3	2	41		P1.1 / T2EX : Timer/counter 2 trigger input
					In GMS9XC54/56/58:
	2	1	40		P1.0 / T2, Clock Out : Timer/counter 2 external count input, Clock Out
P3.0-P3.7	11, 13-19	10-17	5, 7-13	I/O	**Port 3** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 3 pins that are externally pulled low will source current because of the pulls-ups (I_{IL}, in the DC characteristics). Port 3 also serves the special features of the 80C51 family, as listed below.
	11	10	5		P3.0 / RxD receiver data input (asynchronous) or data input output(synchronous) of serial interface 0
	13	11	7		P3.1 / TxD transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0
	14	12	8		P3.2 /$\overline{INT0}$ interrupt 0 input/timer 0 gate control
	15	13	9		P3.3 / $\overline{INT1}$ interrupt 1 input/timer 1 gate control
	16	14	10		P3.4 /T0 counter 0 input
	17	15	11		P3.5 /T1 counter 1 input
	18	16	12		P3.6 / $\overline{WR}$ the write control signal latches the data byte from port 0 into the external data memory
	19	17	13		P3.7 /$\overline{RD}$ the read control signal enables the external data memory to port 0
XTAL2	20	18	14	O	**XTAL2** Output of the inverting oscillator amplifier.

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Symbol	Pin Number			Input/ Output	Function
	PLCC-44	PDIP-40	MQFP-44		
XTAL1	21	19	15	I	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0-P2.7	24-31	21-28	18-25	I/O	**Port 2** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 2 pins that are externally pulled low will source current because of the pulls-ups (I_{IL}, in the DC characteristics).Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 special function register.
$\overline{PSEN}$	32	29	26	O	**The $\overline{\text{Program Store Enable}}$** The read strobe to external program memory when the device is executing code from the external program memory. $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
RESET	10	9	4	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.

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Symbol	Pin Number			Input/ Output	Function
	PLCC-44	PDIP-40	MQFP-44		
ALE / $\overline{PROG}$	33	30	27	O	**The Address Latch Enable / $\overline{\text{Program pulse}}$** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming. **In GMS9XC54/56/58:** If desired, ALE operation can be disabled by setting bit 0 of SFR location $8E_H$. With this bit set, the pin is weakly pulled high. The ALE disable feature will be terminated by reset. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.
$\overline{EA}$ / V_{PP}	35	31	29	I	External Access Enable / Program Supply Voltage $\overline{EA}$ must be external held low to enable the device to fetch code from external program memory locations 0000_H to $FFFF_H$. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than its internal memory size. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. Note; however, that if any of the Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.
P0.0-P0.7	36-43	32-39	30-37	I/O	**Port 0** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the GMS97X5X. External pull-up resistors are required during program verification.
V_{SS}	22	20	16	-	**Circuit ground potential**
V_{CC}	44	40	38	-	**Supply terminal** for all operating modes
N.C.	1,12 23,34	-	6,17 28,39	-	**No connection**

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FUNCTIONAL DESCRIPTION

The GMS90 series is fully compatible to the standard 8051 microcontroller family.

It is compatible with the general 8051 family. While maintaining all architectural and operational characteristics of the general 8051 family.

Figure 1 shows a block diagram of the GMS90 series

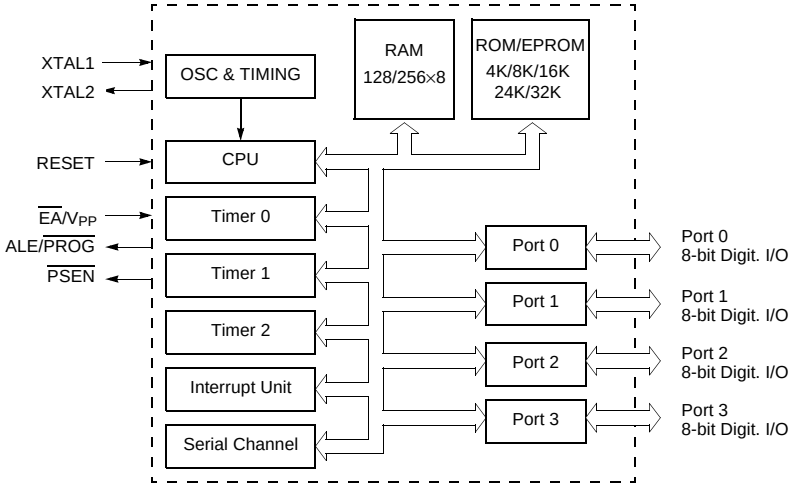

Figure 1. Block Diagram of the GMS90 series

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CPU

The GMS90 series is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1.0µs (40MHz: 300ns).

Special Function Register PSW

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. $D0_H$	**CY**	**AC**	**F0**	**RS1**	**RS0**	**OV**	**F1**	**P**	PSW

Bit	Function
CY	**Carry Flag**
AC	**Auxiliary Carry Flag** (for BCD operations)
F0	**General Purpose Flag**
RS1 ***RS0*** *0 0* *0 1* *1 0* *1 1*	**Register Bank select control bits** Bank 0 selected, data address 00_H - 07_H Bank 1 selected, data address 08_H - $0F_H$ Bank 2 selected, data address 10_H - 17_H Bank 3 selected, data address 18_H - $1F_H$
OV	**Overflow Flag**
F1	**General Purpose Flag**
P	**Parity Flag** Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

Reset value of PSW is 00_H.

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SPECIAL FUNCTION REGISTERS

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 28 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in Table 1, Table 1, and Table 3.

In Table 1 they are organized in numeric order of their addresses. In Table 2 they are organized in groups which refer to the functional blocks of the GMS90 series. Table 3 illustrates the contents of the SFRs.

Table 1. Special Function Registers in Numeric Order of their Addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	**P0** 1)	**FFH**	**90H**	**P1** 1)	**FF_H**
81H	SP	07H	91H	reserved	00_H
82H	DPL	00H	92H	reserved	XXH 2)
83H	DPH	00H	93H	reserved	XXH 2)
84H	reserved	XXH 2)	94H	reserved	XXH 2)
85H	reserved	XXH 2)	95H	reserved	XXH 2)
86H	reserved	XXH 2)	96H	reserved	XXH 2)
87H	PCON	$0XX0000_B$ 2)	97H	reserved	XXH 2)
88H	**TCON** 1)	**00H**	**98H**	**SCON** 1)	**00H**
89H	TMOD	00H	99H	SBUF	XXH 2)
8AH	TL0	00H	9AH	reserved	XXH 2)
8BH	TL1	00H	9BH	reserved	XXH 2)
8CH	TH0	00H	9CH	reserved	XXH 2)
8DH	TH1	00H	9DH	reserved	XXH 2)
8EH 3)	☞ 3)	☞ 3)	9EH	reserved	XXH 2)
8FH	reserved	XXH 2)	9FH	reserved	XXH 2)

1) Bit-addressable Special Function Register.

2) X means that the value is indeterminate and the location is reserved.

3) The GMS9XX54/56/58 have the AUXR0 register at address $8E_H$.

GMS9XX51/52			GMS9XX54/56/58		
$8E_H$	reserved	XXXXXXXX_B 2)	$8E_H$	AUXR0	$XXXXXXX0_B$ 2)

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Table 1. Special Function Registers in Numeric Order of their Addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
A0H	**P2** 1)	**FFH**	**C8H**	**T2CON** 1)	**00H**
A1H	reserved	XXH 2)	C9H 3)	T2MOD	☞ 3)
A2H	reserved	XXH 2)	CAH	RC2L	00H
A3H	reserved	XXH 2)	CBH	RC2H	00H
A4H	reserved	XXH 2)	CCH	TL2	00H
A5H	reserved	XXH 2)	CDH	TH2	00H
A6H	reserved	XXH 2)	CEH	reserved	XXH 2)
A7H	reserved	XXH 2)	CFH	reserved	XXH 2)
A8H	**IE** 1)	**0X000000B** 2)	**D0H**	**PSW** 1)	**00H**
A9H	reserved	XXH 2)	D1H	reserved	XXH 2)
AAH	reserved	XXH 2)	D2H	reserved	XXH 2)
ABH	reserved	XXH 2)	D3H	reserved	XXH 2)
ACH	reserved	XXH 2)	D4H	reserved	XXH 2)
ADH	reserved	XXH 2)	D5H	reserved	XXH 2)
AEH	reserved	XXH 2)	D6H	reserved	XXH 2)
AFH	reserved	XXH 2)	D7H	reserved	XXH 2)
B0H	**P3** 1)	**FFH**	**D8H**	reserved	XXH 2)
B1H	reserved	XXH 2)	D9H	reserved	XXH 2)
B2H	reserved	XXH 2)	DAH	reserved	XXH 2)
B3H	reserved	XXH 2)	DBH	reserved	XXH 2)
B4H	reserved	XXH 2)	DCH	reserved	XXH 2)
B5H	reserved	XXH 2)	DDH	reserved	XXH 2)
B6H	reserved	XXH 2)	DEH	reserved	XXH 2)
B7H	reserved	XXH 2)	DFH	reserved	XXH 2)
B8H	**IP** 1)	**XX000000B** 2)	**E0H**	**ACC** 1)	**00H**
B9H	reserved	XXH 2)	E1H	reserved	XXH 2)
BAH	reserved	XXH 2)	E2H	reserved	XXH 2)
BBH	reserved	XXH 2)	E3H	reserved	XXH 2)
BCH	reserved	XXH 2)	E4H	reserved	XXH 2)
BDH	reserved	XXH 2)	E5H	reserved	XXH 2)
BEH	reserved	XXH 2)	E6H	reserved	XXH 2)
BFH	reserved	XXH 2)	E7H	reserved	XXH 2)
C0H	reserved	**XX_H**	**E8H**	reserved	XXH 2)
C1H	reserved	XXH 2)	E9H	reserved	XXH 2)
C2H	reserved	XXH 2)	EAH	reserved	XXH 2)
C3H	reserved	XXH 2)	EBH	reserved	XXH 2)
C4H	reserved	XXH 2)	ECH	reserved	XXH 2)
C5H	reserved	XXH 2)	EDH	reserved	XXH 2)
C6H	reserved	XXH 2)	EEH	reserved	XXH 2)
C7H	reserved	XXH 2)	EFH	reserved	XXH 2)

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Table 1. Special Function Registers in Numeric Order of their Addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
F0H	**B** 1)	**00H**	**F8H**	reserved	XXH 2)
F1H	reserved	XXH 2)	F9H	reserved	XXH 2)
F2H	reserved	XXH 2)	FAH	reserved	XXH 2)
F3H	reserved	XXH 2)	FBH	reserved	XXH 2)
F4H	reserved	XXH 2)	FCH	reserved	XXH 2)
F5H	reserved	XXH 2)	FDH	reserved	XXH 2)
F6H	reserved	XXH 2)	FEH	reserved	XXH 2)
F7H	reserved	XXH 2)	FFH	reserved	XXH 2)

1) Bit-addressable Special Function Register.

2) X means that the value is indeterminate and the location is reserved.

3) Address $C9_H$ is configured as below.

GMS9XX51/52			**GMS9XX54/56/58**		
$C9_H$	reserved	$XXXXXXX0_B$ 2)	$C9_H$	T2MOD	$XXXXXX00_B$ 2)

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Table 2. Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC B DPH DPL PSW SP	Accumulator B-Register Data Pointer, High Byte Data Pointer, Low Byte Program Status Word Register Stack Pointer	**E0H** 1) **F0H** 1) **83H** 82H **D0H** 1) 81H	00H 00H 00H 00H 00H 07H
Interrupt System	IE IP	Interrupt Enable Register Interrupt Priority Register	**A8H** 1) **B8H** 1)	0X000000B 2) XX000000B 2)
Ports	P0 P1 P2 P3	Port 0 Port 1 Port 2 Port 3	**80H** 1) **90H** 1) **A0H** 1) **B0H** 1)	FFH FFH FFH FFH
Serial Channels	PCON 3) SBUF SCON	Power Control Register Serial Channel Buffer Reg. Serial Channel 0 Control Reg.	87H 99H **98H** 1)	0XXX0000B 2) XXH 2) 00H
Timer 0/ Timer 1	TCON TH0 TH1 TL0 TL1 TMOD	Timer 0/1 Control Register Timer 0, High Byte Timer 1, High Byte Timer 0, Low Byte Timer 1, Low Byte Timer Mode Register	**88H** 1) 8CH 8DH 8AH 8BH 89H	00H 00H 00H 00H 00H 00H
Timer 2	T2CON T2MOD RC2H RC2L TH2 TL2 AUXR0 4)	Timer 2 Control Register Timer 2 Mode Register Timer 2 Reload Capture Reg., High Byte Timer 2 Reload Capture Reg., Low Byte Timer 2, High Byte Timer 2, Low Byte Aux. Register 0	**C8H** 1) C9H CBH CAH CDH CCH 8EH	00H 00H 00H 00H 00H 00H XXXXXXX0B 2)
Power Saving Modes	PCON 3)	Power Control Register	87H	0XXX0000B 2)

1) Bit-addressable Special Function register

2) X means that the value is indeterminate and the location is reserved

3) This special function register is listed repeatedly since some bit of it also belong to other functional blocks

4) The AUXR0 is in the GMS9XX54/56/58 only.

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Table 3. Contents of SFRs, SFRs in Numeric Order

Address	Register	Bit 7	6	5	4	3	2	1	0
80H	P0								
81H	SP								
82H	DPL								
83H	DPH								
87H	PCON	SMOD	-	-	-	GF1	GF0	PDE	IDLE
88H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89H	TMOD	GATE	C/$\overline{T}$	M1	MT	GATE	C/$\overline{T}$	M1	M0
8AH	TL0								
8BH	TL1								
8CH	TH0								
8DH	TH1								
8EH	AUXR0 †	-	-	-	-	-	-	-	A0 †
90H	P1								
98H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99H	SBUF								
A0H	P2								
A8H	IE	EA	-	ET2	ES	ET1	EX1	ET0	EX0
B0H	P3								
B8H	IP	-	-	PT2	PS	PT1	PX1	PT0	PX0

† indicates resident in the GMS9XX54/56/58, not in 9XX51/52.

								SFR bit and byte addressable

	SFR not bit addressable

- : this bit location is reserved

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Table 3. Contents of SFRs, SFRs in Numeric Order (cont'd)

Address	Register	Bit 7	6	5	4	3	2	1	0
C8H	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
C9H	T2MOD	-	-	-	-	-	-	T2OE †	DCEN
CAH	RC2L								
CBH	RC2H								
CCH	TL2								
CDH	TH2								
D0H	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
E0H	ACC								
F0H	B								

† indicates resident in the GMS9XX54/56/58, not in 9XX51/52.

								SFR bit and byte addressable
								SFR not bit addressable

- : this bit location is reserved

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TIMER / COUNTER 0 AND 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in Table 4:

Table 4. Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		Gate	C/$\overline{T}$	M1	M0	internal	external (Max.)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	f_{OSC} ÷(12×32)	f_{OSC} ÷(24×32)
1	16-bit timer/counter	X	X	0	1	f_{OSC} ÷12	f_{OSC} ÷24
2	8-bit timer/counter with 8-bit auto-reload	X	X	1	0	f_{OSC} ÷12	f_{OSC} ÷24
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	f_{OSC} ÷12	f_{OSC} ÷24

In the "timer" function (C/$\overline{T}$ = "0") the register is incremented every machine cycle. Therefore the count rate is f_{OSC}/12.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is f_{OSC}/24. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. Figure 2 illustrates the input clock logic.

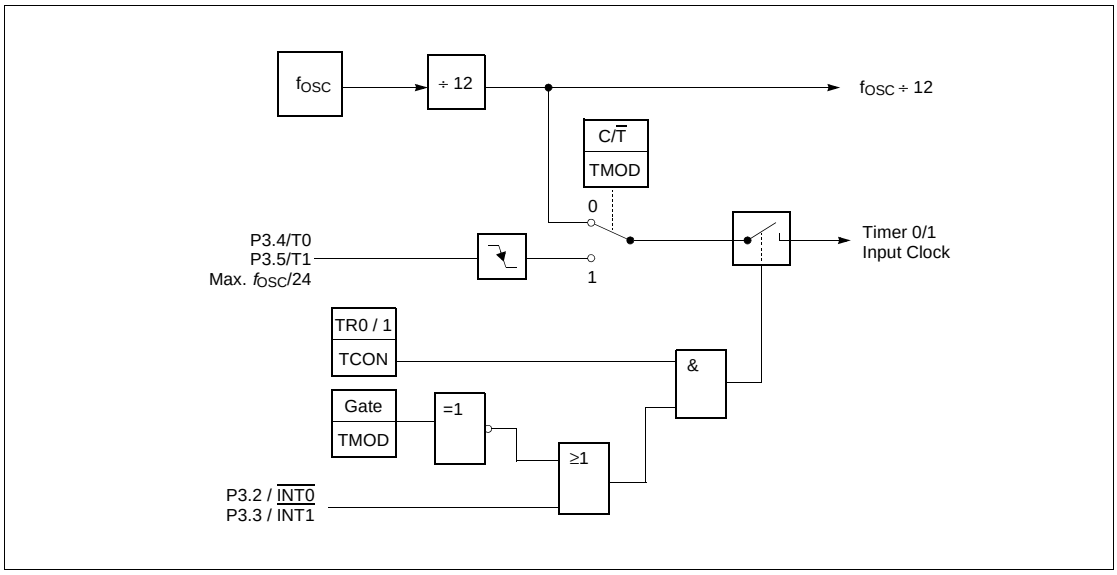

Figure 2. Timer/Counter 0 and 1 Input Clock Logic

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TIMER 2

Timer 2 is a 16-bit timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/$\overline{T2}$ (T2CON.1). It has three operating modes as shown in Table 5.

Table 5. Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	RCLK or TCLK	CP/$\overline{RL2}$	TR2	DCEN	EXEN2			internal	external (P1.0/T2)
16-bit Auto-Reload	0	0	1	0	0	X	reload upon overflow	$f_{OSC} \div 12$	Max. $f_{OSC} \div 24$
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Capture	0	1	1	X	0	X	16 bit Timer/ Counter (only up-counting)	$f_{OSC} \div 12$	Max. $f_{OSC} \div 24$
	0	1	1	X	1	↓	capture TH2,TL2 → RC2H,RC2L		
Baud Rate Generator	1	X	1	X	0	X	no overflow interrupt request (TF2)	$f_{OSC} \div 12$	Max. $f_{OSC} \div 24$
	1	X	1	X	1	↓	extra external interrupt ("Timer 2")		
Off	X	X	0	X	X	X	Timer 2 stops	-	-

Note: ↓ = ↘ falling edge

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SERIAL INTERFACE (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in Table 6. The possible baud rates can be calculated using the formulas given in Table 7.

Table 6. USART Operating Modes

Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$\frac{f_{OSC}}{12}$	Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	$\frac{f_{OSC}}{32}$ or $\frac{f_{OSC}}{64}$	9-bit UART 11 bits are transmitted (TxD) or received (RxD)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7. Formulas for Calculating Baud rates

Baud Rate derived from	Interface Mode	Baudrate
Oscillator	0	$\frac{f_{OSC}}{12}$
	2	$\frac{2^{SMOD}}{64} \times f_{OSC}$
Timer 1 (16-bit timer) (8-bit timer with 8-bit auto reload)	1,3	$\frac{2^{SMOD}}{32} \times (Timer\ 1\ overflow)$
	1,3	$\frac{2^{SMOD}}{32} \times \frac{f_{OSC}}{12 \times [256 - (TH1)]}$
Timer 2	1,3	$\frac{f_{OSC}}{32 \times [65536 - (RC2H, RC2L)]}$

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INTERRUPT SYSTEM

The GMS90 series provides 5 (4K bytes ROM version) or 6 (above 8K bytes ROM version) interrupt sources with two priority levels. Figure 3 gives a general overview of the interrupt sources and illustrates the request and control flags.

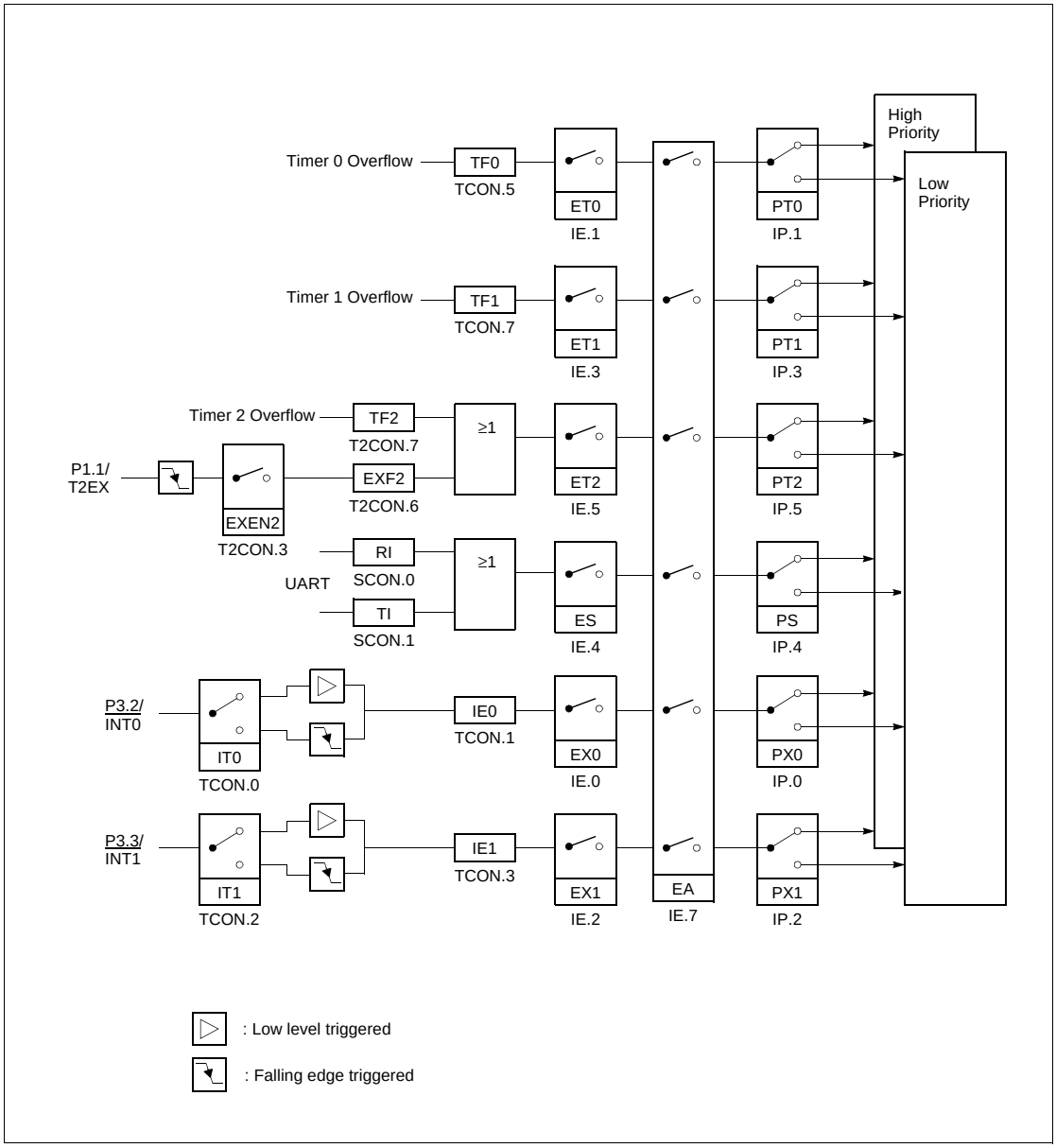

Figure 3. Interrupt Request Sources

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Table 8. Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vectors	Vector Address
RESET	RESET	0000H
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in Table 9.

Table 9. Interrupt Priority-Within-Level

Interrupt Source		Priority
External Interrupt 0	IE0	High
Timer 0 Interrupt	TF0	↓
External Interrupt 1	IE1	↓
Timer 1 Interrupt	TF1	↓
Serial Channel	RI + TI	↓
Timer 2 Interrupt	TF2 + EXF2	Low

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Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. Table 10 gives a general overview of the power saving modes.

Table 10. Power Saving Modes Overview

Mode	Entering Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H	- Enabled interrupt - Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power-Down mode	ORL PCON, #02H	Hardware Reset	Oscillator is stopped, contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR contents).

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Ambient temperature under bias (T_A)..... -40 to + 85 °C

Storage temperature (T_{ST})..... -65 to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... -0.5V to 6.5V

Voltage on any pin with respect to ground (V_{SS}) .....-0.5V to V_{CC} + 0.5V

Input current on any pin during overload condition.....-15mA to +15mA

Absolute sum of all input currents during overload condition.....|100mA|

Power dissipation 1.5W

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.*

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DC Characteristics

DC Characteristics for GMS90C31/32, GMS90C51/52/54/56/58

V_{CC}= 5V + 10%, -15%; V_{SS}=0V; T_A= 0°C to 70°C

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	-0.5	$0.2V_{CC}$ - 0.1	V	-
Input low voltage ($\overline{EA}$)	V_{IL1}	-0.5	$0.2V_{CC}$ - 0.3	V	-
Input low voltage (RESET)	V_{IL2}	-0.5	$0.2V_{CC}$ + 0.1	V	-
Input high voltage (except XTAL1, $\overline{EA}$, RESET)	V_{IH}	$0.2V_{CC}$ + 0.9	V_{CC} + 0.5	V	-
Input high voltage to XTAL1	V_{IH1}	$0.7V_{CC}$	V_{CC} + 0.5	V	-
Input high voltage to $\overline{EA}$, RESET	V_{IH2}	$0.6V_{CC}$	V_{CC} + 0.5	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45	V	I_{OL}= 1.6mA [1)]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	-	0.45	V	I_{OL}= 3.2mA [1)]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 $0.9V_{CC}$	-	V	I_{OH}= -80µA I_{OH}= -10µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.4 $0.9V_{CC}$	-	V	I_{OH}= -800µA [2)] I_{OH}= -80µA [2)]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	µA	V_{IN}= 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	µA	V_{IN}= 2.0V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	-	±1	µA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	f_C= 1MHz T_A= 25°C
Power supply current:					
Active mode, 12MHz [3)]	I_{CC}	-	21	mA	V_{CC}= 5V [4)]
Idle mode, 12MHz [3)]	I_{CC}	-	4.8	mA	V_{CC}= 5V [5)]
Active mode, 24 MHz [3)]	I_{CC}	-	36.2	mA	V_{CC}= 5V [4)]
Idle mode, 24MHz [3)]	I_{CC}	-	8.2	mA	V_{CC}= 5V [5)]
Active mode, 40 MHz [3)]	I_{CC}	-	58.5	mA	V_{CC}= 5V [4)]
Idle mode, 40 MHz [3)]	I_{CC}	-	12.5	mA	V_{CC}= 5V [5)]
Power Down Mode [3)]	I_{PD}	-	50	µA	V_{CC}= 5V [6)]

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1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading: > 50pF at 3.3V, > 100pF at 5V), the noise pulse on ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address lines are stabilizing.
3) I_{CC} Max at other frequencies is given by:
   active mode: $I_{CC} = 1.27 \times f_{OSC} + 5.73$
   idle mode: $I_{CC} = 0.28 \times f_{OSC} + 1.45$ (except OTP devices)
   where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5V.
4) I_{CC} (active mode) is measured with:
   XTAL1 driven with t_{CLCH}, t_{CHCL} = 5ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; XTAL2 = N.C.;
   $\overline{EA}$ = Port0 = RESET = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1mA).
5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
   XTAL1 driven with t_{CLCH}, t_{CHCL} = 5ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; XTAL2 = N.C.;
   RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;
6) I_{PD} (Power Down Mode) is measured under following conditions:
   $\overline{EA}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; all other pins are disconnected.

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DC Characteristics for GMS97C51/52/54/56/58 (H)

V_{CC}= 5V + 10%, -15%; V_{SS}=0V; T_A= 0°C to 70°C

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	-0.5	$0.2V_{CC}$ - 0.1	V	-
Input low voltage ($\overline{EA}$)	V_{IL1}	-0.5	$0.2V_{CC}$ - 0.3	V	-
Input low voltage (RESET)	V_{IL2}	-0.5	$0.2V_{CC}$ + 0.1	V	-
Input high voltage (except XTAL1, $\overline{EA}$, RESET)	V_{IH}	$0.2V_{CC}$ + 0.9	V_{CC} + 0.5	V	-
Input high voltage to XTAL1	V_{IH1}	$0.7V_{CC}$	V_{CC} + 0.5	V	-
Input high voltage to $\overline{EA}$, RESET	V_{IH2}	$0.6V_{CC}$	V_{CC} + 0.5	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45	V	I_{OL}= 1.6mA 1)
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	-	0.45	V	I_{OL}= 3.2mA 1)
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 $0.9V_{CC}$	-	V	I_{OH}= -80µA I_{OH}= -10µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.4 $0.9V_{CC}$	-	V	I_{OH}= -800µA 2) I_{OH}= -80µA 2)
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	µA	V_{IN}= 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	µA	V_{IN}= 2.0V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	-	±1	µA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	f_C= 1MHz T_A= 25°C
Power supply current:					
Active mode, 12MHz 3)	I_{CC}	-	21	mA	V_{CC}= 5V 4)
Idle mode, 12MHz 3)	I_{CC}	-	4.8	mA	V_{CC}= 5V 5)
Active mode, 24 MHz 3)	I_{CC}	-	36.2	mA	V_{CC}= 5V 4)
Idle mode, 24MHz 3)	I_{CC}	-	8.2	mA	V_{CC}= 5V 5)
Active mode, 33 MHz 3)	I_{CC}	-	45	mA	V_{CC}= 5V 4)
Idle mode, 33 MHz 3)	I_{CC}	-	10	mA	V_{CC}= 5V 5)
Power Down Mode 3)	I_{PD}	-	50	µA	V_{CC}= 5V 6)

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DC Characteristics for GMS90L31/32, GMS90L51/52/54/56/58

V_{CC}= 3.3V + 0.3V, -0.6V; V_{SS}=0V; T_A= 0°C to 70°C

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Input low voltage	V_{IL}	-0.5	0.8	V	-
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45 0.30	V	I_{OL}= 1.6mA 1) I_{OL}= 100µA 1)
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	-	0.45 0.30	V	I_{OL}= 3.2mA 1) I_{OL}= 200µA 1)
Output high voltage (ports 1, 2, 3)	V_{OH}	2.0 0.9V_{CC}	-	V	I_{OH}= -20µA I_{OH}= -10µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.0 0.9V_{CC}	-	V	I_{OH}= -800µA 2) I_{OH}= -80µA 2)
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-1	-50	µA	V_{IN}= 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-25	-250	µA	V_{IN}= 2.0V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	-	±1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	-	10	pF	f_C= 1MHz T_A= 25°C
Power supply current: Active mode, 16 MHz 3) Idle mode, 16MHz 3) Power Down Mode 3)	 I_{CC} I_{CC} I_{PD}	 - - -	 15 5 10	 mA mA µA	 V_{CC}= 3.6V 4) V_{CC}= 2.6V 5) V_{CC}=2~ 5.5V 6)

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DC Characteristics for GMS97L51/52/54/56/58

V_{CC}= 3.3V + 0.3V, -0.6V; V_{SS}=0V; T_A= 0°C to 70°C

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	max.		
Input low voltage	V_{IL}	-0.5	0.8	V	-
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45 0.30	V	I_{OL}= 1.6mA 1) I_{OL}= 100µA 1)
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	-	0.45 0.30	V	I_{OL}= 3.2mA 1) I_{OL}= 200µA 1)
Output high voltage (ports 1, 2, 3)	V_{OH}	2.0 0.9V_{CC}	-	V	I_{OH}= -20µA I_{OH}= -10µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.0 0.9V_{CC}	-	V	I_{OH}= -800µA 2) I_{OH}= -80µA 2)
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-1	-50	µA	V_{IN}= 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-25	-250	µA	V_{IN}= 2.0V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	-	±1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	-	10	pF	f_C= 1MHz T_A= 25°C
Power supply current: Active mode, 12MHz 3) Idle mode, 12MHz 3) Power Down Mode 3)	 I_{CC} I_{CC} I_{PD}	 - - -	 15 5 10	 mA mA µA	 V_{CC}= 3.6V 4) V_{CC}= 2.6V 5) V_{CC}=2~ 5.5V 6)

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AC Characteristics

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a 't' (stand for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,
t_{AVLL} = Time from Address Valid to ALE Low
t_{LLPL} = Time from ALE Low to $\overline{PSEN}$ Low

AC Characteristics for GMS90 series (12MHz version)

V_{CC}= 5V : V_{CC}= 5V + 10%, – 15%; V_{SS}= 0V; T_A= 0°C to 70°C
(C_L for port 0. ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all other outputs = 80pF)

V_{CC}= 3.3V : V_{CC}= 3.3V + 0.3V, – 0.6V; V_{SS}= 0V; T_A= 0°C to 70°C
(C_L for port 0. ALE and $\overline{PSEN}$ outputs = 50pF; C_L for all other outputs = 50pF)

Variable clock : Vcc = 5V : $1/t_{CLCL}$ = 3.5 MHz to 12 MHz
Vcc = 3.3V : $1/t_{CLCL}$ = 1 MHz to 12 MHz

External Program Memory Characteristics

Parameter	Symbol	12 MHz Oscillator		Variable Oscillator $1/t_{CLCL}$ = 3.5 to 12MHz		Unit
		Min.	Max.	Min.	Max.	
ALE pulse width	t_{LHLL}	127	-	$2t_{CLCL}$-40	-	ns
Address setup to ALE	t_{AVLL}	43	-	t_{CLCL}-40	-	ns
Address hold after ALE	t_{LLAX}	30	-	t_{CLCL}-53	-	ns
ALE low to valid instruction in	t_{LLIV}	-	233	-	$4t_{CLCL}$-100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	-	t_{CLCL}-25	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	-	$3t_{CLCL}$-35	-	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	-	150	-	$3t_{CLCL}$-100	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} †	-	63	-	t_{CLCL}-20	ns
Address valid after $\overline{PSEN}$	t_{PXAV} †	75	-	t_{CLCL}-8	-	ns

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Parameter	Symbol	12 MHz Oscillator		Variable Oscillator $1/t_{CLCL}$ = 3.5 to 12MHz		Unit
		Min.	Max.	Min.	Max.	
Address to valid instruction in	t_{AVIV}	-	302	-	$5t_{CLCL}$-115	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	-	0	-	ns

† Interfacing the GMS90 series to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

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AC Characteristics for GMS90 series (12MHz)

External Data Memory Characteristics

Parameter	Symbol	12 MHz Oscillator		Variable Oscillator $1/t_{CLCL}$ = 3.5 to 12MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	-	$6t_{CLCL}$-100	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	-	$6t_{CLCL}$-100	-	ns
Address hold after ALE	t_{LLAX2}	53	-	t_{CLCL}-30	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	252	-	$5t_{CLCL}$-165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	97	-	$2t_{CLCL}$-70	ns
ALE to valid data in	t_{LLDV}	-	517	-	$8t_{CLCL}$-150	ns
Address to valid data in	t_{AVDV}	-	585	-	$9t_{CLCL}$-165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	-	$4t_{CLCL}$-130	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	-	t_{CLCL}-50	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	-	$7t_{CLCL}$-150	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	-	t_{CLCL}-50	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

Advance Information (12MHz)

External Clock Drive

Parameter	Symbol	Variable Oscillator (Freq. = 3.5 to 12MHz)		Unit
		Min.	Max.	
Oscillator period (V_{CC}=5V) Oscillator period (V_{CC}=3.3V)	t_{CLCL} t_{CLCL}	83.3 83.3	285.7 1	ns
High time	t_{CHCX}	20	t_{CLCL} - t_{CLCX}	ns
Low time	t_{CLCX}	20	t_{CLCL} - t_{CHCX}	ns
Rise time	t_{CLCH}	-	20	ns
Fall time	t_{CHCL}	-	20	ns

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AC Characteristics for GMS90 series (16MHz version)

V_{CC}= 3.3V + 0.3V, –0.6V; V_{SS}= 0V; T_A= 0°C to 70°C
(C_L for port 0. ALE and $\overline{PSEN}$ outputs = 50pF; C_L for all other outputs = 50pF)

External Program Memory Characteristics

Parameter	Symbol	16 MHz Oscillator		Variable Oscillator $1/t_{CLCL}$ = 3.5 to 16MHz		Unit
		Min.	Max.	Min.	Max.	
ALE pulse width	t_{LHLL}	85	-	$2t_{CLCL}$-40	-	ns
Address setup to ALE	t_{AVLL}	23	-	t_{CLCL}-40	-	ns
Address hold after ALE	t_{LLAX}	23	-	t_{CLCL}-40	-	ns
ALE low to valid instruction in	t_{LLIV}	-	150	-	$4t_{CLCL}$-100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	38	-	t_{CLCL}-25	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	153	-	$3t_{CLCL}$-35	-	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	-	88	-	$3t_{CLCL}$-100	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} †	-	43	-	t_{CLCL}-20	ns
Address valid after $\overline{PSEN}$	t_{PXAV} †	55	-	t_{CLCL}-8	-	ns
Address to valid instruction in	t_{AVIV}	-	198	-	$5t_{CLCL}$-115	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	-	0	-	ns

† Interfacing the GMS90 series to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

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AC Characteristics for GMS90 series (16MHz)

External Data Memory Characteristics

Parameter	Symbol	16 MHz Oscillator		Variable Oscillator $1/t_{CLCL}$ = 3.5 to 16MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{RD}$ pulse width	t_{RLRH}	275	-	$6t_{CLCL}$-100	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	275	-	$6t_{CLCL}$-100	-	ns
Address hold after ALE	t_{LLAX2}	23	-	t_{CLCL}-40	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	183	-	$5t_{CLCL}$-130	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	75	-	$2t_{CLCL}$-50	ns
ALE to valid data in	t_{LLDV}	-	350	-	$8t_{CLCL}$-150	ns
Address to valid data in	t_{AVDV}	-	398	-	$9t_{CLCL}$-165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	138	238	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	120	-	$4t_{CLCL}$-130	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	28	97	t_{CLCL}–35	t_{CLCL}+35	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	13	-	t_{CLCL}–50	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	288	-	$7t_{CLCL}$-150	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	23	-	t_{CLCL}–40	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

Advance Information (16MHz)

External Clock Drive

Parameter	Symbol	Variable Oscillator (Freq. = 3.5 to 16MHz)		Unit
		Min.	Max.	
Oscillator period	t_{CLCL}	62.5	285.7	ns
High time	t_{CHCX}	17	t_{CLCL} - t_{CLCX}	ns
Low time	t_{CLCX}	17	t_{CLCL} - t_{CHCX}	ns
Rise time	t_{CLCH}	-	17	ns
Fall time	t_{CHCL}	-	17	ns

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AC Characteristics for GMS90 series (24MHz version)

V_{CC}= 5V + 10%, –15%; V_{SS}= 0V; T_A= 0°C to 70°C
(C_L for port 0. ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all other outputs = 80pF)

External Program Memory Characteristics

Parameter	Symbol	24 MHz Oscillator		Variable Oscillator $1/t_{CLCL}$ = 3.5 to 24MHz		Unit
		Min.	Max.	Min.	Max.	
ALE pulse width	t_{LHLL}	43	-	$2t_{CLCL}$-40	-	ns
Address setup to ALE	t_{AVLL}	17	-	t_{CLCL}-25	-	ns
Address hold after ALE	t_{LLAX}	17	-	t_{CLCL}-25	-	ns
ALE low to valid instruction in	t_{LLIV}	-	80	-	$4t_{CLCL}$-87	ns
ALE to $\overline{PSEN}$	t_{LLPL}	22	-	t_{CLCL}-20	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	95	-	$3t_{CLCL}$-30	-	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	-	60	-	$3t_{CLCL}$-65	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} †	-	32	-	t_{CLCL}-10	ns
Address valid after $\overline{PSEN}$	t_{PXAV} †	37	-	t_{CLCL}-5	-	ns
Address to valid instruction in	t_{AVIV}	-	148	-	$5t_{CLCL}$-60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	-	0	-	ns

† Interfacing the GMS90 series to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

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AC Characteristics for GMS90 series (24MHz)

External Data Memory Characteristics

Parameter	Symbol	24 MHz Oscillator		Variable Oscillator $1/t_{CLCL}$ = 3.5 to 24MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{RD}$ pulse width	t_{RLRH}	180	-	$6t_{CLCL}$-70	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	180	-	$6t_{CLCL}$-70	-	ns
Address hold after ALE	t_{LLAX2}	15	-	t_{CLCL}-27	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	118	-	$5t_{CLCL}$-90	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	63	-	$2t_{CLCL}$-20	ns
ALE to valid data in	t_{LLDV}	-	200	-	$8t_{CLCL}$-133	ns
Address to valid data in	t_{AVDV}	-	220	-	$9t_{CLCL}$-155	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	75	175	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	67	-	$4t_{CLCL}$-97	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	17	67	t_{CLCL}-25	t_{CLCL}+25	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	-	t_{CLCL}-37	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	170	-	$7t_{CLCL}$-122	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	15	-	t_{CLCL}-27	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

Advance Information (24MHz)

External Clock Drive

Parameter	Symbol	Variable Oscillator (Freq. = 3.5 to 24MHz)		Unit
		Min.	Max.	
Oscillator period	t_{CLCL}	41.7	285.7	ns
High time	t_{CHCX}	12	t_{CLCL} - t_{CLCX}	ns
Low time	t_{CLCX}	12	t_{CLCL} - t_{CHCX}	ns
Rise time	t_{CLCH}	-	12	ns
Fall time	t_{CHCL}	-	12	ns

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AC Characteristics for GMS90 series (33MHz version)

V_{CC}= 5V + 10%, –15%; V_{SS}= 0V; T_A= 0°C to 70°C
(C_L for port 0. ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all other outputs = 80pF)

External Program Memory Characteristics

Parameter	Symbol	33 MHz Oscillator		Variable Oscillator $1/t_{CLCL}$ = 3.5 to 33MHz		Unit
		Min.	Max.	Min.	Max.	
ALE pulse width	t_{LHLL}	40	-	$2t_{CLCL}$-20	-	ns
Address setup to ALE	t_{AVLL}	10	-	t_{CLCL}-20	-	ns
Address hold after ALE	t_{LLAX}	10	-	t_{CLCL}-20	-	ns
ALE low to valid instruction in	t_{LLIV}	-	56	-	$4t_{CLCL}$-65	ns
ALE to $\overline{PSEN}$	t_{LLPL}	15	-	t_{CLCL}-15	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	80	-	$3t_{CLCL}$-20	-	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	-	35	-	$3t_{CLCL}$-55	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} †	-	20	-	t_{CLCL}-10	ns
Address valid after $\overline{PSEN}$	t_{PXAV} †	25	-	t_{CLCL}-5	-	ns
Address to valid instruction in	t_{AVIV}	-	91	-	$5t_{CLCL}$-60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	-	0	-	ns

† Interfacing the GMS90 series to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

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AC Characteristics for GMS90 series (33MHz)

External Data Memory Characteristics

Parameter	Symbol	33 MHz Oscillator		Variable Oscillator $1/t_{CLCL}$ = 3.5 to 33MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{RD}$ pulse width	t_{RLRH}	132	-	$6t_{CLCL}$-50	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	132	-	$6t_{CLCL}$-50	-	ns
Address hold after ALE	t_{LLAX2}	10	-	t_{CLCL}-20	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	81	-	$5t_{CLCL}$-70	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	46	-	$2t_{CLCL}$-15	ns
ALE to valid data in	t_{LLDV}	-	153	-	$8t_{CLCL}$-90	ns
Address to valid data in	t_{AVDV}	-	183	-	$9t_{CLCL}$-90	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	71	111	$3t_{CLCL}$-20	$3t_{CLCL}$+20	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	66	-	$4t_{CLCL}$-55	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	t_{CLCL}-20	t_{CLCL}+20	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	-	t_{CLCL}-25	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	142	-	$7t_{CLCL}$-70	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	10	-	t_{CLCL}-20	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

Advance Information (33MHz)

External Clock Drive

Parameter	Symbol	Variable Oscillator (Freq. = 3.5 to 24MHz)		Unit
		Min.	Max.	
Oscillator period	t_{CLCL}	30.3	285.7	ns
High time	t_{CHCX}	11.5	t_{CLCL} - t_{CLCX}	ns
Low time	t_{CLCX}	11.5	t_{CLCL} - t_{CHCX}	ns
Rise time	t_{CLCH}	-	5	ns
Fall time	t_{CHCL}	-	5	ns

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AC Characteristics for GMS90 series (40MHz version)

V_{CC}= 5V + 10%, – 15%; V_{SS}= 0V; T_A= 0°C to 70°C
(C_L for port 0. ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all other outputs = 80pF)

External Program Memory Characteristics

Parameter	Symbol	40 MHz Oscillator		Variable Oscillator $1/t_{CLCL}$ = 3.5 to 40MHz		Unit
		Min.	Max.	Min.	Max.	
ALE pulse width	t_{LHLL}	35	-	$2t_{CLCL}$–15	-	ns
Address setup to ALE	t_{AVLL}	10	-	t_{CLCL}–15	-	ns
Address hold after ALE	t_{LLAX}	10	-	t_{CLCL}–15	-	ns
ALE low to valid instruction in	t_{LLIV}	-	55	-	$4t_{CLCL}$–45	ns
ALE to $\overline{PSEN}$	t_{LLPL}	10	-	t_{CLCL}–15	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	60	-	$3t_{CLCL}$–15	-	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	-	25	-	$3t_{CLCL}$–50	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} †	-	15	-	t_{CLCL}–10	ns
Address valid after $\overline{PSEN}$	t_{PXAV} †	20	-	t_{CLCL}–5	-	ns
Address to valid instruction in	t_{AVIV}	-	65	-	$5t_{CLCL}$–60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	5	-	5	-	ns

† Interfacing the GMS90 series to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

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AC Characteristics for GMS90 series (40MHz)

External Data Memory Characteristics

Parameter	Symbol	at 40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 to 40MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	-	$6t_{CLCL}$-30	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	-	$6t_{CLCL}$-30	-	ns
Address hold after ALE	t_{LLAX2}	10	-	t_{CLCL}-15	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	75	-	$5t_{CLCL}$-50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	38	-	$2t_{CLCL}$-12	ns
ALE to valid data in	t_{LLDV}	-	150	-	$8t_{CLCL}$-50	ns
Address to valid data in	t_{AVDV}	-	150	-	$9t_{CLCL}$-75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	$3t_{CLCL}$-15	$3t_{CLCL}$+15	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	-	$4t_{CLCL}$-30	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	t_{CLCL}-15	t_{CLCL}+15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	-	t_{CLCL}-20	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	-	$7t_{CLCL}$-50	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	-	t_{CLCL}-20	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

Advance Information (40MHz)

External Clock Drive

Parameter	Symbol	Variable Oscillator (Freq. = 3.5 to 40MHz)		Unit
		Min.	Max.	
Oscillator period	t_{CLCL}	25	285.7	ns
High time	t_{CHCX}	10	t_{CLCL} - t_{CLCX}	ns
Low time	t_{CLCX}	10	t_{CLCL} - t_{CHCX}	ns
Rise time	t_{CLCH}	-	10	ns
Fall time	t_{CHCL}	-	10	ns

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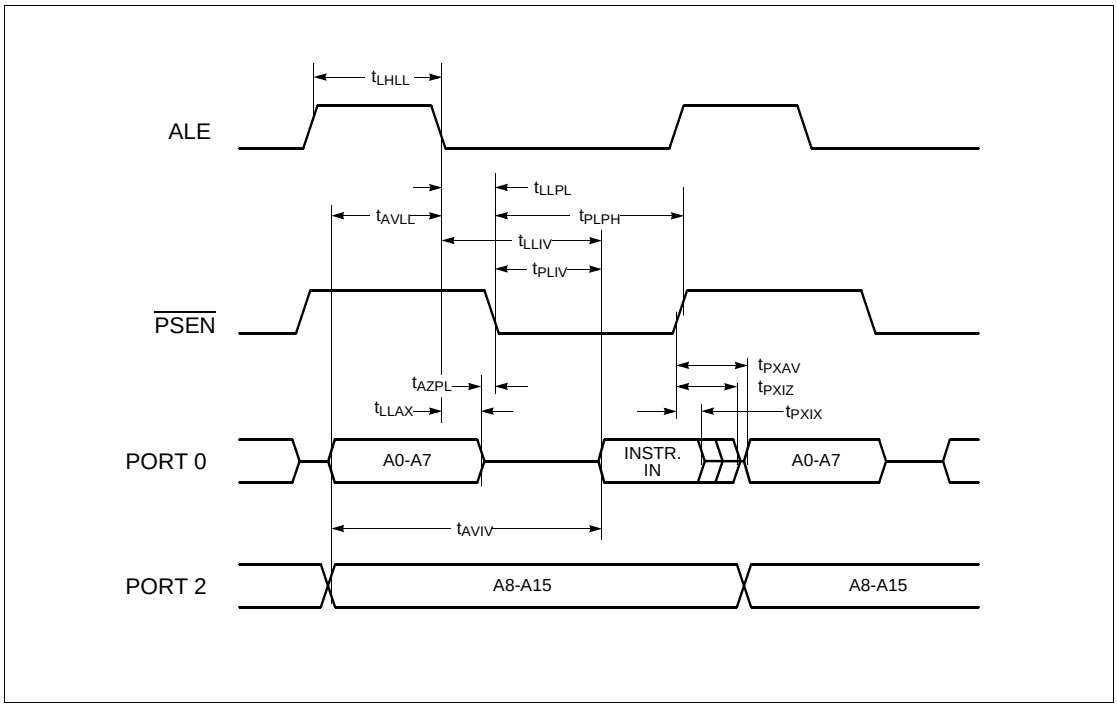

Figure 4. External Program Memory Read Cycle

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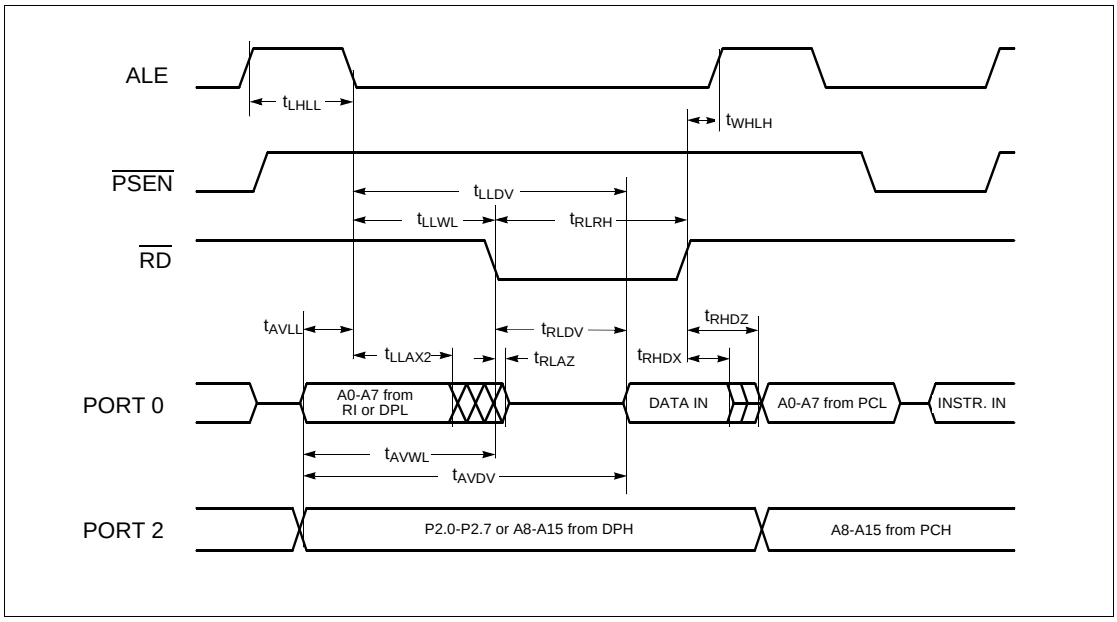

Figure 5. External Data Memory Read Cycle

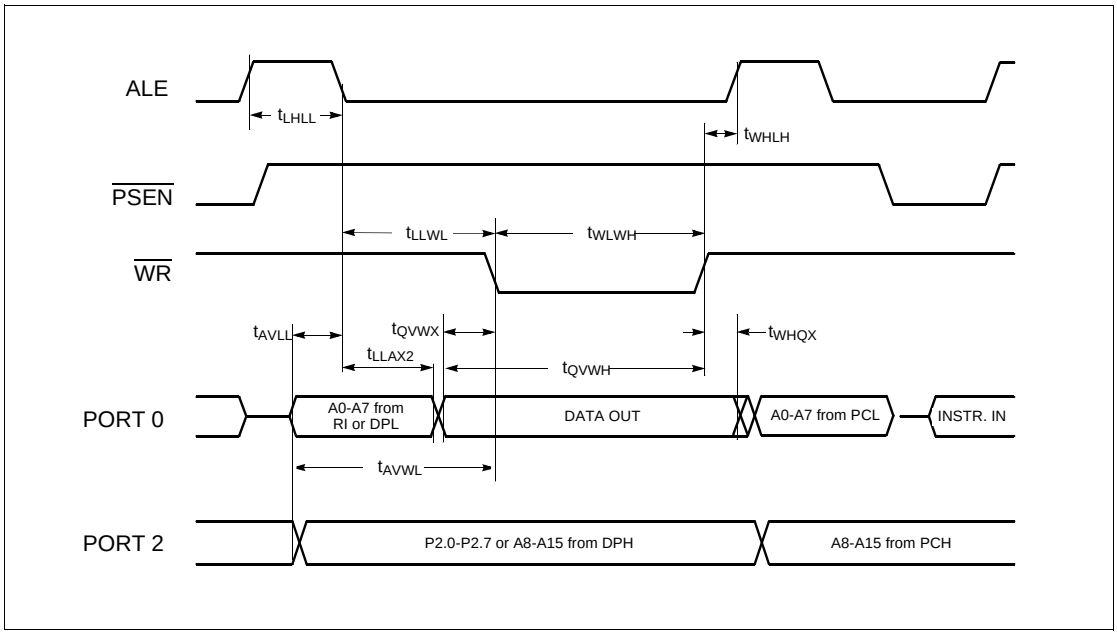

Figure 6. External Data Memory Write Cycle

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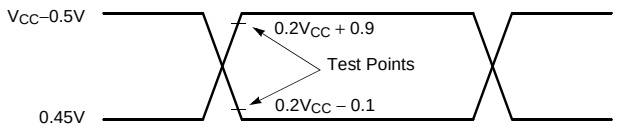
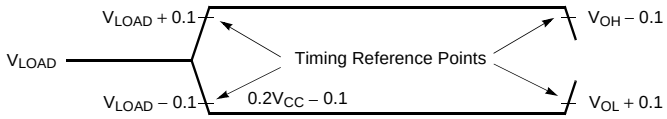


AC Inputs during testing are driven at V_{CC}–0.5V for a logic ‘1’ and 0.45V for a logic ‘0’.
Timing measurements are made a V_{IHmin} for a logic ‘1’ and V_{ILmax} for a logic ‘0’.

Figure 7. AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100mV change from load voltage occurs and begins to float when a 100mV change from the loaded V_{OH} / V_{OL} level occurs.
I_{OL} / I_{OH} ≥ 20mA.

Figure 8. Float Waveforms

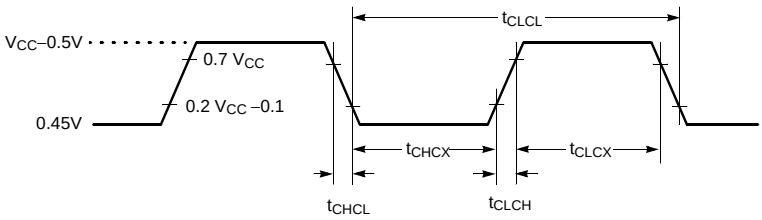


Figure 9. External Clock Cycle

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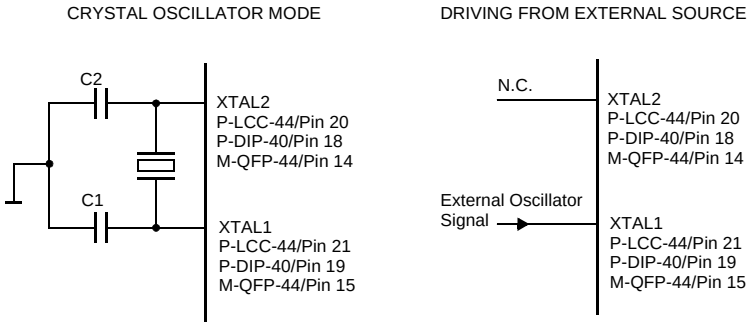
OSCILLATOR CIRCUIT



C1, C2 = 30pF ±10pF for Crystals

For Ceramic Resonators, contact resonator manufacturer.

Figure 10. Recommended Oscillator Circuits

Oscillation circuit is designed to be used either with a ceramic resonator or crystal oscillator. Since each crystal and ceramic resonator have their own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

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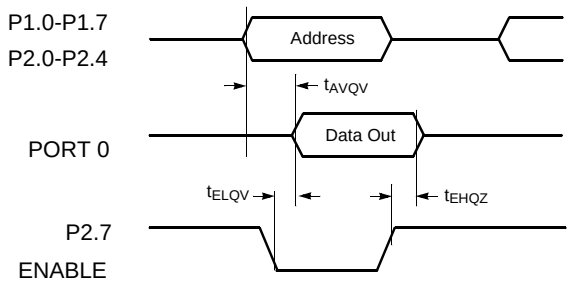
OTP ROM Verification Characteristics

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
Address to valid data	t_{AVQV}	-	$48t_{CLCL}$	
ENABLE to valid data	t_{CLCL}	-	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0-P1.7 = A0-A7
P2.0-P2.5 = A8-A13
P3.4 = A14
Data: P0.0-P0.7 = D0-D7

Input: P2.6-P2.7, $\overline{PSEN} = V_{SS}$
$\overline{ALE} = V_{IH}$
$\overline{EA}$, RESET = V_{IH2}

Figure 11. OTP ROM Verification Mode 1

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EPROM CHARACTERISTICS

The GMS97C5X, 97L5X are programmed by using a modified Quick-Pulse Programming^{TM} algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses. The GMS97C5X, 97L5X contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an manufactured by LGS. Table 11 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figure 12 and Figure 13. Figure 14 show the circuit configuration for normal program memory verification.

Reading the Signature Bytes :

The GMS97X51/52 signature bytes in locations 030_H and 031_H, the GMS97X54/56/58 signature bytes in locations 030_H and 060_H. To read these bytes follow the procedure for EPROM verify, except that P3.6 and P3.7 need to be pulled to a logic low.

The values are:

Device	Location	Contents	Remarks
GMS97X51	30_H 31_H	$E0_H$ 73_H	Manufacturer ID Device ID
GMS97X52	30_H 31_H	$E0_H$ 71_H	Manufacturer ID Device ID
GMS97X54	30_H 60_H	$E0_H$ 54_H	Manufacturer ID Device ID
GMS97X56	30_H 60_H	$E0_H$ 56_H	Manufacturer ID Device ID
GMS97X58	30_H 60_H	$E0_H$ 58_H	Manufacturer ID Device ID

Quick-pulse programming

The setup for microcontroller quick-pulse programming is shown in Figure 13. Note that the GMS97C5X, 97L5X is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 12. The code byte to be programmed into that location is applied to port 0, RST, $\overline{PSEN}$ and pins of port 2 and 3 in Table 11 are held at the "Program Code Data" levels indicated in Table 11. The ALE/$\overline{PROG}$ is pulsed low 25 times(10 times for 97X54/56/58) as shown Figure 13.

To program the encryption table, repeat the 25 pulses (10 pulses for 97X54/56/58) programming sequence for addresses 0 through $1F_H$($3F_H$ for 97X54/56/58), using the "Program Encryption Table" levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 25 pulses (10 pulses for 97X54/56/58) programming sequence using the "Pgm Security Bit" levels after one security bit is programmed, further programming of the code memory and

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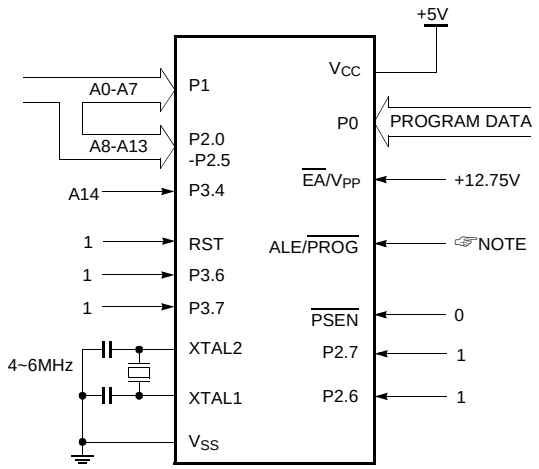
encryption table is disabled. However, the other security bit can still be programmed. Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free glitches and overshoot.



NOTE:
GMS97X51/52: 100µs × 25 pulses to GND
GMS97X54/56/58: 100µs × 10 pulses to GND

Figure 12. Programming Configuration

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory location to be read is applied to ports 1 and 2 as shown in Figure 15. The other pins are held at the "Verify Code Data" levels indicated in Table 11. The contents of the address location will be emitted on port 0 for this operation. If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

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Program Memory Lock Bits

The two-level Program Lock system consists of 2 Lock bits and a 32-byte (64-byte for GMS97X54/56/58) Encryption Array which are used to protect the program memory against software piracy.

Lock Bit Protection Modes

Mode	LB1	LB2	Protection Type
1	U	U	No program lock features
2	P	U	Further programming of the EPROM is disabled
3	P	P	Same as mode 2, also verify is disabled

U: unprogrammed, P: programmed

Encryption Array:

Within the EPROM array are 32 bytes (64 bytes for GMS97X54/56/58) of Encryption Array that are initially unprogrammed (all 1s). Every time that a byte is addressed during a verify, address lines are used to select a byte of the Encryption array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an Encrypted Verify byte.

The algorithm, with the array in the unprogrammed state (all 1s), will return the code in its original, unmodified form, It is recommended that whenever the Encryption Array is used, at least one of the Lock Bits be programmed as well.

Program / Verify algorithms

Any algorithm in agreement with the conditions listed in Table 11, and which satisfies the timing specifications is suitable.

Table 11. EPROM programming modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read Signature	1	0	1	1	0	0	0	0
Program Code Data	1	0	0	V_{PP}	1	0	1	1
Verify Code Data	1	0	1	1	0	0	1	1
Program encryption table	1	0	0	V_{PP}	1	0	1	0
Program security bit 1	1	0	0	V_{PP}	1	1	1	1
Program security bit 2	1	0	0	V_{PP}	1	1	0	0

Notes:
1. “0” = Valid low for that pin, "1" = valid high for that pin.
2. V_{PP} = 12.75V ± 0.25V
3. V_{CC} = 5V ± 10% during programming and verification.
4. ALE/$\overline{PROG}$ receives 25 (10 for GMS97X54/56/58) programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100us (± 10us) and high for a minimum of 10µs.

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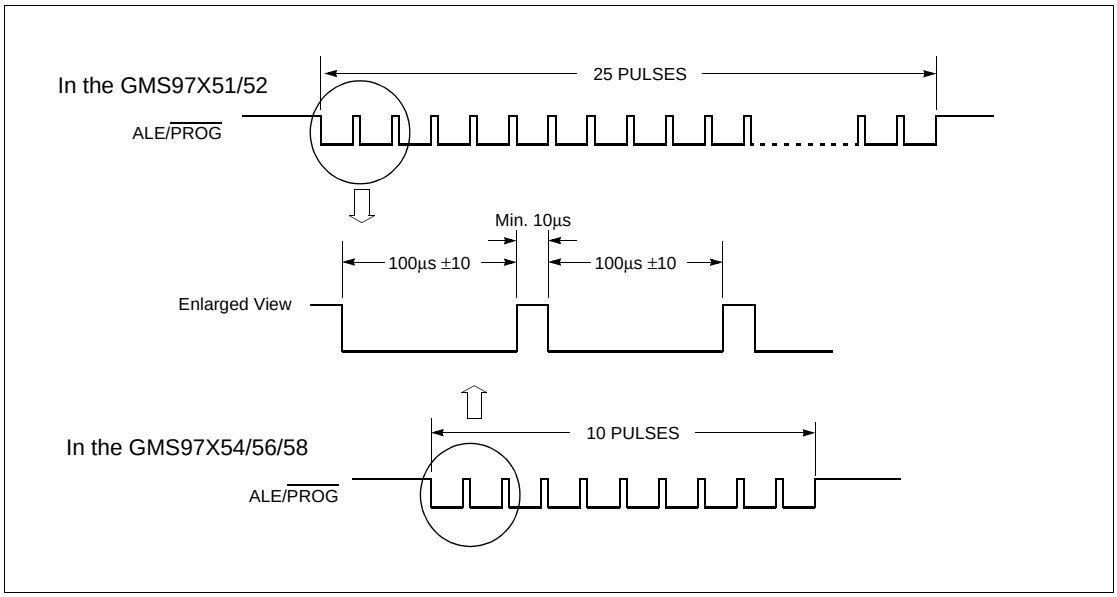

Figure 13. $\overline{\text{PROG}}$ Waveform

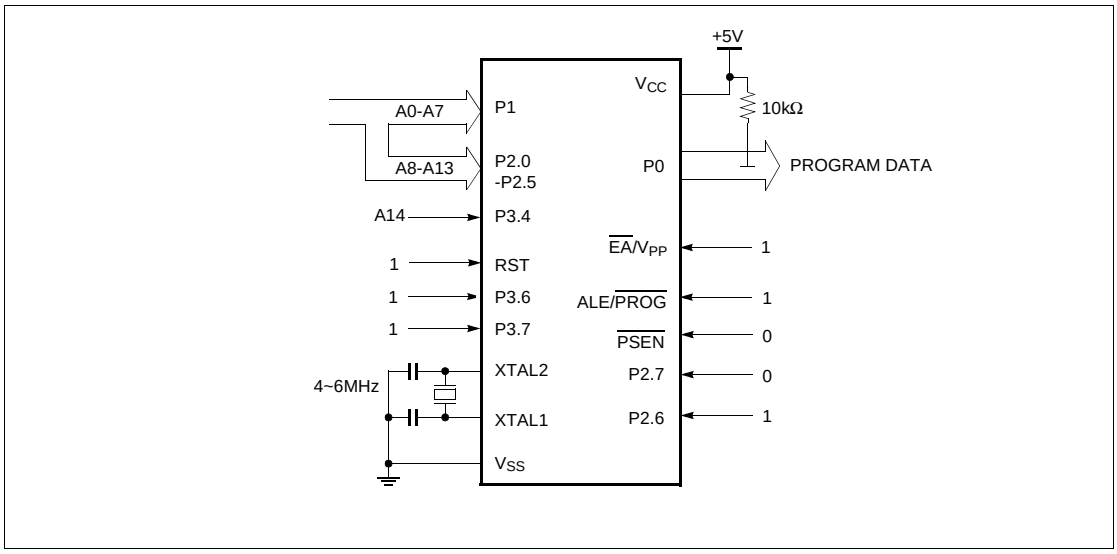

Figure 14. Program Verification

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EPROM Programming and Verification Characteristics

T_A= 21°C to 27°C, V_{CC}= 5V + 10%, – 15%; V_{SS}=0V;

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
Programming supply voltage	V_{PP}	12.5	13.0	V
Programming supply current	I_{PP}	-	50	mA
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz
Address setup to $\overline{PROG}$ low	t_{AVGL}	$48t_{CLCL}$	-	-
Address hold after $\overline{PROG}$	t_{GHAX}	$48t_{CLCL}$	-	-
Data setup to $\overline{PROG}$	t_{DVGL}	$48t_{CLCL}$	-	-
Data hold after $\overline{PROG}$	t_{GHDX}	$48t_{CLCL}$	-	-
P2.7 ($\overline{ENABLE}$) high to V_{PP}	t_{EHSH}	$48t_{CLCL}$	-	-
V_{PP} setup to $\overline{PROG}$	t_{SHGL}	10	-	µs
V_{PP} hold after $\overline{PROG}$	t_{GHSL}	10	-	µs
$\overline{PROG}$ width	t_{GLGL}	90	110	µs
Address to data valid	t_{AVQV}	-	$48t_{CLCL}$	-
$\overline{ENABLE}$ low to data valid	t_{ELQV}	-	$48t_{CLCL}$	-
Data float after $\overline{ENABLE}$	t_{EHQZ}	0	$48t_{CLCL}$	-
$\overline{PROG}$ high to $\overline{PROG}$ low	t_{GHGL}	10	-	µs

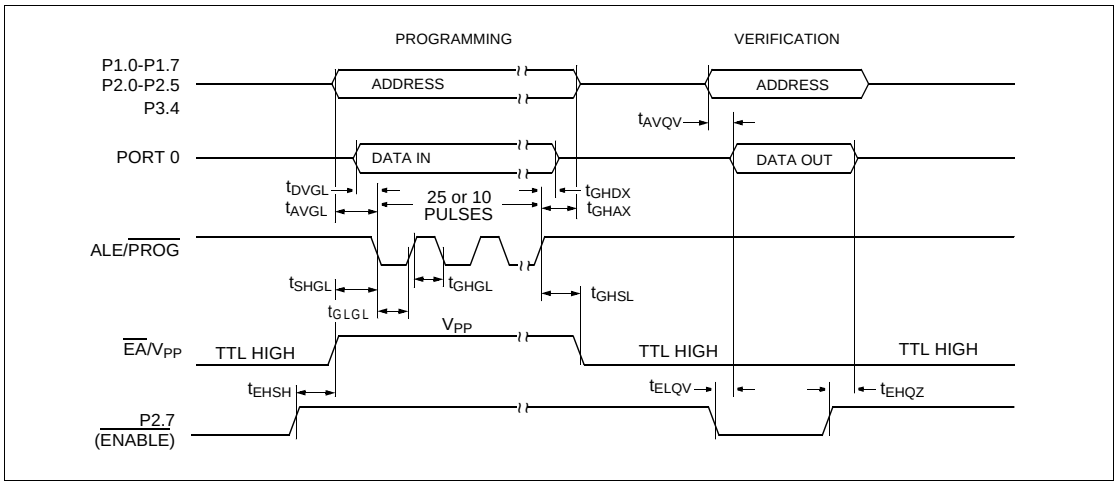

Figure 15. EPROM Programming and Verification

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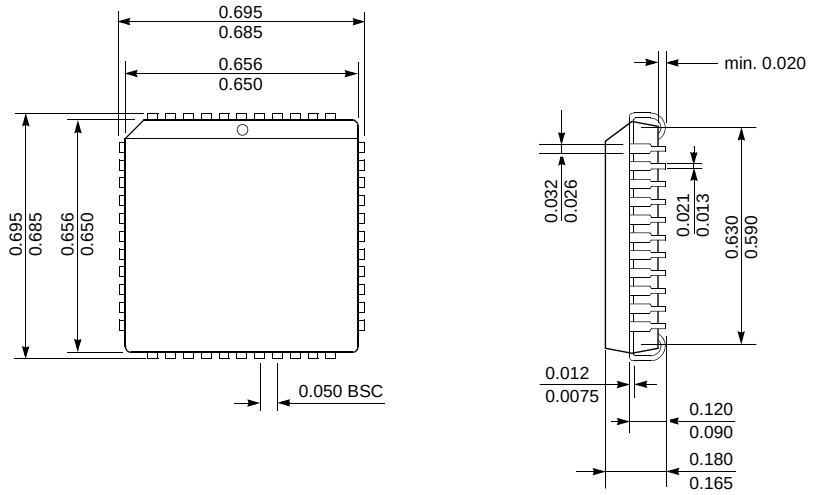
Plastic Package P-LCC-44

(Plastic Leaded Chip-Carrier)

44PLCC

UNIT: INCH



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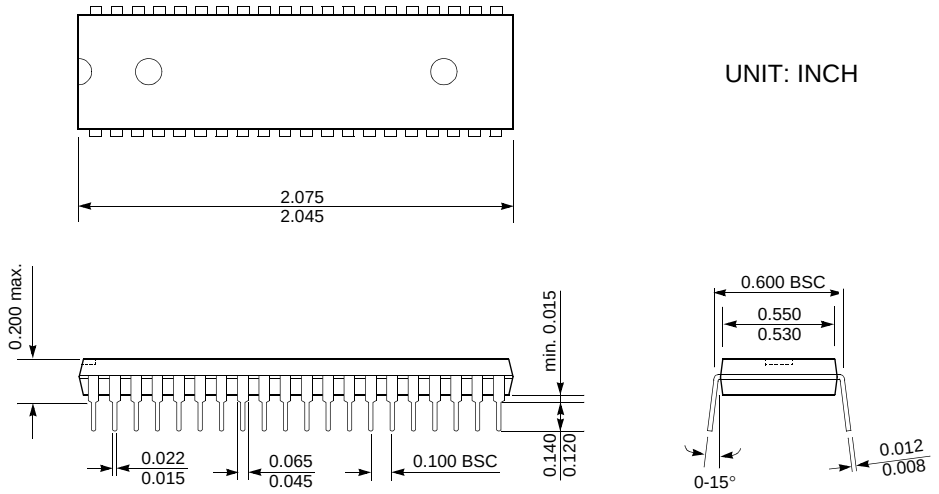
Plastic Package P-DIP-40

(Plastic Dual in-Line Package)

40DIP



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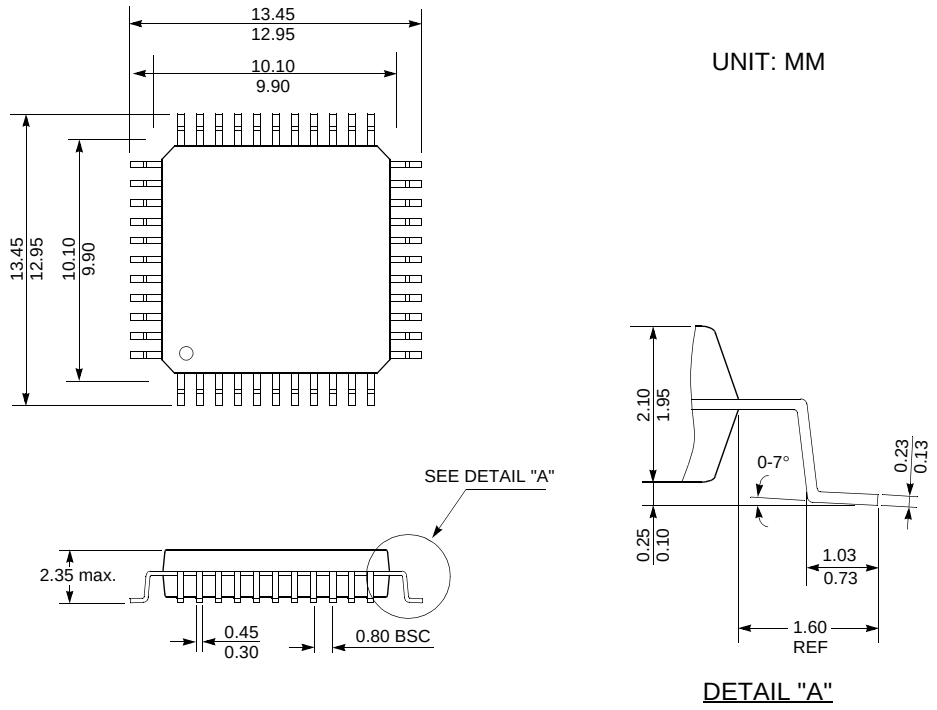
Plastic Package P-MPQF-44

(Plastic Metric Quad Flat Package)

44MQFP



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MASK ORDER & VERIFICATION SHEET

GMS90X5X-GB ☐☐☐

Customer should write inside thick line box.

1. Customer Information

Company Name	
Application	
Order Date	YYYY MM DD • •
Tel:	Fax:
Name & Signature:	

2. Device Information

ROM size	Package	Vol. / Freq.
☐ 4K ☐ 8K ☐ 16K ☐ 24K ☐ 32K	☐ 44MQFP ☐ 44PLCC ☐ 40PDIP	5V { ☐ 12MHz, ☐ 24MHz, ☐ 40MHz } 3V { ☐ 12MHz, ☐ 16MHz }

ROM Protection: ROM: 4K,8K — ☐ Without; ROM: 16,24,32K — ☐ Normal ☐ Super

Mask Data:
File Name: (.HEX)
Check Sum: ☐☐☐☐
☐ Internet ☐ Chollian ☐ Hitel

(Please check mark into ☐)

3. Marking Specification

40PDIP or 44PLCC

```
LGS
GMS90①5②-GB□□□
□□□□□□□□□□□□□□
YYWW    KOREA
©SIEMENS '92
```

44MQFP

```
LGS
90①5②-GB□□□
□□□□□□□□□□□□□□
YYWW    KOREA
©SIEMENS '92
```

① C: 5V
L: 3V

② ROM size
1: 4K
2: 8K
4: 16K
6: 24K
8: 32K

Customer's part number

☐☐☐☐☐☐☐☐☐☐☐☐☐

4. Delivery Schedule

	Date	Quantity	LG Confirmation
Customer Sample	YYYY MM DD • •	pcs	
Risk Order	YYYY MM DD • •	pcs	

5. ROM Code Verification

Verification Date:	YYYY MM DD • •
Please confirm our verification data.	
Check Sum:	
Tel:	Fax:
Name & Signature:	

This box is written after "5.Verification".

Approval Date:	YYYY MM DD • •
I agree with your verification data and confirm you to make mask set.	
Tel:	Fax:
Name & Signature:	

LG Semicon

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