

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4556B

MSI

Dual 1-of-4 decoder/demultiplexer

Product specification
File under Integrated Circuits, IC04

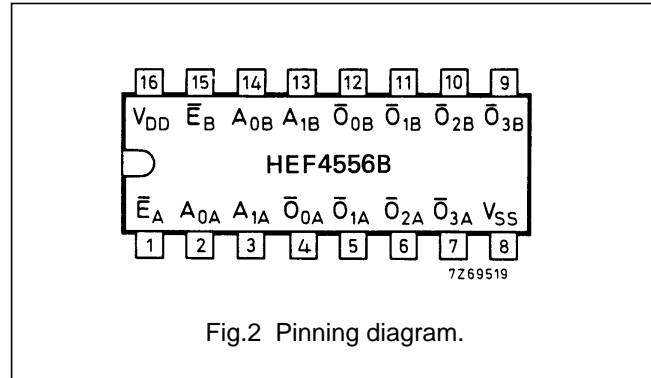
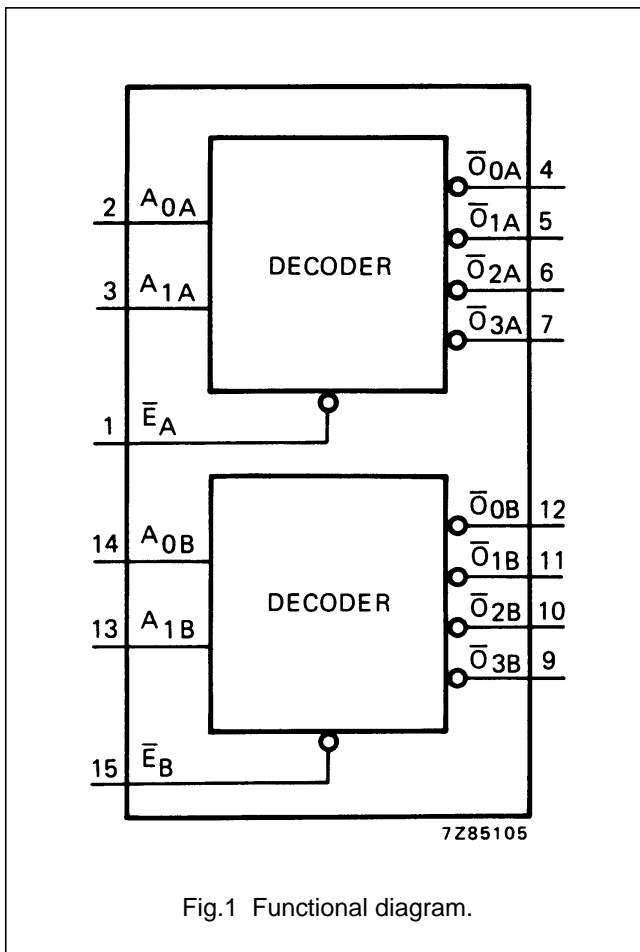
January 1995

Dual 1-of-4 decoder/demultiplexer

HEF4556B MSI

DESCRIPTION

The HEF4556B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input (\bar{E}) and four mutually exclusive outputs which are active LOW (\bar{O}_0 to \bar{O}_3). When used as a decoder, \bar{E} when HIGH, forces \bar{O}_0 to \bar{O}_3 HIGH. When used as a demultiplexer, the appropriate output is selected by the information on A_0 and A_1 with \bar{E} as data input. All unselected outputs are HIGH.



- HEF4556BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4556BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4556BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- \bar{E} enable inputs (active LOW)
- A_0 and A_1 address inputs
- \bar{O}_0 to \bar{O}_3 outputs (active LOW)

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

Dual 1-of-4 decoder/demultiplexer

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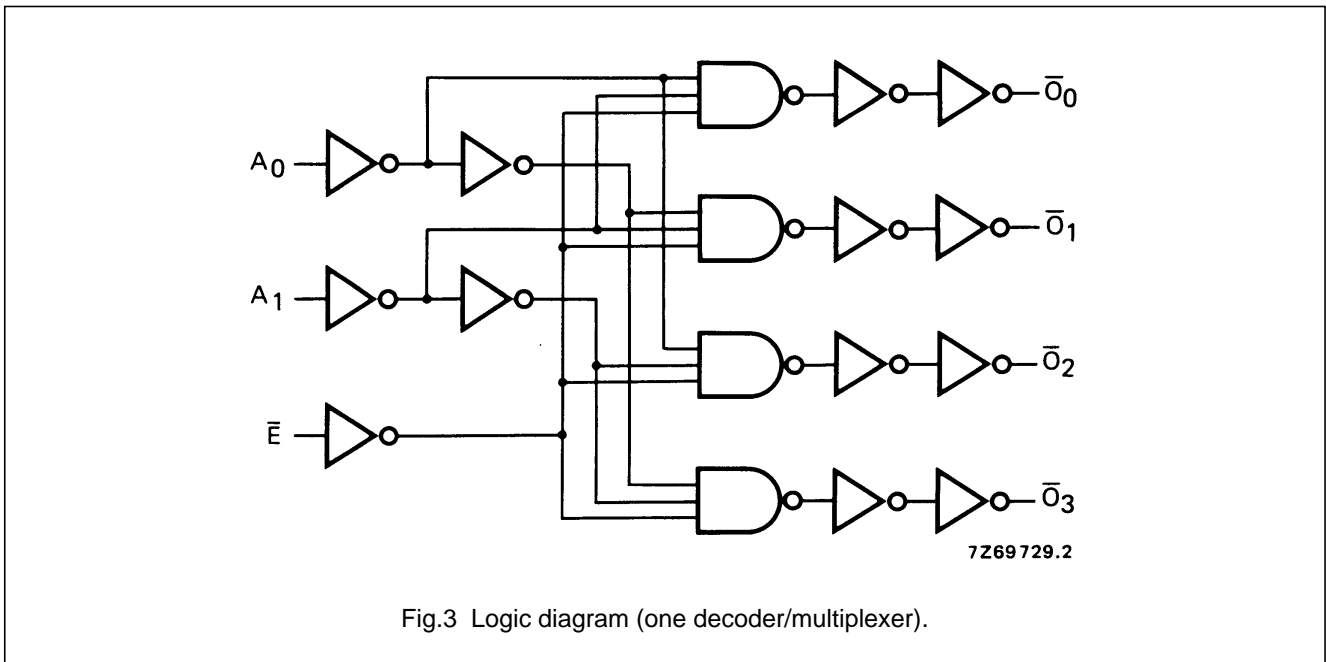


Fig.3 Logic diagram (one decoder/multiplexer).

TRUTH TABLE

INPUTS			OUTPUTS			
\bar{E}	A_0	A_1	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial

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AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA				
Propagation delays	5	t_{PHL}		130	255	ns	$103 \text{ ns} + (0,55 \text{ ns/pF}) C_L$			
				HIGH to LOW	10	50	100	ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
					15	35	65	ns	$27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
	LOW to HIGH				5	105	210	ns	$78 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
				10	40	85	ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$		
				15	30	60	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$		
	$\bar{E}_n \rightarrow \bar{O}_n$	5	t_{PHL}		120	240	ns	$93 \text{ ns} + (0,55 \text{ ns/pF}) C_L$		
					HIGH to LOW	10	45	90	ns	$34 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
						15	30	60	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
		LOW to HIGH				5	105	205	ns	$78 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
					10	40	80	ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
					15	30	60	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
Output transition times	5	t_{THL}		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$			
				HIGH to LOW	10	30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
					15	20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
	LOW to HIGH				5	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
				10	30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$		
				15	20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$		

	V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5	$4400 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$18\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$43\,300 f_i + \sum (f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4556B are:

- Code conversion.
- Address decoding.
- Demultiplexing: when using the enable input as data input.