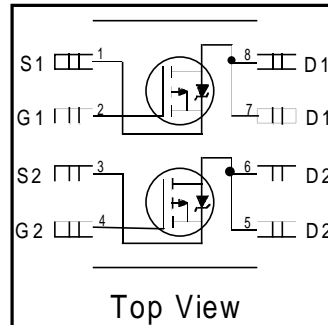


- Advanced Process Technology
- Ultra Low On-Resistance
- Dual P-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching

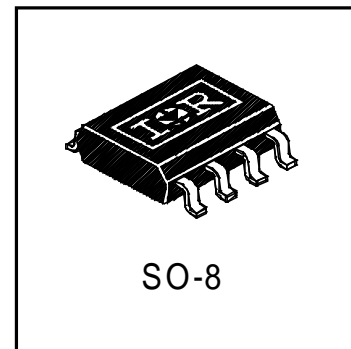
Description

Fourth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and dual-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



$V_{DSS} = -20V$
$R_{DS(on)} = 0.250\Omega$
$I_D = -2.3A$



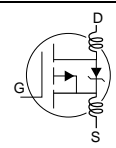
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-2.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-1.8	
I_{DM}	Pulsed Drain Current ①	-10	
$P_D @ T_C = 25^\circ C$	Power Dissipation	2.0	W
	Linear Derating Factor	0.016	W/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
dv/dt	Peak Diode Recovery dv/dt ②	-3.0	V/nS
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

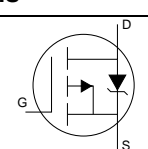
Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	—	62.5	°C/W

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.015	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	0.19	0.25	Ω	$V_{GS} = -10V, I_D = -1.0A$ ③
		—	0.30	0.40		$V_{GS} = -4.5V, I_D = -0.50A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-3.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	—	2.5	—	S	$V_{DS} = -15V, I_D = -2.3A$ ③
I_{DSS}	Drain-to-Source Leakage Current	—	—	-2.0	μA	$V_{DS} = -16V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -16V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 12V$
Q_g	Total Gate Charge	—	9.3	25	nC	$I_D = -2.3A$
Q_{gs}	Gate-to-Source Charge	—	1.6	—		$V_{DS} = -10V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	3.0	—		$V_{GS} = -10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	12	40	ns	$V_{DD} = -10V$
t_r	Rise Time	—	16	40		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	42	90		$R_G = 6.0\Omega$
t_f	Fall Time	—	30	50		$R_D = 10\Omega$ ③
L_D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	6.0	—		
C_{iss}	Input Capacitance	—	290	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	210	—		$V_{DS} = -15V$
C_{rss}	Reverse Transfer Capacitance	—	67	—		$f = 1.0\text{MHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-9.2		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -1.25A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	69	100	ns	$T_J = 25^\circ\text{C}, I_F = -1.25A$
Q_{rr}	Reverse Recovery Charge	—	90	140	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

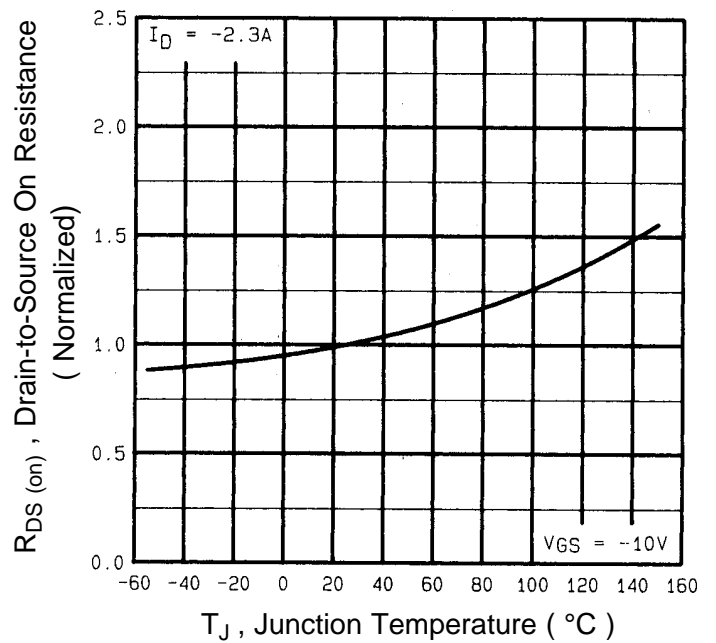
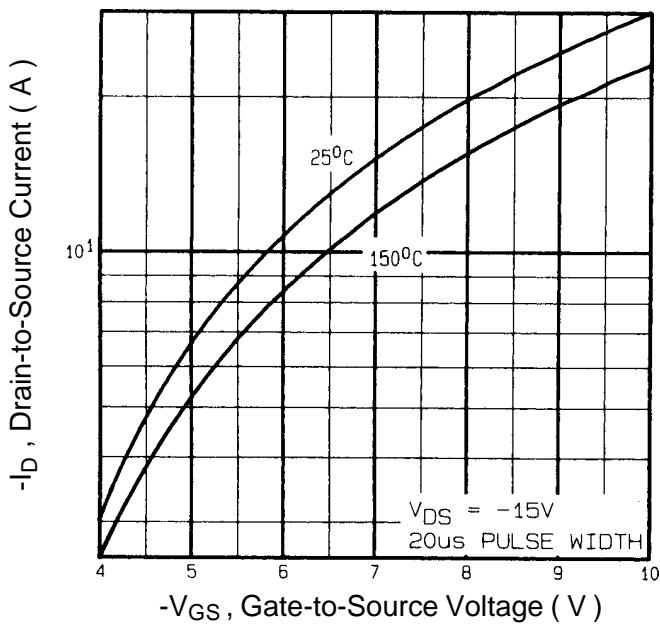
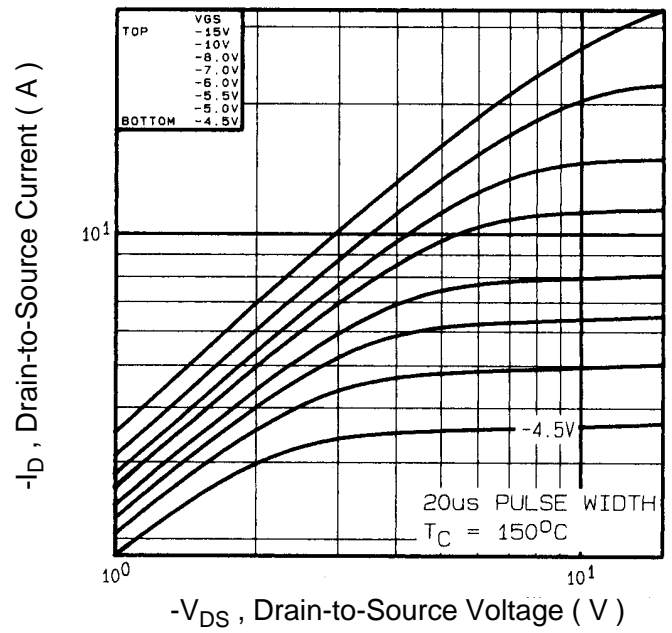
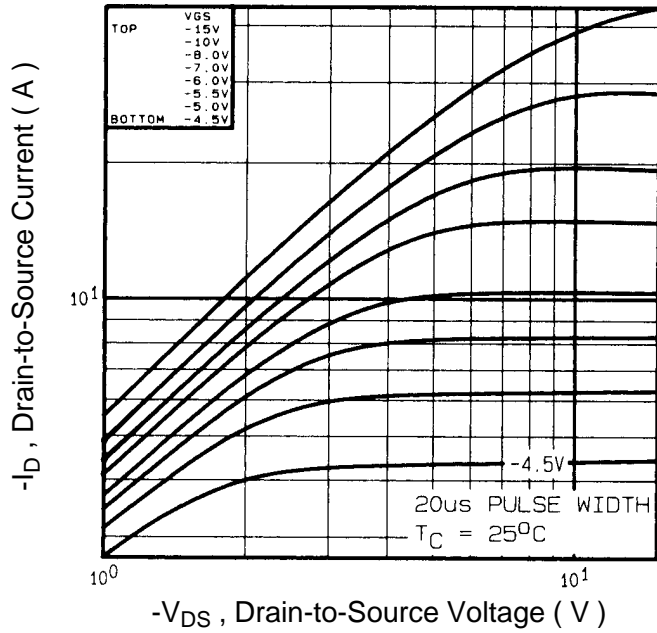
Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

② $I_{SD} \leq -2.3A, di/dt \leq 100A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.



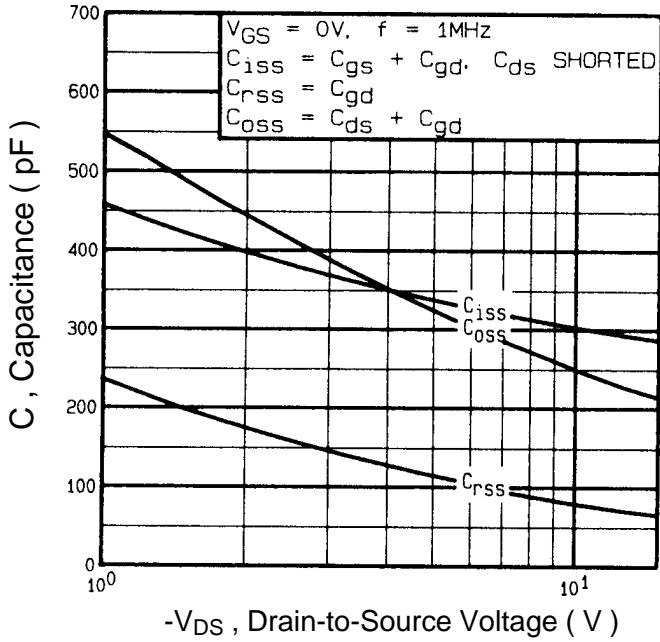


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

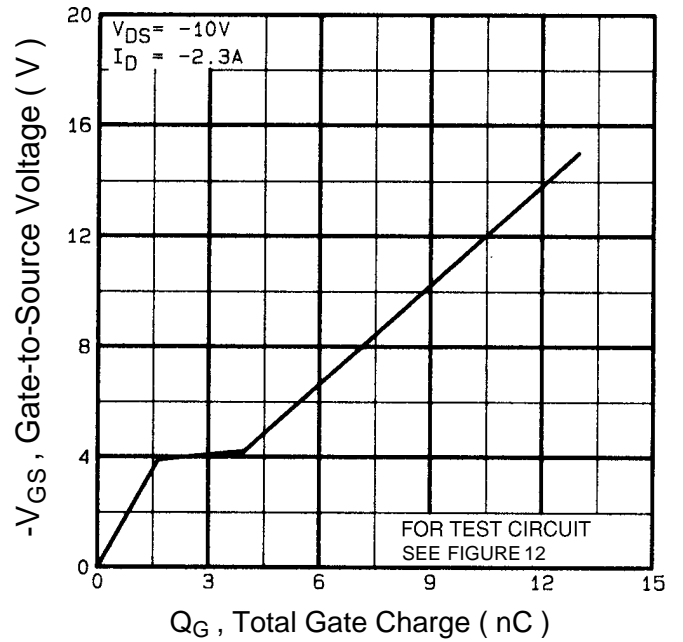


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

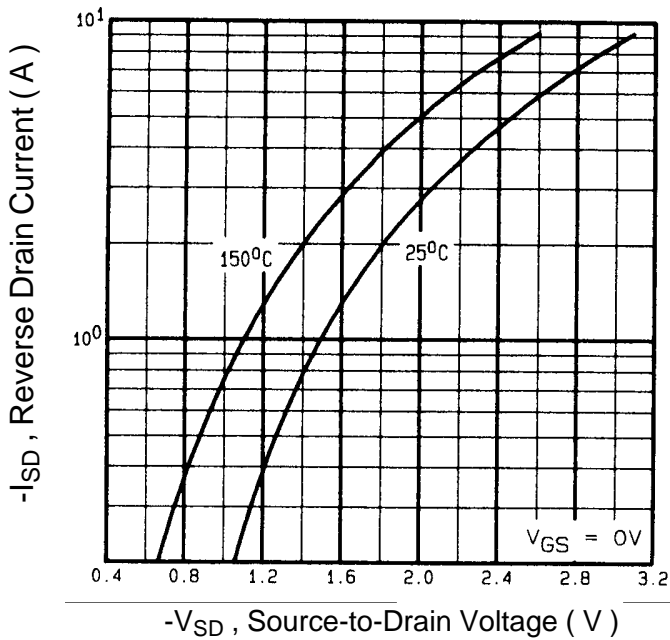


Fig 7. Typical Source-Drain Diode Forward Voltage

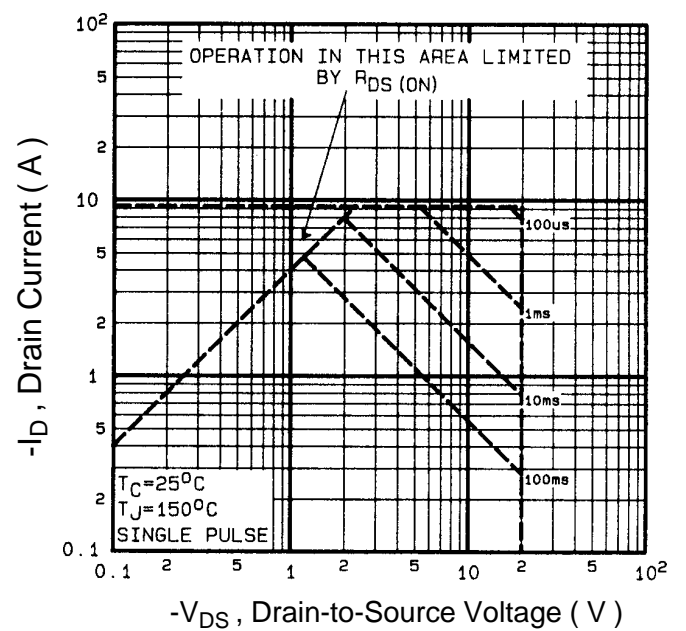


Fig 8. Maximum Safe Operating Area

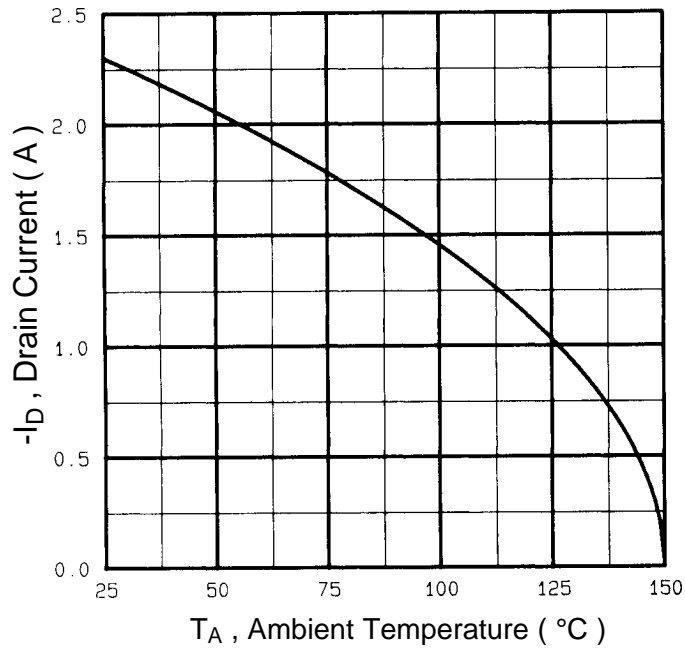


Fig 9. Maximum Drain Current Vs. Ambient Temperature

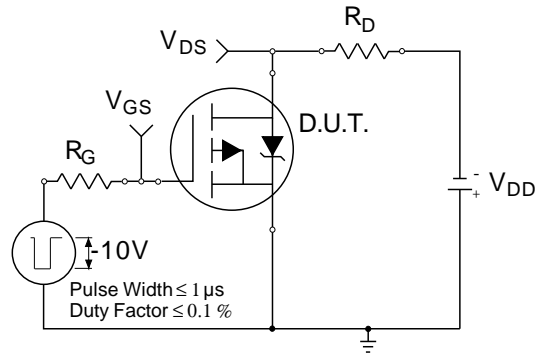


Fig 10a. Switching Time Test Circuit

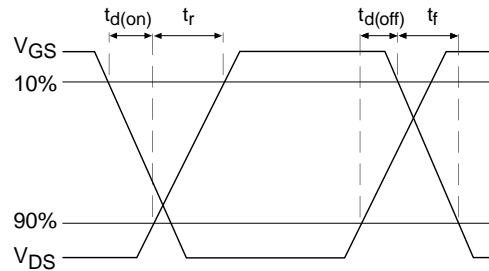


Fig 10b. Switching Time Waveforms

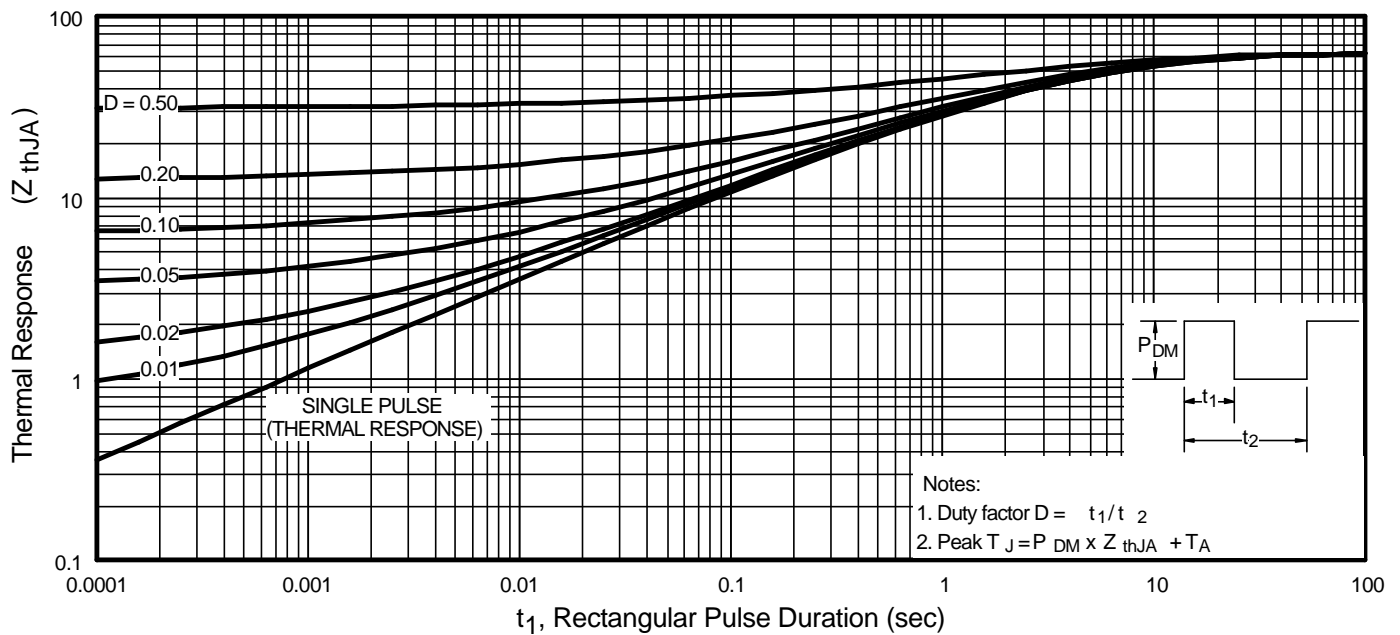


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

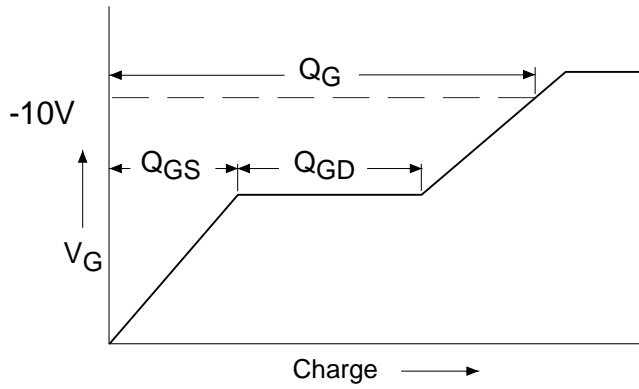


Fig 12a. Basic Gate Charge Waveform

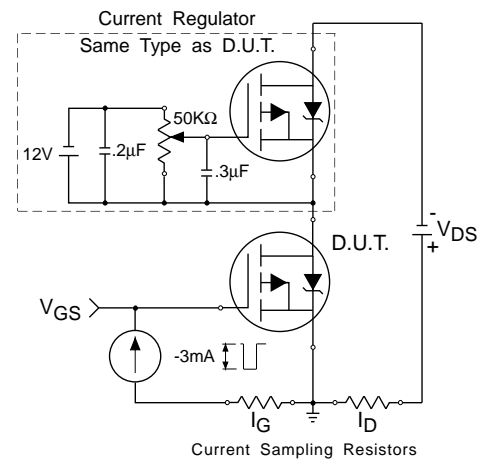
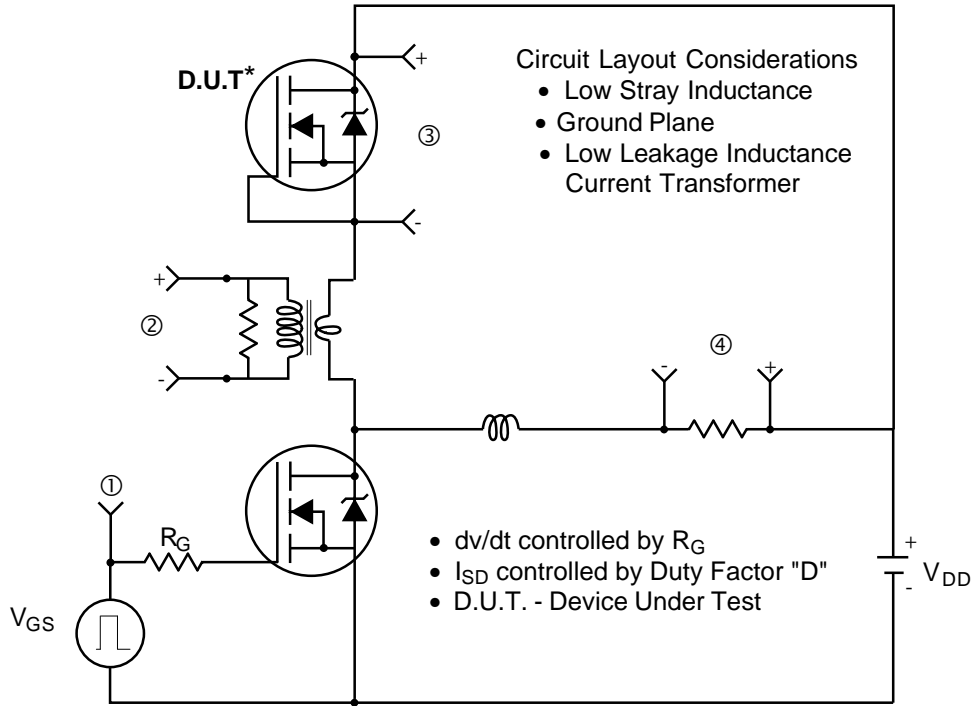
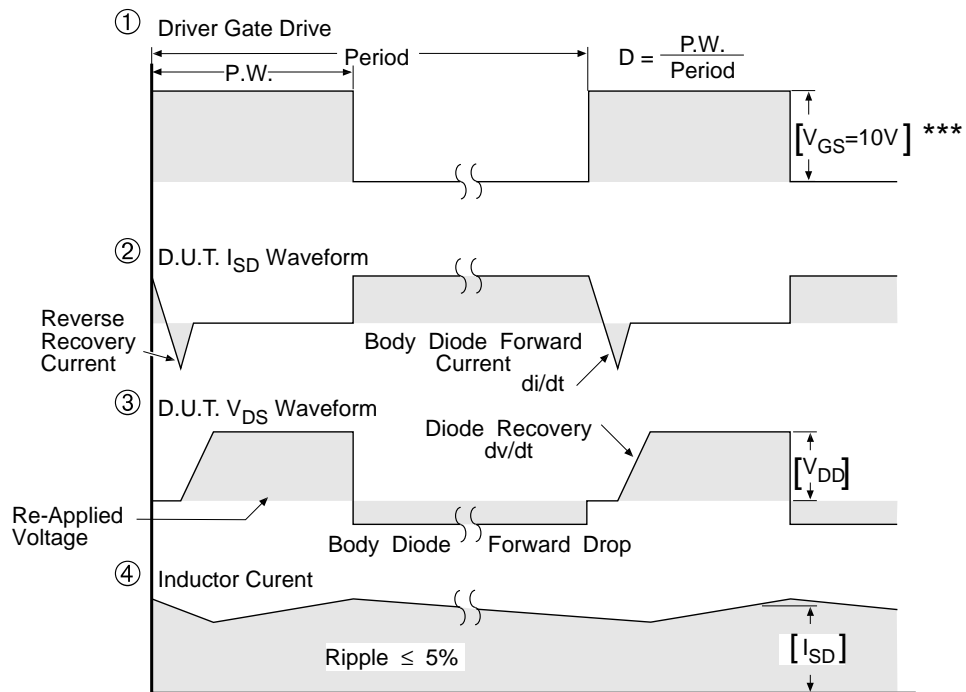


Fig 12b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



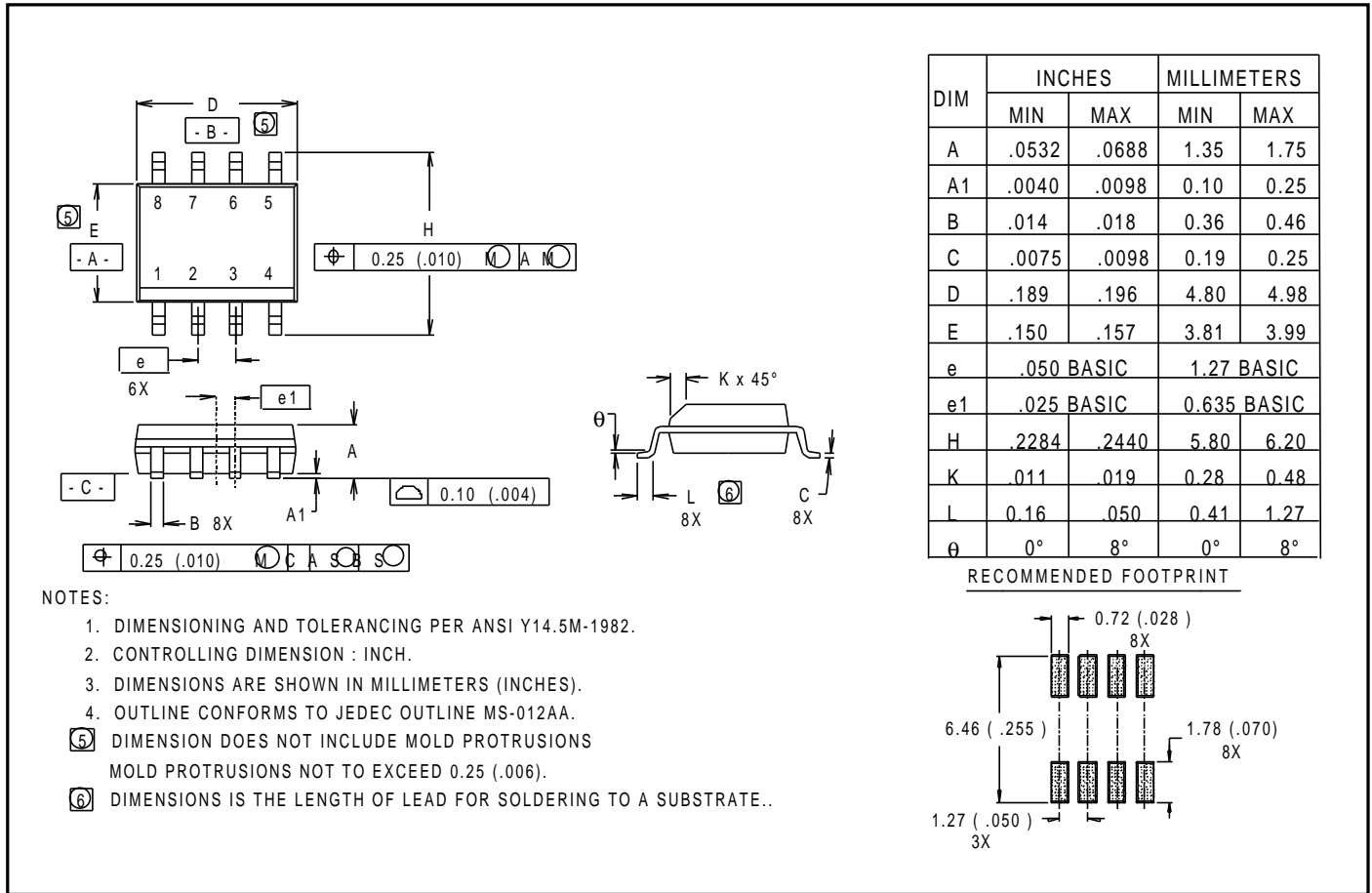
* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

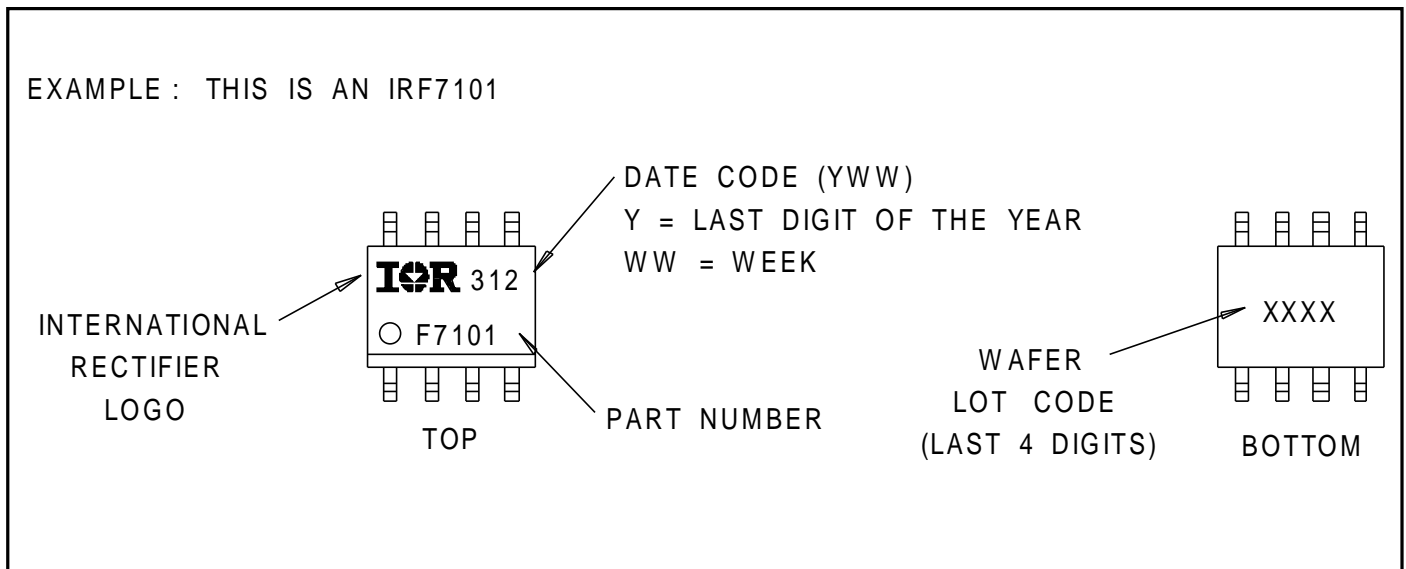
Fig 13.For P-Channel HEXFETS

Package Outline SO8 Outline



Part Marking Information

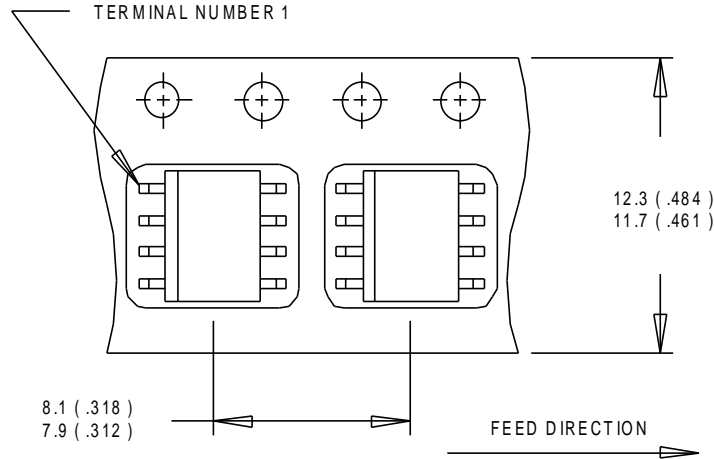
SO8



Tape & Reel Information

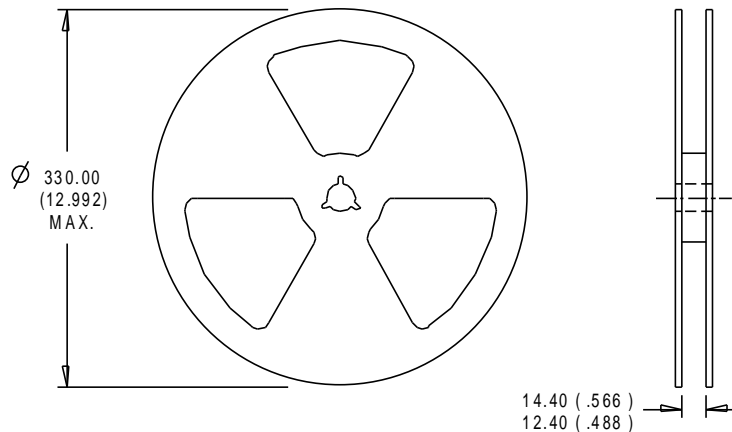
S08

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

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