

# M5238AL/P/FP

## DUAL LOW-NOISE J-FET INPUT OPERATIONAL AMPLIFIERS

### DESCRIPTION

The M5238 is a semiconductor integrated circuit designed as a low-noise Bi-FET operational amplifier which adopts J-FETs in the input stage. Noise reduction characteristic in the input stage has been improved by 3 - 4dB, when compared with the M5221 general-purpose Bi-FET operational amplifier, and two circuits for yielding a high input impedance, high slew rate and low bias current and other excellent characteristics, are housed in an 8-pin SIP, DIP or FP.

It can be widely used as a general-purpose operational amplifier in stereo equipment, tape decks, digital audio disc players and other similar products as well as in VCRs, video disc players and video related players.

### FEATURES

- Low noise, input-referred noise  $V_{NI}=1.9\mu\text{Vrms}(\text{typ.})$   
 $(R_s=100\text{k}\Omega \text{ BW}10\text{Hz}\sim 30\text{kHz FLAT})$   
 $S/N=73\text{dB}(\text{typ.})$   
 (Shorted input, RIAA, IHF-A network, PHONO 2.5mVrms)
- High input impedance due to J-FET input  
 $R_i=1000\text{M}\Omega(\text{typ.})$
- High slew rate  $S_R=20\text{V}/\mu\text{s}(\text{typ.})$
- High gain, low distortion  
 $G_{VO}=100\text{dB}(\text{typ.})$ ,  $\text{THD}=0.002\%$   
 $(G_V=35.6\text{dB, RIAA, } V_O=5\text{Vrms})$
- Large load current and allowable current  
 $I_{LP}=\pm 50\text{mA}$ ,  $P_d=800\text{mW}(\text{SIP})$   
 $P_d=625\text{mW}(\text{DIP})$ ,  $P_d=440\text{mW}(\text{FP})$

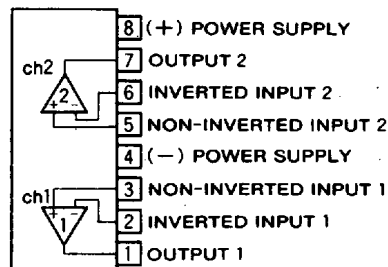
### APPLICATION

General purpose preamplifier in stereo equipment, tape decks and digital audio disc players, VCRs and video disc players.

### RECOMMENDED OPERATING CONDITION

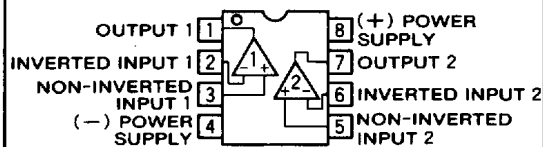
- Supply voltage range  $\pm 5\sim\pm 15\text{V}$
- Rated supply voltage  $\pm 15\text{V}$

### PIN CONFIGURATION (TOP VIEW)



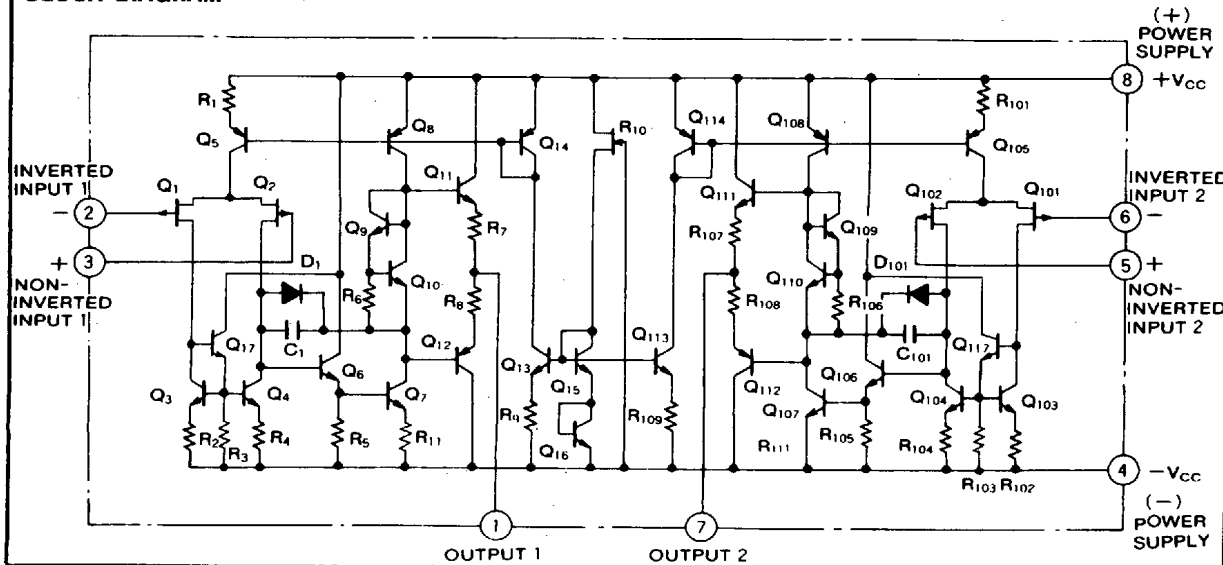
Outline 8P5 (AL)

DIP, MINI FLAT



Outline 8P4 (AP)  
8P2S-A (AFP)

### BLOCK DIAGRAM



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DUAL LOW-NOISE J-FET INPUT OPERATIONAL AMPLIFIERS

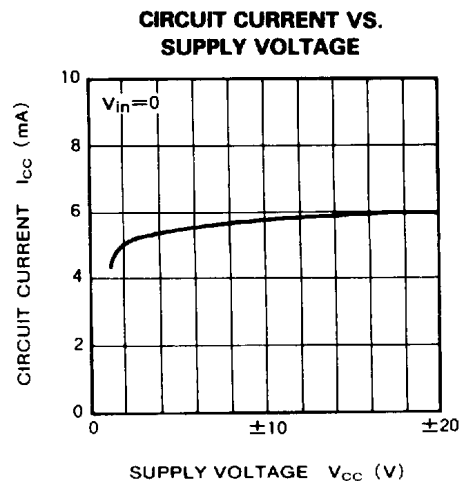
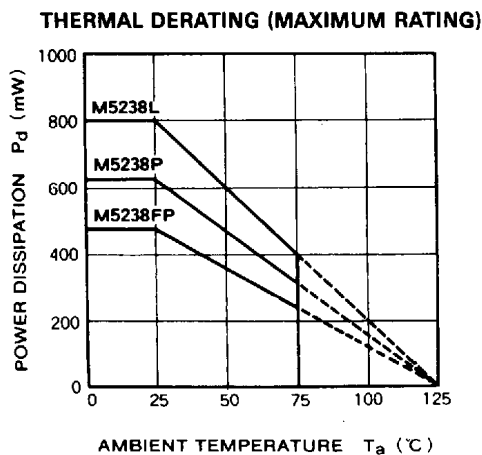
ABSOLUTE MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage		$\pm 18$	V
$I_{LP}$	Load current		$\pm 50$	mA
$V_{id}$	Differential input voltage		$\pm 30$	V
$V_{ic}$	Common input voltage		$\pm 15$	V
$P_d$	Power dissipation		800(SIP)/625(DIP)/440(FP)	mW
$K_\theta$	Thermal derating	$T_a \geq 25^\circ\text{C}$	8(SIP)/6.25(DIP)/4.4(FP)	mW/°C
$T_{opr}$	Ambient temperature		$-20 \sim +75$	°C
$T_{stg}$	Storage temperature		$-55 \sim +125$	°C

ELECTRICAL CHARACTERISTICS ( $T_a=25^\circ\text{C}$ ,  $V_{CC}=\pm 15\text{V}$ )

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$I_{CC}$	Circuit current	$V_{in}=0$		5.8	9.0	mA
$V_{IO}$	Input offset voltage	$R_s \leq 10\text{k}\Omega$		2.0	10.0	mV
$I_{IO}$	Input offset current			5	200	pA
$I_{IB}$	Input bias current			30	400	pA
$R_{in}$	Input resistance			$10^3$		M $\Omega$
$G_{VO}$	Open loop voltage gain	$R_L \geq 2\text{k}\Omega$ , $V_o = \pm 10\text{V}$	86	106		dB
$V_{OM}$	Maximum output voltage	$R_L \geq 10\text{k}\Omega$	$\pm 12$	$\pm 14$		V
		$R_L \geq 2\text{k}\Omega$	$\pm 10$	$\pm 13$		V
$V_{CM}$	Common input voltage width		$\pm 10$	$\pm 12$		V
CMRR	Common mode rejection ratio	$R_s \leq 10\text{k}\Omega$	70	76		dB
SVRR	Supply voltage rejection ratio	$R_s \leq 10\text{k}\Omega$		30	150	$\mu\text{V/V}$
$P_d$	Power dissipation			174	270	mW
SR	Slew rate	$G_v=0\text{dB}$ , $R_L=2\text{k}\Omega$		20		V/ $\mu\text{s}$
$f_T$	Gain bandwidth product			6		MHz
$V_{NI}$	Input referred noise voltage	$R_s=100\Omega$ , BW=10Hz~30kHz		1.9		$\mu\text{Vrms}$

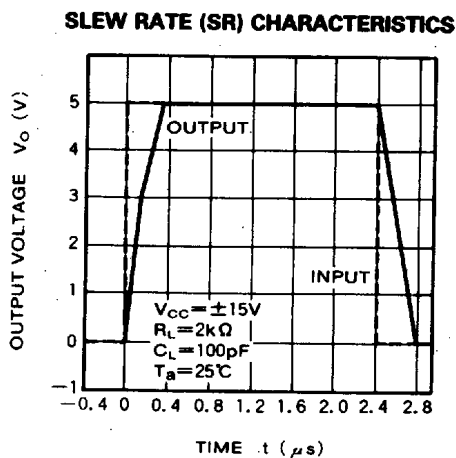
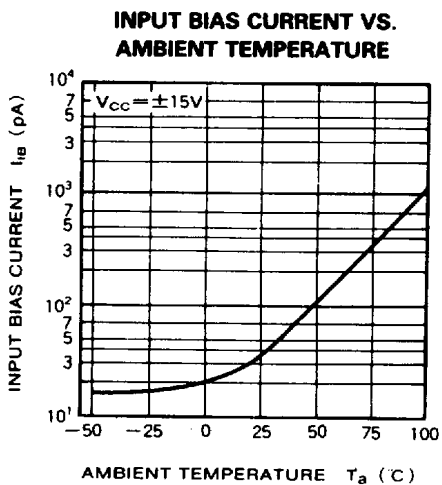
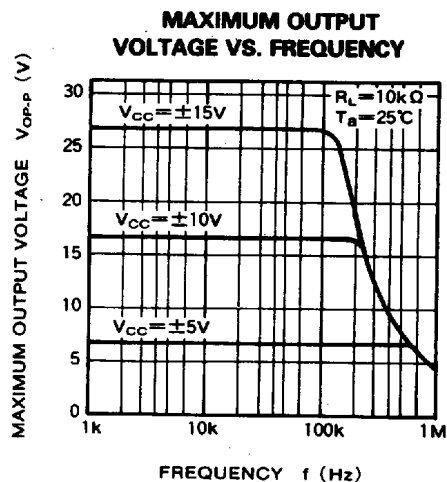
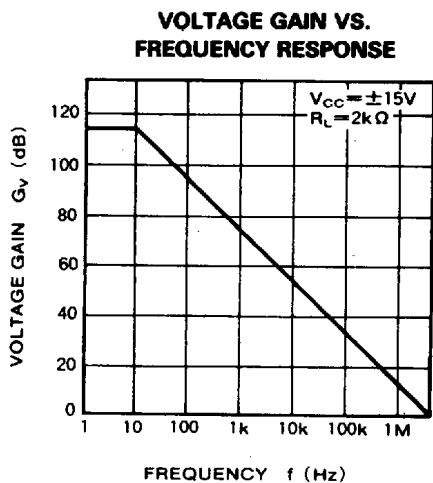
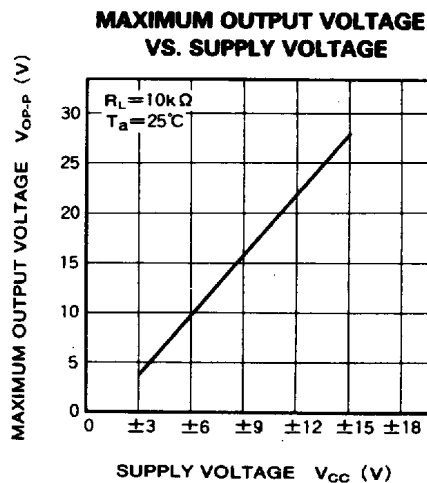
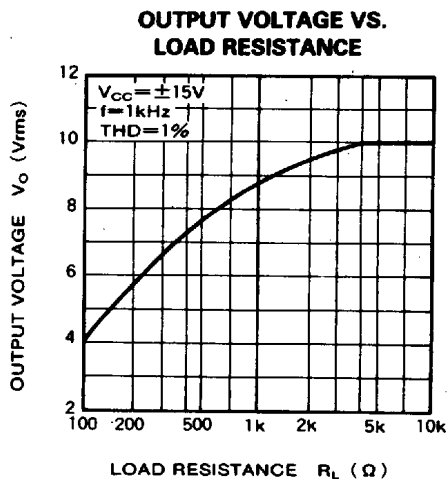
TYPICAL CHARACTERISTICS



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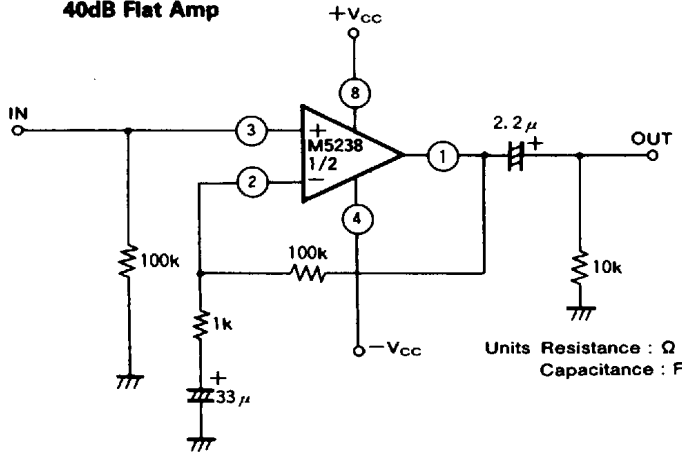


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DUAL LOW-NOISE J-FET INPUT OPERATIONAL AMPLIFIERS

APPLICATION CIRCUIT 1

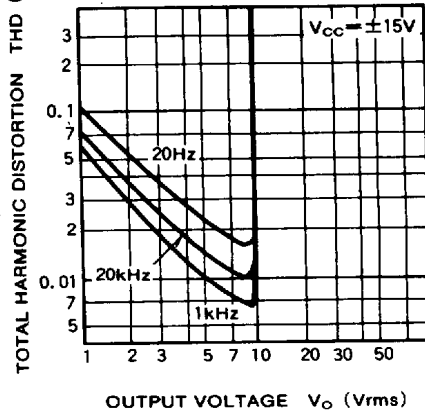
40dB Flat Amp



TYPICAL CHARACTERISTICS

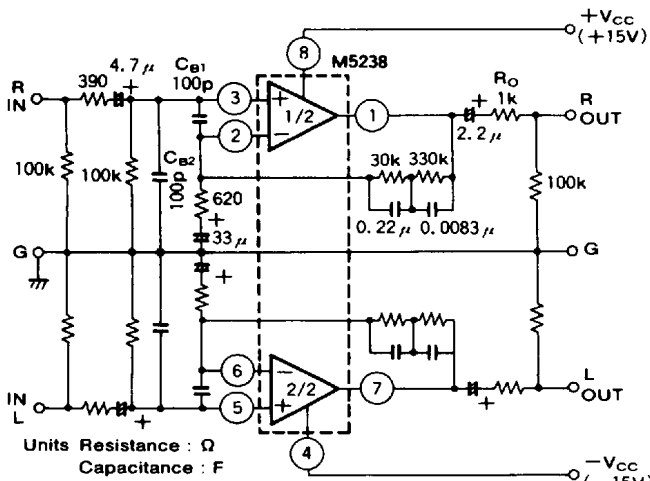
- $V_{CC} = \pm 15V$
- $G_V = 40dB (f = 1kHz)$
- $V_O = 9.5V_{rms} (f = 1kHz, THD = 0.1\%)$
- $THD = 0.007\% (f = 1kHz, V_O = 7V_{rms})$

TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



APPLICATION CIRCUIT 2

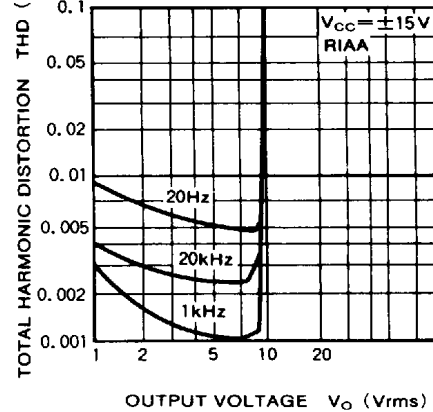
Stereo equalizer amplifier circuit



TYPICAL CHARACTERISTICS ( $V_{CC} = \pm 15V, RIAA$ )

- $G_V = 35.6dB (f = 1kHz)$
- $V_{NI} = 1.9\mu V_{rms} (R_S = 100\Omega, BW = 20Hz \sim 30kHz)$
- $S/N = 73dB$  (IHF-A network, shorted input, 2.5mVrms input sensitivity)
- $THD = 0.001\% (f = 1kHz, V_O = 7V_{rms})$

TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



$L_{Ch}$  circuit constants are identical to those of  $R_{Ch}$ .

$C_{B1}, C_{B2}$ : Capacitors for buzz prevention, use if required.

$R_O$ : Resistor used to prevent parasitic oscillation for capacitive loads and current limiting with shorted and other abnormal load conditions.

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