19-1431; Rev 4; 6/05

Direct-Conversion Tuner IC for Digital DBS Applications

General Description

The MAX2104 low-cost direct-conversion tuner IC is designed for use in digital direct-broadcast satellite (DBS) television set-top box units. Its direct-conversion architecture reduces system cost compared to devices with IF-based architectures. The MAX2104 directly converts L-band signals to baseband signals using a broadband I/Q downconverter. The operating frequency range extends from 925MHz to 2175MHz.

The IC includes an LNA gain control, I and Q downconverting mixers, lowpass filters with gain control and frequency control, a local oscillator (LO) buffer with a 90° quadrature network, and a charge-pump based PLL for frequency control. The MAX2104 also has an on-chip LO, requiring only an external varactor-tuned LC tank for operation. The output of the LO drives the internal quadrature generator and dual modulus prescaler. An on-chip crystal amplifier drives a reference divider as well as a buffer amplifier to drive off-chip circuitry. The MAX2104 is offered in a 48-pin TQFP-EP package.

Applications

DirecTV, PrimeStar, EchoStar DBS Tuners

DVB-Compliant DBS Tuners

Broadband Systems

LMDS

Features

- ♦ **Low-Cost Architecture**
- ♦ **Operates from Single 5V Supply**
- ♦ **925MHz to 2175MHz Input Frequency Range**
- ♦ **On-Chip Quadrature Generator, Dual-Modulus Prescaler (/32, /33)**
- ♦ **On-Chip Crystal Amplifier**
- ♦ **PLL Mixer with Gain-Controlled Charge Pump**
- ♦ **Input Levels: -25dBm to -65dBm per Carrier**
- ♦ **Over 40dB Gain Control Range**
- ♦ **Noise Figure = 11.5dB; IIP3 = 7dBm (at 1550MHz)**
- ♦ **Automatic Baseband Offset Correction**
- ♦ **Loopthrough Replaces External Splitter**
- ♦ **Crystal Output Buffer**

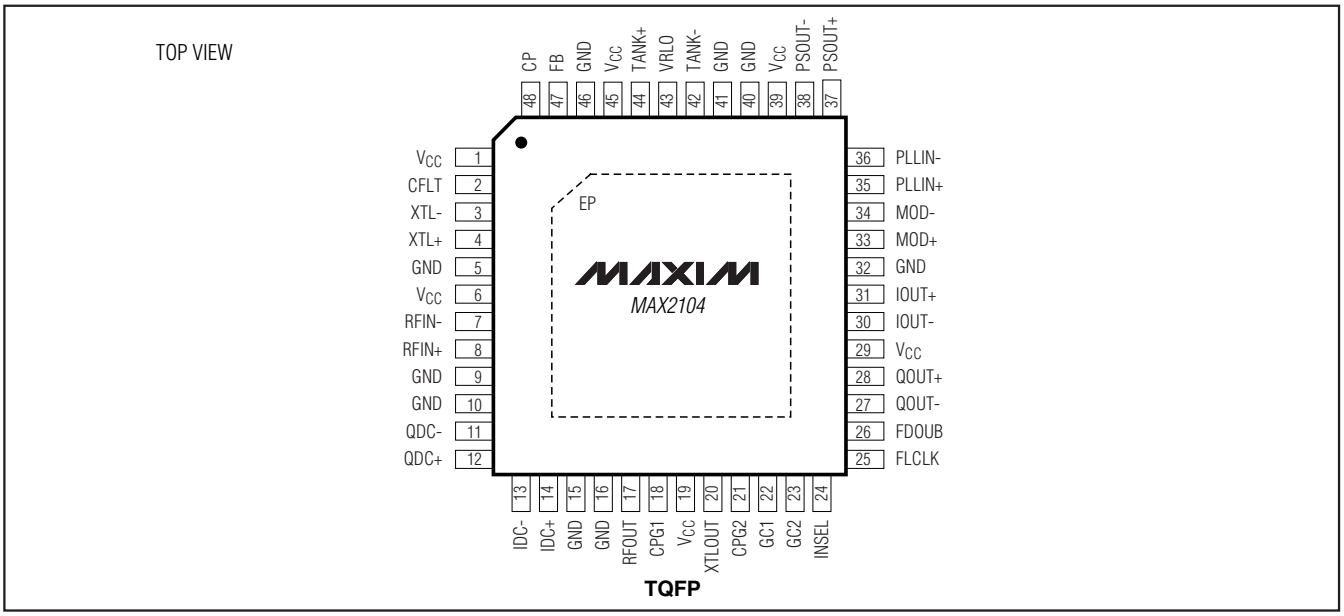
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX2104CCM*	0°C to +70°C	48 TQFP-EP**	C48E-10
MAX2104CCM+	0°C to +70°C	48 TQFP-EP**	C48E-10

*Contact factory for availability.
**EP = Exposed paddle.
+Denotes lead-free package.

Functional Diagram appears at end of data sheet.

Pin Configuration



Direct-Conversion Tuner IC for Digital DBS Applications

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.5V to +7V
All Other Pins to GND.....-0.3V to (V_{CC} + 0.3V)
RF1+ to RF1-, RF2+ to RF2-, TANK+ to TANK-, IDC+ to IDC-, QDC+ to QDC- .....±2V
IOUT_, QOUT_ to GND Short-Circuit Duration 10s
PSOUT+, PSOUT- to GND Short-Circuit Duration 10s
Continuous Current (any pin).....20mA

Continuous Power Dissipation (T_A = +70°C) (derate 30.4mW/°C above +70°C).....2.43W
Operating Temperature Range.....0°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, V_{FB} = 2.4V, $C_{IOUT\_}$ = $C_{QOUT\_}$ = 10pF, f_{FLCLK} = 2MHz, RFIN_ = floating, $R_{IOUT\_}$ = $R_{QOUT\_}$ = 10kΩ, V_{FDOUB} = V_{INSEL} = V_{CPG1} = V_{CPG2} = 2.4V, V_{PLLIN+} = V_{MOD+} = 1.3V, V_{PLLIN-} = V_{MOD-} = 1.1V, T_A = +25°C. Typical values are at V_{CC} = 5.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{CC}		4.75		5.25	V
Operating Supply Current	I_{CC}			190	275	mA
STANDARD DIGITAL INPUTS (FDOUB, INSEL, CPG1, CPG2)						
Digital Input Voltage High	V_{IH}		2.4			V
Digital Input Voltage Low	V_{IL}				0.5	V
Digital Input Current	I_{IN}		-15		+10	µA
SLEW-RATE-LIMITED DIGITAL INPUTS						
FLCLK Input Voltage High			1.85			V
FLCLK Input Voltage Low					1.45	V
FLCLK Input Current (Note 1)		R_{SOURCE} = 50kΩ, V_{FLCLK} = 1.65V	-1		+1	µA
DIFFERENTIAL DIGITAL INPUTS (MOD+, MOD-, PLLIN+, PLLIN-)						
Common-Mode Input Voltage	V_{CMI}		1.08	1.2	1.32	V
Input Voltage Low (Note 2)		Referenced to V_{CMI}			-100	mV
Input Voltage High (Note 2)		Referenced to V_{CMI}	100			mV
Input Current (Note 1)			-5		5	µA
DIFFERENTIAL DIGITAL OUTPUTS (PSOUT+, PSOUT-)						
Common-Mode Output Voltage	V_{CMO}		2.16	2.4	2.64	V
Output Voltage Low (Note 3)		Referenced to V_{CMO}		-215	-150	mV
Output Voltage High (Note 3)		Referenced to V_{CMO}	150	215		mV
FREQUENCY SYNTHESIZER						
Prescaler Ratio		(V_{MOD+} - V_{MOD-}) = 200mV	32		32	
		(V_{MOD+} - V_{MOD-}) = -200mV	33		33	
Reference Divider Ratio			8		8	
Charge-Pump Output High Measured at FB		V_{CPG1} = V_{CPG2} = 0.5V	0.08	0.1	0.12	mA
		V_{CPG1} = 0.5V, V_{CPG2} = 2.4V	0.24	0.3	0.36	
		V_{CPG1} = 2.4V, V_{CPG2} = 0.5V	0.48	0.6	0.72	
		V_{CPG1} = V_{CPG2} = 2.4V	1.44	1.8	2.16	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.25V, V_{FB} = 2.4V, $C_{IOUT\_}$ = $C_{QOUT\_}$ = 10pF, f_{FLCLK} = 2MHz, RFIN_ = floating, $R_{IOUT\_}$ = $R_{QOUT\_}$ = 10kΩ, V_{FDOUB} = V_{INSEL} = V_{CPG1} = V_{CPG2} = 2.4V, V_{PLLIN+} = V_{MOD+} = 1.3V, V_{PLLIN-} = V_{MOD-} = 1.1V, T_A = +25°C. Typical values are at V_{CC} = 5.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge-Pump Output Low Measured at FB		V_{CPG1} = V_{CPG2} = 0.5V	-0.12	-0.1	-0.08	mA
		V_{CPG1} = 0.5V, V_{CPG2} = 2.4V	-0.36	-0.3	-0.24	
		V_{CPG1} = 2.4V, V_{CPG2} = 0.5V	-0.72	-0.6	-0.48	
		V_{CPG1} = V_{CPG2} = 2.4V	-2.16	-1.8	-1.44	
Charge-Pump Output Current Matching Positive to Negative		Measured at FB	-5		5	%
Charge-Pump Output Leakage		Measured at FB	-25		25	nA
Charge-Pump Output Current Drive (Note 1)		Measured at CP	100			µA
ANALOG CONTROL INPUTS (GC_)						
Analog Control Input Current	$I_{GC\_}$	$V_{GC\_}$ = 1V to 4V	-50		+50	µA
BASEBAND OUTPUTS (IOUT+, IOUT-, QOUT+, QOUT-)						
Differential Output Voltage Swing		R_L = 2kΩ differential	1			V_{P-P}
Common-Mode Output Voltage (Note 1)			0.65		0.85	V
Offset Voltage (Note 1)			-50		+50	mV

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, $V_{IOUT\_}$ = $V_{QOUT\_}$ = 0.59V_{P-P}, $C_{IOUT\_}$ = $C_{QOUT\_}$ = 10pF, f_{FLCLK} = 2MHz, $R_{IOUT\_}$ = $R_{QOUT\_}$ = 10kΩ, V_{FDOUB} = V_{INSEL} = V_{CPG1} = V_{CPG2} = 2.4V, V_{PLLIN+} = V_{MOD+} = 1.3V, V_{PLLIN-} = V_{MOD-} = 1.1V, T_A = +25°C. Typical values are at V_{CC} = 5.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RF FRONT END							
RFIN_ Input Frequency Range	f_{RFIN}			925		2175	MHz
RFIN_ Input Power for 0.59Vp-p Baseband Levels		Single carrier	V_{GC1} = V_{GC2} = +4V (min gain)		-20		dBm
			V_{GC1} = V_{GC2} = +1V (max gain)		-68	-65	dBm
RFIN_ Input Third-Order Intercept (Note 4)	$IP3_{RFIN\_}$	PRFIN_ = -25dBm per tone	f_{LO} = 2175MHz		5		dBm
			f_{LO} = 1550MHz		7		
			f_{LO} = 950MHz		8		
RFIN_ Input Second-Order Intercept (Note 5)	$IP2_{RFIN\_}$	$P_{RFIN\_}$ = -25dBm per tone, f_{LO} = 951MHz			15.5		dBm
Output-Referred 1dB Compression Point (Note 6)	$P1_{dBOUT\_}$	$P_{RFIN\_}$ = -40dBm, signals within filter bandwidth			2		dBV
Noise Figure	NF	$P_{RFIN\_}$ = -65dBm, $f_{RFIN\_}$ = 1550MHz, V_{GC1} = 1V, V_{GC2} adjusted 0.59Vp-p baseband level			11.5		dB
RFIN_ Return Loss (Note 7)		$f_{RFIN\_}$ = 925MHz			10		dB
		$f_{RFIN\_}$ = 2175MHz			10		
LO 2nd Harmonic Rejection (Note 8)		Average level of $V_{IOUT\_}$, $V_{QOUT\_}$		27			dBc
LO Half Harmonic Rejection (Note 9)		Average level of $V_{IOUT\_}$, $V_{QOUT\_}$		31	38		dBc

Direct-Conversion Tuner IC for Digital DBS Applications

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.25V, $V_{IOUT\_}$ = $V_{QOUT\_}$ = 0.59V_{P-P}, $C_{IOUT\_}$ = $C_{QOUT\_}$ = 10pF, f_{FLCLK} = 2MHz, $R_{IOUT\_}$ = $R_{QOUT\_}$ = 10kΩ, V_{FDOUB} = V_{INSEL} = V_{CPG1} = V_{CPG2} = 2.4V, V_{PLLIN+} = V_{MOD+} = 1.3V, V_{PLLIN-} = V_{MOD-} = 1.1V, T_A = +25°C. Typical values are at V_{CC} = 5.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LO Leakage Power (Notes 7, 10)		Measured at RFIN_		-66		dBm
RFOUT PORT (LOOPTHROUGH)						
RFIN_ to RFOUT Gain (Note 11)		f = 925MHz		0.5		dB
		f = 1550MHz		1.8		
		f = 2175MHz		2.5		
RFOUT Output Third-Order Intercept Point (Note 11)		f = 925MHz		9		dBm
		f = 1550MHz		7		
		f = 2175MHz		4		
RFOUT Noise Figure (Note 11)		f = 925MHz		15		dB
		f = 1550MHz		12		
		f = 2175MHz		11.5		
RFOUT Return Loss (Notes 1, 11)		925MHz < f < 2175MHz			8	dB
BASEBAND CIRCUITS						
Output Real Impedance (Note 1)		IOUT_, QOUT_			50	Ω
Baseband Highpass Frequency (Note 1)		$C_{IDC\_}$ = $C_{QDC\_}$ = 0.22µF			750	Hz
LPF -3dB Cutoff-Frequency Range (Note 1)		Controlled by FLCLK signal	8		33	MHz
Baseband Frequency Response (Note 1)		Deviation from ideal 7th order, Butterworth, up to 0.7 x f_C	-0.5		+0.5	dB
LPF -3dB Cutoff-Frequency Accuracy (Note 1)		f_{FLCLK} = 0.5MHz, f_C = 8MHz	-5.5		+5.5	%
		f_{FLCLK} = 1.25MHz, f_C = 19.3MHz	-10		+10	
		f_{FLCLK} = 2.0625MHz, f_C = 31.4MHz	-10		+10	
Ratio of In-Filter-Band to Out-of-Filter-Band Noise		f_{IN_BAND} = 100Hz to 22.5MHz, f_{OUT_BAND} = 67.5MHz to 112.5MHz		19		dB
Quadrature Gain Error		Includes effects from baseband filters, measured at 125kHz baseband			1.2	dB
Quadrature Phase Error		Includes effects from baseband filters, measured at 125kHz baseband			4	degrees

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.25V, $V_{IOUT\_}$ = $V_{QOUT\_}$ = 0.59V_{P-P}, $C_{IOUT\_}$ = $C_{QOUT\_}$ = 10pF, f_{FLCLK} = 2MHz, $R_{IOUT\_}$ = $R_{QOUT\_}$ = 10kΩ, V_{FDOUB} = V_{INSEL} = V_{CPG1} = V_{CPG2} = 2.4V, V_{PLLIN+} = V_{MOD+} = 1.3V, V_{PLLIN-} = V_{MOD-} = 1.1V, T_A = +25°C. Typical values are at V_{CC} = 5.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNTHESIZER						
XTLOUT Output Voltage Swing		Load = 10pF ll 10kΩ, f_{XTLOUT} = 6MHz	0.75	1	1.5	V_{P-P}
XTLOUT Output Voltage DC				2		V
Crystal Frequency Range (Note 1)			4		7.26	MHz
MOD+, MOD- Setup Time (Note 1)	t_{SUM}	Figure 1	7			ns
MOD+, MOD- Hold Time (Note 1)	t_{HM}	Figure 1	0			ns
LOCAL OSCILLATOR						
LO Tuning Range (Note 1)			590		1180	MHz
LO Phase Noise (Notes 7, 12)		At 1kHz offset, f_{LO} = 2175MHz		-55		dBc/Hz
		At 10kHz offset, f_{LO} = 2175MHz		-75		
		At 100kHz offset, f_{LO} = 2175MHz		-95		
RFIN_ to LO Input Isolation (Note 10)		$f_{RFIN\_}$ = 2150MHz		57		dB

Note 1: Minimum and maximum values are guaranteed by design and characterization over supply voltage.
Note 2: With external 100Ω termination resistor.
Note 3: Driving differential load of 10kΩ ll 15pF.
Note 4: Two signals are applied to RFIN_ at f_{LO} - 100MHz and f_{LO} - 199MHz. V_{GC2} = 1V; V_{GC1} is set such that the baseband outputs are at 590mV_{P-P}. IM products are measured at baseband outputs but are referred to RF inputs.
Note 5: Two signals are applied to RFIN_ at 1200MHz and 2150MHz. V_{GC2} = 1V, V_{GC1} is set such that the baseband outputs are at 590mV_{P-P}. IM products are measured at baseband outputs but are referred to RF inputs.
Note 6: $P_{RFIN\_}$ = -40dBm so that front end IM contributions are minimized.
Note 7: Using L64733/L64734 demo board from LSI Logic.
Note 8: Downconverted level, in dBc, of carrier present at f_{LO} x 2, f_{LO} = 1180MHz, f_{VCO} = 590MHz, V_{FDOUB} = 2.4V.
Note 9: Downconverted level, in dBc, of carrier present at f_O / 2, f_{LO} = 2175MHz, f_{VCO} = 1087.5MHz, V_{FDOUB} = 2.4V.
Note 10: Leakage is dominated by board parasitics.
Note 11: V_{CPG1} = V_{CPG2} = V_{FDOUB} = V_{INSEL} = 0.5V, f_{FLCLK} = 0.5MHz.
Note 12: Measured at tuned frequency with PLL locked. All phase noise measurements assume tank components have a Q > 50.

Direct-Conversion Tuner IC for Digital DBS Applications

Pin Description

PIN	NAME	FUNCTION
1, 6, 19, 29, 39, 45	V_{CC}	V_{CC} Power-Supply Input. Connect each pin to a +5V ±5% low-noise supply. Bypass each V_{CC} pin to the nearest GND with a ceramic chip capacitor.
2	CFLT	External Bypass for Internal Bias. Bypass this pin with a 0.1µF ceramic chip capacitor to GND.
3	XTL-	Inverting Input to Crystal Oscillator. Consult crystal manufacturer for circuit loading requirements.
4	XTL+	Noninverting Input to Crystal Oscillator. Consult crystal manufacturer for circuit loading requirements.
5, 9, 10, 15, 16, 32, 40, 41, 46	GND	Ground. Connect each of these pins to a solid ground plane. Use multiple vias to reduce inductance where possible.
7	RFIN-	RF Inverting Input. Bypass RFIN- with 47pF capacitor in series with a 75Ω resistor to GND.
8	RFIN+	RF Noninverting Input. Connect to 75Ω source with a 47pF ceramic chip capacitor.
11	QDC-	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from QDC- to QDC+ (pin 12).
12	QDC+	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from QDC+ to QDC- (pin 11).
13	IDC-	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from IDC- to IDC+ (pin 14).
14	IDC+	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from IDC+ to IDC- (pin 13).
17	RFOUT	Buffered RF Output. Enabled when INSEL is low.
18	CPG1	Charge-Pump Gain Select. High-impedance digital input. Sets the charge-pump output scaling. See the *DC Electrical Characteristics* section for available gain settings.
20	XTLOUT	Buffered Crystal Oscillator Output
21	CPG2	Charge-Pump Gain Select. High-impedance digital input. Sets the charge-pump output scaling. See the *DC Electrical Characteristics* section for available gain settings.
22	GC1	Gain Control Input for RF Front End. High-impedance analog input, with an input range of 1V to 4V. See the *AC Electrical Characteristics* section for transfer function.
23	GC2	Gain Control Input for Baseband Signals. High-impedance analog input, with an input range of 1V to 4V. See the *AC Electrical Characteristics* section for transfer function.
24	INSEL	Loopthrough Mode Enable. High-impedance digital input. Drive low to enable the RFOUT buffer and disable the internal downconverters. Connect to V_{CC} for normal tuner operation.
25	FLCLK	Baseband Filter Cutoff Adjust. Connect to a slew-rate-limited clock source. See the *AC Electrical Characteristics* section for transfer function.
26	FDOUB	LO Frequency Doubler. High-impedance digital input. Drive high to enable the LO frequency doubler. Drive low to disable the doubling function.
27	QOUT-	Baseband Quadrature Output. Connect to inverting input of high-speed ADC.
28	QOUT+	Baseband Quadrature Output. Connect to noninverting input of high-speed ADC.
30	IOUT-	Baseband In-Phase Output. Connect to inverting input of high-speed ADC.
31	IOUT+	Baseband In-Phase Output. Connect to noninverting input of high-speed ADC.
33	MOD+	PECL Modulus Control. A PECL high on MOD+ sets the dual-modulus prescaler to divide by 32. A PECL logic low sets the divide ratio to 33. Drive with a differential PECL signal with MOD- (pin 34).

Pin Description (continued)

PIN	NAME	FUNCTION
34	MOD-	PECL Modulus Control. A PECL low on MOD- sets the dual-modulus prescaler to divide by 32. A PECL logic high sets the divide ratio to 33. Drive with a differential PECL signal with MOD+ (pin 33).
35	PLLIN+	PECL Phase-Locked Loop Input. Drive with a differential PECL signal with PLLIN- (pin 36).
36	PLLIN-	PECL Phase-Locked Loop Input. Drive with a differential PECL signal with PLLIN+ (pin 35).
37	PSOUT+	PECL Prescaler Output. Differential output of the dual-modulus prescaler. Used with PSOUT- (pin 38). Requires PECL-compatible termination.
38	PSOUT-	PECL Prescaler Output. Differential output of the dual-modulus prescaler. Used with PSOUT+ (pin 37). Requires PECL-compatible termination.
42	TANK-	LO Tank Oscillator Input. Connect to an external LC tank with varactor tuning.
43	VRLO	LO Internal Regulator. Bypass with a 100pF ceramic chip capacitor to GND.
44	TANK+	LO Tank Oscillator Input. Connect to an external LC tank with varactor tuning.
47	FB	Feedback Output. Control of external charge-pump transistor.
48	CP	Voltage Drive Output. Control of external charge-pump transistor.
—	EP	Exposed Paddle. Connect EP to GND.

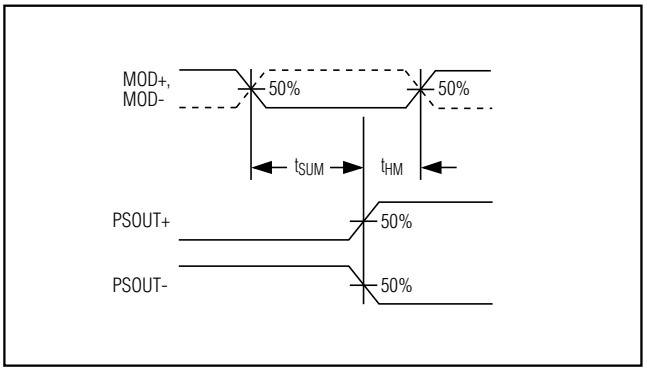
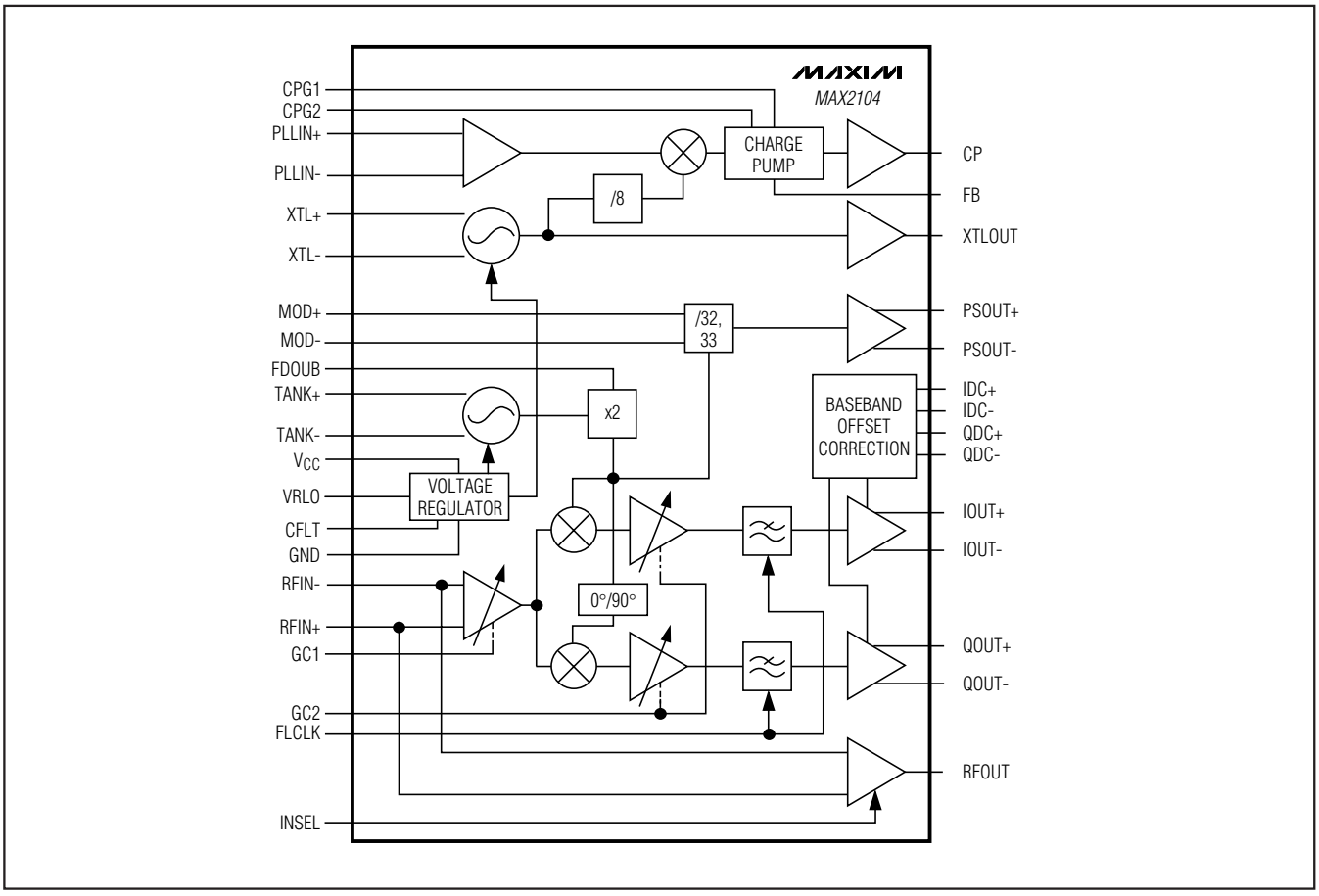


Figure 1. Timing Diagram

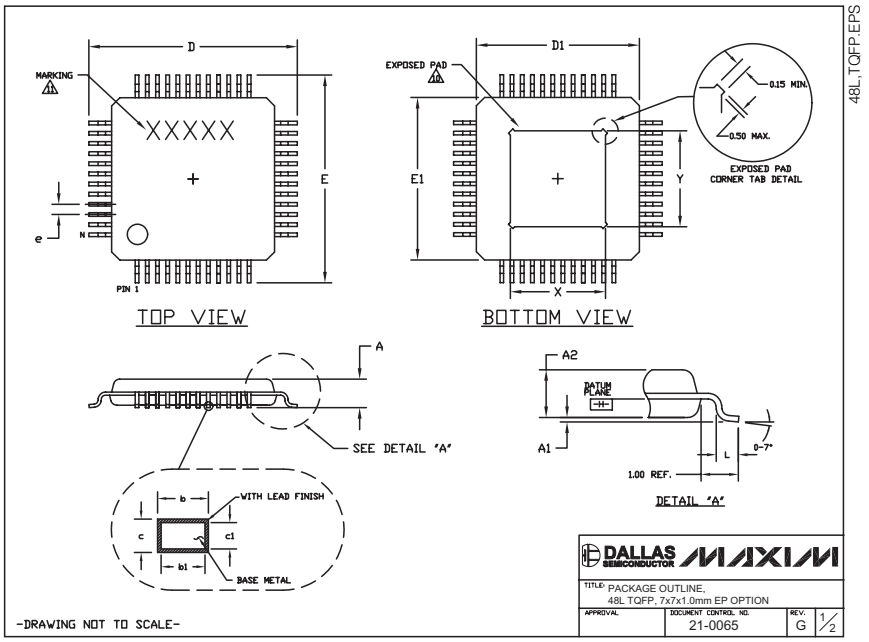
Direct-Conversion Tuner IC for Digital DBS Applications

Functional Diagram



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊣H⊢ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATION ABA-HD.
8. LEADS SHALL BE COPLANAR WITHIN 0.08 MM.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

SYMBOL	JEDEC VARIATION ABC-HD		
	MIN.	NOM.	MAX.
A			1.20
A_1	0.05	0.10	0.15
A_2	0.95	1.00	1.05
D	8.90	9.00	9.10
D_1	6.90	7.00	7.10
E	8.90	9.00	9.10
E_1	6.90	7.00	7.10
L	0.45	0.60	0.75
N	48		
e	0.50 BSC.		
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	--	0.20
c1	0.09	--	0.16

PKG. CODE	EXPOSED PAD VARIATIONS X			Y		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
C48E-7	3.70	4.00	4.30	3.70	4.00	4.30
C48E-8	4.70	5.00	5.30	4.70	5.00	5.30
C48E-10	3.70	4.00	4.30	3.70	4.00	4.30

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 48L TQFP, 7x7x1.0mm EP OPTION
APPROVAL
DOCUMENT CONTROL NO. 21-0065
REV. G
2/2