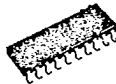
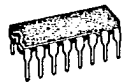




T-74-05-01



3006B

3036B

CMOS IC

3V-Operated Electronic Volume Control

E1374C

Use : Attenuation of signal

Features :

- . C MOS process 3V typ. operation.
 - . Up/down operation is performed with SW input.
 - . 4-bit, 16-step counter. Step 6* is set with initial input (INIT).
 - . Center tap provided.
 - . Maximum attenuation : -60dB or less
 - . Attenuation curve : Pseudo curve A. Left/right simultaneous setting.
- (Note) *: Step 6 means mode 6.

TENTATIVE

Absolute Maximum Ratings at Ta=25°C

| | | | unit |
|-----------------------------|-------------|----------------------|------|
| Maximum Supply Voltage | V_{DDmax} | V_{SS} to 6 | V |
| Applied Voltage | V_I | V_{SS} to V_{DD} | V |
| Allowable Power Dissipation | P_dmax | 100 | mW |
| Operating Temperature | Topg | -30 to +75 | °C |
| Storage Temperature | Tstg | -40 to +125 | °C |

Allowable Operating Conditions at Ta=25°C

| | | | unit |
|-------------------------|----------|-------------------------|------|
| Supply Voltage | V_{DD} | 2.1 to 4.5 | V |
| Input "H" Level Voltage | V_{IH} | $0.7V_{DD}$ to V_{DD} | V |
| Input "L" Level Voltage | V_{IL} | 0 to $0.3V_{DD}$ | V |

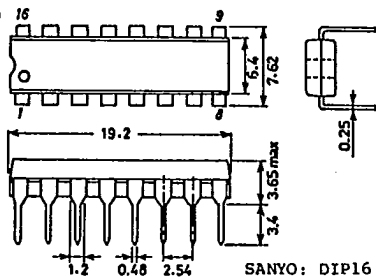
Electrical Characteristics at Ta=25°C

| | | | |
|----------------------------|-----------|------------------------------------|-----------|
| Signal Distortion | THD1 | $V_{DD}=3V, R_L=50kohms, f=1kHz$ | 0.5% max |
| | THD2 | $V_{DD}=1.8V, R_L=50kohms, f=1kHz$ | 1% typ |
| Output at Attenuation Mode | X_{OUT} | 0dBm input, 1kHz, 51kohm load | -60dB max |



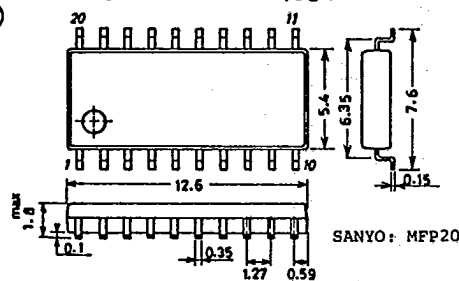
Case Outline 3006B-D16IC LC7533

(unit:mm)



Case Outline 3036B-M20IC LC7534M

(unit:mm)

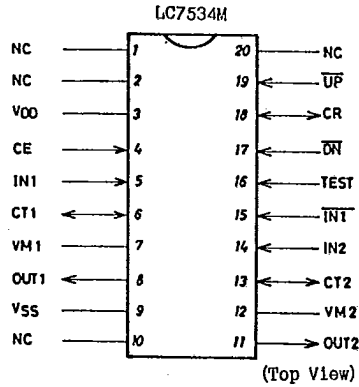
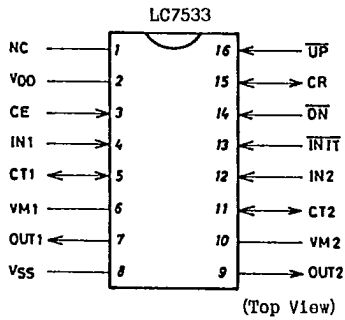


7048YT/7235MW/9034/9303KI, TS No.1374-1/2

LC7533,7534M

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Pin Assignment

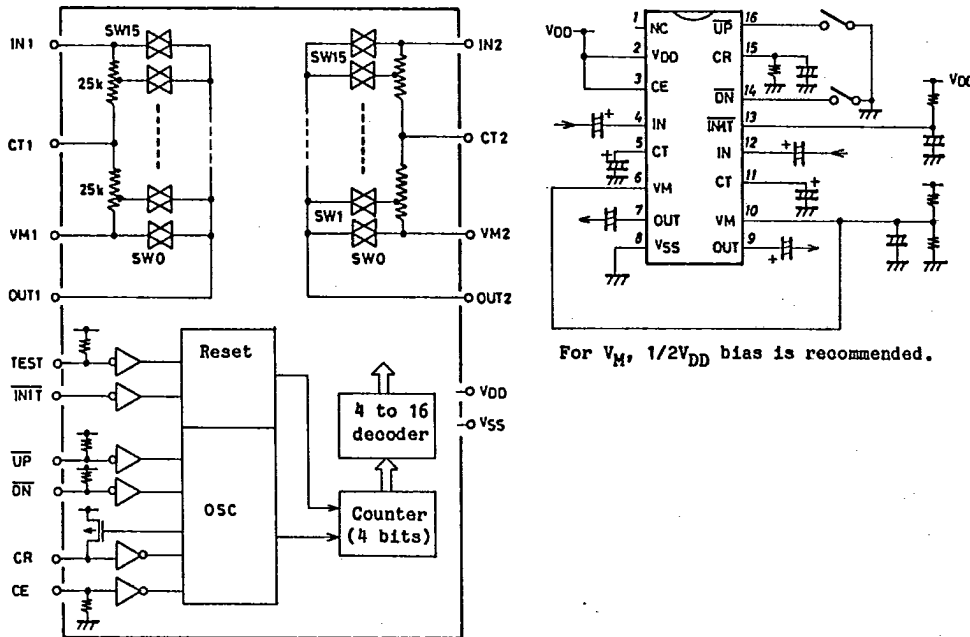


- Note 1. No bonding exists on the inside of NC pin. It is recommended that the outside should be shorted to V_{DD}, V_{SS}, etc. on the printed circuit board.
- Note 2. The MFP package only is provided with the TEST pin. It should be connected to V_{SS}.
 TEST=0 causes the power-on reset function to be performed.
 (The power-on reset function means that mode 6 is entered at the time of application of power.)

Equivalent Circuit Block Diagram

Sample Application Circuit

Common to LC7533/LC7534M (LC7533 DIP-16)



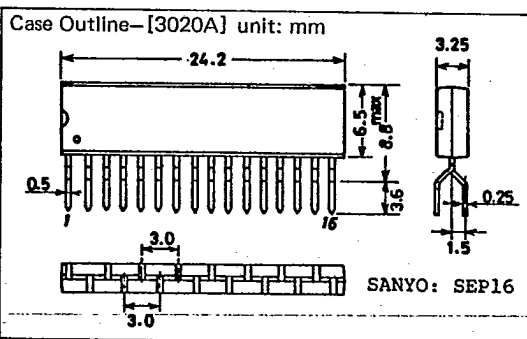
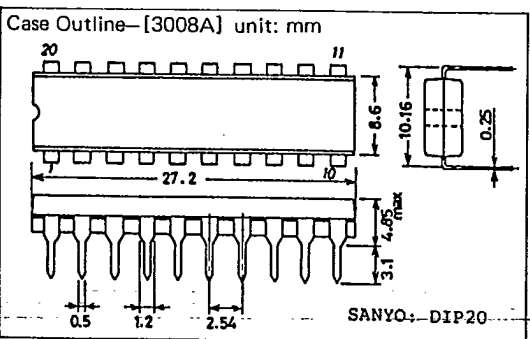
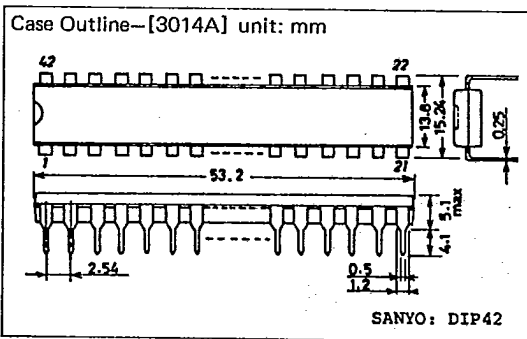
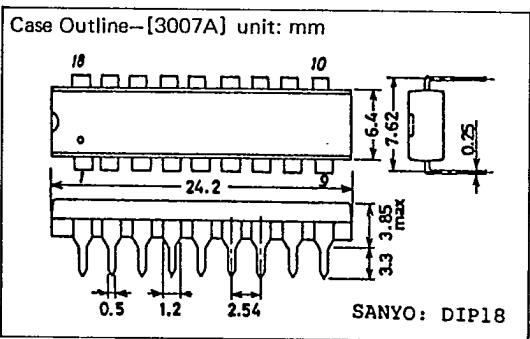
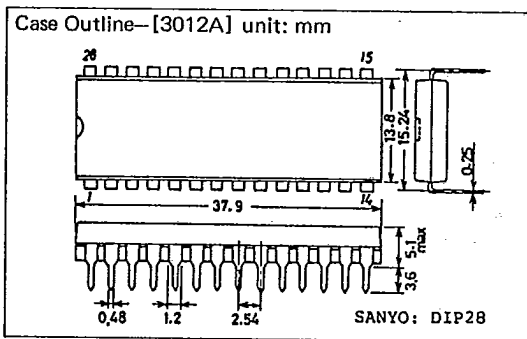
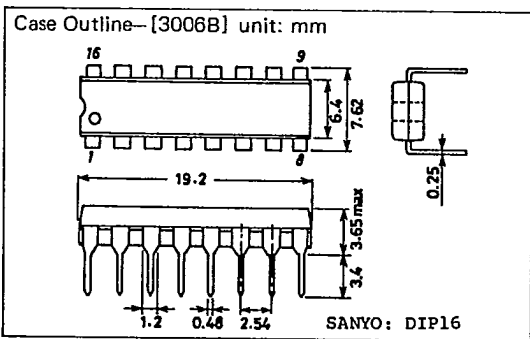
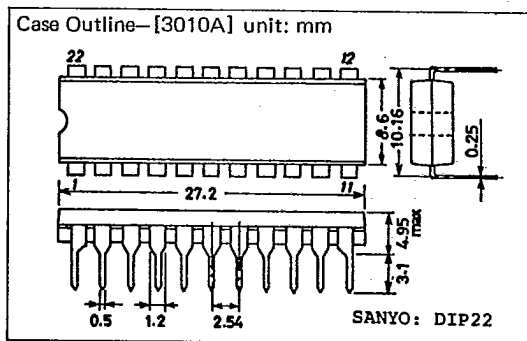
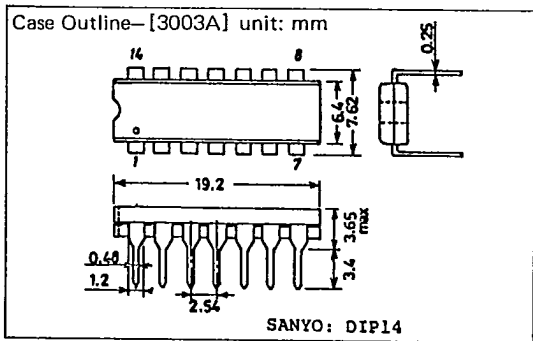
For V_M, 1/2V_{DD} bias is recommended.

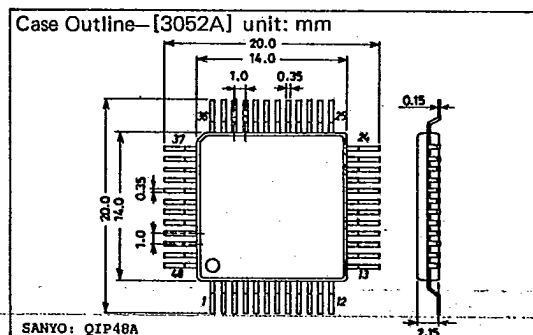
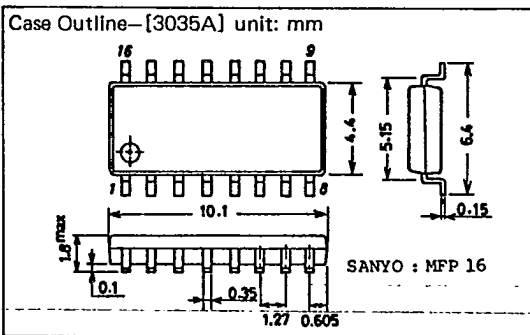
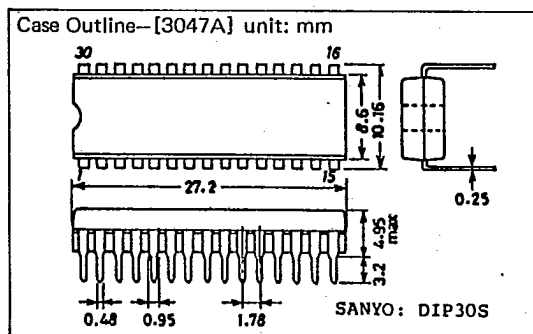
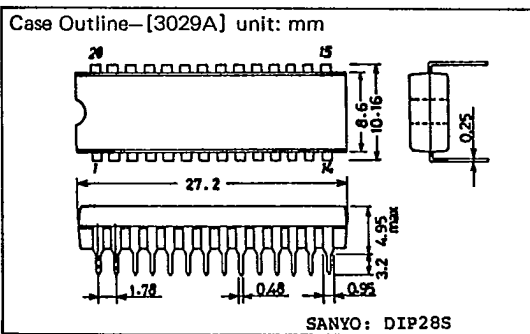
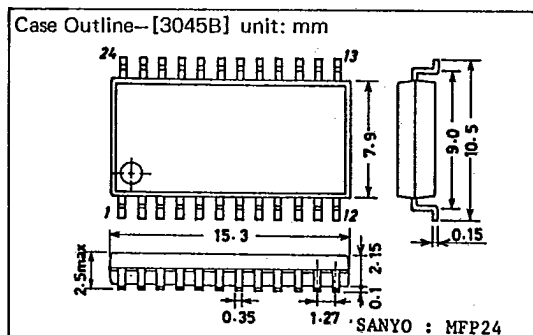
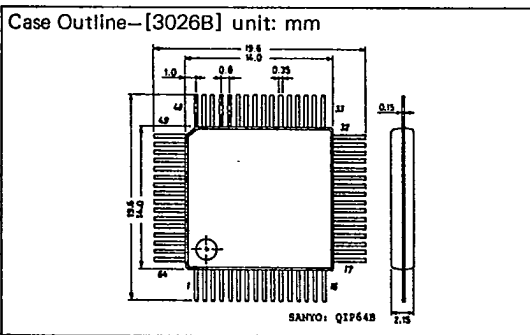
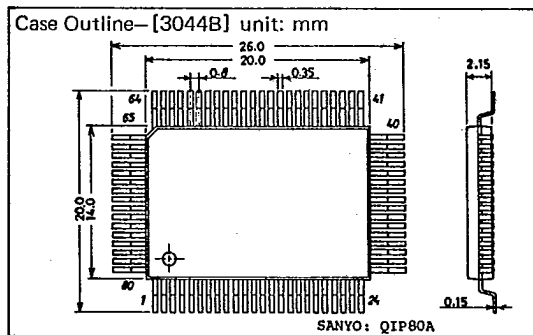
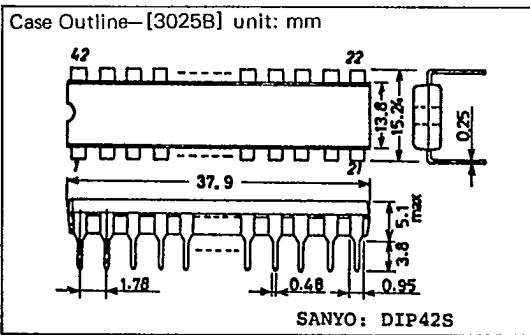
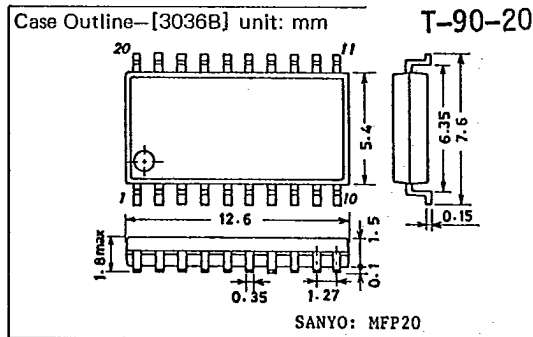
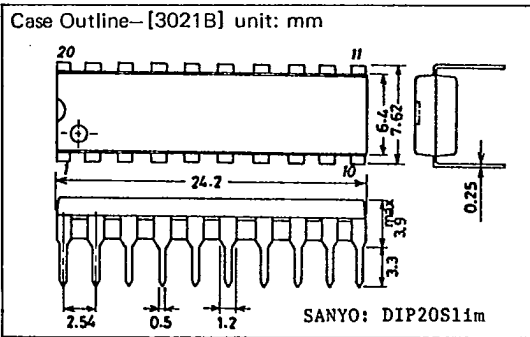
Note 1. The TEST pin is bonded only when the MFP20 is used.

T-90-20

AUDIO-USE MOS IC CASE OUTLINES

- All of Sanyo audio-use MOS IC case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.





T-90-20

